MAXIM

1989 Integrated Circuits Data Book

A/D Converters
D/A Converters
True RMS-to-DC Converters
Voltage References
Operational Amplifiers & Buffers
Power Supply Circuits

Display Drivers/Counters
Timers/Counters
Interface
Switched Capacitor Filters
Analog Multiplexers
Analog Switches

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Guide To Using This Data Book

Maxim is a full line supplier of analog and interface products. This data book contains detailed product data sheets for Maxim's broad line of products that include:

- A/D and D/A Converters
- Precision Voltage References
- True RMS-to-DC Converters
- Operational Amplifiers (Precision CMOS and Bipolar)
- Video Amplifiers and Buffers
- Power Amplifiers and Programmable Gain Amplifiers
- CMOS Power Supply Circuits
  - — Linear Regulators
  - — DC-DC Converters
  - — AC-DC Regulators
  - — Supervisory Circuits
  - — Charge Pump Converters
  - — Voltage Detectors
- CMOS Display Drivers/Counters
- CMOS Timers/Counters
- RS-232 Drivers and Receivers
- CMOS Switched Capacitor Filters
- CMOS Analog Switches and Multiplexers

These circuits utilize Maxim's CMOS, Bipolar and advanced Hybrid technologies. All of Maxim's monolithic devices are available in surface mount packages that increase board density with little impact on power handling capability.

At the beginning of most sections are selection tables that can assist you in selecting the product most suitable for your application(s). The selection guide also contains page numbers for individual product data sheets. A complete listing by function is contained in the Table of Contents with a brief product description to assist you in finding any device of interest.

Data Sheet Identifiers

IDENTIFIER	PRODUCT STATUS	COMMENTS
None	Full Production	Data Sheet Finalized
Introductory	Initial Production	Data Sheet based on limited number of devices
Advance Information	Samples Only	Data Sheet based on design goals

Maxim's goal is to develop products which advance the state of the art in analog and interface circuits for applications such as analog signal processing, data acquisition, test systems, instrumentation and communications. Some of the significant product advances introduced in this data book include:

- Complete 8- and 12-bit CMOS A/D converters that include voltage references and track and hold functions (MAX150, MAX162 and MAX172).
- 3½ digit integrating A/D converters with LCD and LED display drivers, onboard negative charge pump converters for operation off a single positive supply, and bipolar input capability.
- 3¾ digit μP compatible Digital Multimeter circuits that offer superior performance and flexibility compared to previous integrating A/D converters (MAX133 and MAX134).
- Industry standard and proprietary voltage reference devices that are offered in plastic DIPs, Cerdips and surface mount Small Outline packages. In particular, the MAX672 and MAX673 offer superior performance for the price.
- World's lowest Offset Bipolar Op Amp, the MAX400, with just 10μV offset error and 0.3μV/°C drift.
- World's first ±15V Chopper Stabilized Op Amps, the MAX420 and MAX430 families. These amplifiers have just 5μV maximum offset error and 0.05μV/°C drift.
- A family of Video CMOS amplifiers that combine wide bandwidth of 50MHz with 2, 4 and 8 channel input multiplexers (MAX452 family).
- Single supply RS-232 Drivers and Receivers that use patented '+' and '–' charge pump converters to generate ±10V supplies for the RS-232 Drivers from a single +5V supply. Maxim has more RS-232 Driver/Receiver combinations than any other manufacturer.
- AC-DC regulators that convert the line voltage directly to +5V with minimal external components (MAX610 family).
- Linear regulators with microamp quiescent currents for battery powered applications (MAX663/4/6).
- DC-DC converters which significantly simplify system design by economically generating different power supply voltages on individual PCBs (MAX630 and MAX640 families).
- Monitoring/supervisory circuits which generate reliable power fail and reset signals for power switch-on and power fail μP applications (MAX690 family).
- Switched capacitor filters that require no external components and allow precise filter cutoff frequencies. They are digitally programmable, offering flexibility in design (MAX260 family).
- Overvoltage Fault Protected analog multiplexers that continue to protect input and output signal sources even after power to the multiplexer has been removed (MAX358/359).

Maxim will continue to serve analog and interface designers with new innovative products offering the highest standards of performance, quality and reliability. We appreciate the opportunity to serve you.

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Analog Switches

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Appendix

MAXIM

A/D Converters

A/D Converter Selector

Integrating

Part Number	Resolution	Output Type	Supply Voltage	Supply Current (Typ/Max mA)	Comments	Reference	Page No.
MAX130	3 1/2 Digit ±2000 Counts	LCD	+4.5V to 14V	0.1/0.25	Replacement for ICL7106	Low T.C. Bandgap	1-1
MAX131	3 1/2 Digit ±2000 Counts	LCD	+4.5V to 14V	0.06/0.1	Replacement for ICL7136	Low T.C. Bandgap	1-1
MAX133	3 3/4 Digit ±4000 Counts	µP	+9V	0.09/0.2	Digital Multimeters 50ms conversion	External	1-13
MAX134	3 3/4 Digit ±4000 Counts	µP	±5V	0.09/0.2	µP/50ms conversion	External	1-13
MAX136	3 1/2 Digit ±2000 Counts	LCD	+9V	0.06/0.15	Hold function, Low power	Bandgap	1-31
MAX138	3 1/2 Digit ±2000 Counts	LCD	+2.25V to 7V	0.2/0.8	2 cell battery operation ± Signal Input	Low T.C. Bandgap	1-35
MAX139	3 1/2 Digit ±2000 Counts	LED	+5V	0.2/0.8	± Inputs (from GND)	Low T.C. Bandgap	1-35
MAX140	3 1/2 Digit ±2000 Counts	LED	+5V	0.2/0.8	2-3mA seg I	Low T.C. Bandgap	1-35
ICL7106	3 1/2 Digit ±2000 Counts	LCD Drive	+9V	0.6/1.8	Digital multimeters	Zener	1-119
ICL7107	3 1/2 Digit ±2000 Counts	LED Drive	+9V	0.6/1.8	Digital Panel Meters	Zener	1-119
ICL7109	12 Bits + Sign ±4096 Counts	8/16 bit µP and UART	±5V	0.7/1.5	3-state Binary Up to 30 conversion/sec	Zener	1-131
ICL7116	3 1/2 Digit ±2000 Counts	LCD	+9V	0.8/1.8	Same as ICL7106, but adds Hold Function	Zener	1-149
ICL7117	3 1/2 Digit ±2000 Counts	LED	±5V	0.8/1.8	Same as ICL7107, but adds Hold Function	Zener	1-149
ICL7126	3 1/2 Digit ±2000 Counts	LCD	+9V	0.6/0.1	Use ICL7136 for new designs	Zener	1-153
MAX7129 ICL7129A	4 1/2 Digit ±20,000 Counts	Triplexed LCD	+9V	1.0/1.4	DPMs, Instruments Lowest Noise A/D– 3µV (7129A)	External	1-161
ICL7135	4 1/2 Digit ±20,000 Counts	Multiplexed BCD	±5V	1.0/2.0	DMM, DPM, Data Loggers	External	1-173
ICL7136	3 1/2 Digit ±2000 Counts	LCD	+9V	0.06/0.1	Low Power version of ICL7106, Very Low Noise	Zener	1-185
ICL7137	3 1/2 Digit ±2000 Counts	LED	±5V	0.06/0.2	Low Power when LED display turned off	Zener	1-193

SAR and Half-Flash

Part Number	Resolution	Integral Linearity	Conversion Time	Supply Voltage	Input Range	Features	Reference	Page No.
MAX150	8 bits	1/2 LSB	1.34µs	+5V	+5V	Track/Hold	Internal	1-43
MAX154	8 bits/4 ch	1/2 LSB	2µs	+5V	+5V	Track/Hold	Internal	1-55
MAX158	8 bits/8 ch	1/2 LSB	2µs	+5V	+5V	Track/Hold	Internal	1-55
MAX160	8 bits	1/2 LSB	4µs	+5V	±15V	Fast AD7574		1-67
MAX161	8 bits/8 ch	1/2 LSB	20µs	+5V	±15V	Fast AD7581 Dual port RAM	External	1-79
MAX162	12 bits	1/2 LSB	3.25µs	+5V/-12V	+5V	Fast AD7572	Internal	1-87
MAX172	12 bits	1/2 LSB	10µs	+5V/-12V	+5V	Low cost	Internal	1-103
AD578	12 bits	1/2 LSB	3µs	±15V	±10V	Parallel/Serial Output	Onboard	1-107
ADC0820	8 bits	1/2 LSB	1.4µs	+5V	+5V	Half-Flash, Internal Clock Track/Hold		1-113
AD7572	12 bits	1/2 LSB	5µs	+5V/-15V	+5V		Internal	1-87
AD7574	8 bits	1/2 LSB	15µs	+5V	±15V	Analog V_{IN} > V_{SUPP}	External	1-67
AD7581	8 bits/8 ch.	1/2 LSB	66.6µs	+5V	±15V	8 byte RAM	External	1-79
AD7820	8 bits	1/2 LSB	1.34µs	+5V	+5V	Half-Flash	External	1-43
AD7824	8 bits/4 ch	1/2 LSB	2.0µs	+5V	+5V	4 Channels	External	1-55
AD7828	8 bits/8 ch	1/2 LSB	2.0µs	+5V	+5V	8 Channels	External	1-55

Analog/Digital Converter Terminology

Absolute Accuracy: The difference between the ideal expected ADC output code and the actual output for a specified input or range of inputs.

Analog-To-Digital Converter: Also ADC, A/D, and A-to-D. A device which translates an analog signal to a digital code.

Bipolar: Describes an ADC input range covering positive and negative input signals, +V to -V inputs.

Differential Inputs: Allow an ADC to measure the difference between two input signals. Improves noise rejection and simplifies connections to tranducers by reducing external circuitry.

Flash ADC: A type of ADC where a number of comparators simultaneously compare the analog input to a number of reference voltages. Decoding logic generates an output code based on the comparator decisions. The main advantage is very high conversion speed.

Full-Scale Error: Also Gain Error. The difference between the actual and ideal ADC output for a Full-Scale input. Expressed in % of FSR, or LSBs.

Integrating ADC: A type of ADC where the analog input is integrated over a specified time. A deintegration cycle then gates a digital counter so that its accumulated total is proportional to the input voltage. Advantages included high resolution, noise rejection and linearity.

Least Significant Bit (LSB): The ADC digital output bit that has the smallest weight. Also the analog input change that causes an output code change of 1. As an analog quantity, 1 LSB = FSR × 2^{-N}, where N is the number of ADC output bits.

Linearity: Also Nonlinearity and Integral Nonlinearity. See Relative Accuracy.

Most Significant Bit (MSB): The ADC digital output bit that has the largest weight.

No Missing Codes: Describes a property of an ADC whereby every possible output code can be obtained by "sweeping" through the analog input range. It is similar to Monotonicity in DACs.

R-2R Ladder: A resistor network used to generate binarily weighted currents or voltages in Successive Approximation Analog-to-Digital Converters.

Ratiometric Conversion: Where the unknown input signal is derived from a reference voltage that is also used as the reference for the ADC. Eliminates the need for a precision reference source since the transfer function is independent of the reference value. Commonly employed with strain gauges.

Relative Accuracy: (or End-Point Nonlinearity) The maximum deviation from a straight line which passes through the endpoints of the ADC transfer function (Zero and Full Scale). It is expressed in % or ppm of the Full Scale Range (FSR) or in LSBs.

Resolution: The number of counts that an ADC divides the input signal. Expressed in number of bits. An ADC with N-bit resolution divides its input range into 2^N steps.

Rollover Error: For an ADC with a Bipolar Input Range, the output difference for inputs of equal magnitude but opposite polarity. Specified in Counts or LSBs.

Sample-Hold: Also Track-and-Hold. A device which takes a "snap shot" of an analog signal so that it is held stationary for an A/D Conversion. Generally, Sample-Holds are only required for Successive Approximation ADCs which require that the input signal be ½ LSB stable during the conversion time.

Successive Approximation ADC: A type of ADC where the analog input is subject to a sequence of comparisons with binarily weighted references to determine output code. The input is first compared to a reference of ½ Full Scale. The MSB will be 1 if the input is greater, and 0 if it is less. This result determines if the input is then compared to ¼ FS or ¾ FS for the next bit. The tests continue until all bits are determined. Advantages are speed combined with high resolution.

Temperature Coefficient: The variation of a parameter (such as Zero Error, Full Scale Gain, or Linearity) with ambient temperature. Specified in %/°C or ppm/°C.

Total Unadjusted Error: Includes Full Scale, Relative Accuracy, and Zero Code Error specifications. The Maximum output deviation from the ideal expected values. Specified in LSBs or % of FSR at a fixed reference voltage, usually +10V.

Unipolar: Describes an ADC input range covering one polarity of signal, either 0 to +V or 0 to -V input.

Zero Error: Also Offset Error. The ADC output code for an input of 0V.

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

3½ Digit A/D Converters with Bandgap Reference

General Description

The MAX130 and MAX131 are 3½ digit A/D converters with onboard LCD display drivers. The MAX130 and MAX131 use a bandgap reference to generate an analog Common voltage which has the excellent long term stability of a bandgap reference and a guaranteed maximum temperature coefficient of 100ppm/°C. For more demanding applications the "A suffix" parts, the MAX130A and MAX131A, have a 50ppm/°C maximum temperature coefficient.

The MAX130 uses the same circuit and component values as the ICL7106, but draws a maximum supply current of only 250μA maximum (100μA typical) from a 9V battery, much lower than the 1800μA maximum supply current of the ICL7106. The MAX131 uses the same circuit and component values as the ICL7136, with a maximum supply current of 100μA (65μA typical).

These devices are available with both 0°C to 70°C and -40°C to +85°C operating temperature ranges. The operating voltage range is from 4.5V to 14V.

Applications

Digital Multimeters

Digital Panel Meters

Temperature Meters

pH Meters

Features

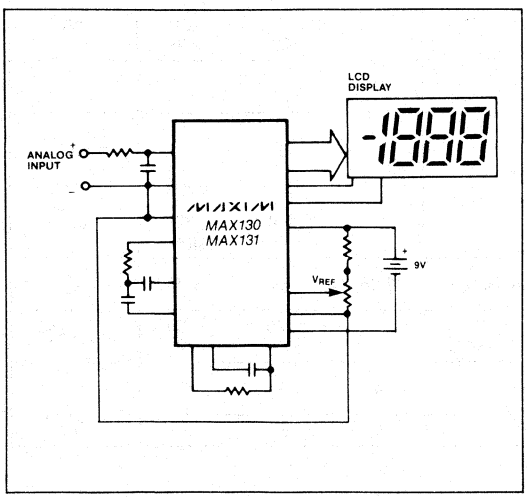
- **Pin Compatible Upgrade for ICL7106 and ICL7136**
- **High Stability Bandgap Reference**
- **50ppm/°C Maximum Temperature Coefficient (MAX130A/MAX131A)**
- **100μA Maximum Supply Current (MAX131)**
- **4.5V to 14V Supply Voltage Range**
- **Onboard 3½ Digit LCD Display Driver**
- **Available in Industrial Temperature Grades**

Ordering Information

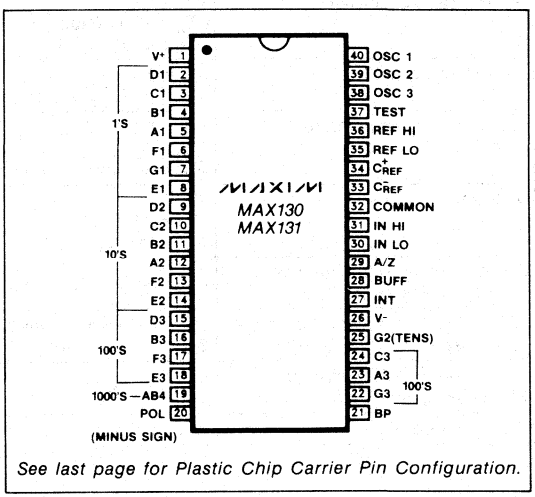
PART	TEMP. RANGE	PACKAGE
MAX130CPL	0°C to +70°C	40 Lead Plastic DIP
MAX130CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX130C/D	0°C to +70°C	Dice
MAX130EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX130EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier
MAX130ACPL	0°C to +70°C	40 Lead Plastic DIP
MAX130ACQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX130AEPL	-40°C to +85°C	40 Lead Plastic DIP
MAX130AEQH	-40°C to +85°C	44 Lead Plastic Chip Carrier
MAX131CPL	0°C to +70°C	40 Lead Plastic DIP
MAX131CQH	0°C to +70°C	44 Lead Plastic Chip Carrier

(Ordering information continued on last page.)

Typical Operating Circuit



Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration.

3½ Digit A/D Converters with Bandgap Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+
Power Dissipation (Note 2)
CERDIP Package 1000mW
Plastic Package 800mW

Operating Temperature Range
MAX130C/AC, MAX131C/AC ..... 0°C to +70°C
MAX130E/AE, MAX131E/AE ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS (MAX130, MAX130A)

(V^+ = 9V, T_A = 25°C, f_{CLOCK} = 48kHz; test circuit - Figure 1; unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 3) T_{MIN} to T_{MAX} (Note 4)	 -000.0 -000.0	 ±000.0 ±000.0	 +000.0 +000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 3) T_{MIN} to T_{MAX} (Note 4)	 999 998	 999/1000 999/1000	 1000 1001	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV T_A = 25°C (Note 3) T_{MIN} to T_{MAX} (Note 4)	-1	±.2 ±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V (Note 5)	-1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0 T_A = 25°C (Note 3) T_{MIN} to T_{MAX}		1 20	10 200	pA
Zero Reading Drift	V_{IN} = 0 T_{MIN} to T_{MAX} (Note 3)		0.2		μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV T_{MIN} to T_{MAX} (Ext. Ref. 0ppm/°C) (Note 3)		1		ppm/°C
V^+ Supply Current	V_{IN} = 0 T_A = 25°C T_{MIN} to T_{MAX}		100	250 400	μA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.95	3.05	3.15	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply (Note 7) MAX130 MAX130A		±20 ±20	±100 ±50	ppm/°C
Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	With Respect to V^+	4	5	6	V

ELECTRICAL CHARACTERISTICS (MAX131, MAX131A)

(V^+ = 9V, T_A = 25°C, f_{CLOCK} = 48kHz; test circuit - Figure 2; unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 3) T_{MIN} to T_{MAX} (Note 4)	 -000.0 -000.0	 ±000.0 ±000.0	 +000.0 +000.0	 Digital Reading Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 3) T_{MIN} to T_{MAX} (Note 4)	 999 998	 999/1000 999/1000	 1000 1001	 Digital Reading Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV T_A = 25°C (Note 3) T_{MIN} to T_{MAX} (Note 4)	 -1	 ±.2 ±.2	 +1	 Counts Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V (Note 5)	-1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		1		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		µV
Input Leakage Current	V_{IN} = 0 T_A = 25°C (Note 3) T_{MIN} to T_{MAX}		1	10 200	pA
Zero Reading Drift	V_{IN} = 0 T_{MIN} to T_{MAX} (Note 3)		0.2		µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV T_{MIN} to T_{MAX} (Ext. Ref. 0ppm/°C) (Note 3)		1		ppm/°C
V^+ Supply Current	V_{IN} = 0 T_A = 25°C T_{MIN} to T_{MAX}		60	100 120	µA
Analog Common Voltage (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply	2.95	3.05	3.15	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply (Note 7) MAX131A MAX131		±20 ±20	±50 ±100	ppm/°C
Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	With Respect to V^+	4	5	6	V

Note 3: Test condition is V_{IN} applied between pin IN-HI and IN-LO through a 1MΩ series resistor as shown in Figures 1 and 2.
Note 4: 1MΩ resistor is removed in Figures 1 and 2.
Note 5: Guaranteed by design.
Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1.)
Note 7: MAX130 and MAX131 temperature coefficient is guaranteed by sample testing. MAX130A and MAX131A temperature coefficient is 100% tested.

3½ Digit A/D Converters with Bandgap Reference

Basic Applications

Figures 1 and 2 show the basic MAX130 and MAX131 applications circuits. Note that the circuits for the MAX130 and the MAX131 use different values for the integration and oscillator components. The MAX130 can operate using the MAX131 component values, but the MAX131 will not operate using the MAX130 component values. The lower supply current device, the MAX131, must always use the higher value integrator resistor as shown in component value table in Figure 2. With a typical operating current of only 65μA, the MAX131 will operate for about 8500 hours when powered by a typical 550mAhr alkaline 9V battery. The MAX130 will operate for 2200 hours with a 550mAhr battery.

Compatibility with ICL7106 and ICL7136

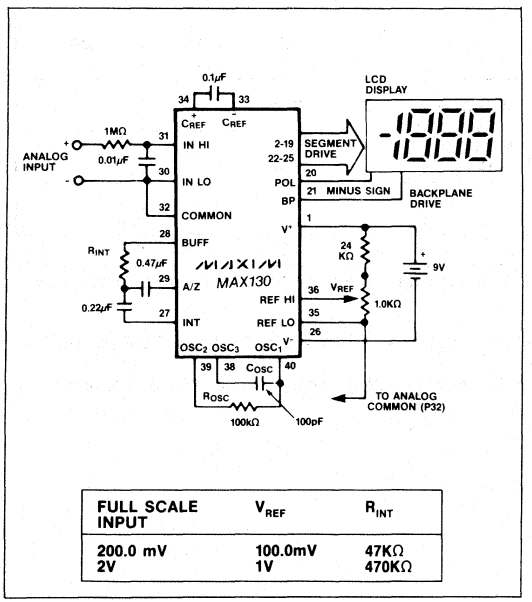
The MAX130 and MAX131 can directly replace the ICL7106 and ICL7136 with no circuit layout or component value changes in circuits which are designed to use the Common voltage as the reference. In ICL7106/7136 circuits which are designed to use an external bandgap reference, the bandgap reference diode can be removed with no circuit changes required. Normally the value of the resistor between V^+ and the bandgap reference diode is the only component value that must be changed to allow the removal of an external bandgap reference diode.

System Reference Point

The analog block diagram (Figures 3) of the MAX130 is similar to that of the MAX131 (Figure 4). The only difference is the voltage at the non-inverting terminal of the integrator during the de-integrate, autozero and zero integrator phases. The MAX130 drives the non-inverting terminal of the integrator with the Common pin during these phases, as does the ICL7106. The MAX131 uses the In Lo pin as the reference point for the integrator during all phases, as does Maxim's ICL7136.

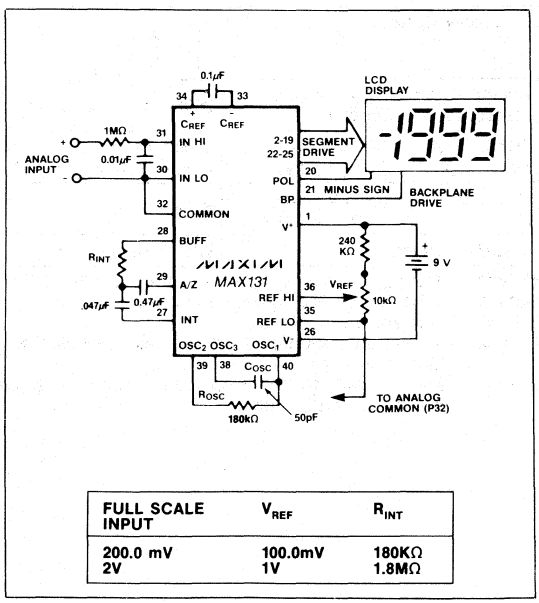
The circuit configuration of the MAX131 results in an excellent 120dB rejection of DC common mode voltages applied to In Hi and In Lo. The MAX131 configuration, though, does not have good rejection of AC noise on the In Lo pin during de-integration. If an AC-DC converter is used with a MAX131 it should either be a half-wave circuit (leaving In Lo connected to Common) or should have adequate filtering to avoid inducing additional noise.

The circuit configuration of the MAX130 is unaffected by AC noise on the In Lo pin during de-integrate, but the rejection of DC common mode signals on In Hi and In Lo is only about 86dB, the same as the ICL7106. The input voltage at the MAX130 In Lo pin should be restricted to no more than 1V above the Common pin.



FULL SCALE INPUT	V_{REF}	R_{INT}
200.0 mV	100.0mV	47KΩ
2V	1V	470KΩ

Figure 1. Maxim MAX130 Typical Operating Circuit, 3 Conversions per Second



FULL SCALE INPUT	V_{REF}	R_{INT}
200.0 mV	100.0mV	180KΩ
2V	1V	1.8MΩ

Figure 2. Maxim MAX131 Typical Operating Circuit, 3 Conversions per Second

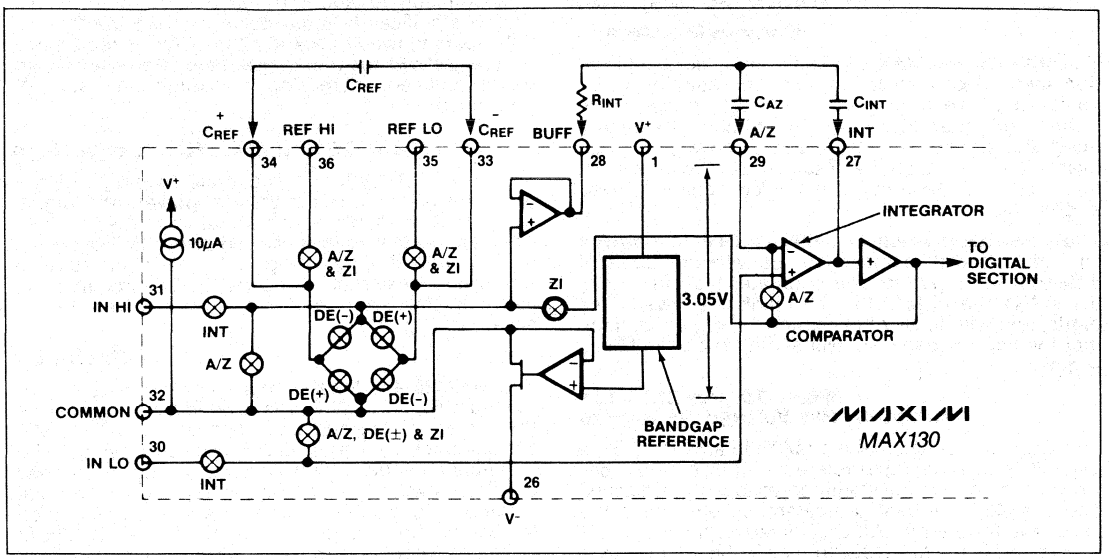


Figure 3. Analog Section of MAX130

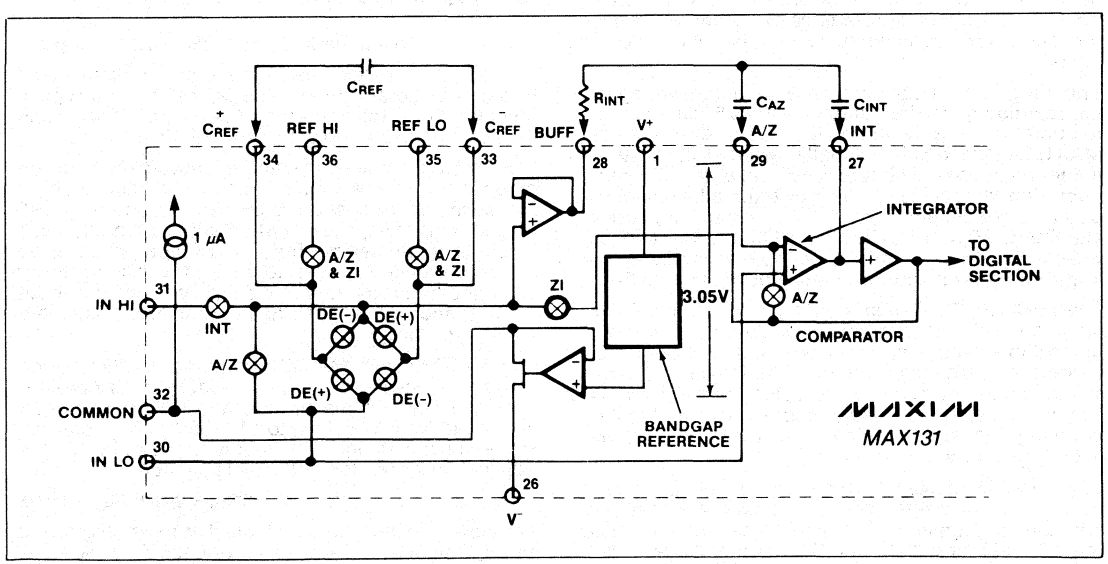


Figure 4. Analog Section of MAX131

3½ Digit A/D Converters with Bandgap Reference

Detailed Description

Conversion Method

The MAX130 and MAX131 use the dual-slope integration method of conversion, with the addition of an autozero phase to compensate for the offset of the buffer and integrator, and the addition of a zero integrator phase to ensure rapid recovery from an overrange conversion. Refer to the ICL7106 data sheet for a detailed description of the conversion phases and timing.

The conversion result is 1000 × (In Hi-In Lo)/(Ref Hi-Ref Lo), with a maximum conversion result of ±1999. If the input voltage is greater than full scale, the MAX130 and MAX131 will blank the lower three digits, and will display the leading "1" digit and, if the input voltage is negative, will also turn on the Minus segment.

MAX130 and MAX131 Common Pin Voltage Reference

The Common voltage of the MAX130 and MAX131 is derived from a bandgap reference, unlike earlier devices which derive the Common voltage from a zener. The MAX130/131 bandgap reference eliminates the excessive long term drift associated with low current zeners, and the MAX130/131 can a be source of a high quality reference voltage without the use of external bandgap reference diodes. The MAX130/131 Common voltage does have slightly more wideband noise than does a zener-derived Common voltage, but a 0.1μF or greater reference capacitor will reduce the bandwidth sufficiently to virtually eliminate the noise.

The long term stability of the common voltage is approximately 0.01% (100ppm or 1/5 count). The temperature coefficient of the each MAX130A and MAX131A device is individually tested at 25°C, at the minimum operating temperature, and at the maximum operating temperature. The maximum allowable temperature coefficient from 25°C to either temperature extreme is 50ppm/°C. The MAX130 and MAX131 devices without the A suffix are sample tested to ensure a maximum temperature coefficient of 100ppm/°C.

The MAX130/131 Common voltage is buffered by an op amp which has an output impedance of 1 ohm and up to 2mA output sink current, and a short circuit current of approximately 35mA. The Common pin has a small pullup current of 1μA typical, and if desired it can be driven to a voltage more negative than its internally generated voltage by overpowering the pullup current source.

Since the MAX130/131 Common voltage is derived from a bandgap reference, it remains at a relatively constant voltage until V^+ drops to less than 4V, unlike the ICL7106 and ICL7136 Common voltage which starts to fall once V^+ drops to around 7V. The PSRR of Common is 0.1mV/V (80dB) typical for a V^+ voltage change of 9V to 4.5V.

The Common voltage is trimmed to 3.05V ± 100mV. This is significantly more accurate than the 2.4V to 3.2V span allowed in the ICL7106. The better voltage accuracy allows the trim range of the reference voltage to be reduced, increasing resolution and ease of adjustment.

MAX130 and MAX131 Test Voltage

The MAX130/131 internally generate a supply which is 4V to 6V below V^+. This voltage powers the digital logic section, including the LCD display driver section. This internal test voltage is coupled to the Test pin via a 500 ohm resistor. See Figure 5. Test pin is suitable for powering external low power CMOS circuitry such as the decimal point and annunciator driver circuits shown in Figure 6.

Oscillator

The MAX130 and MAX131 oscillator circuit is shown in Figure 5. The oscillator is divided by 4 to generate the system clock, and each conversion takes 4000 system clock cycles or 16,000 oscillator cycles. The integration period is 1000 system clock cycles or 4000 oscillator cycles. For maximum rejection of normal mode AC signals the integration period should be an integer multiple of the interfering signal. A 40kHz oscillator frequency will reject both 50Hz and 60Hz since this sets the integration period equal to 6 cycles of 60Hz and 5 cycles of 50Hz. Either a 50pF or 100pF oscillator capacitor can be used and the resistor is calculated from the equation $f \approx 0.40/RC$.

In Lo and In Hi Differential Inputs

These A/D converters measure the differential voltage between In Lo and In Hi. The MAX130 has a typical common mode rejection ratio (CMRR) of 86dB; while the MAX131 has a typical CMRR of 120dB.

In Hi has a guaranteed maximum input leakage current of only 10pA, and can be directly driven by high source impedances such as pH sensors and by the 10 Megohm input impedance attenuators normally used in digital multimeters. Both In Hi and In Lo have protection clamp diodes to V^+ and V^-. If the input voltage can go above V^+ or below V^- then the input currents should be limited to less than 1mA to prevent damage to the A/D.

The MAX130 and MAX131 common mode voltage range for In Hi and In Lo is a minimum of ±1V around Common. Under some circumstances, In Hi and In Lo can range from V^- + 1.5V to V^+ - 1.5V. See "Common Mode Voltage Range Considerations" section of the Application Notes for further information.

Reference and C_{REF} Pins

As shown in the analog block diagrams, Figures 3 and 4, Ref Hi and Ref Lo are connected to the C_{REF} pins during autozero and zero integrate phases via analog switches. This charges an external reference capacitor, which is then used as either a positive or a

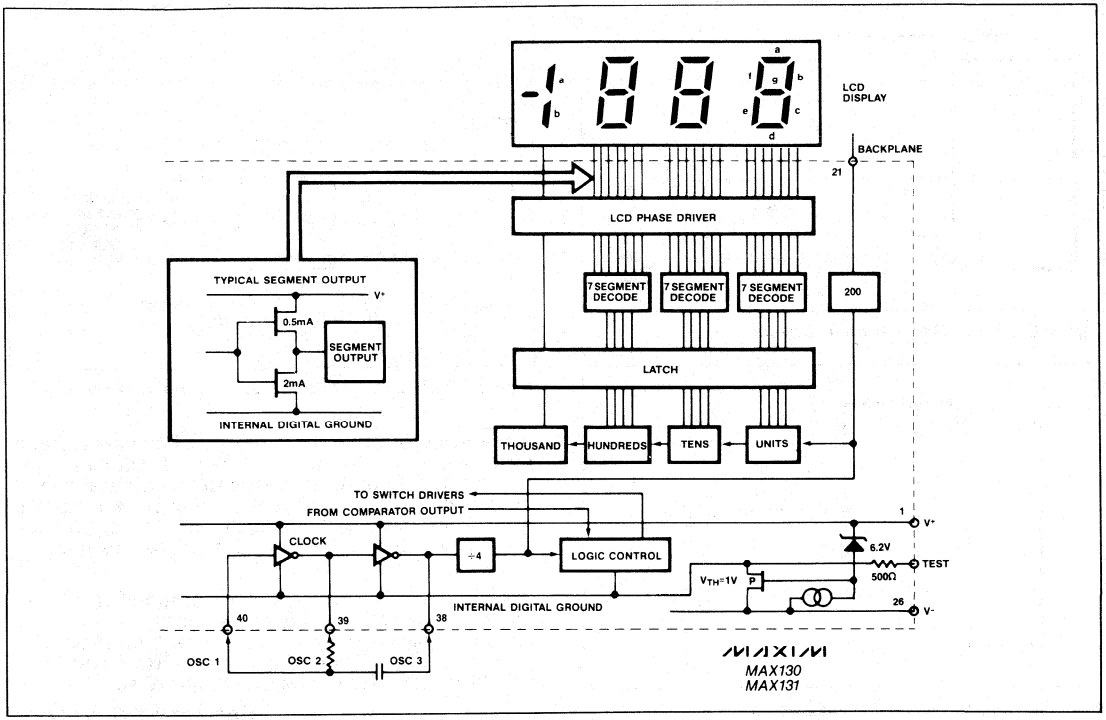


Figure 5. MAX130/131 Digital Section and Oscillator

negative reference voltage as needed during the de-integration phase. The common mode voltage range (CMVR) of Ref Hi and Ref Lo is V^+ to V^-—any voltage between V^+ and V^- can be used to drive the Ref Hi and Ref Lo inputs. The differential voltage between Ref Hi and Ref Lo sets the full scale voltage. A full scale output of ±1999 counts occurs with an input voltage of ±1.999 times the differential voltage between Ref Hi and Ref Lo. If the differential reference voltage is 1.0V the full scale input voltage is 1.999V. With 100mV reference the full scale input voltage is 199.9mV.

LCD Display Driver Outputs

The MAX130 and MAX131 LCD display driver outputs swing from V^+ to the Test pin voltage at a frequency 20 times the conversion rate (50Hz for an oscillator frequency of 40kHz and conversion rate of 2.5 times per second). The output impedance is approximately 3kΩ. The LCD display driver outputs are non-multiplexed or direct drive, and drive in-phase with the backplane output to turn an LCD segment off and drive 180° out of phase with the backplane output to turn an LCD segment on.

The BP or Backplane output has an output impedance of 500Ω. The LCD drive waveforms are 50% duty cycle with matched rise and fall times to minimize the DC component across the LCD display.

Component Selection

Integrator Resistor, R_{INT}

The MAX130 integrator and buffer amplifiers have a class A output stage which can deliver up to 6μA with high linearity. Normally, the MAX130 integrator resistor is chosen to set the maximum current to approximately 4μA by setting its value to $2 \times V_{REF}/4\mu A$. For a 1V reference the correct value is 470kΩ. For a 100mV reference the correct value is 47kΩ. Since the absolute value of R_{INT} does not affect the conversion accuracy, the type of resistor used for R_{INT} is not critical.

The MAX131 integrator and buffer also have up to 4μA of output current capability, with a maximum output current of 1.1μA being the recommended operating point. For 1V reference (2V full scale) R_{INT} should be 1.8MΩ. Use 180kΩ for R_{INT} when using a 100mV reference (200mV full scale).

Integrator Capacitor

The integrator capacitor is normally polypropylene, which has low dielectric absorption. Dielectric absorption will cause integral linearity errors. For example, if polyester or Mylar is used, the measured value of inputs near full scale will be approximately 0.1% lower than expected, while the measured value of low input voltages will be as expected.

3½ Digit A/D Converters with Bandgap Reference

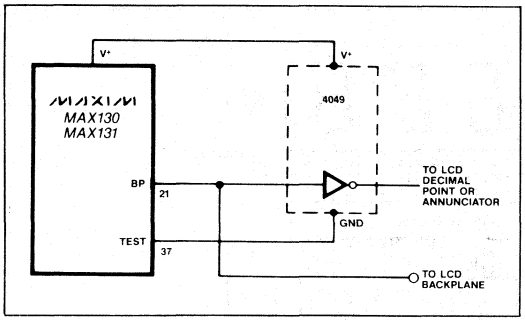


Figure 6A. Fixed Decimal Point Drivers

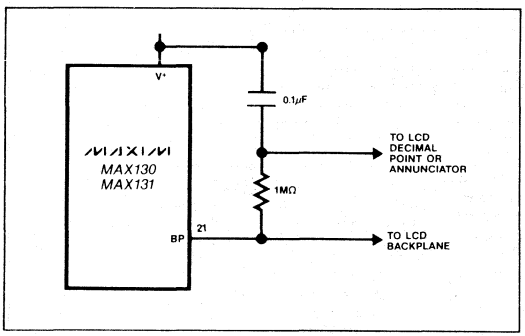


Figure 6B. Fixed Decimal Point Drivers

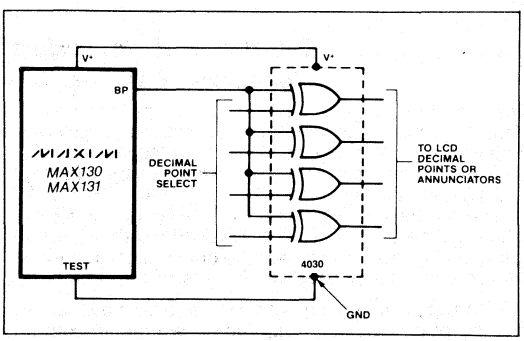


Figure 6C. Exclusive "OR" Gate for Decimal Point Drive

Proper selection of the integrator capacitor value can be verified by monitoring the output swing of the integrator with ±full scale input voltages. In a properly operating circuit, ±full scale input voltages will cause the integrator output (INT pin) to swing to about ±2V. The integrator output can drive to about 0.3V from either supply while maintaining high linearity. Integrator swing is inversely proportional to the oscillator frequency, so the integrator capacitor value must be increased in circuits with conversion rates less than 3 conversions per second.

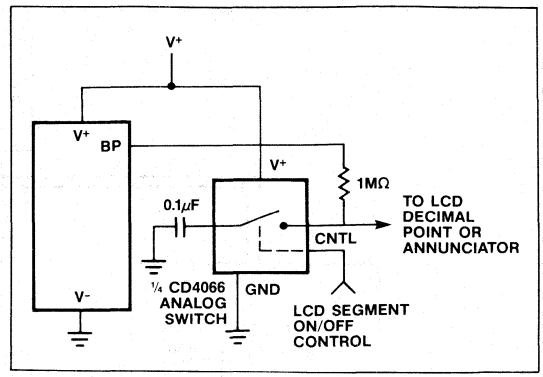


Figure 6D. Analog Switch for Decimal Point Drive

If the value of the integrator capacitor or integrator resistor is too low, ±full scale inputs will cause the integrator to saturate as it attempts to drive above V^+ or below V^-. If this occurs, operation will appear normal for low input voltages, but the conversion results for higher output voltages will be less than full scale.

Very low integrator swing will increase the amount of noise or "flicker" of the conversions. A full scale integrator swing of ±1V is sufficient to avoid any significant degradation of the noise performance, and should be used for operation with a 5V supply.

Reference Capacitor

For most circuits a reference capacitor value of 0.1µF is adequate. However, a larger value is needed to prevent rollover error if there is significant stray capacitance at the reference capacitor terminals. Minimize the stray capacitance on the reference capacitor terminals to reduce the rollover error, and if necessary, increase the reference capacitor value to 1.0µF.

The printed circuit board should be carefully cleaned to minimize leakage at the C_{REF} terminals since leakage will cause both gain and rollover errors. Due to the increased leakage of the MAX130 and MAX131 at +70°C, a 1.0µF reference capacitor is recommended to reduce rollover and gain errors at high temperature.

The reference capacitor is typically a low leakage film capacitor. Polyester (Mylar) is acceptable in applications where the reference voltage is constant. A low dielectric absorption capacitor such as polypropylene should be used if the reference voltage is variable, since any dielectric absorption will increase the settling time in response to a change in reference voltage. Since the reference voltage varies in circuits which measure resistance ratiometrically, a polypropylene reference capacitor should be used in ohmmeters.

Autozero Capacitor

The noise of the A/D is influenced by the autozero capacitor. For the best noise performance, an autozero capacitor value of at least 4 times the integrator

capacitor value is recommended. For a 2V scale, a 0.047μF (47nF) capacitor is adequate. An autozero capacitor of 0.47μF or greater is recommended for a 200mV full scale. All of Maxim's integrating A/D converters have a Zero Integrator phase which allows the use of high values for the autozero capacitor without causing hysteresis or slowing the overload recovery time.

The autozero capacitor can be any low leakage film capacitor in most applications. A low dielectric polypropylene capacitor is recommended if there are rapid changes in common mode voltage, or if the A/D must rapidly stabilize upon power-up.

Oscillator Components, MAX130 and MAX131

For three conversions per second either use 100kΩ R_{OSC} and a 100pF C_{OSC}, or use a 180kΩ R_{OSC} and a 50pF C_{OSC}. The MAX130 test circuits show 100kΩ/100pF and the MAX131 test circuits show 180kΩ/50pF, but both A/Ds will operate correctly with either set of components. Other conversion rates can be set by changing the oscillator components. Each conversion takes 16,000 oscillator cycles, and the oscillator frequency is approximated by the equation $f_{OSC} = 0.45/RC$, where $C = C_{OSC} + 5pF$.

Typical part-to-part variation of oscillator frequency is ±5%, and the typical variation with temperature is an decrease in frequency of 3% at 70°C, and an increase in frequency of 1% at 0°C. Normal mode rejection of 50Hz and 60Hz can be improved by driving the OSC1 pin with an external clock signal of precisely 40.00kHz. The OSC1 pin is the input of a CMOS inverter powered from V^+ and the Test pin voltage. Either drive OSC1 directly with a signal that swings from the Test voltage to V^+, or drive it via an AC-coupled 2Vpk-pk to 5Vpk-pk signal.

Application Notes

Common Mode Voltage Range Considerations

In many applications In Lo is connected to Common, and the supply voltage is greater than 6V. In these cases the common mode voltage range restrictions on In Hi and In Lo will not be a design consideration. On the other hand, operation with low supply voltages, or operation with either In Lo or In Hi near either supply calls for careful evaluation of the effect of common mode voltages.

Since the MAX131 performs all conversion phases, including autozero and deintegration, using In Lo as the reference point, the MAX131 has excellent common mode rejection of approximately 120dB. The MAX130 uses the Common voltage as the reference point for autozero and deintegration and the common mode rejection ratio of the MAX130 is about 86dB.

There are four basic internal limitations on the allowable common mode voltage (see Figures 3 and 4):

1) The buffer input CMVR is (V^- + 1.5V) to (V^+ - 1.5V).
2) The integrator CMVR is (V^- + 1.5V) to (V^+ - 1.5V).
3) The integrator output swing is limited to V^- to V^+.
4) The MAX130 In Lo must not go more than 1.0V above Common.

Figure 3 shows that the MAX130 buffer input can be connected to either In Hi, (Common + V_{REF}), or (Common - V_{REF}), where V_{REF} is the differential reference voltage between Ref Hi and Ref Lo and is independent of the Common voltage at Ref Hi and Ref Lo. Further inspection shows that the integrator is connected either to In Lo (during Integrate) or Common (during deintegrate).

Figure 4 shows that the MAX131 buffer input can be connected to either In Hi, (In Lo + V_{REF}), or (In Lo - V_{REF}). The integrator non-inverting input is always connected to In Lo.

Combining the four system CMVR limitations with the possible connections results in the limitations shown in Table 1.

Operation with Low Supply Voltages

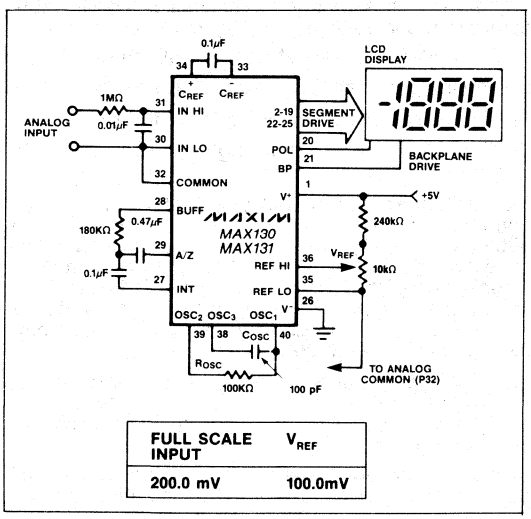
Unlike the ICL7106 and ICL7136 which use a 6V to 7V zener to generate their Common voltage, the MAX130 and MAX131 use a bandgap reference. Therefore the MAX130 and MAX131 generate an accurate Common voltage with supply voltages as low as 4.5V. Operation with a 5V supply, though, does require attention to both the common mode voltage range of the buffer, and the output swing limitations of the integrator. In particular, the input common mode voltage range does not include the negative supply voltage. Maxim's MAX138, which includes a charge pump voltage inverter and requires only slight circuit modifications of a MAX130/ICL7106 circuit, is recommended for +5V single supply applications where a ground-referred signal is to be measured.

Table 1. Common Mode Voltage Limits

DEVICE	IN HI	IN LO	INTEGRATOR SWING
MAX130 with Positive Input Voltages	V^- + 1.5V to V^+ - 1.5V	V^- + 1.5V to V_{COMMON} + 1.0V	(In Lo - V^-) or (V_{COMMON} - V^-), whichever is smaller.
MAX130 with Negative Input Voltages	V^- + 1.5V to V^+ - 1.5V	V^- + 1.5V to V^+ - 1.5V	(V^+ - In Lo) or (V^+ - V_{COMMON}), whichever is smaller.
MAX131 with Positive Input Voltage	V^- + 1.5V to V^+ - 1.5V	V^- + (1.5V + V_{REF}) to V^+ - 1.5V	(In Lo - V^-)
MAX131 with Negative Input Voltage	V^- + 1.5V to V^+ - 1.5V	V^- + 1.5V to V^+ - (1.5V + V_{REF})	(V^+ - In Lo)

3½ Digit A/D Converters with Bandgap Reference

Figure 7 shows typical components for +5V single supply MAX130/131 operation with a 200mV full scale range. Since the common voltage is 3.05V below V^+, it is less than 2V above ground. This means that the integrator swing must be reduced by increasing the value of the integrator capacitor. The value shown will result in about 1V to 1.5V integrator swing.



FULL SCALE INPUT	V_{REF}
200.0 mV	100.0mV

Figure 7. Single Supply +5V Operation

The voltage at the buffer input must stay in the common mode voltage range of (V^- + 1.5V) to (V^+ - 1.5V). With the maximum common voltage of 3.15 and a full scale negative input of -200mV, this limit is met with a 4.85V or greater supply.

With a 2V full scale, the input buffer will exceed its negative common mode voltage range when a -2V input is applied with less than 6.7V supply voltage.

Operation on ±5V Supplies

The MAX130/131 can easily be used with ±5V supplies. Connect V^+ to +5V, V^- to -5V. If the voltages to be measured are referred to ground, then connect In Lo to ground. In most cases, Ref Hi and Ref Lo should be connected to a resistive divider string between V^+ and Common, as shown in the standard application circuits of Figures 1 and 2. If Common is not used to generate the reference it can either be left floating or can be connected to ground. If the MAX130/131 oscillator is driven by 5V logic, or if the MAX130/131 LCD outputs drive 5V logic, then connect the Test pin to ground. If the MAX130/131 open circuit Test voltage is above ground, then connecting Test pin to ground will set the internal digital ground to approximately ground. If, however, the open circuit Test voltage is negative, then the internal digital ground voltage will remain negative, additional V^+ supply current will be drawn, and the LCD segments will continue to swing below ground. The OSC1 pin, however, will respond to a voltage swing of 0V to 5V in either case.

Low Battery Detector Circuit

Since the voltage between Common and V^+ is between 2.95V and 3.15V until the voltage between V^+ and V^- falls to less than 4V, a simple low battery detector can be made using a transistor voltage detector as shown in Figure 8. When Q2 is off the Low Battery segment is driven in phase with the backplane and is off. When Q1 and Q2 turn on, the Low Battery segment is held approximately midway between the Test voltage and V^+, and the Low Battery LCD segment becomes visible. Q1 and Q2 turn on when the voltage at the base of Q1 is one base-emitter voltage more positive than Common voltage. With the 4.7MΩ/4.7MΩ divider shown, this occurs when the battery voltage is approximately 6V. Decrease the value of R1 to lower the battery detection voltage.

A similar circuit using only one transistor can be made using the Test pin as the reference voltage rather than Common. Since the Test pin voltage may range from 4V to 6V, the low battery detection voltage when using the Test pin as a reference is not as accurate as Figure 8, which uses the Common voltage as the reference.

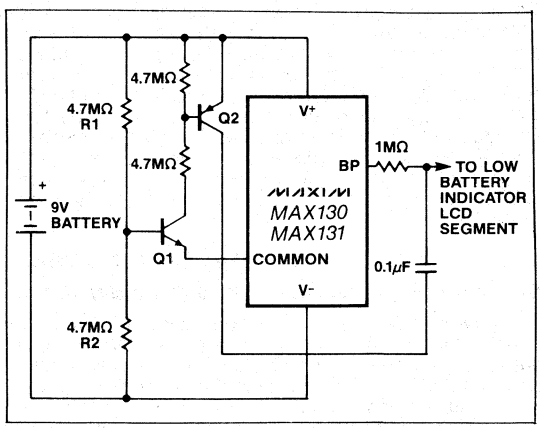


Figure 8. Low Battery Detector and LCD Segment Drive

Common Problems and Their Solutions

Erratic, Unpredictable Readings

Make sure that In Lo is connected to Common. Leaving both In Lo and In Hi floating with respect to Common and the power supplies will cause erratic readings since In Lo and In Hi will unpredictably float from V^+ to V^- unless a DC connection between either In Lo or In Hi and Common is provided.

Look at the INT (pin 27 of the 40 pin DIP) with an oscilloscope. With 0V input the INT pin should be at approximately the same voltage as the In Lo pin.

With a full scale input voltage the INT pin voltage should be a triangular waveform. If no triangular waveform is seen, or if it is not in the 2Hz to 4Hz frequency range, then review the oscillator circuit connections and components to make sure they are correct.

Overload Display

The least significant three digits are blanked if the input voltage exceeds full scale. The leading "1" is displayed for positive overloads, and a "-1" is displayed for negative overloads. Any of the conditions that cause erratic readings as discussed above may cause overload readings. In addition, check the differential voltage between In Hi and In Lo and make sure that it is no more than twice the differential voltage between Ref Hi and Ref Lo. Also make sure that the voltage at Ref Hi is more positive than the voltage at Ref Lo, since incorrect reference polarity will always cause an overload reading.

Gross Nonlinearity

If the results are linear for low input voltages, but the displayed result stops increasing as higher input voltages are applied, then the most likely cause is saturation of the integrator output. With a full scale voltage applied, look at the voltage on the INT pin. It should not come closer than 0.3V to either supply. Increase the integrator capacitor value if the INT output swing is excessive. Alternatively, increase the oscillator frequency by changing the oscillator resistor and capacitor values.

Nonlinearities of 2 to 20 Counts

A polyester (Mylar) integrator capacitor will result in about 2 or 3 counts of nonlinearity at full scale. Use polypropylene for best linearity. Leakages into the integrator capacitor, the autozero capacitor, or the reference capacitor will also cause linearity errors. Make sure that printed circuit boards are thoroughly cleaned after soldering.

Gain Error and Rollover Error

A gross gain error will result if the integrator output current capabilities are exceeded. Make sure that $R_{INT} \geq V_{REF}/2.5\mu A$ for the MAX130, and $\geq V_{REF}/0.6\mu A$ for the MAX131.

Gain errors less than ten counts are generally caused by either too much stray capacitance on the C_{REF} terminals, or by excessive printed circuit board leakage. Stray capacitance and leakage can be detected by reducing the reference capacitor by a factor of ten. If the error dramatically increases, then either stray capacitance or leakage at the reference capacitor terminals is the culprit. Error caused by stray capacitance tend to be a pure gain error, while errors due to leakage tend to be nonlinear—typically square law. Errors due to leakage can also be detected by cleaning the board, then baking to reduce moisture content.

Offset Errors, or Non-Zero Reading with 0V Input

This type of error is most often caused by leakages into the input pins, the integrator capacitor, or the autozero capacitor.

A very high clock rate can also make the MAX130 and particularly the MAX131 show ±001 with 0V input. Either return the oscillator frequency to the standard 40 or 48kHz range, or if a higher clock frequency must be used, then put a resistor of a few hundred ohms in series with the integration capacitor.

The MAX130/131 have better performance with low integrator swing than do the ICL7106 or ICL7136, but extremely low integrator swing may still result in a non-zero reading with 0V input. Increase integrator swing to at least ±0.5V with a ±full scale input, with ±2V swing being preferred.

Missing Segments on the LCD Display

This is very, very rarely a problem of the MAX130/131. More often it is caused by open circuits in the LCD connector/bezel, particularly if an elastomeric connector (zebra strip) is used. Check the voltage waveform at the pins of the MAX130/131. A signal in-phase with the backplane turns off an LCD segment, a signal 180° out of phase from the backplane turns on an LCD segment.

Noisy Readings

The most common reason for noisy readings, particularly in engineering labs, is simply that the input signal is noisy. The 1MΩ/10nF input filter shown in Figures 1 and 2 will significantly reduce high frequency noise, and the capacitor value can be increased to further attenuate 50/60Hz.

If the input signal is clean, then the next thing to check is integrator swing since low integrator swing will increase the noise. If the integrator swing must be reduced to less than 1V for some reason, then increasing the value of the autozero capacitor will improve the noise performance. For most circuits, the integrator swing should be approximately ±2V.

A very low value for the autozero capacitor will also make the readings noisy. The value of the autozero capacitor should be at least twice the value of the integration capacitor, and increasing the autozero capacitor value to between 4 and 10 times that of the integrator capacitor will improve the noise performance, particularly with low reference voltages.

Stray coupling of noise signals, either digital/microprocessor noise or 50/60Hz and 100/120Hz ripple can also be a cause of noisy readings. The circuit area most likely to pick up stray signals is the autozero capacitor. The distance between the autozero capacitor and the AZ pin should be minimized, as should the distance between the autozero capacitor and the integration resistor and capacitor. If possible, use a ground plane around the sensitive analog section that includes C_{INT}, C_{AZ}, and R_{INT}. Since the BUFF and INT pins are the outputs of op amps, they are less sensitive to noise pick-up than is the AZ pin, which is the input of an op amp. Orient the integration capacitor such that its outer foil is connected to the INT pin.

3½ Digit A/D Converters with Bandgap Reference

The MAX131, unlike the MAX130, is sensitive to AC noise at In Lo during the de-integrate phase. In particular, full wave AC-DC converters should be used with the MAX131 only if both outputs of the AC-DC converter output are well filtered.

The Common outputs of the MAX130 and MAX131, being derived from a bandgap reference, are noisier than the ICL7106 and ICL7136 Common outputs, which are derived from zeners. This could cause an increase in conversion noise, but only if the C_{REF} is less than 0.1μF, and there is no bypassing at the reference inputs.

Poor bypassing of the supply voltage may cause a couple of counts of noise in the readings, particularly if the power supply also powers digital logic, since high frequency spikes on the power supply might cause the comparator to falsely indicate zero crossing one or two clock cycles early. Ordinary 0.1μF bypass capacitors are adequate in most cases. Since the MAX130 and MAX131 draw very little current, a simple RC filter can be used to provide greater spike and ripple attenuation in those cases where the power supply is exceptionally noisy.

Since the oscillator frequency is slightly affected by the supply voltage, large changes in the supply voltage during a conversion may cause a few counts of error. A typical case where the effect must be considered is in a battery powered circuit where the battery is also being used to drive high current loads such as motors or lamps. For extreme cases where high current loads momentarily change the battery voltage a volt or more, use a series diode and a capacitor of 10μF or greater.

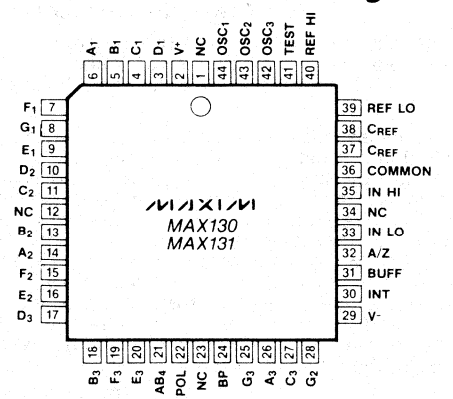
Application Hints

1. See the ICL7136 and ICL7106 data sheets for a variety of application circuits which can also be used with the MAX130 and MAX131.
2. In some applications it may be useful to apply a fixed reference voltage between In Hi and In Lo, and to apply the signal to Ref Hi and Ref Lo. In this mode of operation the displayed reading is inversely proportional to the input voltage. In other words, the displayed reading is the result of *dividing* the fixed reference voltage by the signal voltage. A typical application where this function is useful is in an RPM meter, where a voltage proportional to the period of a signal is divided into a fixed voltage to convert period into RPM (frequency). Another example is in a conductance meter, where the conversion between ohms and Siemens is performed by swapping the positions of the unknown and reference resistors.
3. A serial output pulse stream can be obtained from the MAX130/131 by monitoring the voltage at the C_{REF} terminals as shown in the circuit of Figure 23 in the ICL7106 data sheet. Use an AND gate to combine the resulting End-of-Conversion signal with the oscillator output from OSC3, pin 38.
4. If the input signal polarity is reversed from the desired polarity, then use the "Minus" segment to drive the vertical bar of a plus sign, and permanently turn on the horizontal bar of the plus sign using one of the decimal point driver circuits of Figure 6. When the MAX130/131 measures a negative polarity, a "+" will be displayed. When the MAX130/131 measures a positive polarity, then a "-" will be displayed. (Normal operation of the MAX130/131 is no polarity indication for a positive input, and a "-" sign for a negative input.)
5. It is not normally practical to multiplex one LCD display between a MAX130/131 and another IC, since this requires an analog switch in series with every LCD segment. One design alternative is to convert all signals to pulse streams (see #3, above), then to multiplex the pulse streams into a counter/LCD driver such as the ICM7224. Another alternative is to use a BCD output A/D converter such as the ICL7135 in combination with the ICM7211 display driver.

Ordering Information (Continued)

PART	TEMP. RANGE	PACKAGE
MAX131C/D	0°C to +70°C	Dice
MAX131EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX131EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier
MAX131ACPL	0°C to +70°C	40 Lead Plastic DIP
MAX131ACQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX131AEPL	-40°C to +85°C	40 Lead Plastic DIP
MAX131AEQH	-40°C to +85°C	44 Lead Plastic Chip Carrier

Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

MAXIM
3¾ Digit DMM Circuit

General Description

The MAX133 and MAX134 are integrating A/D converters for 3¾ digit multimeters and data acquisition systems such as data loggers and weigh scales. The A/D's internal resolution is ±40,000 counts. An extra digit is supplied as a guard digit to allow autozero or tare of a 4000 count displayed reading to 1/10 of a displayed count. The conversion time is 50ms.

The MAX133 and MAX134 differ only in their microprocessor interface. The MAX133 has a 4 bit multiplexed address/data bus while the MAX134 has 3 separate address lines and a 4 bit bidirectional data bus. Both devices can be used with 4, 8, and 16 bit microprocessors.

When controlled by a microprocessor, the MAX133 and MAX134 can perform auto-ranging measurements from ±400.0mV to ±4000V full scale. External attenuator resistors are required, but range switching is performed by the A/D.

The power supply is typically a 9V battery or ±5V. Operating current is typically 100μA while standby current in only 25μA.

Applications

Digital Panel Meters
Weigh Scales
Data Loggers
Data Acquisition Systems

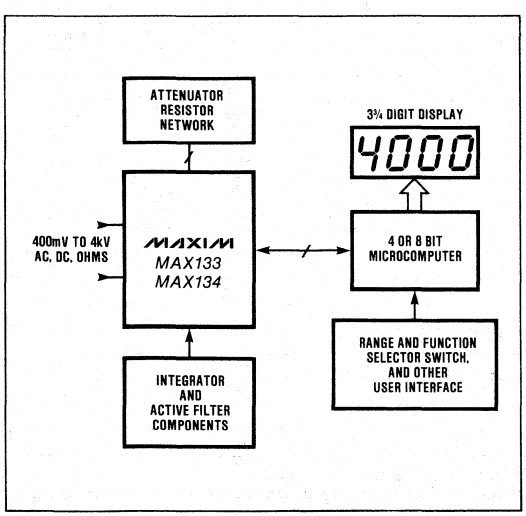
Features

- **40,000 Count Resolution**
- **0.025% Accuracy**
- **20 Conversions per Second**
- **Microprocessor Interface**
- **100μA Operating Supply Current**
- **Low External Component Count**
- **5μV Resolution**
- **Demonstration Kit Available MAX134/DEMO**

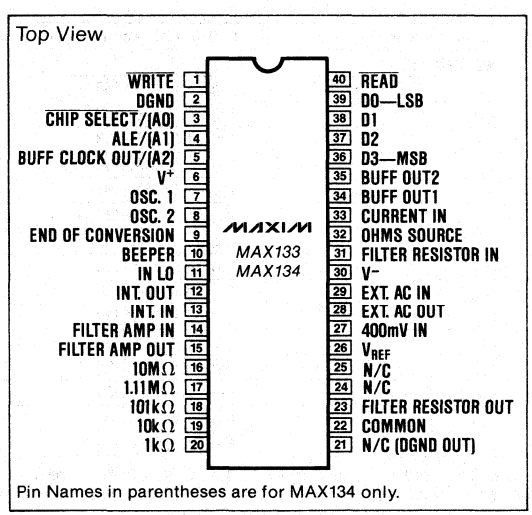
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX133CPL	0° C to +70° C	40 Lead Plastic DIP
MAX133CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX133C/D	0° C to +70° C	Dice
MAX133EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX133EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier
MAX134CPL	0° C to +70° C	40 Lead Plastic DIP
MAX134CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX134C/D	0° C to +70° C	Dice
MAX134EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX134EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier

Typical Operating Circuit



Pin Configuration



Pin Names in parentheses are for MAX134 only.

3¾ Digit DMM Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V^+ to V^- ..... +15V
- V^+ to DGND ..... +6V
- V^- to DGND ..... -9V

Analog Input Voltage (any input) (Note 1) ..... V^+ to V^-

Reference Input Voltage ..... V^+ to V^-
Digital Inputs ..... (DGND - 0.3V) to (V^+ + 0.3V)
Power Dissipation 800mW
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ANALOG					
Zero Input Reading	Read Zero Mode, DC Volts Zero Input Offset Reading will be corrected Digitally in the µP			±5000	Count
ΔZero Input Reading	Difference between 1000VDC Scale, V_{IN} = 0 and 3VDC and Scale, V_{IN} = 0 (Note 3)	-2		+2	Count
$I_{10M\Omega}$	Leakage Current into 10MΩ Pin			20	pA
Rollover Error	$\|V_{IN}+\|$ = $\|V_{IN}-\|$ = 3V	-10		+10	Count
Integral Linearity	Best Fit Line 300mVDC Scale Not production tested	-10		+10	Count
Differential Nonlinearity	Deviation from ideal Count size Not production tested		0.1	5	Count
Recovery Time	Number of Conversions to settle to within 2 Counts of final reading on 3 VDC Scale after attempting to measure a 2.95V Input on the 300mV Scale. Unfiltered DC Mode Settle to 1 Count		1 2		Conv.
CMRR	V_{CM} = ±500mV V_{CM} is (IN LO - Common)		86		dB
Noise	300mVDC Scale Zero Reading Mode Pk-Pk Value exceeded less than 5% of readings		2 2		Count
Zero Reading Drift			0.1		Count/°C
Scale Factor Tempco	300 mVDC scale 0ppm ext Reference			5	ppm/°C
AC TIMING					
t_{AL}	Figure 5, MAX133		130		ns
t_{CC}	Figure 5, MAX133		60		ns
t_{LA}	Figure 5, MAX133		-100		ns
t_{LC}	Figure 5, MAX133		1500		ns
t_{LL}	Figure 5, MAX133		20		ns
t_{RD}	Figure 5, MAX133		100		ns
t_{CL}	Figure 5, MAX133		-130		ns
t_{DW}	Figure 5, MAX133		100		ns
t_{ACC}	Figure 4, MAX134		3250		ns
t_{EN}	Figure 4, MAX134		80		ns
t_{OP}	Figure 4, MAX134		80		ns
t_{AS}	Figure 4, MAX134		2500		ns
t_{DS}	Figure 4, MAX134		150		ns
t_{DH}	Figure 4, MAX134		-75		ns
t_{AH}	Figure 4, MAX134		-85		ns

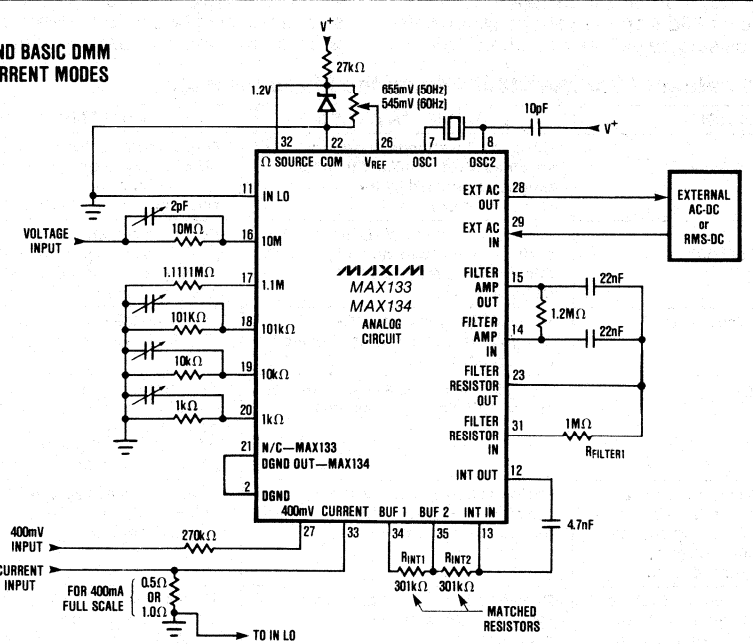
Note 1: Input Voltage may exceed supply voltages, provided the Input Current is limited to ±1mA.
Note 2: Analog performance is specified in counts relative to a 40,000 count full scale; i.e. a spec of 5 counts would correspond to 1/2 of one count on a 3¾ digit meter.
Note 3: This parameter is guaranteed by testing the input bias currents of the input pins 10MΩ and 1.11MΩ.

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY AND DIGITAL SECTION						
Digital Ground Voltage	DGND	Referenced to V^+ $5\mu A < I_{SINK} < 500\mu A$	-4.5	-5	-5.5	V
Analog COMMON Voltage		(V^+ - Common) 250kΩ between V^+ and COMMON	2.8	3.0	3.3	V
Analog COMMON Sink Impedance		ΔV, I_{COMMON} = 10μA to I_{COMMON} = 2mA		4	20	Ω
Analog Common Source Capability		For $\Delta V_{COMMON} < 0.5V$		1		μA
Tempco of Common				80		ppm/°C
Output High	V_{OH}	D_{0-3}, Data Ready I_{OUT} = -100μA	V^+ - 0.5			V
Output Low	V_{OL}	D_{0-3}, Data Ready I_{OUT} = 400μA			0.4	V
Input High	V_{IH}	D_{0-3}, A_{0-3}, Data Ready, RD, WR	70	45		% (V^+ - DGND)
Input Low	V_{IL}	D_{0-3}, A_{0-3}, Data Ready, RD, WR		1.6	0.8	V
Supply Current	I_{SUPP}			100	250	μA
Sleep Current	I_{SLEEP}			25		μA
Low Battery	V_{LBAT}	Low Battery Flag On	6.3	6.8	7.5	V

TEST CIRCUIT AND BASIC DMM VOLTAGE AND CURRENT MODES



NOTE: Pin Numbers are for the 40 Lead DIP.

3¾ Digit DMM Circuit

System Considerations

The MAX133/134 is intended for use with a microprocessor. The MAX133/134 contains an A/D and auxilliary circuitry such as attenuator range switches, a piezoelectric beeper driver, an active filter, a low battery detector, and both analog and digital power supplies; but it does not include any display drive capability. The MAX133/134 reduces the component count and system cost by minimizing the external components required for the analog portion of the system, but does not restrict final product features by including autoranging or other digital control functions. The MAX133/134 is intended to work as the analog front end of a microprocessor, with the features of the end product being determined by the microprocessor software. Table 1 shows how the execution of several typical functions is partitioned between the MAX133/134 and the microprocessor.

The MAX133/134 provides all of the logic and counters for control of the conversion sequence, and the external microprocessor does not have to perform any critical timing or complex control of the MAX133/134. The MAX133/134 has range switches for a 5 decade attenuator which uses external resistors, and has additional mode-selection circuitry for performing voltage, current, AC or DC, ohms, and continuity measurements. The 5 decade attenuator and mode-selection circuitry is controlled by an external microprocessor via control bits written into the MAX133/134.

The MAX133/134 has normal mode rejection of line frequency of at least 80dB on the voltage ranges; the microprocessor selects rejection of either 50Hz or 60Hz by setting a MAX133/134 control bit. A two pole active filter can also be turned on by the microprocessor, adding about 40 dB normal mode rejection above 50Hz. See the "Digital Interface" section for details on which functions can be controlled by the external microprocessor.

The basic blocks of the MAX133/134 are

- A/D section
- Input Range Switching
- Ohms Circuitry
- Active Filter
- Power Supply, Common, Low Battery Detector
- Oscillator and Beeper Driver
- Digital Interface

A/D Section

The A/D uses a "residue multiplication" conversion scheme to provide a full ±40,000 count resolution reading every 50 milliseconds, while still providing the excellent noise performance and power line normal mode rejection associated with integrating A/Ds. See "Conversion Method and Timing" below for details of the conversion method. All timing and A/D conversion phase control is performed by the MAX133/134 without microprocessor intervention. The A/D section will perform a non-zero-corrected conversion every 50 milliseconds (20 conversions per second).

The microprocessor must periodically direct the MAX133/134 to perform a read zero conversion, which also takes 50 milliseconds. This read zero conversion is a conversion performed with IN LO internally

Table 1. Coordination of the MAX133/134 and the Microprocessor

FUNCTION	MAX133/134 ACTION	MICROPROCESSOR ACTION
Autoranging	Contains the attenuator control switches. Selects 400mV to 4000V ranges as directed by the microprocessor.	Detects overload and commands the MAX133/134 to select the next higher range. Range switching hysteresis and manual range selection is controlled by the microprocessor.
Zero Reading (system offset correction)	Internally shorts the A/D inputs and performs a measurement of system offset when directed by the microprocessor.	Periodically commands the MAX133/134 to perform a zero reading. Subtracts this zero reading from normal readings to correct for the internal offset of the MAX133/134.
Range/Function Selection	Selects Ohms/Current/ AC-DC/Voltage/Continuity as directed by the microprocessor.	Maintains the user interface, and directs the MAX133/134 to select the desired range.
Display of Readings	Max 133/134 provides raw, non-zero-corrected data to microprocessor.	The microprocessor performs zero correction and any gain correction or scaling that is desired. The microprocessor then displays the information, using either its own display driver capability or an external display driver.
Value added DMM features such as display hold, peak hold, either manual range selection or autoranging, peak reading hold, min/max display, thermocouple linearization, etc.	Performs conversions as directed by the microprocessor, returning the A/D results to the microprocessor.	Uses the MAX133/134 conversion results and software routines to provide a multitude of product features.
Digital panel meter features such as zero and span adjustment, high/low limit alarms, display in engineering units, etc.	Performs conversions and range selection as directed by the microprocessor.	Takes the MAX133/134 readings, performs zero offset and scale corrections, then displays the results. The microprocessor also performs such functions as high/low limit alarms.

shorted to IN HI, and the result of this zero conversion must be subtracted (by the microprocessor) from normal measurements to obtain a zero-corrected reading. The zero correction that must be subtracted is determined by the MAX133/134's internal offsets. Since these offsets are relatively slow changing, zero conversion readings need only be taken often enough to track long term drifts and temperature changes. The zero conversion reading will change slightly with a change in common mode input voltage or reference voltage, and a new zero conversion reading should be taken if either of these change.

In ratiometric ohms measurement the reference voltage will change significantly as the value of the unknown resistor varies. To reduce the errors caused by the system offset the MAX133/134 "chops" the input buffer and integrator. The "chop" consists of a reversal of the input transistors during the conversion cycle. The timing of this chop is such that in the R/2 or ohms measurement mode, the system offset is almost completely nulled out if the X2 mode is not selected. Even if the X2 mode is selected, the system offset does not exceed 5000 counts on any range. Since the internal full scale range of the MAX133/134 is greater than ±49,000 counts, at least ±40,000 counts of resolution are available after zero offset correction.

Each conversion result is latched into a Conversion Register which can be read by the microprocessor. The data format is nines complement BCD (a zero reading is 00000, a -1 reading is 99999, a -25000 reading is 75000). The nines complement form is the most convenient BCD format since the addition of the nines complement of a number is equivalent to subtracting that number. See "Software Notes" for simple BCD to binary conversion algorithms.

The last digit of conversion is used for digital autozero and is usually not displayed. Note that each count of the least significant digit of the MAX133/134 output corresponds to 1/10 of a count if a 4000 count full scale display is used. For current ranges with a voltage drop of only 200mV, the measured reading can be multiplied by two by using the X2 ("times 2") function of the MAX133/134. The X2 function reduces the R_{INT} resistor value by a factor of two during the Integrate phase. With the X2 range, a 200mV input voltage will result in a full scale, 4000.0 measured reading. Alternatively, the normal 400mV range can be used, with the multiplication by two being done by the microprocessor digitally. In this case, each count of the least significant digit is 1/5 of a displayed count. A 100mV full scale voltage drop can be achieved by using both the MAX133/134 X2 range and a digital times 2 multiplication in the microprocessor.

Each of the 20 conversions per second has a Zero Integrator phase to ensure rapid recovery from overload, and the MAX133/134 will recover to within 2 counts one conversion after an overload of 10 times full scale when the onboard active filter is not used.

Input Range Switching

In voltage measurement ranges other than 400mV, voltages are applied to the pin labeled 10MΩ through a 10MΩ resistor. By selecting the proper shunt resistors (1.1MΩ through 1KΩ) the input voltage will be attenuated to a 400mV range. The input attenuator switch section includes analog switches to switch both the input current and to sense the voltage on the shunt resistor. Other input switching functions select between the output of the input attenuator and the voltage developed across the current sensing resistors during current measurement. See Figure 1.

The 5pA input bias current of the MAX133/134 might result in unacceptable errors with a 10MΩ input resistor on the 400mV scale, so a separate pin with a 100kΩ to 1MΩ input resistor is used for the 400mV scale. The 10MΩ resistor used on the higher voltage ranges does not cause appreciable error since the input leakage current is shunted to ground through the 1.11MΩ to 1kΩ attenuator shunt resistors.

To avoid errors that might occur through coupling of high frequency, high voltage signals from the input of the attenuator to the low level 400mV and Current inputs, these two inputs have 10kΩ switches which connect them to Common whenever they are not selected.

The input section also includes switches to allow an external AC-DC converter to be inserted into the signal path. Figure 10 shows a typical average-sensing RMS-calibrated AC-DC converter.

Ohms and Diode Measurement

The input attenuator resistors are also used as reference resistors in the ohms mode. Note that the 10MΩ resistor must be externally paralleled with the other resistors to get exactly 1MΩ, 100kΩ, etc. The ohms source buffer input is usually connected directly to the external bandgap reference or to another 1.25V source. In the 4kΩ through 40MΩ ranges there will be a total of 1.25V across the series combination of reference resistor, unknown resistor, and the input protection network; and the maximum voltage across the unknown resistor at full scale will be less than 400mV. On the 400Ω range, the ohms voltage source is a diode connected to V^+ through a 2kΩ p-channel switch. With a 3V Common voltage, this supplies approximately 2.2V across the series combination of reference resistor, unknown resistor, and input protection network. This higher voltage is used on the 400Ω range to compensate for the decrease in reference voltage caused by the input protection network. The MAX133/134 are designed to operate with PTC protection resistors of 2kΩ or less.

The voltage across the reference resistor is used as the reference voltage for the A/D when in the ohms mode, and the differential voltage between IN LO and IN HI is the input signal. The integration period is 500 counts, independent of the 50/60Hz control bit setting.

3¾ Digit DMM Circuit

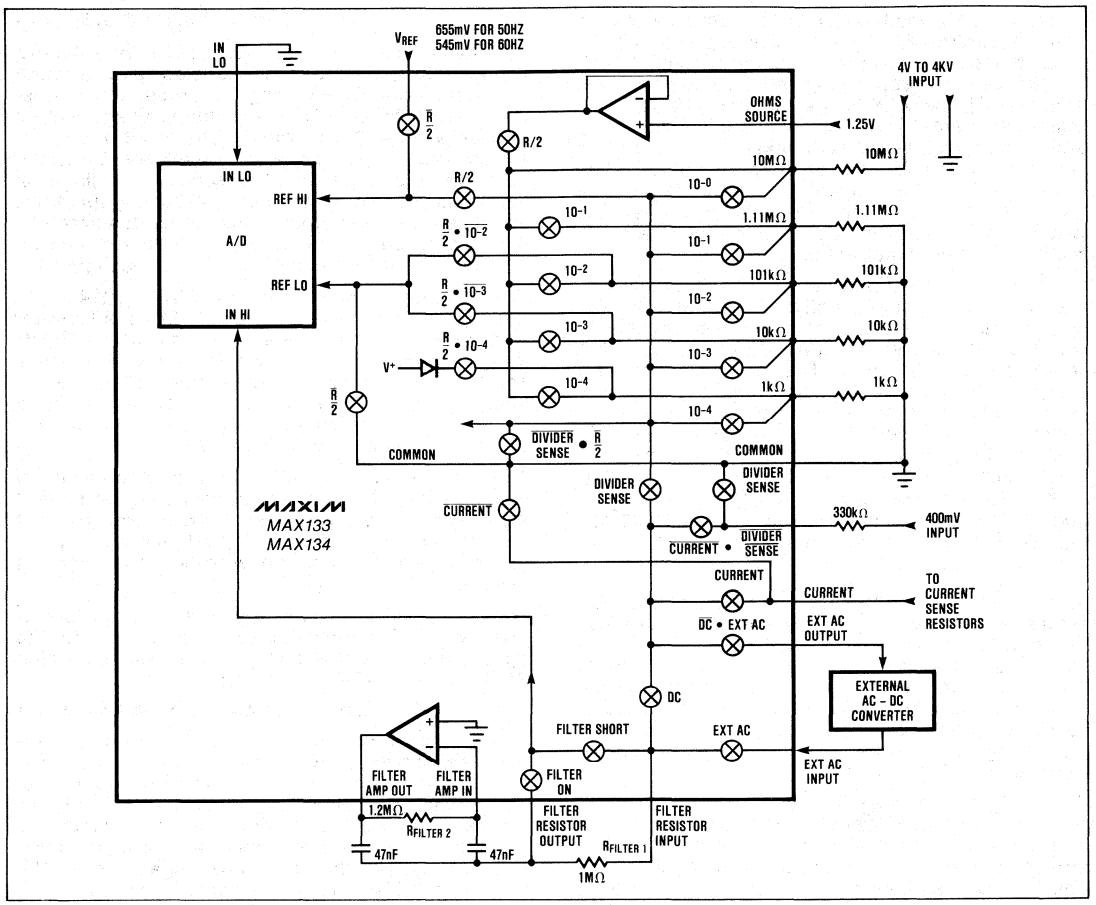


Figure 1. MAX133/134 Input Section

The digital output code is

$$50000 \times \frac{R_{UNKNOWN}}{R_{REF}}$$

with a maximum non-zero-corrected output code of ±49,520 and a maximum zero reading of 5000.

A 1kΩ reference resistor is used for the 400Ω full scale, a 10kΩ reference for a 4kΩ full scale, etc. A 10MΩ reference resistor is used for both the 4MΩ full scale and the 40MΩ full scale. To get the correct results in the ohms measurement or R/2 mode, the conversion result must be multiplied by two either digitally by the microprocessor or by using the X2 range, except on the 40MΩ scale. The 40MΩ range has the same reference resistor as the 4MΩ range but a times 10 scale factor is obtained by not multiplying by 2, and by activating the ÷5 function. If the times 2 multiplication is performed by the microprocessor, the Read Zero offset of the MAX133/134 in the ohms mode will be just a few counts, and will be nearly independent of the value of the unknown resistor being measured. If the MAX133/134 X2 mode is used to multiply by 2, then frequent Read Zero readings should be taken, since the read zero offset is inversely proportional to the reference voltage, and the reference voltage varies as the resistance of the unknown resistor varies.

Since the input protection PTC resistor shown in Figure 2 reduces the reference and input voltage, particularly on the 400Ω scale, the PTC resistance should be as low as is possible while maintaining the desired level of protection. Greater than 2kΩ PTC resistance will increase the noise level of measurements on the 400Ω range.

Since the MAX133/134 does not use a reference capacitor, the only limit on the response time in the ohms mode is the active filter. Even when the active filter is turned off, $R_{FILTER1}$ is still connected, and the input voltage must charge the filter capacitors. This will generally be noticed only on the 4MΩ and 40MΩ ranges.

A diode test range can be implemented by simply connecting to V^+ the PTC used for input protection in the ohms ranges. The PTC then delivers approximately 1mA of current to the diode. The diode voltage can be measured either on the standard 4V scale, or on the 400mV scale with the ÷5 function activated to result in a 2V full scale. As always, the latched continuity circuit is active, and it will latch whenever the input voltage goes below approximately 100mV. The microprocessor can also test the measured voltage at the end of each conversion if a more precise detection of continuity threshold is desired.

Active Filter

The 2 pole active filter circuit is shown in Figure 3. The op amp's offset has no effect on the DC accuracy since the op amp is only AC coupled and the DC signal path is only through the passive 1MΩ resistor. Note that the active filter will limit the speed of response of the MAX133/134 to input voltage changes, and for that reason it may be desirable to disconnect the input filter during autoranging. Since the source impedance at the filter input varies with the input attenuator selected, the response time will be slower on the 4V range.

Oscillator and Beeper Driver

The MAX133/134 is designed to operate with a 32768Hz tuning fork crystal similar to the Statek CX-1V, using only one external capacitor and no external resistors. If desired, the MAX133/134's OSC1 pin can be driven externally.

The 32kHz clock is used internally as the clock for the sequence and measurement counters. The 32kHz clock is also divided down to 2048Hz and 4096Hz for driving a beeper. The beeper output swings from V^+ to V^- and can directly drive piezoelectric beepers. Two control bits set by the microprocessor select the frequency (2048 or 4096 Hz) of the beeper and turn it on or off. Since the beeper is controlled by the microprocessor, it can be used for both continuity indication and for an audible operator feedback signal for peak hold or range changes.

Power Supply: Common, Digital Ground, Low Battery Detector

Both the MAX133 and MAX134 can operate from either a nominal 9V battery or a ±5V supply. The maximum power supply current in DC voltage and DC current modes is 250μA, with a typical operating current of 100μA.

Analog Common is derived from a zener and is nominally 3.0V below V^+. For lowest cost applications the Common voltage, with a tempco of 80ppm/°C, may be usable as a reference. In most applications, a bandgap reference will be connected to Common, with a pullup resistor to V^+, and a voltage divider connected across the bandgap reference to generate the 545mV (60Hz operation) or 655 (50 Hz operation) reference voltage. In a battery powered meter, the Analog Common pin is used as the system ground reference point.

The MAX133 and MAX134 also generate a Digital Ground voltage, which is nominally 5V below V^+,

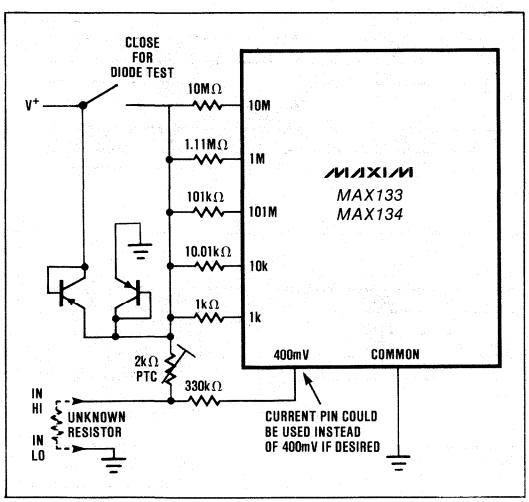


Figure 2. Ohms Mode and Diode Test

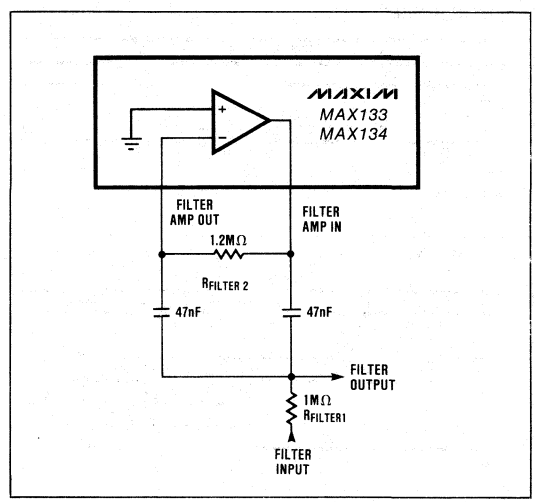


Figure 3. Active Filter

3¾ Digit DMM Circuit

and which will remain in the range of 5V ±10% while sinking 5μA to 500μA. The DGND generator has substantial current sinking capability, but can easily be pulled to a more negative voltage since the current sourcing capability is only 1 μA typical. The MAX133 internally connects the Digital Ground generator to the DGND pin. Normally the MAX133 is powered by a 9V battery and the Ground, V^-, or V_{SS} pin of the microprocessor is connected to the MAX133 DGND pin.

The MAX134 connects the DGND voltage generator to the pin, DGND Out, and the MAX134 DGND pin is an input only. For use with 9V batteries, externally connect the MAX134 DGND Out pin to the MAX134 DGND pin. For use with external ±5V power supplies, connect the DGND pin to ground, V^+ to +5V and V^- to -5V.

The MAX133/134 has an onboard low battery detect circuit that will indicate when the battery voltage is approaching the minimum operating voltage of the MAX133/134, which is approximately 6.8V.

Digital Interface

The MAX133 and MAX134 differ only in their digital interface. The MAX133 has a multiplexed address and bidirectional data bus, while the MAX134 has 3 separate address lines in addition to a bidirectional data bus. In both products, the data bus has 4 bits, allowing the use of the MAX133/134 with both 4 bit and 8 bit microprocessors.

MAX134 Digital Interface

The digital interface between the MAX134 and the controlling microprocessor is via a 4 bit bidirectional bus, D0-D3. In addition to the 4 data bus lines, there are 3 address lines and 2 control signals: A0-A2, $\overline{WR}$, and $\overline{RD}$.

The three address lines, A0-A2 select one of 5 control registers. When $\overline{WR}$ goes low, data will be written from the bus into the MAX134 control register addressed by A0-A2. When $\overline{RD}$ is low, the MAX134 will drive the bidirectional bus, placing on it the data contained in the results or status register addressed by the address inputs A0-A2. Figure 4 shows typical read and write sequences.

Digital Interface, MAX133

The MAX133 uses only 7 lines to interface with the microprocessor. The microprocessor first selects the register to be read or written to by placing the address of the register onto the 4 bit multiplexed address/data bus. The microprocessor then pulses the Address Latch Enable (ALE) line high to latch the register address into the MAX133. To read the selected register, the microprocessor then drives the Read line low, and the MAX133 places the register data onto the data bus. To write to the selected register the address is latched as described above, then the microprocessor places the data onto the bus and then pulses the Write line low. The MAX133 latches the data into the data into the selected register on the rising edge of Write. See Figure 5. The Chip Select ($\overline{CS}$) line must be low to enable either the $\overline{RD}$ or $\overline{WR}$ lines, but ALE is not gated by $\overline{CS}$.

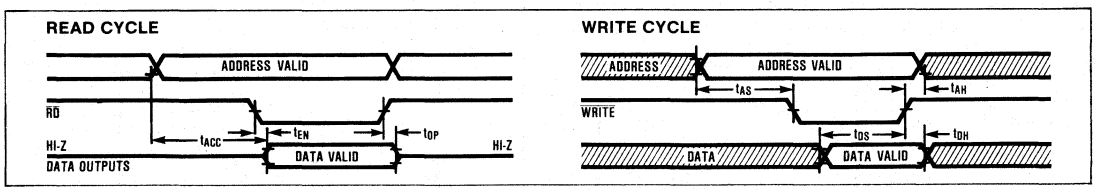


Figure 4. MAX134 Read and Write Sequence

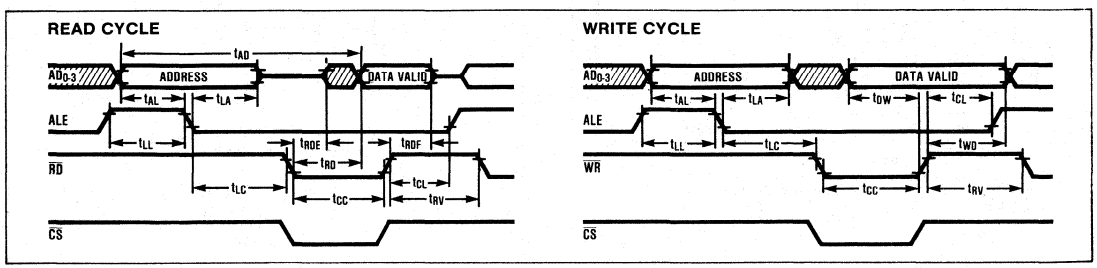


Figure 5. MAX133 Read and Write Sequence

Digital Interface, MAX133 and MAX134

In most cases, the EOC signal will be either monitored by an I/O pin, or it will drive an Interrupt pin on the microprocessor. In battery powered systems, it may be desirable to put the microprocessor into a sleep or standby mode until EOC goes high. The microprocessor then performs any required data processing and display updates, then reenters the sleep mode. This conserves battery power since the microprocessor power consumption is minimized.

The data that has been latched in the MAX133/134 control registers does not immediately affect operation. The input registers are double buffered, and the control bits take effect during the 21st clock cycle after EOC goes high. In the hold mode, the double buffered registers are transparent, and any updates to the registers take effect immediately, as do any changes made during the one clock cycle period at the end of each conversion during which the second rank of buffers are being updated.

Description of Output Bits

The data format is nines complement BCD. For example:

MEASUREMENT RESULT	BCD DATA
+40000	40000
—	—
+00100	00100
—	—
+00001	00001
+00000	00000
(there is NO -00000)	
-00001	99999
—	—
-00100	99900
—	—
-40000	60000

The Latched Continuity bit will be high if the input voltage has gone below the continuity threshold of approximately 100mV since the last time the register was read. Each time this register (Register 5) is read, the continuity latch is reset.

The Low Battery bit is high whenever the battery voltage is below the low battery detect voltage.

The $\overline{\text{Holding}}$ bit is low whenever the MAX133/134 is in the hold state.

Description of Control Bits

Hold. A 1 in Hold will stop conversions at the end of the next conversion. If the MAX133/134 is in the Hold mode, a conversion will start on the next clock cycle after Hold is set to 0. The oscillator continues to run and all circuitry is active during the Hold mode.

High Frequency. A 1 in the High Frequency bit will select 4096Hz as the beeper frequency. A 0 will select 2048Hz.

Beeper On. A 1 turns on the beeper driver.

Sleep. A 1 in Sleep puts the MAX133/134 into the standby or sleep mode. The Common voltage buffer is turned off and the internal analog circuits are turned off, but the DGND circuitry is still active. The oscillator continues to run. Current consumption is reduced to 25μA. Several conversions must be performed after exiting the Sleep mode before full conversion accuracy is obtained.

10-0 through 10-4. These bits control the attenuator network switches. The 10-0 bit selects the 10MΩ input without activating any shunt resistors. This is an alternate 400mV input. The 10-1 bit activates the 10:1 attenuation by selecting the 10MΩ input and connecting the 1.111MΩ shunt. Similarly, 10-2, 10-3, and 10-4 bits selects input attenuation factors of 100, 1000, and 10,000 respectively. In the ohms mode these bits set the resistance range.

Table 2: Register Map of Output Data From the MAX133/134 to the Microprocessor

ADDRESS OR REGISTER NUMBER	REGISTER NAME	REGISTER CONTENTS			
0	Ones	Conversion Result BCD data for least significant digit (The undisplayed digit used for digital autozero)			
1	Tens	BCD data of Conversion Result (Least significant displayed digit)			
2	Hundreds	BCD Data of Conversion Result			
3	Thousands	BCD Data of Conversion Result			
4	10 Thousands	BCD Data of Conversion Result			
5	Status	D3 Always 1	D2 Latched Continuity	D1 $\overline{\text{Holding}}$	D0 Low Battery

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Table 3. Register Map of Input Data From the Microprocessor to the MAX133/134

ADDRESS OR REGISTER NUMBER	D3	D2	D1	D0
0	Hold	High Frequency	Beeper ON	Sleep
1	10-0	Filter Short	÷5	50Hz
2	10-4	10-3	10-2	10-1
3	DC	Ext AC	Divider Sense	Ohms R/2
4	Current	X2	Read Zero	Filter On

BIT SET	VOLTAGE RANGE	OHMS RANGE
10-0	400mV	4MΩ and 40MΩ
10-1	4V	400kΩ
10-2	40V	40kΩ
10-3	400V	4kΩ
10-4	4000V	400Ω

NOTE: The divider sense bit must also be set to enable the 10-0 through 10-4 bits.

50Hz. When set to 1 the integration period for voltage measurement is one cycle of the 50Hz power mains (655 clock cycles). When 0, the integration period is one 60Hz power line cycle (545 clock cycles).

X2. Setting the bit to 1 activates the MAX133/134 "times 2" function. When X2 is active, R_{INT2} only is used as the integrator resistor during the integration phase. R_{INT1} and R_{INT2} in series are used as the integration resistor for all deintegration phases and for the integration phase when X2 is 0. If $R_{INT1} = R_{INT2}$ then setting the X2 bit doubles the digital output for a given input voltage.

÷5. When this bit is set to a 1 the integration period is reduced by a factor of 5. This reduces the digital output code by a factor of 5, and allows a higher input voltage to be used. The full scale input voltage is multiplied by 5 when this bit is set, but caution should be used to make sure that the 2μA maximum recommended integrator output current is not exceeded, or the MAX133/134 linearity will be degraded.

Ohms or R/2. Setting this bit to a 1 selects the ohms measurement mode. See "Ohms and Diode Measurement" section above. Set the Divider Sense to 0 for ohms measurements.

Read Zero. Setting this bit to a 1 causes the next conversion to be a Read Zero conversion. A read zero conversion is performed with In Hi and In Lo internally shorted, and the reference selected by the other control bits is used. The read zero conversion result is proportional to the internal offsets of the MAX133/134, and this result should be subtracted from other measurements to get zero-corrected readings.

Filter On and Filter Short. These bits control the active filter. See Figures 1 and 3.

FILTER ON	FILTER SHORT	FUNCTION
1	0	Normal filter on condition
1	1	Filter on, $R_{FILTER1}$ is bypassed. Use this bit combination to compensate for the higher source impedance of the 4V range.
0	1	Bypasses the Filter.
0	0	Invalid combination, do not use.

DC. This bit selects the DC mode when set to 1 and selects the AC mode when it is 0. This bit should also be set for ohms measurement.

External AC. This bit should be set to 1 whenever the AC mode is selected (DC=0).

Divider Sense. This bit, the 10-0 through 10-4, and the Current bits select the input signal source. Divider sense should be 1 whenever the input attenuator is selected. Set Divider Sense to 0 to select the 400mV input.

Current. Set divider sense to 0 and the Current bit to 1 to select the Current input. Note that while this bit and the associated pin are named "Current", the actual input is the voltage drop across an external current sensing resistor.

Component Selection

Integration Resistors

For an accurate times 2 multiplication in the X2 mode, the two R_{INT} resistors must be exactly equal. If the X2 mode is not needed, then connect a 604kΩ R_{INT1} between Buffer Out1 and the integration capacitor C_{INT}, and leave Buffer Out2 open. The value of both R_{INT1} and R_{INT2} is normally 301kΩ for a 545mV or 655mV reference. This sets the integrator output current to 2μA during the Deintegrate phase. resistors proportionately. Do not exceed 8μA integrator current.

Integration Capacitor

The normal value for the integration capacitor is 4.7nF. This value, in combination with the integrator output current and the clock frequency sets the integrator swing to about 3V for the voltage ranges when R_{INT1} = R_{INT2} = 301kΩ and the clock frequency is 32,768Hz. While the same integrator swing can be achieved with other values of capacitors by changing the value of R_{INT}, lower values of C_{INT} may introduce more noise through increased pickup of noise and 50/60Hz signals. Excessively high values of C_{INT} will also cause noise problems by reducing the integrator swing to unacceptably low values, causing the comparator noise to dominate the conversion errors. Large values of C_{INT} will also cause linearity errors since the settling time of the internal times 10 circuitry is affected by the value of C_{INT}.

The dielectric absorption of the integration capacitor directly affects the integral linearity, and high quality polypropylene capacitors are recommended. Polycarbonate and polystyrene capacitors may give satisfactory performance in less demanding applications, while the fourth choice, polyester (Mylar), will cause about 0.1% integral non-linearity.

Active Filter Components

The RC time constant of the active filter components sets the rolloff frequency of the filter. The effective value of the $R_{FILTER1}$ (Figure 3) is the sum of its value plus the source impedance driving the filter. In the 30V range for example, the effective source impedance is the 101kΩ resistor in the attenuator. In the 3V range, the effective source impedance is 1MΩ. This variable source impedance will alter the filter characteristics somewhat as the different voltage ranges are selected. The effect of the different source impedances can be minimized by increasing the value of the filter resistors while decreasing the value of the filter capacitors proportionately. This, however, will increase the offset error caused by the A/D input leakage current flowing through the filter resistors. For most applications, filter resistor values between 1MΩ and 3MΩ are optimal.

The RC time constant sets the filter rolloff frequency. A low rolloff frequency improves the normal mode rejection, but at the expense of a longer settling time in response to input voltage step changes. Another consideration when an LCD bargraph is used is aliasing. If the bargraph is updated at 20 times per second and there is a 19Hz component in the signal being measured, the beat frequency of 1Hz will appear on the LCD bargraph display. To avoid aliasing effects, the filter time constant is normally set to less than 10Hz. A 3Hz rolloff (RC = 40ms) further reduces the aliasing effects and increases normal mode rejection while still maintaining an acceptable transient response with fast varying signals.

Dielectric absorption in the filter capacitors will create a small, long time constant settling error; therefore polypropylene capacitors are recommended.

Crystal, and Crystal Oscillator Capacitor

The MAX133/134 oscillator is designed to use high Q, low power 32,768Hz crystals such as the Statek CX-1V. The series resistance should be less than 30kΩ.

The oscillator capacitor connected to OSC2 is typically 10pF, but should be adjusted to optimize performance with the chosen crystal. If overtone oscillations are observed, then increase the value of the oscillator capacitor. If on the other hand, the oscillator has start-up problems, then reduce or eliminate the oscillator capacitor. Keep the stray capacitance across the crystal to a minimum since excessive stray capacitance will prevent oscillation.

Attenuator Network

The attenuator network and the associated range selection switches are shown in Figure 1. If the resistance of the internal range selection switches were 0Ω, then the theoretically ideal values for the attenuator network would be 10MΩ, 1.1111MΩ, 101.101kΩ, 10.01kΩ and 1.0001kΩ.

The voltage coefficient of the 10MΩ resistor should be as low as possible, since it will have high voltages applied to it in the 400V and 4,000V ranges. In addition, the temperature coefficients of the various attenuator resistors should be as low as practical since this affects the accuracy of the ohms measurements. The temperature coefficients of the attenuator resistors should track each other since the ratio of the resistor values sets the accuracy of the voltage measurements.

Input Attenuator Compensation Capacitors

The input attenuator is often compensated with low value capacitors to maintain a constant attenuation ratio over a wide bandwith. The value of the compensation capacitors should be as low as practical, otherwise the 10MΩ pin will be driven above V^+ or below V^- when high frequency, high voltage signals are applied to the attenuator input, causing gross conversion errors.

Positive Temperature Coefficient Resistor (PTC)

As shown in Figure 2, a PTC is normally used as part of the protection circuit in the ohms mode. Excessive values of PTC resistance, however, reduce the voltage across the unknown and reference resistors, particularly on the 400Ω range. PTC resistances above 2kΩ will degrade system performance by reducing the signal level on the 400Ω range, thereby increasing the conversion noise. Values above 5kΩ will cause additional error since the voltage drop across the PTC appears at the A/D as a common mode difference between IN HI and Ref LO.

Microprocessors

For low cost 2 chip digital multimeters, 4 bit microprocessors with LCD display drive capability are

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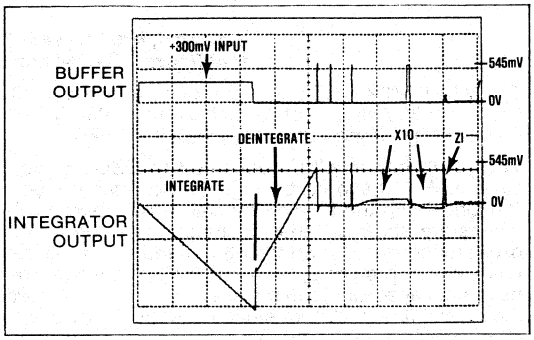

Figure 6. Buffer and Integrator Waveforms with Fullscale Positive Input Voltage

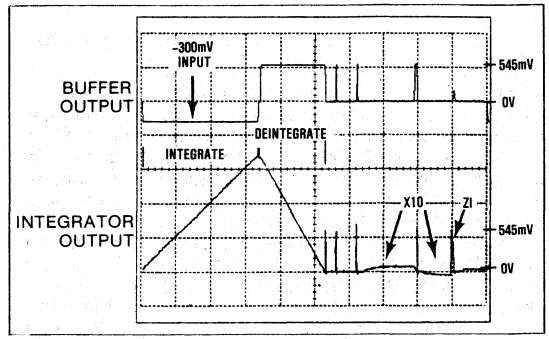

Figure 7. Buffer and Integrator Waveforms with Fullscale Negative Input Voltage

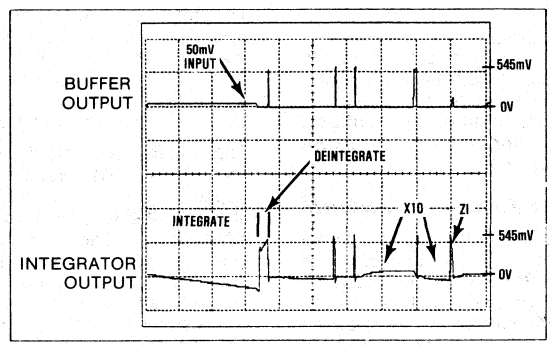

Figure 8. Buffer and Integrator Waveforms with a Small Positive Input Voltage

recommended. Typical 4 bit microprocessor families include the Sharp SM4 and SM5, the NEC μPD75XX family, and the Hitatchi LCD-III and LCD-IV families. If additional calculation power is needed, or if software development costs and time need to be minimized, then 8 bit microcontrollers such as the 8048, 8051 or 6803 should be used.

A/D Conversion Method and Timing

The MAX133/134 uses a "residue multiplication" technique to perform a ±40,000 count conversion in only 1638 clock cycles. Figures 6, 7 and 8 show typical integrator and buffer waveforms for a large positive, a large negative, and a small positive input voltage respectively.

Integration Phase

The unknown signal is integrated by connecting the non-inverting input of the integrator to IN LO, and the buffer input to In Hi. The integration period varies from 100 counts to 655 counts as shown in Table 5. The MAX133/134 is in the Zero Integration phase while in hold, between conversions, and before the start of the integration period.

Table 5. Integration Periods

MODE	INTEGRATION PERIOD (clock cycles)	
Voltage, 60Hz	545	(16.63ms)
Voltage, 50Hz	655	(19.99ms)
Voltage, 60Hz, ÷ 5	109	
Voltage, 50Hz, ÷ 5	131	
Ohms	500	
Ohms, ÷ 5	100	

$$\text{Digital Output Code} = \text{Integration Period} \times 100 \times \frac{V_{IN}}{V_{REF}}$$

where V_{IN} is the differential voltage applied to the A/D's internal In Hi and In LO, and V_{REF} is the differential voltage applied to the A/D's internal Ref Hi and Ref Lo.

First Deintegration Phase

The polarity of the first Deintegrate phase is determined by polarity of the voltage on the integration capacitor at the end of the integration period. Figure 9 shows the MAX133/134 A/D section. Note that no reference capacitor is needed, thereby improving the response time in ohms measurement. Also note that since the non-inverting input of the integrator is connected to Ref Hi for a positive deintegration, the voltage at the integrator output will have a step voltage change equal to the reference voltage.

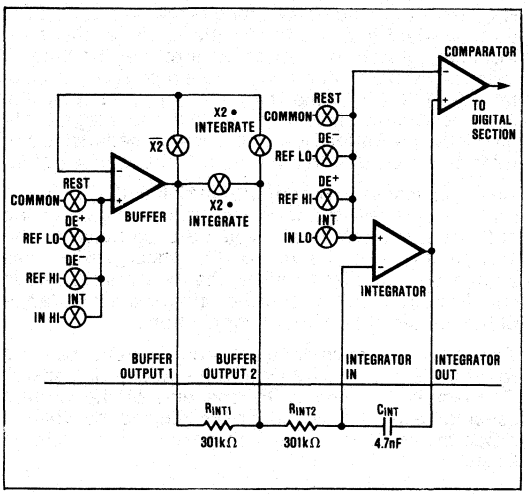

Figure 9. A/D Analog Section.

The first deintegration phase terminates when the comparator detects that the integration capacitor has been discharged. The MAX133/134 then goes into an "Idle" state where both the buffer input and the non-inverting input of the integrator are connected to common. This causes the system offset to be integrated.

Near the end of the maximum allowable deintegration period, the polarity of the voltage on the integration capacitor is again tested and either a positive or negative deintegration cycle occurs.

Times 10 (X10) Phase

When zero crossing is detected at the end of a deintegration phase the deintegration is continued until the next clock cycle. This causes the integrator to overshoot zero crossing slightly, leaving a small residual voltage on the integration capacitor. Any comparator delay causes an additional residual voltage on the integration capacitor. The times 10 phase inverts and multiplies this residual by a factor of 10.

Second Deintegration Phase

The second deintegration phase deintegrates the residual voltage on the integration capacitor that has been inverted and multiplied by 10 in the X10 phase. Note that, since the voltage across the integration capacitor has been multiplied by 10, each clock cycle of deintegration during the second deintegration corresponds to 1/10 of one clock cycle during the first deintegration.

Second X10 and Third Deintegration

The residual voltage left on the integration capacitor after the second deintegrate phase is multiplied by the second X10 phase, and this multiplied residual is deintegrated in the third deintegration phase. Since the residual voltage on the integration capacitor has twice been multiplied by 10, the third deintegration phase has 100 times finer resolution than does the first deintegration phase.

Sequence Counter and Results Counter

The sequencing or timing of the various conversion phases are controlled by a binary sequence counter. This counter counts upward continuously except during the hold mode. Some phases, such as the integration periods, are both started and stopped at preset counts. The deintegration phases are started at predetermined counts, but are terminated when the comparator detects zero crossing at the integrator output.

The results counter accumulates counts during all deintegration phases. It is an up/down BCD counter, with the count direction being determined by the deintegration polarity. The first deintegration phase causes the results counter to count by hundreds. Since the second deintegration phase is deintegrating a residual voltage that has been multiplied by 10, the results counter is incremented or decremented by tens during the second deintegration phase. The results counter is incremented or decremented by ones during the third deintegration phase. The content of the results counter is transferred to the results register at the end of each conversion.

Application Notes

Sleep and Hold Mode

The Hold mode stops the internal sequence counter at the end of the next conversion but does not turn off the oscillator or any analog circuitry. The Hold mode can be used to speed up autoranging — see "Autoranging", below. Dielectric absoption in the integration capacitor will cause the first two or three readings after an extended Hold period to have a lower magnitude than the steady state reading.

The Sleep mode puts the MAX133/134 into a low power quiescent mode by shutting off all analog circuitry except the DGND power supply and the oscillator. A typical use of the Sleep mode is to reduce power consumption by turning off the MAX133/134 if the meter is idle for a long period. A

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typical method of detecting when the meter is no longer being used is to detect when the reading stays constant and there are no operator inputs such as range or mode changes for an extended period.

Since the Sleep mode turns off all analog circuitry, the first conversion after coming out of the sleep mode is not valid. It will take several readings before the reading has stabilized to within 1 count.

Input Protection for Digital Multimeters

Figure 2 shows a typical multimeter input circuit for ohms measurement. The positive temperature coefficient (PTC) thermistor normally has a resistance of only 2kΩ, but under overload conditions it limits the fault current since the fault current heats the PTC, thereby increasing its resistance several orders of magnitiude. Protection on the voltage ranges is automatic, since the 10MΩ input resistor will limit the input current to safe limits, even with 4000V applied. Current ranges must be protected with fuses or circuit breakers, and the current sense resistors should be bypassed with diodes to limit the voltage drop across the current sense resistors to no more than 2 diode drops.

External AC-DC Converter

Figure 10 shows a typical half wave external AC-DC converter. This circuit is an average-sensing, RMS-calibrated AC-DC converter. This means that the output is proportional to the average AC value rather than the RMS value, but that the output has been multiplied by the 1.11 to correct for the ratio of the average voltage to the RMS voltage of a sine wave. If desired, a true RMS to DC converter can be connected between Ext AC Out and Ext AC In.

Printed Circuit Board Layout

Since the integrator output makes common mode voltage steps equal to the reference voltage to perform a positive deintegration, any stray capacitance on the integration capacitor will cause errors. Stray capacitive loading on the Buffer output should also be minimized to avoid ringing on the buffer output.

The Integrator In node is particularly sensitive to stray pickup of noise and 50/60Hz, therefore C_{INT} should be located as near as possible to the Integrator In pin.

Minimize capacitance on the node that joins the two R_{INT} resistors since this capacitance sets up an RC time constant that rounds off the edges of the input to the integrator and can cause errors. If the times 2 mode is not used, then connect a single R_{INT1} directly from Buff OUT1 to the Integrator In pin. Locate the R_{INT1} resistor as close as possible to the Integrator In pin since the Buffer Output is a low impedance point while the Integrator In pin is a high impedance point.

Any resistance between the MAX133/134 1kΩ pin and the 1kΩ resistor adds the effective value of the 1kΩ resistor, as does any voltage drop between the 1kΩ resistor and the In Lo pin. These resistances should be minimized and/or the 1kΩ resistor value should be reduced to compensate for the resistance of the printed circuit board connections.

The effective resistance of any current sensing resistors is affected by where the voltage is sensed. Connect In Lo directly to one end of the current sensing resistor to avoid errors caused by voltage drops in the Common traces on the printed circuit board.

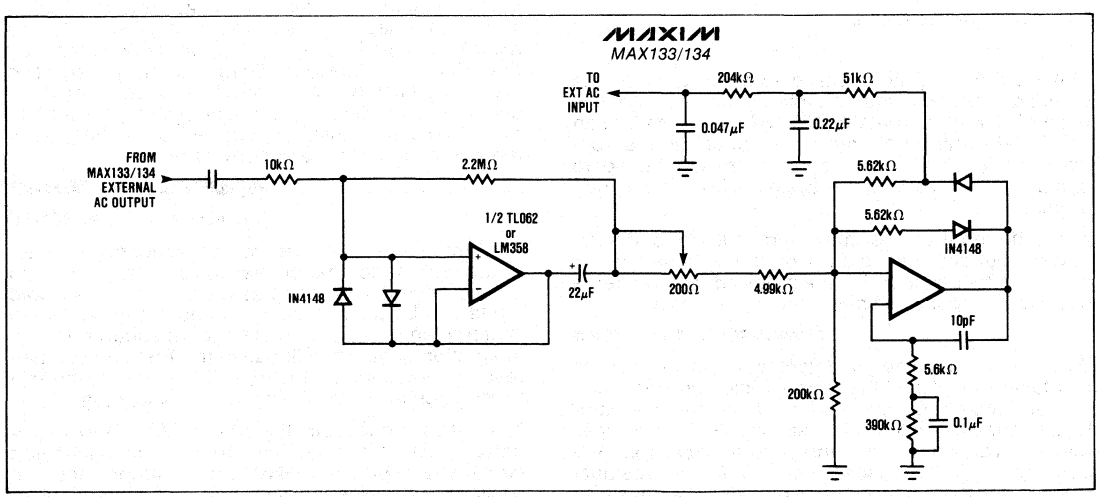

Figure 10. External AC-DC Converter.

Software Notes

Autoranging

The sequence in which the registers are loaded has no effect provided that all registers are loaded before the next end of conversion. Control bits take effect only when the MAX133/134 is in Hold or completes the current conversion. If the MAX133/134 runs continuously, the autoranging sequence will be as shown in Figure 11A. If the MAX133/134 is put into the hold mode during autoranging the autoranging time can be reduced in those cases where several ranges must be tried. See Figure 11B. A simple test that detects most overrange readings is to check if the two most significant digits (Registers 3 and 4) are greater than ±45. A second test of the zero-corrected reading should also be performed to make sure that it is within the desired full scale range.

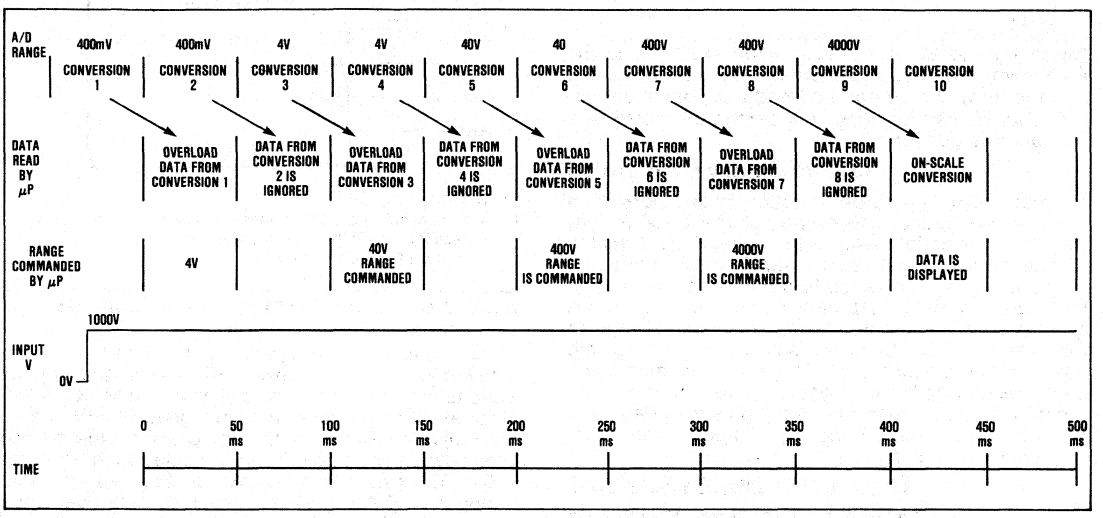

Figure 11a. Autoranging with MAX133/134 Running Continuously

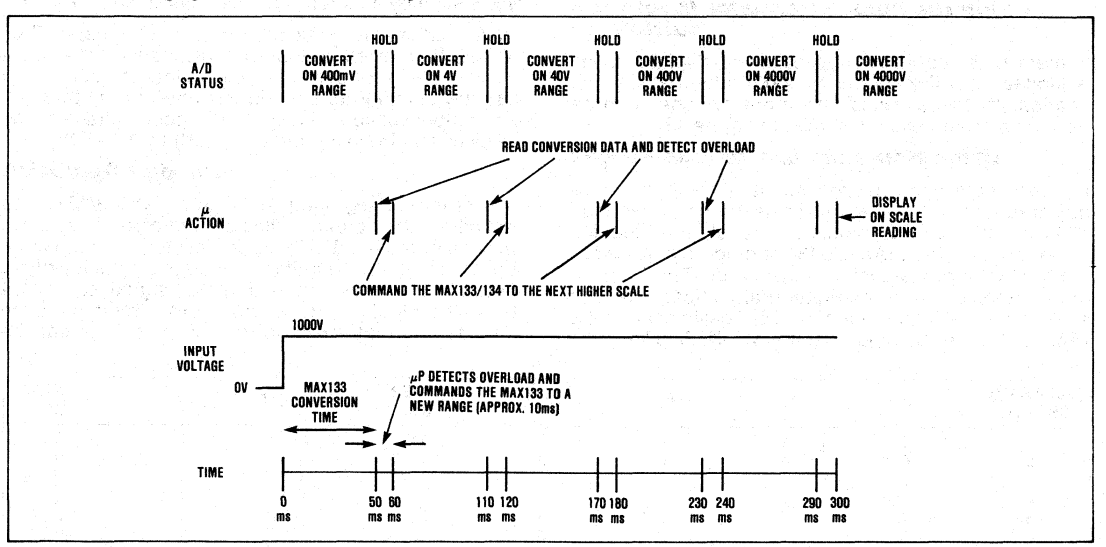

Figure 11b. Autoranging With Hold Between Conversions

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Reduction of Conversion Noise by Averaging Readings

The MAX133/134 has approximately ±1 counts of noise. In most cases where only 4000 counts are being displayed, averaging is not required since the noise is only 1/10 of one displayed count. In data acquisition systems where the full resolution is being used, averaging N readings will reduce the noise by a factor of

$\sqrt{N}$.

Since the noise of zero-corrected readings is the RMS sum of the noise of both the Read Zero reading and the normal reading, the Read Zero offset correction should also be averaged if optimum noise performance is desired.

BCD to Binary Conversion

Normally, if only a zero correction or tare correction is to be applied to the output of the MAX133/134, then the conversion result is left in the BCD format. If a scale factor or gain correction is to be made, the result is usually converted to a binary format. Any of the standard BCD to binary conversion algorithms can be used. A simple method of conversion is to read the MAX133/134 conversion result starting with the most significant digit. Put the most significant digit's result into a multi-byte accumulator and multiply it by 10. Then read the next digit's result and add it to the accumulator. Repeat the "multiply-read-add" sequence for all 5 digits.

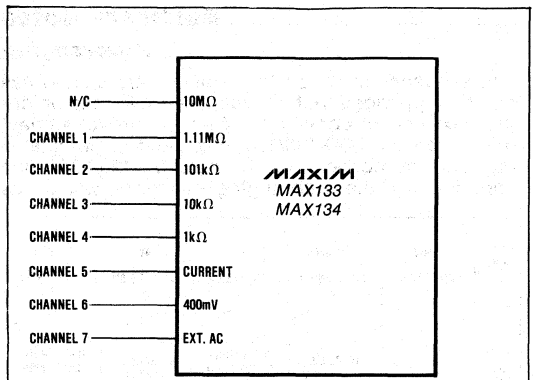
Using the MAX133/134 in Data Acquisition Systems

Using the Input Attenuator Inputs as a Multiplexer

In many data acquisition applications the voltage range is limited, and the 400mV to 4000V attenuator is not needed. In these cases, the input switches can be used as a multiplexer as shown in Figure 12.

Using Non-standard Voltage Ranges

In many data acquisition systems the voltage to be measured may have a full scale range other than 400mV, 4V, etc. For maximum resolution, the full scale range of the MAX133/134 should be adjusted to match the input signal voltage span. This can be done either through attenuation/amplification of the signal to make it match the ±400mV basic span of the MAX133/134, or by adjusting the MAX133/134 voltage span.



NOTES:
1. Channels 5 and 6 are connected to Common via a 5kΩ resistor when they are not selected.
2. Voltage Span is ±400mV.

Figure 12. MAX133/134 Input Section used as a Multiplexer.

Table 5 shows the integration periods of the various conversion modes. These different modes can be used to change the full scale span of the MAX133/134. If for example the reference voltage is 545mV, setting the 50Hz bit changes the integration time to 655 clock cycles and the 400mV full scale range becomes a 545/655 x 400mV = 333mV full scale range. Activating the ÷5 bit increases the full scale span by a factor of 5, while setting the X2 bit decreases the full scale span by a factor of 2 (assuming $R_{INT1} = R_{INT2}$).

In all cases, the values of R_{INT1}, R_{INT2}, and C_{INT} should be chosen so that integrator swing is at least 2V, and integrator current is always less than 3μA both during deintegrate and during integrate with a full scale input voltage. The common mode voltage range of IN Hi and In Lo is from (V^- +1.5V) to (V^+ -1.0V).

Unipolar Operation

Unlike most integrating A/Ds, the MAX133/134 does not have extra non-linearities around zero. This allows the use of the full 80,000 count resolution to measure unipolar signals. All that is needed is a resistive offset network to translate the unipolar signal so that it becomes bipolar. An external zero circuit must be included so that errors in the offset resistor can be

SELECTED CHANNEL	10^{-1}	10^{-2}	10^{-3}	10^{-4}	DIVIDER SENSE	CURRENT	DC	EXT AC
1	1	0	0	0	1	X	1	0
2	0	1	0	0	1	X	1	0
3	0	0	1	0	1	X	1	0
4	0	0	0	1	1	X	1	0
5	0	0	0	0	0	1	1	0
6	0	0	0	0	0	0	1	0
7	0	0	0	0	X	X	0	1

0 = set to 0 1 = set to 1 X = Don't Care

measured and subtracted. Note that the zero correction software is the same as would be used to correct for the internal zero error of the MAX133/134, except that in this case the external zero offset will be nearly 40,000 counts.

Ratiometric Measurements of Load Cell and Strain Gauges

In many weigh scale, pressure transducer, and load cell applications ratiometric measurements are desired. If the reference voltage is referenced to the ground or Common pin, then simply connect the reference voltage to the Ref In pin, connect the voltage to be measured to In Hi and In Lo and perform any of the voltage mode conversions. If, on the other hand, the reference voltage is a differential signal, use the circuit of Figure 13 and select the ohms measurement mode. Note that the non-inverting input of the integrator will be connected to either Ref Lo or REF Hi during deintegration. The integrator swing should be reduced if the integrator output goes within 0.5V of either V^+ or V^-. In no case should either Ref Hi or Ref Lo be lower than (V^- + 1.5V) or higher than (V^+ - 1.0V).

Operation with Clock Frequencies Other Than 32,768Hz

Operation with clock frequencies lower than 32kHz slightly improves the noise performance, while at the same time reducing the reading rate proportionately. With clock frequencies less than 10kHz, leakages during the X10 phase will introduce differential linearity errors at high temperatures.

Clock frequencies higher than 50kHz are not recommended since the X10 period will not completely settle within its allotted time period, causing differential nonlinearity errors. Another potential problem at very high clock frequencies is that, although the comparator delay is a fixed time period, it increases in terms of clock cycles as the clock frequency increases. At very high clock frequencies the residue cannot be fully deintegrated in the allotted number of clock cycles after having been multiplied by 10 in the X10 phase.

When using a clock frequency other than 32,768Hz, change the value of the integration capacitor C_{INT} to keep integrator swing at approximately 2V.

Converting the Times 2 Mode to a ± 40mV Full Scale Range

The sensitivity of the times two mode is increased by the factor

$$\frac{R_{INT1} + R_{INT2}}{R_{INT1}}$$

In the normal DMM aplication $R_{INT1} = R_{INT2}$ and the X2 mode increases the sensitivity of the MAX133/134 by a factor of 2. If the two resistors have a 9 to 1 ratio, the X2 bit will increase the sensitivity of the MAX133/134 by a factor of 10. This can be used to get 1μV resolution on a 40mV scale.

Disabling the Active Filter

Since the signal source impedance in many data acquisition systems is very low, the value of the filter resistors, $R_{FILTER1}$ and $R_{FILTER2}$, can be lowered to reduce the error caused by the leakage current of the A/D flowing through $R_{FILTER1}$. If rapid settling is needed in a multichannel data acquisition system, then the filter should be disabled by leaving the pins Filter Resistor In and Filter Resistor Out open, and shorting Filter Amp Out to Filter Amp In. Do not leave the filter amplifier connection open circuited, since oscillations may occur.

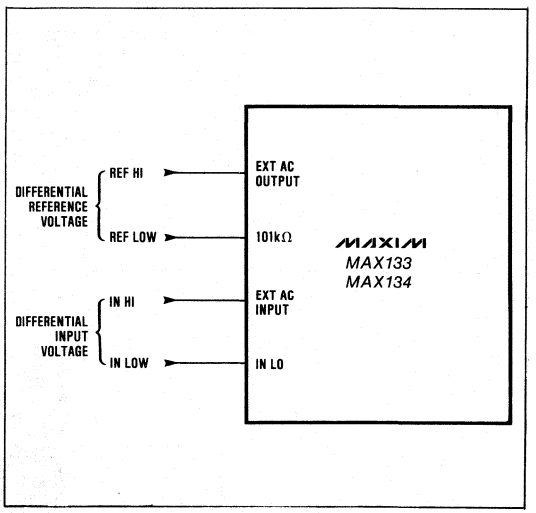


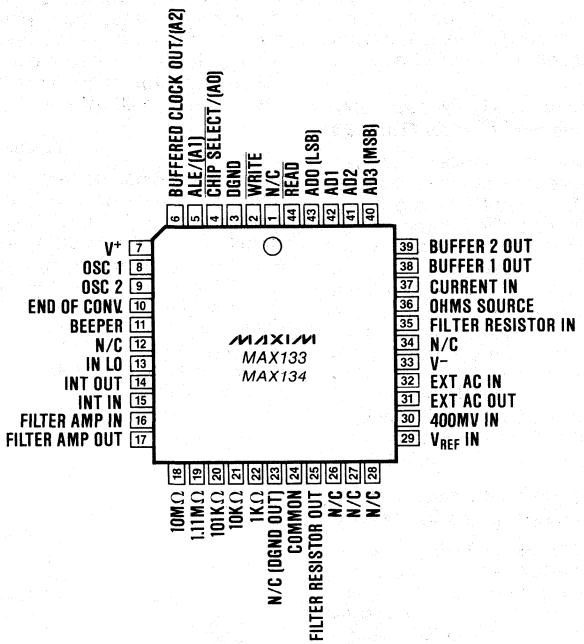
Figure 13. Configuration for Differential Reference Input.

BIT PATTERN					
10^{-0} TO 10^{-4}	R/2	DIVIDER SENSE	CURRENT	DC	EXT AC
0	1	1	0	0	1

3¾ Digit DMM Circuit

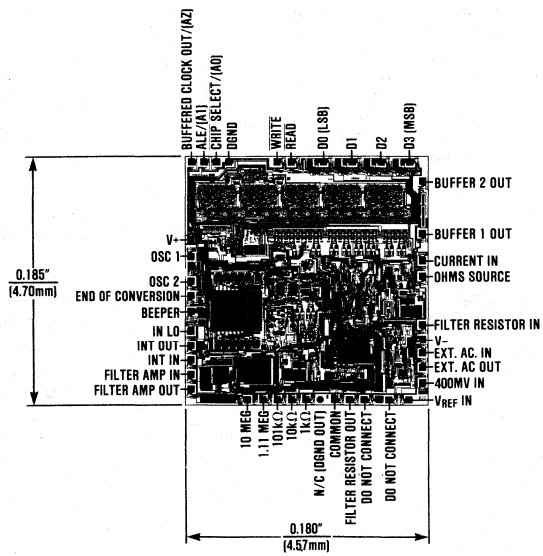
Pin Configuration

TOP VIEW



Pin Names in parentheses are for MAX134 only.

Chip Topography



Low Power, 3½ Digit A/D Converter With Display Hold

General Description

The Maxim MAX136 is a monolithic analog to digital converter with very high input impedance. It differs from the Maxim ICL7136 in that the MAX136 provides a Hold pin, which makes it possible to hold or "freeze" a reading. The MAX136 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external drive circuitry. With minor external component changes, it is pin compatible with the ICL7116 but with significantly reduced power consumption, making the MAX136 a superior device for portable systems.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. True differential inputs allow direct measurements of bridge transducer outputs or load cells. The zero-integrator phase eliminates overrange hangover and hysteresis effects. The MAX136 offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

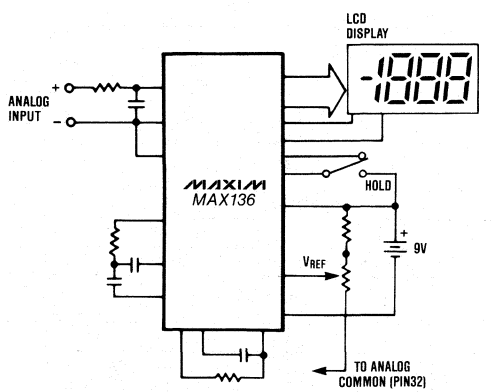
Features

- **Power dissipation guaranteed less than 1mW-9V battery life 3000 hours typical**
- **Hold pin allows indefinite display hold**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required**
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **Zero Input Gives Zero Reading**
- **True Polarity Indication for Precision Null Applications**
- **Key Parameters Guaranteed over Temperature**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX136CPL	0°C to +70°C	40 Lead Plastic DIP
MAX136CJL	0°C to +70°C	40 Lead CERDIP
MAX136CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX136C/D	0°C to +70°C	Dice

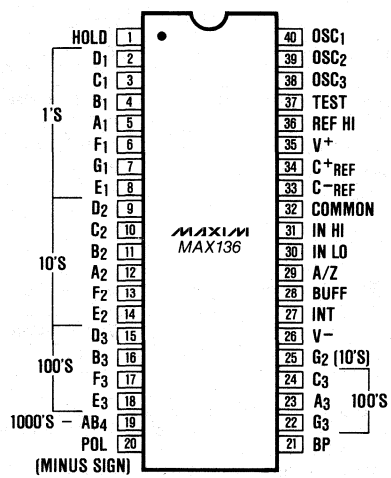
Typical Operating Circuit



(Detailed Circuit Diagram—See 3rd page)

Pin Configuration

Top View



See last page for Plastic Chip Carrier Pin Configuration

Low Power, 3½ Digit A/D Converter With Display Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input, Hold Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 800mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±1mA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1 unless noted.)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 -000.0 -000.0	 ±000.0 ±000.0	 +000.0 +000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 999 998	 999/1000 999/1000	 1000 1001	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 -1	 ±0.2 ±0.2	 +1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	 -1	 ±0.2	 +1	Counts
Common Mode Rejection Ratio (Note 7)	V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV		 5		 µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		 10		 µV
Input Leakage Current	V_{IN} = 0, T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C		 1 20	 10 200	 pA
Zero Reading Drift	V_{IN} = 0, 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		 1	 5	 ppm/°C
V^+ Supply Current	V_{IN} = 0 T_A = 25°C 0° ≤ T_A ≤ 70°C		 80	 150 200	 µA
Analog Common Voltage (with respect to Pos. supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply	250kΩ between Common & Pos. Supply		75		ppm/°C
Input Resistance, Pin 1			1000		MΩ
V_{IL}, Pin 1				TEST +1.5	V
V_{IH}, Pin 1		V^+ -1.5			V
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V (Note 8)	4	5	6	V
Test Pin Voltage	With Respect to V^+	4	5	6	V
Overload Recovery Time (Note 5)	V_{IN} changing from ± 10V to 0V		0	1	Measurement Cycles

Note 3: Test condition is V_{IN} applied between pins IN-HI and IN-LO, i.e., 1MΩ resistor in Figures 1 and 2.
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883C, Method 3015 .2)
Note 5: Number of measurement cycles for display to give accurate reading.
Note 6: 1MΩ resistor is removed in Figures 1 and 2.
Note 7: Refer to "Differential Input" discussion (See Maxim's ICL7136 data sheet).
Note 8: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Low Power, 3½ Digit A/D Converter With Display Hold

Detailed Description

The Maxim MAX136 3½ digit A/D converter is similar to the Maxim ICL7136 except for the addition of a Hold pin. For a detailed product description, and applications information (other than the operation of the Hold pin described below), refer to Maxim's ICL7136 data sheet.

Hold Input

The Hold input is a digital input with a logic threshold approximately midway between V^+ and Test. The MAX136 continuously performs conversions, independent of the Hold input. When the Hold input is at V^+ the display latch pulse is inhibited, and the display latches are not updated; when the Hold input is low or at the Test voltage, the display is updated at the end of each conversion. The MAX136 maintains low power dissipation even during display hold by eliminating the pull-down resistor between Hold and Test present on the ICL7116. The Hold input is CMOS compatible, and can also be driven by a switch connected between Test and V^+ (Figure 1).

Reference Input

Unlike the ICL7136, the MAX136 does not have a Reference Low input. Apply the reference voltage between Reference High (REF HI) and Common.

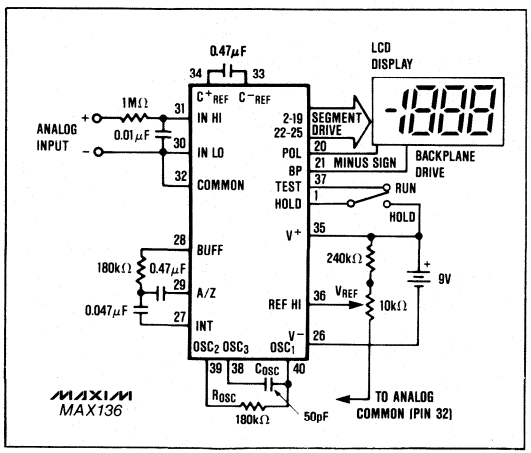


Figure 1. Maxim MAX136 Typical Operating Circuit, 200mV Full Scale.

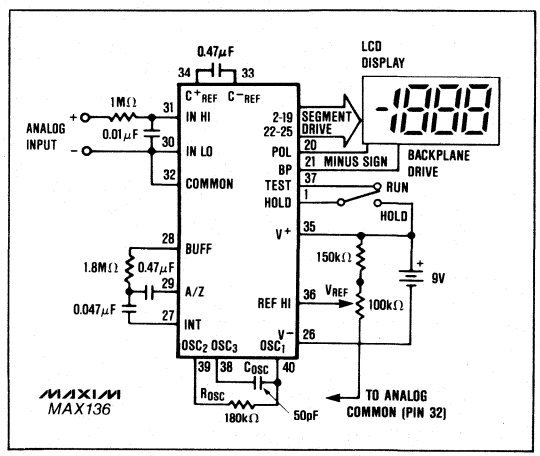
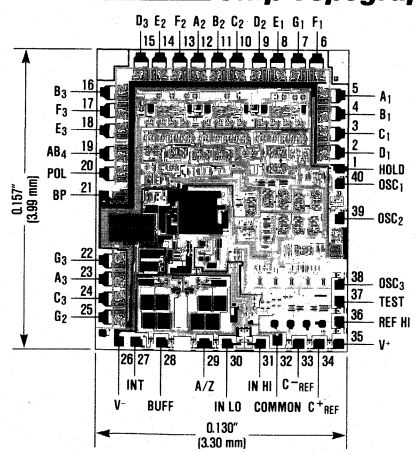
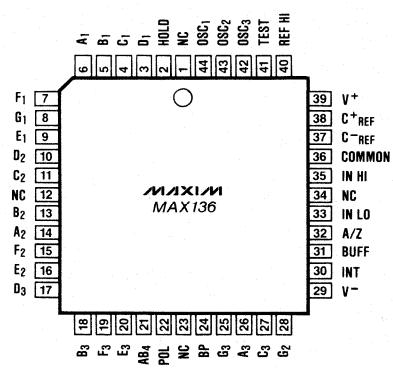


Figure 2. Maxim MAX136 Typical Operating Circuit, 2.0V Full Scale.

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

MAXIM

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

General Description

The MAX138 and MAX139 are 3½ digit A/D converters with onboard LCD (MAX138) and LED (MAX139) display drivers. The MAX138 and MAX139 also contain a charge pump voltage inverter. The charge pump inverter allows the MAX138/139 to measure both positive and negative input voltages while operating from a single power supply voltage from +2.5V to +7V. The operating circuits of the MAX138 and MAX139 are similar to those of the ICL7136 and ICL7137 respectively, except that the MAX138/139 have an internal oscillator, and an external charge pump capacitor is connected to pins 38 and 40.

MAX140 is a low segment current version of MAX139 intended for use with low current LED displays.

Applications

+5V Powered Panel Meters

+3V Powered DMMs

Instruments

Portable Monitors

Weigh Scales

Digital Thermometers

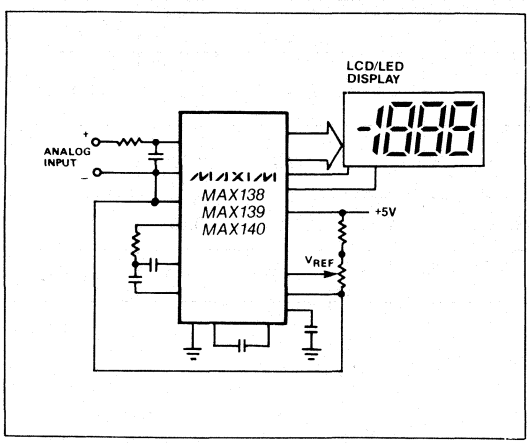
Features

- ◆ **Single Supply +2.5V to +7.0V Operation**
- ◆ **Measures Both Positive and Negative Input Voltages**
- ◆ **Charge Pump Voltage Inverter Generates a Negative Supply Voltage**
- ◆ **Internal Bandgap Reference**
- ◆ **Onboard Display Driver**
- ◆ **Low Segment Current (MAX140)**

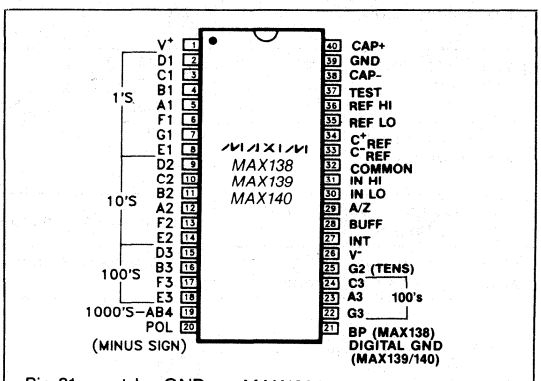
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX138CPL	0°C to +70°C	40 Lead Plastic DIP
MAX138CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX138C/D	0°C to +70°C	Dice
MAX138EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX138EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier
MAX139CPL	0°C to +70°C	40 Lead Plastic DIP
MAX139CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX139C/D	0°C to +70°C	Dice
MAX139EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX139EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier
MAX140CPL	0°C to +70°C	40 Lead Plastic DIP
MAX140CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX140C/D	0°C to +70°C	Dice
MAX140EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX140EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier

Typical Operating Circuit



Pin Configuration



Pin 21 must be GND on MAX139/140.

See last page for Plastic Chip Carrier Pin Configuration.

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to GND) 7.5V
Supply Voltage (V^+ to GND)
MAX138 ..... +7.5V
MAX139, MAX140 ..... +6.0V
Analog Input Voltage (either input) (Note 2) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Power Dissipation (Note 3)
CERDIP Package 1000mW
Plastic Package 800mW
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Note 1: V^- is generated on the device and is equal to V^+ but opposite in polarity.
Note 2: Input voltages may exceed the supply voltages, provided the input current is limited to ±1mA.
Note 3: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS (MAX138, MAX139, MAX140)

(V^+ = +5V, T_A = +25°C, test circuit—Figure 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200mV T_A = 25°C (Note 4) 0° ≤ T_A ≤ 70°C (Note 5)	 -000.0 -000.0	 ±000.0 ±000.0	 +000.0 +000.0	 Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 4) 0° ≤ T_A ≤ 70°C (Note 5)	 999 998	 999/1000 999/1000	 1000 1001	 Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200mV T_A = 25°C (Note 4) 0° ≤ T_A ≤ 70°C (Note 5)	 -1	 ±0.2 ±0.2	 +1	 Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or full scale = 2.000V (Note 6)	 -1	 ±0.2	 +1	 Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200mV		 50		 μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200mV		 15		 μV
Input Leakage Current	V_{IN} = 0 T_A = 25°C (Note 4) 0° ≤ T_A ≤ 70°C		 1 20	 10 200	 pA
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 4)		 0.2		 μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 4)		 1		 ppm/°C
V^+ Supply Current (See Figure 4A)	V_{IN} = 0 T_A = 25°C 0° ≤ T_A ≤ 70°C		 200	 500 800	 μA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.95	3.05	3.15	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply (Note 7)		±20	±100	ppm/°C

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

ELECTRICAL CHARACTERISTICS (MAX138)

(V^+ = +5V, T_A = +25°C; test circuit—Figure 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage		4	5	6	V
Test Pin Voltage	With Respect to V^+	4	5	6	V

ELECTRICAL CHARACTERISTICS (MAX139, MAX140)

(V^+ = +5V, T_A = +25°C; test circuit—Figure 2)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Segment Drive Current	MAX139	Except Pin 19	5	9	15	mA
		Pin 19	10	18	30	
	MAX140	Except Pin 19	1.5	2.5	4	mA
		Pin 19	3	5	8	

Note 4: Test condition is V_{IN} applied between pin IN HI and IN LO through a 1MΩ series resistor as shown in Figures 1 and 2.
Note 5: 1MΩ resistor is removed in Figures 1 and 2.
Note 6: Guaranteed by design.
Note 7: Sample tested to ensure compliance.

Basic Applications

Figures 1 and 2 show the typical operating circuit for the MAX138/139/140 when powered by a single +5V supply.

Compatibility with ICL7106, ICL7136 and ICL7137

The MAX138/139/140 can replace the ICL7106/ICL7136 and ICL7137 with minor circuit and component value changes. The ICL7106/36/37 oscillator components are not used, and are replaced with a 1μF capacitor connected between pins 38 and 40. There must be a 1μF filter capacitor connected to V^-. The filter capacitor can be connected between either V^- and GND or V^- and V^+.

System Reference Point

The analog block diagram of the MAX138/139 is shown in Figure 3. The MAX138/139 use the IN LO pin as the reference point for the integrator.

The circuit configuration of the MAX138/139 results in a superior 120dB rejection of common mode voltages applied to IN HI and IN LO. The MAX138/139 configuration, though, does not have good rejection of AC noise on the IN LO pin during de-integration. If an AC-DC converter is used with a MAX138/139, it should either be a half-wave circuit or should have adequate filtering to avoid inducing additional noise.

Detailed Description

Conversion Method

The MAX138/139/140 use the dual-slope integration method of conversion, with the addition of an auto-zero phase to compensate for the offset of the buffer and integrator, and the addition of a zero integrator phase to ensure rapid recovery from an overrange conversion. Refer to the ICL7106 data sheet for a detailed description of the conversion phases and timing.

The conversion result is 1000 × (IN HI-IN LO)/(REF HI-REF LO), with a maximum conversion result of ±1999. If the input voltage is greater than full scale, the MAX138/139/140 will blank the lower three digits, and will display the leading "1" digit and, if the input voltage is negative, will also turn on the Minus segment.

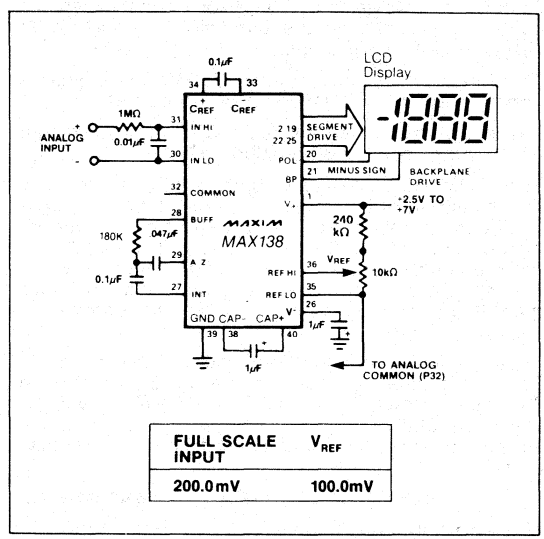
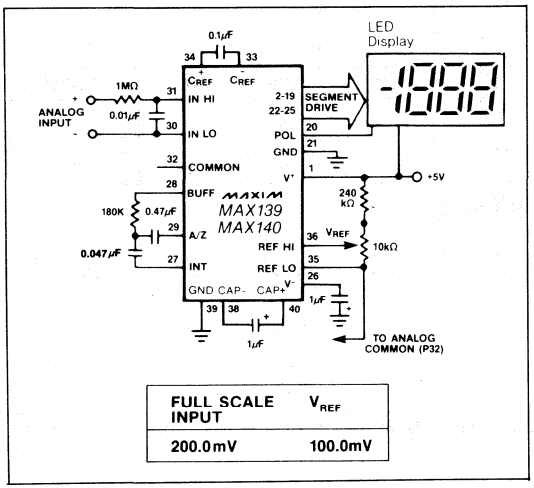


Figure 1. MAX138 Typical Operating Circuit

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter



FULL SCALE INPUT	V_{REF}
200.0mV	100.0mV

Figure 2. MAX139/MAX140 Typical Operating Circuit

Common Pin Voltage Reference

The COMMON voltage is derived from a bandgap reference, unlike earlier devices which derive the COMMON voltage from a zener. The bandgap reference eliminates the excessive long term drift associated with low current zeners, and the MAX138/139/140 can be a source of a high quality reference voltage without the use of external bandgap reference diodes. The COMMON voltage does have slightly more wideband noise than does a zener-derived COMMON voltage, but a 0.1µF or greater reference capacitor will reduce the bandwidth sufficiently to virtually eliminate the noise.

The long term stability of the COMMON voltage is approximately 0.01% (100ppm or 1/5 count).

These devices are sample tested to ensure a maximum temperature coefficient of 100ppm/°C.

The COMMON voltage is buffered by an op amp which has an output impedance of 1 ohm and up to 2mA output sink current, and a short circuit current of approximately 25mA max at 3.5V. The COMMON pin has a small pull-up current of 1µA typical, and if desired it can be driven to a voltage more negative than its internally generated voltage by overpowering the pull-up current source.

The COMMON voltage is trimmed to 3.05V ± 100mV. This is significantly more accurate than the 2.4V to 3.2V span allowed in the ICL7106. The better voltage accuracy allows the trim range of the reference voltage to be reduced, increasing resolution and ease of adjustment.

MAX139 and MAX140 Test Voltage

This internal test voltage is coupled to the TEST pin via a 500 ohm resistor. When this pin is pulled high, all segments are turned on.

Oscillator

The MAX138/139/140 oscillator circuit uses no external components. It is trimmed during production to 40kHz nominal. This results in a conversion rate of approximately 2.5 conversions per second. The typical characteristics graph (Figure 4B) shows the variation with changes in supply voltage.

In Lo and In Hi Differential Inputs

These A/D converters measure the differential voltage between IN LO and IN HI. The typical common mode rejection ratio (CMRR) is 120dB.

IN HI has a guaranteed maximum input leakage current of only 10pA, and can be directly driven by high source impedances such as pH sensors and by the 10 Megohm input impedance attenuators normally used in digital multimeters. Both IN HI and IN LO have protection clamp diodes to V^+ and V^-. If the input voltage can go above V^+ or below V^-, then the input currents should be limited to less than 1mA to prevent damage to the A/D.

The MAX138/139/140 common mode voltage range for IN HI and IN LO is a minimum of ±1V around COMMON. Under some circumstances, IN HI and IN LO can range from V^- + 1.5V to V^+ - 1.5V. See "Common Mode Voltage Range Considerations" section of the Application Notes for further information.

Reference and C_{REF} Pins

As shown in the analog block diagram, Figure 3, REF HI and REF LO are connected to the C_{REF} pins during autozero and zero integrate phases via analog switches. This charges an external reference capacitor, which is then used as either a positive or a negative reference voltage as needed during the deintegration phase. The common mode voltage range (CMVR) of REF HI and REF LO is V^+ to V^-—any voltage between V^+ and V^- can be used to drive the REF HI and REF LO inputs. The differential voltage between REF HI and REF LO sets the full scale voltage. A full scale output of ±1999 counts occurs with an input voltage of ±1.999 times the differential voltage between REF HI and REF LO. If the differential reference voltage is 1.0V the full scale input voltage is 1.999V. With 100mV reference the full scale input voltage is 199.9mV.

LCD Display Driver Outputs

The MAX138 LCD display driver outputs swing from V^+ to GND at a frequency of 20 times the conversion rate. The output impedance is approximately 3k ohms. The LCD display driver outputs are non-multiplexed or direct drive, and drive in-phase with the backplane output to turn an LCD segment off and drive 180° out of phase with the backplane output to turn an LCD segment on.

The BP or backplane output has an output impedance of 500Ω. The LCD drive waveforms are 50% duty cycle with matched rise and fall times to minimize the DC component across the LCD display.

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

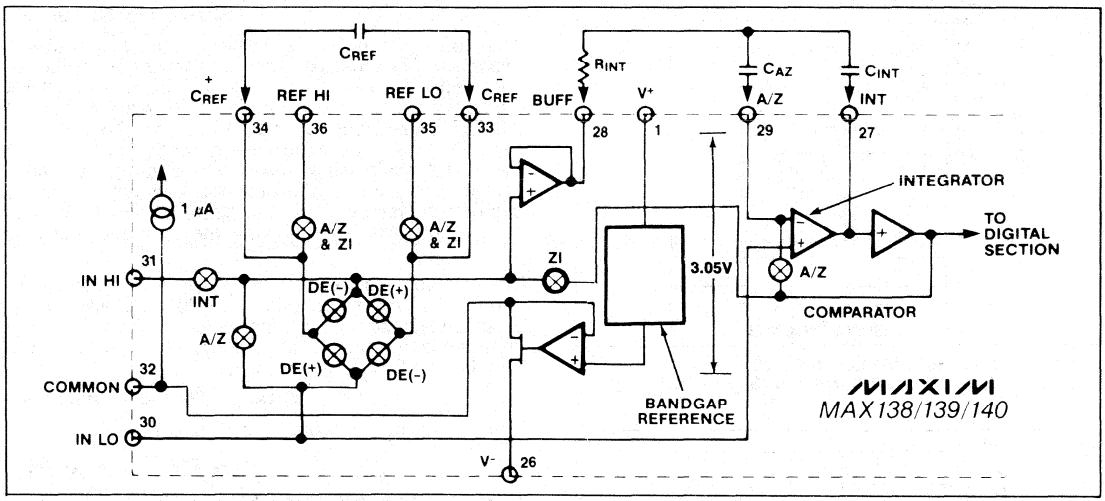


Figure 3. Analog Section of MAX138, MAX139, and MAX140

The MAX139/140 LED display driver outputs are N-Channel current sinks with output current vs. voltage characteristics as shown in the typical characteristics graphs.

Component Selection

Integrator Resistor, R_{INT}

The MAX138/139/140 integrator and buffer amplifiers have a class A output stage which can deliver up to 4µA with high linearity. Normally, the MAX138/139/140 integrator resistor is chosen to set the maximum current to 1.1µA by setting its value to $2 \times V_{REF}/1.1\mu A$. For a 1V reference the correct value is 1.8MΩ. For a 100mV reference the correct value is 180k. Since the absolute value of R_{INT} does not affect the conversion accuracy, the type of resistor used for R_{INT} is not critical.

Integrator Capacitor

The integrator capacitor is normally polypropylene, which has low dielectric absorption. Dielectric absorption will cause integral linearity errors. For example, if polyester or Mylar is used, the measured value of inputs near full scale will be approximately 0.1% lower than expected, while the measured value of low input voltages will be as expected.

Proper selection of the integrator capacitor value can be verified by monitoring the output swing of the integrator with ±full scale input voltages. In a properly operating circuit, ±full scale input voltages will cause the integrator output (INT pin) to swing to about ±2V. The integrator output can drive to about 0.3V from either supply while maintaining high linearity.

If the value of the integrator capacitor or integrator resistor is too low, ±full scale inputs will cause the integrator to saturate as it attempts to drive above V^+ or below V^-. If this occurs, operation will appear normal for low input voltages, but the conversion results for higher output voltages will be less than full scale.

Very low integrator swing will increase the amount of noise or "flicker" of the conversions. A full scale integrator swing of ±1V is sufficient to avoid any significant degradation of the noise performance, and should be used for operation with a 2.5V supply.

Reference Capacitor

For most circuits a reference capacitor value of 0.1µF is adequate. However, a larger value is needed to prevent rollover error if there is significant stray capacitance at the reference capacitor terminals. Minimize the stray capacitance on the reference capacitor terminals to reduce the rollover error, and if necessary, increase the reference capacitor value to 1.0µF.

The printed circuit board should be carefully cleaned to minimize leakage at the C_{REF} terminals since leakage will cause both gain and rollover errors. Due to the increased leakage of the MAX138/139/140 at +70°C, a 1.0µF reference capacitor is recommended to reduce rollover and gain errors at high temperature.

The reference capacitor is typically a low leakage film capacitor. Polyester (Mylar) is acceptable in applications where the reference voltage is constant. A low dielectric absorption capacitor such as polypropylene should be used if the reference voltage is variable, since any dielectric absorption will increase the settling time in response to a change in reference voltage. Since the reference voltage varies in circuits which measure resistance ratiometrically, a polypropylene reference capacitor should be used in ohmmeters.

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

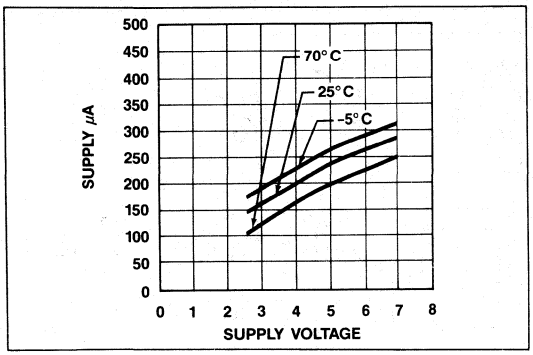


Figure 4A. MAX138, MAX139, MAX140 Typical Supply Current vs. Supply Voltage

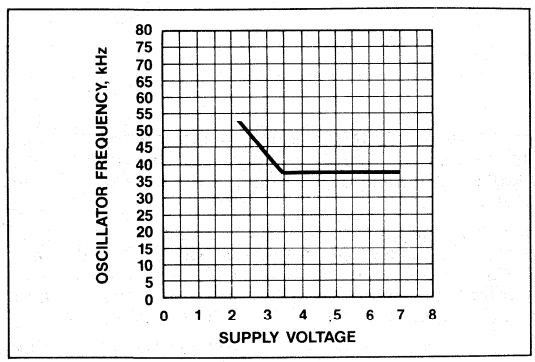


Figure 4B. MAX138, MAX139, MAX140 Typical Oscillator Frequency vs. Supply Voltage

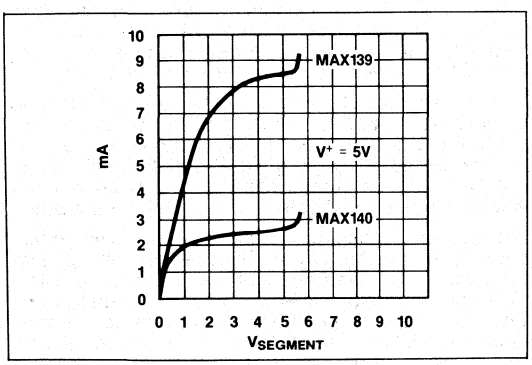


Figure 5. Output Current vs. Output Voltage

Autozero Capacitor

The noise of the A/D is influenced by the autozero capacitor. For the best noise performance, and autozero capacitor value of at least 4 times the integrator capacitor value is recommended. For a 2V scale, a 0.047µF (47nF) capacitor is adequate. An autozero capacitor of 0.47µF or greater is recommended for a 200mV full scale. All of Maxim's integrating A/D converters have a zero integrator phase which allows the use of high values for the autozero capacitor without causing hysteresis or slowing the overload recovery time.

The autozero capacitor can be any low leakage film capacitor in most applications. A low dielectric polypropylene capacitor is recommended if there are rapid changes in common mode voltage, or if the A/D must rapidly stabilize upon power up.

Charge Pump Capacitors

The charge pump capacitors should be 1µF.

Application Notes

Common Mode Voltage Range Considerations

Operation with low supply voltages, or operation with either IN LO or IN HI near either supply calls for careful evaluation of the effect of common mode voltages.

Since the MAX138/139/140 perform all conversion phases, including autozero and de-integration, using IN LO as the reference point, they have excellent normal mode rejection of approximately 120dB.

There are three basic internal limitations on the allowable common mode voltage (see Figure 3):

1) The buffer input CMVR is (V^- + 1.5V) to (V^+ - 1.5V).
2) The integrator CMVR is (V^- + 1.5V) to (V^+ - 1.5V).
3) The integrator output swing is limited to V^- to V^+.
4) The IN LO must not go higher than 1.0V above Common.

Figure 3 shows that the buffer input can be connected to either IN HI, (IN LO + V_{REF}), or (IN LO - V_{REF}). The integrator non-inverting input is always connected to IN LO.

Combining both system CMVR limitations with the possible connections results in the limitations shown in Table 1.

Low Battery Detector Circuit

Since the voltage between Common and V^+ is between 2.95V and 3.15V until the voltage between V^+ and V^- falls to less than 4V, a simple low battery detector can be made using transistor voltage detector as shown in Figure 6. When Q1 is off the Low Battery segment is driven in phase with the backplane and is off. When Q1 turns on, the Low Battery LCD segment becomes visible. Q1 turns on when the voltage at the base of Q1 is one base-emitter voltage more positive than COMMON voltage.

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

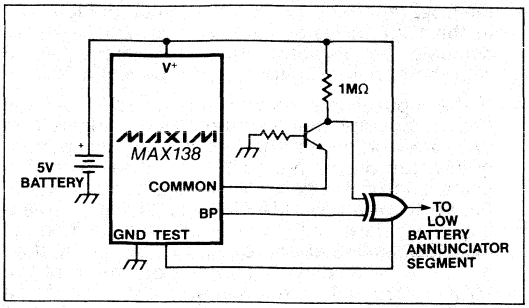


Figure 6. Low Battery Detector and LCD Segment Drive

Overload Display

The least significant three digits are blanked if the input voltage exceeds full scale. The leading "1" is displayed for positive overloads, and a "-1" is displayed for negative overloads. Any of the conditions that cause erratic readings as discussed above may cause overload readings. In addition, check the differential voltage between IN HI and IN LO and make sure that it is no more than twice the differential voltage between REF HI and REF LO. Also make sure that the voltage at REF HI is more positive than the voltage at REF LO, since incorrect reference polarity will always cause an overload reading.

Gross Nonlinearity

If the results are linear for low input voltages, but the displayed result stops increasing as higher input voltages are applied, then the most likely cause is saturation of the integrator output. With a full scale voltage applied, look at the voltage on the INT pin. It should not come closer than 0.3V to either supply. Increase the integrator capacitor value if the INT output swing is excessive. Alternatively, increase the oscillator frequency by changing the oscillator resistor and capacitor values.

Nonlinearities of 2 to 20 Counts

A polyester (Mylar) integrator capacitor will result in about 2 or 3 counts of nonlinearity at full scale. Use polypropylene for best linearity. Leakages into the integrator capacitor, the autozero capacitor, or the reference capacitor will also cause linearity errors. Make sure that printed circuit boards are thoroughly cleaned after soldering.

Gain Error and Rollover Error

A gross gain error will result if the integrator output current capabilities are exceeded. Make sure that $R_{INT} \geq V_{REF}/0.6\mu A$.

Gain errors less than ten counts are generally caused by either too much stray capacitance on the C_{REF} terminals, or by excessive printed circuit board leakage. Stray capacitance and leakage can be detected by reducing the reference capacitor by a factor of ten. If the error dramatically increases, then either stray capacitance or leakage at the reference capacitor terminals is the culprit. Error caused by stray capacitance tend to be a pure gain error, while errors due to leakage tend to be nonlinear—typically square law. Errors due to leakage can also be detected by cleaning the board, then baking to reduce moisture content.

Missing Segments on the LCD Display

This is very, very rarely a problem of the MAX138. More often it is caused open circuits in the LCD connector/bezel, particularly if an elastomeric connector (zebra strip) is used. Check the voltage waveform at the pins of the MAX138. A signal in-phase with the backplane turns off an LCD segment, a signal 180° out of phase from the backplane turns on an LCD segment.

Noisy Readings

The most common reason for noisy readings, particularly in engineering labs, is simply that the input signal is noisy. The 1MΩ/10nF input filter shown in Figures 1 and 2 will significantly reduce high frequency noise, and the capacitor value can be increased to further attenuate 50/60Hz.

If the input signal is clean, then the next thing to check is integrator swing since low integrator swing will increase the noise. If the integrator swing must be reduced to less than 1V for some reason, then increasing the value of the autozero capacitor will improve the noise performance. For most circuits, the integrator swing should be approximately ±2V.

A very low value for the autozero capacitor will also make the readings noisy. The value of the autozero capacitor should be at least twice the value of the integration capacitor, and increasing the autozero capacitor value to between 4 and 10 times that of the integrator capacitor will improve the noise performance, particularly with low reference voltages.

Stray coupling of noise signals, either digital/microprocessor noise or 50/60Hz and 100/120Hz ripple can also be a cause of noisy readings. The circuit area most likely to pick up stray signals is the autozero capacitor. The distance between the autozero capacitor and the AZ pin should be minimized, as should the distance between the autozero capacitor and the

Table 1. Common Mode Voltage Limits

DEVICE	IN HI	IN LO	INTEGRATOR SWING
Positive Input Voltage	V^- + 1.5V to V^+ - 1.5V	V^- + (1.5V + V_{REF}) to V^+ - 1.5V	(IN LO - V^-)
Negative Input Voltage	V^- + 1.5V to V^+ - 1.5V	V^- + 1.5V to V^+ - (1.5V + V_{REF})	(V^+ - IN LO)

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

integration resistor and capacitor. Since the BUFF and INT pins are the outputs of op amps, they are less sensitive to noise pick-up than is the AZ pin, which is the input of an op amp.

The MAX138/139/140 are sensitive to AC noise at IN LO during the de-integrate phase. In particular, full wave AC-DC converters should be used only if both outputs of the AC-DC converter output are well filtered.

The COMMON output of the MAX138/139/140, being derived from a bandgap reference, are noisier than the ICL7106 and ICL7136 Common outputs, which are derived from zeners. This could cause an increase in conversion noise, but only if the C_{REF} is less than 0.1μF, and there is no bypassing at the reference inputs.

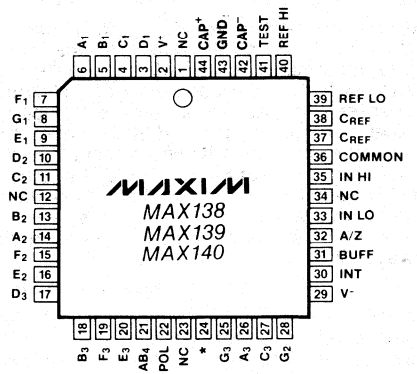
Poor bypassing of the supply voltage may cause a couple of counts of noise in the readings, particularly if the power supply also powers digital logic, since high frequency spikes on the power supply might cause the comparator to falsely indicate zero crossing one or two clock cycles early. Ordinary 0.1μF bypass capacitors are adequate in most cases. Since the MAX138/139/140 draw very little current, a simple RC filter can be used to provide greater spike and ripple attenuation in those cases where the power supply is exceptionally noisy.

Since the oscillator frequency is slightly affected by the supply voltage, large changes in the supply voltage during a conversion may cause a few counts of error. A typical case where the effect must be considered is in a battery powered circuit where the battery is also being used to drive high current loads such as motors or lamps. For extreme cases where high current loads momentarily change the battery voltage a volt or more, use a series diode and a capacitor of 10μF or greater.

Application Hints

1. See the ICL7136 and ICL7106 data sheets for a variety of application circuits which can also be used with the MAX138/139/140.
2. In some applications it may be useful to apply a fixed reference voltage between IN HI and IN LO, and to apply the signal to REF HI and REF LO. In this mode of operation the displayed reading is inversely proportional to the input voltage. In other words, the displayed reading is the result of *dividing* the fixed reference voltage by the signal voltage. A typical application where this function is useful is in an RPM meter, where a voltage proportional to the period of a signal is divided into a fixed voltage to convert period into RPM (frequency). Another example is in a conductance meter, where the conversion between ohms and Siemens is performed by swapping the positions of the unknown and reference resistors.
3. A serial output pulse stream can be obtained from the MAX138/139/140 by monitoring the voltage at the C_{REF} terminals as shown in circuit of Figure 23 in the ICL7106 data sheet. Use an AND gate to combine the resulting End-of-Conversion signal with the oscillator output from OSC3, pin 38.
4. If the input signal polarity is reversed from the desired polarity, then use the "Minus" segment to drive the vertical bar of a plus sign, and permanently turn on the horizontal bar of the plus sign using one of the decimal point driver circuits of Figure 6. When the MAX138/139/140 measures a negative polarity, a "+" will be displayed. When the MAX138/139/140 measures a positive polarity, then a "-" will be displayed. (Normal operation of the MAX138/139/140 is no polarity indication for a positive input, and a "-" sign for a negative input.)

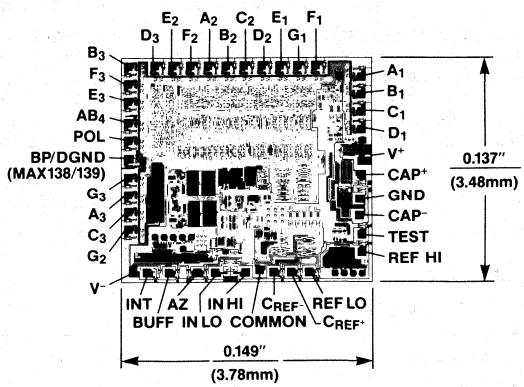
Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

***Note:** BP (MAX 138)
DIGITAL GND (MAX139/140)

Chip Topography



CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

General Description

The MAX150/AD7820 is a high speed, microprocessor compatible, 8 bit analog to digital converter which uses a half-flash technique to achieve a conversion time of 1.34 μs. The converter has a 0V to +5V analog input range and uses a single +5V supply.

A built-in track-and-hold function is included, eliminating the need for an external track-and-hold for input slew rates up to 100mV/μs. The MAX150 also provides an on-chip 2.5 V reference output, making it a complete analog to digital converter.

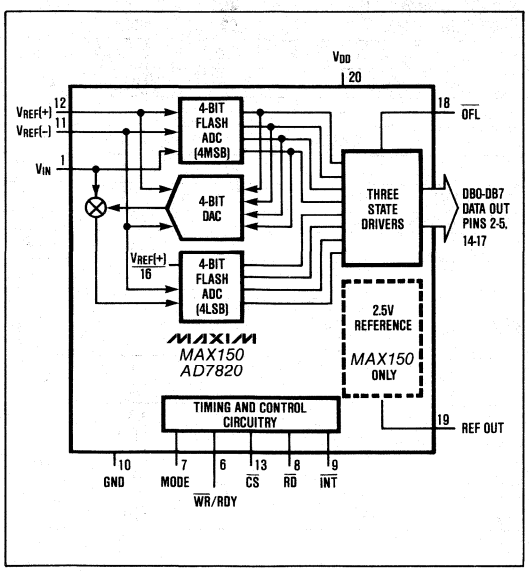
The A/Ds easily interface with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. The data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port. An over-flow output is also provided for cascading devices to achieve higher resolution.

The AD7820 is pin compatible with Analog Devices' AD7820. The MAX150 is also compatible with the AD7820 but also includes an internal 2.5V reference.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Loops
Audio Systems

Functional Block Diagram



Features

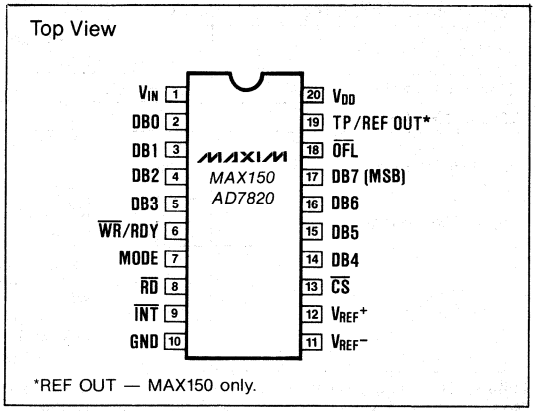
- **Fast Conversion Time: 1.34μs Max.**
- **Built-in Track-and-Hold Function**
- **No Adjustment Required**
- **No External Clock**
- **Single +5V Supply**
- **Easy Interface To Microprocessors**
- **Internal 2.5V Reference (MAX150 only)**

Ordering Information

PART	TEMP. RANGE	PACKAGE†	ERROR
MAX150ACPP	0°C to +70°C	Plastic DIP	±½ LSB
MAX150BCPP	0°C to +70°C	Plastic DIP	±1 LSB
MAX150BC/D	0°C to +70°C	Dice*	±1 LSB
MAX150ACWP	0°C to +70°C	Small Outline	±½ LSB
MAX150BCWP	0°C to +70°C	Small Outline	±1 LSB
MAX150AEPP	-40°C to +85°C	Plastic DIP	±½ LSB
MAX150BEPP	-40°C to +85°C	Plastic DIP	±1 LSB
MAX150AEWP	-40°C to +85°C	Small Outline	±½ LSB
MAX150BEWP	-40°C to +85°C	Small Outline	±1 LSB
MAX150AMJP	-55°C to +125°C	CERDIP	±½ LSB
MAX150BMJP	-55°C to +125°C	CERDIP	±1 LSB

† *All devices — 20 lead packages*
* *Consult factory for dice specifications.*
Ordering Information continued on last page

Pin Configuration



*REF OUT — MAX150 only.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins
(Pins 1-9, 11-19) ..... GND - 0.3V, V_{DD} +0.3V
Output current (Pin 19) 30mA
Power Dissipation (Any Package) to 75°C 450mW
Derate Above +75°C by ..... 6mW/°C

Operating Temperature Ranges
MAX150XCXX, AD7820LN/KN/LCWP/KCWP ... 0°C to +70°C
AD7820BQ/CQ ..... -25°C to +85°C
MAX150XEXX ..... -40°C to +85°C
MAX150XMXX, AD7820TQ/UQ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		MAX150A, AD7820L/C/U MAX150B, AD7820K/B/T			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
REFERENCE INPUT						
Reference Resistance		T_A = +25°C T_A = T_{MIN} to T_{MAX}	1.4 1.25	2.2	4.0 4.0	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD} + 0.1	V
V_{REF}^- Input Voltage Range			GND - 0.1		V_{REF}^+	V
REFERENCE OUTPUT MAX150 ONLY (Note 2)						
Output Voltage	**REF OUT**	**T_A = +25°C**	**2.47**	**2.50**	**2.53**	V
Load Regulation		**I_L = 0 to 10mA T_A = +25°C**		**-6**	**-10**	mV
Power Supply Sensitivity		**V_{DD} ±5% T_A = +25°C**		**±1**	**±3**	mV
Temperature Drift (Note 3)		**MAX150XC T_A = 0°C to +70°C MAX150XE T_A = -40°C to +85°C MAX150XM T_A = -55°C to +125°C**		**40 40 60**	**70 70 100**	ppm/°C
Output Noise				**200**		µV/rms
Capacitive Load					**0.01**	µF
ANALOG INPUT						
Analog Input Voltage Range	V_{INR}		GND - 0.1		V_{DD} + 0.1	V
Analog Input Capacitance	C_{VIN}			45		pF
Analog Input Current	I_{VIN}	V_{IN} = 0V to +5V T_A = +25°C T_A = T_{MIN} to T_{MAX}			±0.3 ±3	µA
Slew Rate, Tracking (Note 4)	SR			0.2	0.1	V/µs
LOGIC INPUTS						
Input HIGH Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$; MAX150 AD7820 MODE	2.0 2.4 3.5			V
Input LOW Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE			0.8 1.5	V
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$; T_A = +25°C T_{MIN} to T_{MAX} $\overline{WR}$; T_A = +25°C T_{MIN} to T_{MAX} MODE; T_A = +25°C T_{MIN} to T_{MAX}		 50	0.3 1 0.3 3 150 200	µA

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Specified with no external load unless otherwise noted.
Note 3: Temperature drift is defined as change in output voltage from +25°C to T_{MIN} or T_{MAX} divided by (25 - T_{MIN}) or (T_{MAX} - 25).
Note 4: Sample tested at +25°C by Quality Assurance to ensure compliance.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
LOGIC INPUTS (continued)						
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE T_A = +25°C T_{MIN} to T_{MAX}			-0.3 -1	µA
Input Capacitance (Note 5)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0–DB7, $\overline{OFL}$, $\overline{INT}$ V_{DD} = +4.75V I_{OUT} = -360µA V_{DD} = +4.75V I_{OUT} = -10µA	4.0 4.5			V
Output LOW Voltage	V_{OL}	DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY V_{DD} = +4.75V I_{OUT} = 1.6mA			0.4	V
Three-state Output Current		DB0–DB7, RDY T_A = +25°C T_{MIN} to T_{MAX}			±0.3 ±3	µA
Output Source Current	I_{SRC}	DB0–DB7, $\overline{OFL}$, $\overline{INT}$; V_{OUT} = 0	-10	-25		mA
Output Sink Current	I_{SINK}	DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{OUT} = V_{DD}	15	40		mA
Output Capacitance (Note 5)	C_{OUT}	DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		5	8	pF
POWER SUPPLY						
Supply Voltage	V_{DD}	+5V ±5% for specified performance	4.75		5.25	V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 T_A = +25°C T_{MIN} to T_{MAX}		5	10 15	mA
Power Dissipation		$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0		25		mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

Note 5: Guaranteed by design.

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog input; range = GND < V_{IN} < V_{DD}.
2	DB0	Three-state data output, bit 0 (LSB).
3	DB1	Three-state data output, bit 1.
4	DB2	Three-state data output, bit 2.
5	DB3	Three-state data output, bit 3.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode selection input. This input is internally pulled low with a 50µA current source. RD Mode: MODE low/open. WR-RD Mode: MODE high.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
10	GND	Ground.

PIN	NAME	FUNCTION
11	V_{REF}^-	Lower limit of reference span. Sets the zero code voltage. Range: GND to V_{REF}^+
12	V_{REF}^+	Upper limit of reference span. Sets the Full Scale input voltage. Range: V_{REF}^- to V_{DD}.
13	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs
14	DB4	Three-state data output, bit 4.
15	DB5	Three-state data output, bit 5.
16	DB6	Three-state data output, bit 6.
17	DB7	Three-state data output, bit 7 (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is greater than V_{REF}^+, $\overline{OFL}$ will be high at the end of the conversion. It can be used to cascade two or more devices to increase resolution.
19	TP REF OUT	Test pin for AD7820. Do not connect pin 19 for AD7820. 2.5V Internal reference output for MAX150 only.
20	V_{DD}	Power supply voltage, +5V.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

TIMING CHARACTERISTICS (Note 1, 2) — MAX150, AD7820

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX150C/E AD7820K/L/B/C		MAX150M AD7820T/U		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to $\overline{RDY}$ Delay	t_{RDY}	C_L = 50pF, R = 3kΩ		35	70		90		100	ns
Conversion Time (RD Mode)	t_{CRD}			1.2	1.6		2.0		2.5	µs
Data Access Time (RD Mode) (See Figure 4)	t_{ACC0}	(Note 3)		t_{CRD} + 10	t_{CRD} + 20		t_{CRD} + 35		t_{CRD} + 50	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		60	125		175		225	ns
Data Hold Time	t_{DH}	(Note 4)		40	60		80		100	ns
Delay Time Between Conversions	t_P		500			600		600		ns
Write Pulse Width	t_{WR}		600		50,000	600	50,000	600	50,000	ns
Conversion Time ($\overline{WR}$/$\overline{RD}$ Mode)	t_{CWR-RD}		1.34			1.5		1.53		µs
Delay between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		600			700		700		ns
Data Access Time ($\overline{WR}$/$\overline{RD}$ Mode) (See Figure 6)	t_{ACC1}	$t_{RD} < t_{INTL}$, (Note 3)		110	160		225		250	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}			100	140		200		225	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}			600	1000		1400		1700	ns
Data Access Time ($\overline{WR}$/$\overline{RD}$ Mode) (See Figure 5)	t_{ACC2}	$t_{RD} > t_{INTL}$, (Note 3)		60	70		90		110	ns
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone)	t_{IHWR}	C_L = 50pF		70	100		130		150	ns
Data Access Time After $\overline{INT}$	t_{ID}			10	50		65		75	ns

Note 1: Sample tested at +25°C by Quality Assurance to ensure compliance.
Note 2: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 3: Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 4: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

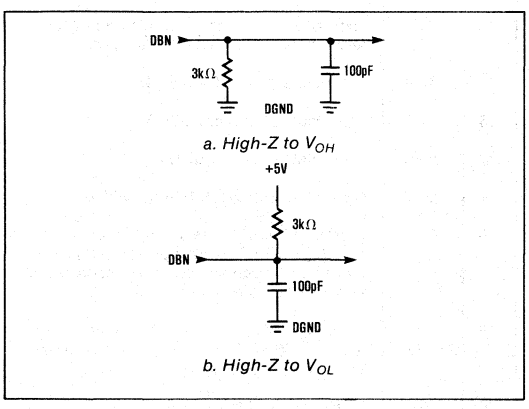


Figure 1. Load Circuits for Data Access Time Test

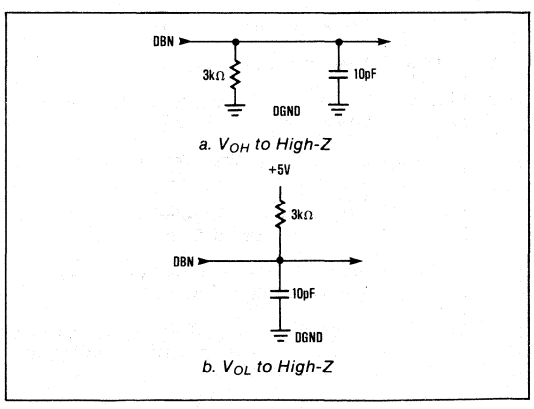
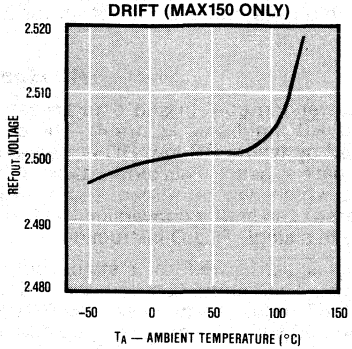


Figure 2. Load Circuits for Data Hold Time Test

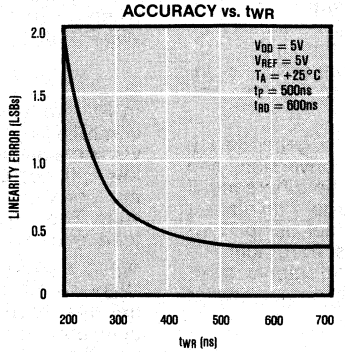
CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Typical Operating Characteristics

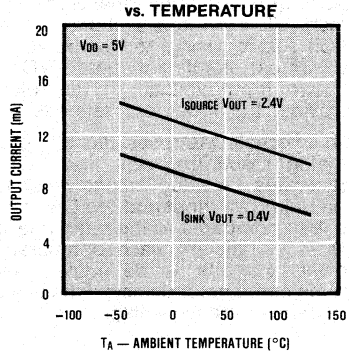
REFERENCE TEMPERATURE DRIFT (MAX150 ONLY)



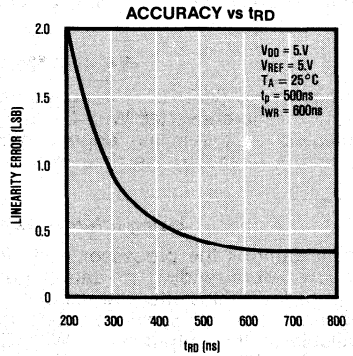
ACCURACY vs. tWR



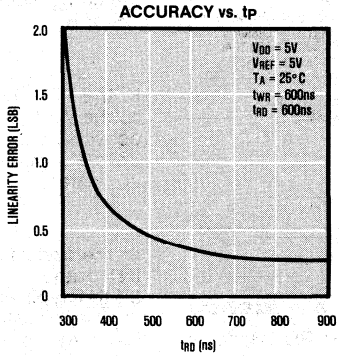
OUTPUT CURRENT vs. TEMPERATURE



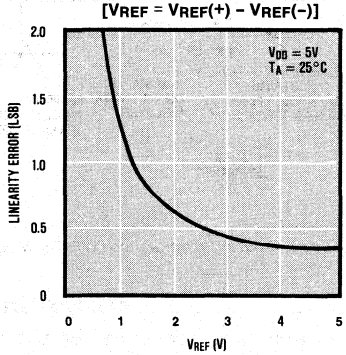
ACCURACY vs tRD



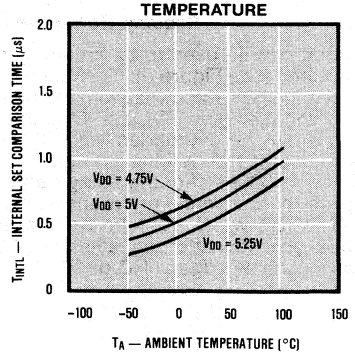
ACCURACY vs. tP



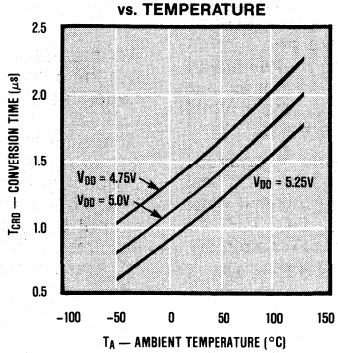
ACCURACY vs. VREF [VREF = VREF(+) - VREF(-)]



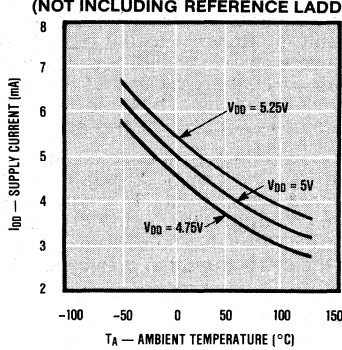
tINTL INTERNAL TIME DELAY vs. TEMPERATURE



CONVERSION TIME (RD MODE) vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE (NOT INCLUDING REFERENCE LADDER)



CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Detailed Description

Converter Operation

The MAX150/AD7820 uses a "half-flash" conversion technique (see Functional Block Diagram). Two 4-bit flash A/D converter sections are used to achieve an 8-bit result. Using 15 comparators, the upper 4-bit MS (most significant) flash A/D compares the unknown input voltage to the reference ladder and provides the upper four data bits.

An internal DAC uses the MS bits to generate the analog result from the first flash conversion, and generates a residue voltage which is the difference of the unknown input and the DAC voltage. The residue is then compared to the reference ladder using 15 LS (least significant) flash comparators to obtain the lower four bits of the output. An additional overrange comparator detects if the analog input is greater than the reference voltage.

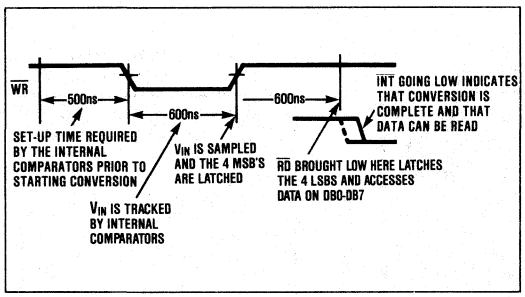


Figure 3. Operating Sequence (WR-RD Mode).

Operating Sequence

The operating sequence for the WR-RD Mode is shown in Figure 3. The conversion is initiated by a falling edge of WR. The comparator inputs track the analog input voltage for the duration of WR low. A minimum of 600ns is required for the input voltage to be acquired. When WR returns high, the MS flash result is latched into the output buffers and the LS conversion begins. INT goes low approximately 600ns later, indicating the end of the conversion, and that the lower 4 data bits are latched into the output buffers. RD going low then accesses the data.

If an externally controlled conversion time is required, the RD line can be brought low as soon as 600ns after WR goes high. This will latch the lower 4 data bits and output the conversion result on DB0-DB7. At least 500ns setup time is required from INT going low to the start of another conversion (WR going low).

Digital Interface

The MAX150/AD7820 has two basic interface modes which are set by the status of the MODE input pin. When this pin is low, the converter is in the RD mode, when this pin is high the converter is set up for the WR-RD mode.

RD Mode

In RD mode, conversion control and data access is controlled by the RD input (see Figure 4). The conversion is initiated by taking RD low. RD is then kept low until output data appears. This mode is useful for microprocessors which can be forced into a WAIT state. The processor can start a conversion, wait, and then read data with a single READ instruction.

Pin 6 (WR/RDY) is configured as a status output (RDY) in RD mode. This output can be used to drive the READY or WAIT input of a processor. RDY is an open collector output (with no internal pull-up device) which goes low after the falling edge of CS and goes high impedance at the end of the conversion. An INT output is also provided which goes low at the end of the conversion and returns high on the rising edge of CS or RD.

WR-RD Mode

In the WR-RD mode, pin 6 (WR/RDY) is configured as the WRITE input for the converter. With CS low, a conversion is initiated on the falling edge of WR. Several options exist for reading the data from the converter.

Using Internal Delay

In the first of these options the processor waits for INT output to go low before reading the data (Figure 5). INT typically goes low 600ns after the rising edge of WR, indicating that the conversion is complete and the result is available in the output latch. With CS low, data outputs DB0-DB7 can be accessed by pulling RD low. INT is then reset by the rising edge of CS or RD.

Reading Before Delay

An alternative option can be used to externally control the conversion time (see Figure 6). The internally generated 600ns delay varies somewhat with temperature and supply voltage (see Typical Operating Characteristics) and can be overridden with RD. To achieve this, the status of INT is ignored and RD is brought low as soon as 600ns after the rising edge of WR. This completes the conversion and enables the output buffers, DB0-DB7, which contain the conversion result. INT also goes low after the falling edge of RD and is reset on the rising edge of RD or CS.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Pipelined Operation

In addition to the two standard WR-RD mode options, "pipe-lined" operation can be achieved by tying $\overline{WR}$ and $\overline{RD}$ together (see Figure 7). With $\overline{CS}$ low, $\overline{WR}$ and $\overline{RD}$ going low initiates a conversion, and reads the result of the previous conversion at the same time.

Stand-Alone Operation

The converter can also be used in a stand-alone operation (see Figure 8). $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by pulling $\overline{WR}$ low. Output data is valid approximately 600ns after the rising edge of $\overline{WR}$.

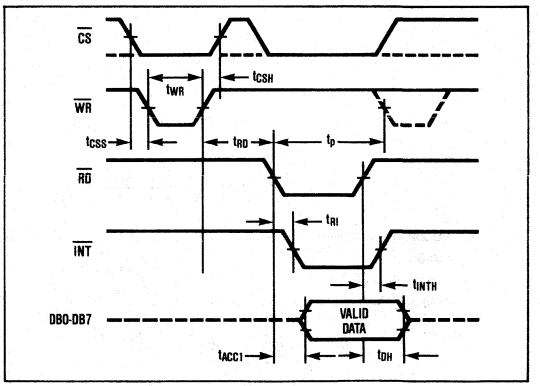


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$).

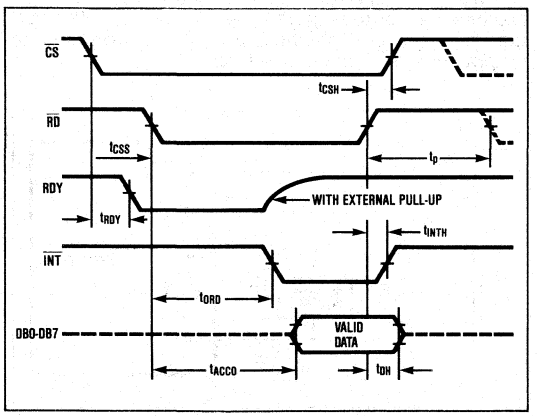


Figure 4. RD Mode Timing.

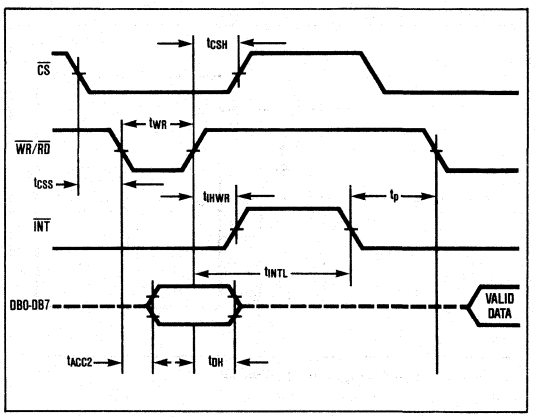


Figure 7. WR-RD Mode Pipe-Lined Timing $\overline{WR} = \overline{RD}$.

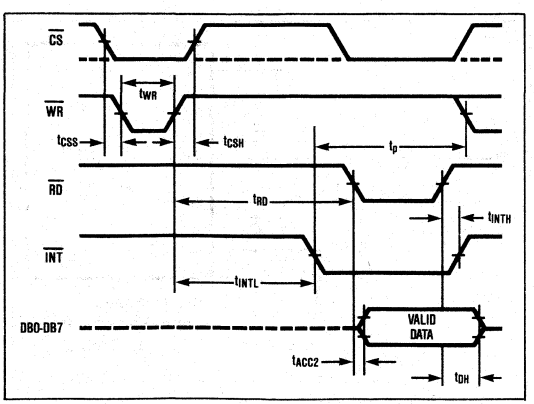


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$).

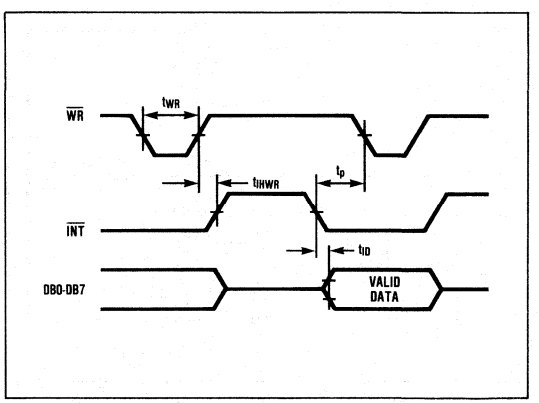


Figure 8. WR-RD Mode Stand-Alone Timing $\overline{CS} = \overline{RD} = 0$.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

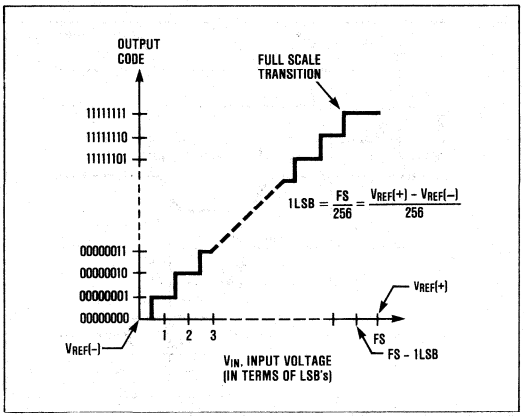


Figure 9. Transfer Function.

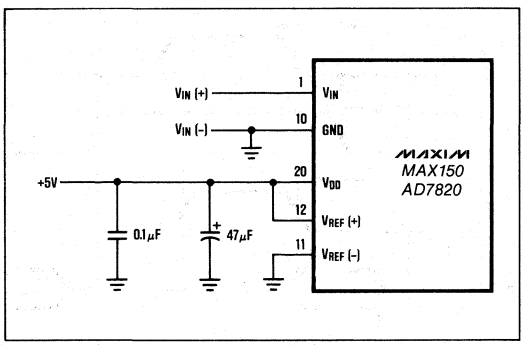


Figure 10a. Power Supply as Reference.

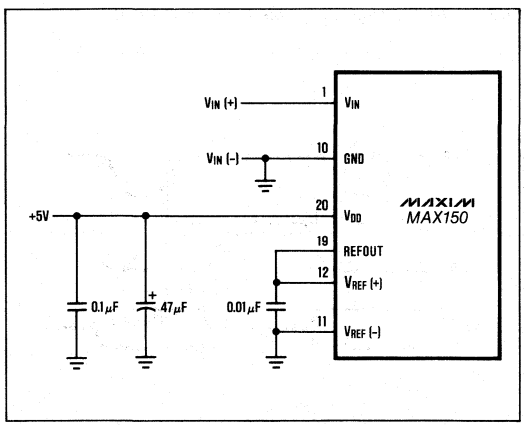


Figure 10c. Internal Reference (MAX150 only).

Analog Considerations

Reference

The MAX150 includes an internal 2.5V reference (REFOUT) which is appropriate for the majority of 8 bit measurement applications. To use the on-chip reference, connect REFOUT, pin 19, to V_{REF}^+, pin 12, and connect V_{REF}^-, pin 11, to ground. The 2.5V output is referred to GND, pin 10. Both the MAX150 and the AD7820, which does not have an on-chip reference, can be used with an external reference if desired.

Figure 10 shows some possible reference connections. For the MAX150, a 0.01µF bypass capacitor to GND should be used to reduce the high frequency output impedance of the internal reference. Larger capacitors should not be used as this degrades the stability of the reference buffer.

The V_{REF}^+ and V_{REF}^- inputs of both converters set the full-scale and zero input voltages of the A/D. In other words, the voltage at V_{REF}^- defines the input which produces an output code of all zeroes, and the voltage at V_{REF}^+ defines the input which produces an output code of all ones (see Figure 9).

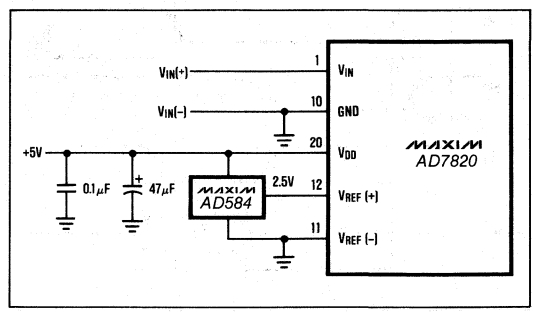


Figure 10b. External Reference 2.5V Full-Scale.

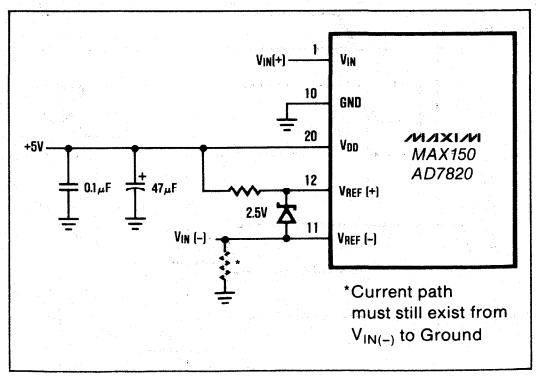


Figure 10d. Input Not Referenced to GND.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. These capacitors should have the minimum possible lead length. Excess lead length may contribute to conversion errors and instability.

If the reference inputs (pins 11, 12) are driven by long lines, they should be bypassed to GND with 0.1 μF capacitors at the V_{REF} pins.

Input Current

The MAX150/AD7820 analog input behaves somewhat differently from conventional A/D converters. The sampled data comparators take varying amounts of current from the input depending on the cycle they are in.

The equivalent circuit of the converter is shown in Figure 11. When the conversion starts and $\overline{WR}$ is low, V_{IN} is connected to the MS and LS comparators. Thus, V_{IN} is connected to thirty-one 1pF capacitors.

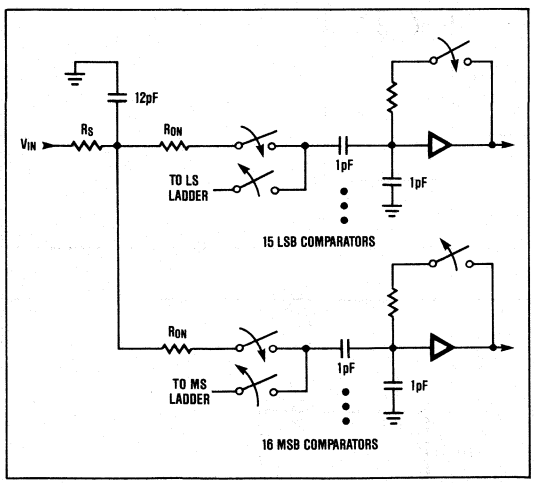


Figure 11a. Equivalent Input Circuit.

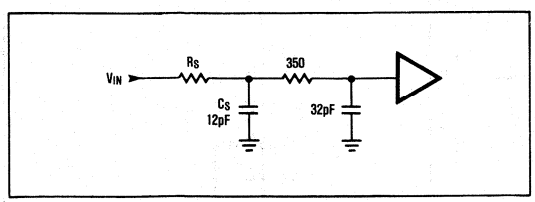


Figure 11b. RC Network Model.

During this acquisition phase ($\overline{WR}$ = Low in the WR-RD Mode) the input capacitors must be charged to the input voltage through the resistance of the internal analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of stray capacitance must be charged. The input can be modelled as an equivalent RC network shown in Figure 11. As R_S (source impedance) increases, the capacitors take longer to charge.

Typical input capacitances of 45pF allow source resistances of up to 1kΩ to be used without settling problems. For larger resistances, the width of the $\overline{WR}$ pulse must be increased from 600ns. Since the length of this acquisition time is internally set when in the RD mode, large source resistances (greater than 1kΩ) may cause settling errors. In this case, use the WR-RD mode and greater than 600ns RD time or use a buffer to drive the analog input.

Input Filtering

The transients in the analog input due to the sampled data comparators do not degrade the converter's performance since the A/D does not "look" at the input when these transients occur. The comparator's outputs track the input while $\overline{WR}$ is low, and are latched once $\overline{WR}$ goes high. Therefore, at least 600ns will be provided to charge the ADC's input capacitance. It is not necessary to filter these transients with an external capacitor on the V_{IN} terminal.

Inherent Track-and-Hold

Due to its sampling behavior, the MAX150/AD7820 has the ability to measure a variety of high speed input signals without the help of an external sample-and-hold. In a conventional SAR type converter, the analog input must remain stable within 1/2 LSB for the duration of the conversion to maintain accuracy. This requires the use of external sample-and-holds whenever the input is a high speed signal. Although the conversion time for the MAX150/AD7820 is 1.34μs, the time for which the input must be stable is much less.

The MAX150/AD7820 tracks the input while $\overline{WR}$ is low (in the WR-RD mode) and finishes sampling it approximately 100ns after the rising edge of $\overline{WR}$. This aperture delay is caused by the internal logic propagation delay. Input signals with slew rates typically below 200mV/μs can be converted without error. However, faster signals may cause differential linearity errors due different delays through the MS and LS comparators. Still, the errors caused by fast input signals are far less than the errors caused in a conventional SAR type ADC without a sample-and-hold. A 1μs SAR converter would still not be able to measure a 1kHz, 5V sine wave without the aid of an external sample-and-hold. The MAX150/AD7820 with no such help, can typically measure 5V, 10kHz waveforms.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

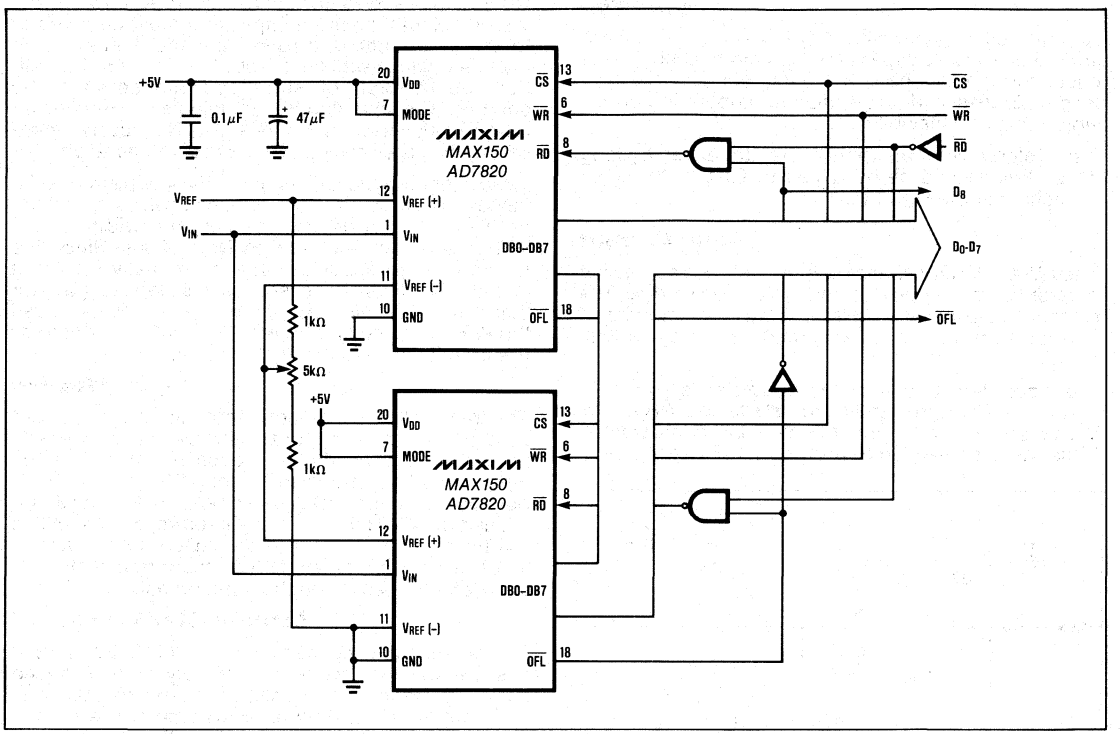


Figure 12. 9-Bit Resolution

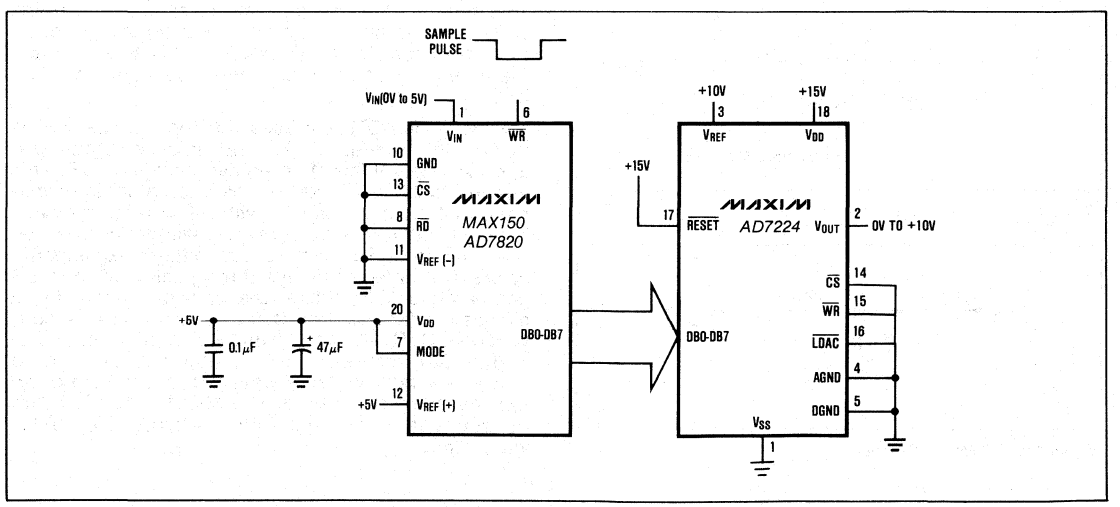


Figure 13. Fast Sample-and-Infinite Hold

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

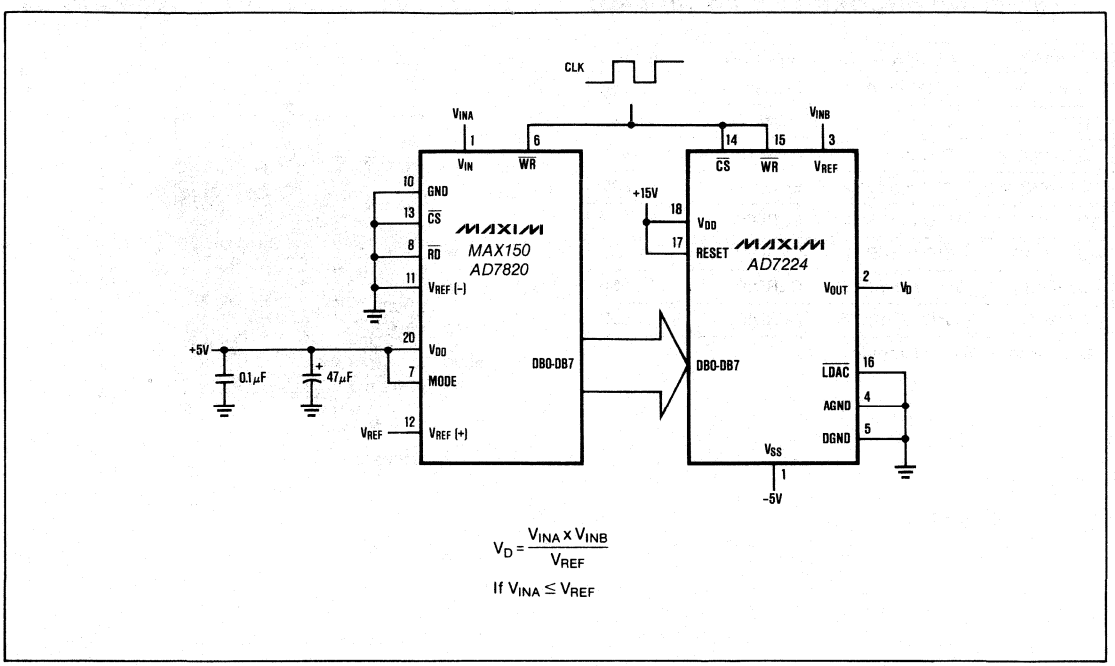


Figure 14. 8-Bit Analog Multiplier

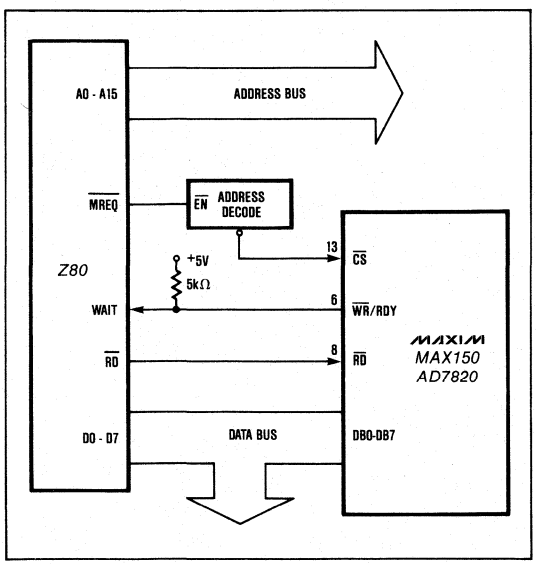
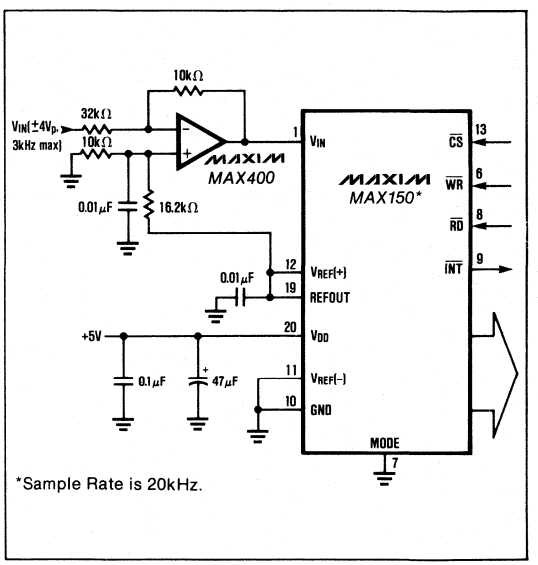


Figure 15. Simple $\overline{RD}$-Mode Interface



*Sample Rate is 20kHz.

Figure 16. Telecom A/D Converter

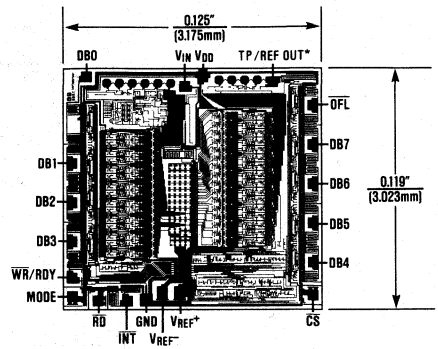
CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE†	ERROR
AD7820LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7820KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7820LCWP	0° C to +70° C	Small Outline	±½ LSB
AD7820KCWP	0° C to +70° C	Small Outline	±1 LSB
AD7820CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7820BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7820UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7820TQ	-55° C to +125° C	CERDIP	±1 LSB

† *All devices — 20 lead packages*

Chip Topography



*MAX150 Only.

MAXIM

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

General Description

The MAX154/MAX158 and AD7824/AD7828 are high speed multi-channel A/D converters. The MAX154 and AD7824 have 4 analog input channels while the MAX158 and AD7828 have 8 channels. Conversion time for all devices is 2.5μs. The MAX154/MAX158 also features a 2.5V on-chip reference, forming a complete high speed data acquisition system.

All converters include a built-in track-and-hold, eliminating the need for an external track-and-hold with many input signals. The analog input range is 0V to +5V although the A/D operates from a single +5V supply.

Microprocessor interface's are simplified by the ADC's ability to appear as a memory location or I/O port without the need for external logic. The data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port.

The AD7824 and AD7828 are pin compatible with Analog Devices' AD7824 and AD7828. The MAX154 and MAX158, which feature internal references, are also compatible with these products.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Control
Audio Instrumentation

Features

- **One-Chip Data Acquisition System**
- **4 or 8 Analog Input Channels**
- **2.5μs Per Channel Conversion Time**
- **Internal 2.5V Reference (MAX154/MAX158 only)**
- **Built in Track/Hold Function**
- **½ LSB Error Specification**
- **Single +5V Supply Operation**
- **No External Clock**

Ordering Information

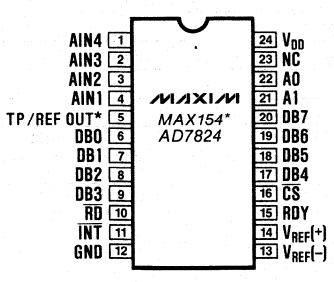
PART	TEMP RANGE	PACKAGE*	ERROR
MAX154ACNG	0° C to +70° C	Plastic DIP	±½ LSB
MAX154BCNG	0° C to +70° C	Plastic DIP	±1 LSB
MAX154BC/D	0° C to +70° C	Dice	±1 LSB
MAX154ACWG	0° C to +70° C	Small Outline	±½ LSB
MAX154BCWG	0° C to +70° C	Small Outline	±1 LSB
MAX154AENG	-40° C to +85° C	Plastic DIP	±½ LSB
MAX154BENG	-40° C to +85° C	Plastic DIP	±1 LSB
MAX154AEWG	-40° C to +85° C	Small Outline	±½ LSB
MAX154BEWG	-40° C to +85° C	Small Outline	±1 LSB
MAX154AMRG	-55° C to +125° C	CERDIP	±½ LSB
MAX154BMRG	-55° C to +125° C	CERDIP	±1 LSB

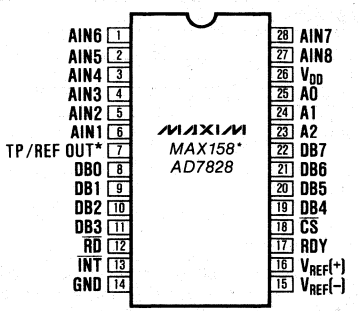
* *MAX154/AD7824 — 24 lead package, MAX158/AD7828 — 28 lead package*

Ordering Information continued on last page.

Pin Configurations

Top View





*Test Point for AD7824/AD7228. Do not connect. REFOUT on MAX154/MAX158 only.

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins ..... GND - 0.3V, V_{DD} +0.3V
Output current (REF_{OUT}) 30mA
Power Dissipation (Any Package) to 75°C 450mW
Derate Above +25°C by ..... 6mW/°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Operating Temperature Ranges
MAX154, MAX158
XCXX ..... 0°C to +70°C
XEXX ..... -40°C to +85°C
XMXX ..... -55°C to +125°C
AD7824, AD7828
KN/LN/KCWX/LCWX ..... 0°C to +70°C
BQ/CQ ..... -25°C to +85°C
TQ/UQ ..... -55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, MODE 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		MAX15XA, AD782XL/C/U MAX15XB, AD782XK/B/T			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
Channel to Channel Mismatch					±1/4	LSB
REFERENCE INPUT						
Reference Resistance		T_A = T_{MIN} to T_{MAX}	1		4	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD}	V
V_{REF}^- Input Voltage Range			GND		V_{REF}^+	V
REFERENCE OUTPUT — MAX154/MAX158 ONLY (NOTE 2)						
Output Voltage	**REF OUT**	**T_A = +25°C**	**2.47**	**2.50**	**2.53**	**V**
Load Regulation		**I_L = 0 to 10mA T_A = +25°C**		**-6**	**-10**	**mV**
Power Supply Sensitivity		**V_{DD} ±5% T_A = +25°C**		**±1**	**±3**	**mV**
Temperature Drift (Note 3)		**MAX15XXC T_A = 0°C to +70°C MAX15XXE T_A=-40°C to +85°C MAX15XXM T_A=-55°C to +125°C**		**40 40 60**	**70 70 100**	**ppm/°C**
Output Noise	**e_N**			**200**		**μV/rms**
Capacitive Load					**0.01**	**μF**
ANALOG INPUT						
Analog Input Voltage Range	A_{INR}		V_{REF}^-		V_{REF}^+	V
Analog Input Capacitance	C_{AIN}			45		pF
Analog Input Current	I_{AIN}	Any Channel, AIN = 0V to +5V			±3	μA
Slew Rate, Tracking (Note 4)	SR			0.7	0.157	V/μs
LOGIC INPUTS (RD, CS, A0, A1, A2)						
Input HIGH Voltage	V_{INH}		2.4			V
Input LOW Voltage	V_{INL}				0.8	V
Input High Current	I_{INH}				1	μA
Input Low Current	I_{INL}				-1	μA
Input Capacitance (Note 8)	C_{IN}			5	8	pF

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Specified with no external load unless otherwise noted.
Note 3: Temperature drift is defined as change in output voltage from +25°C to T_{MIN} or T_{MAX} divided by (25 - T_{MIN}) or (T_{MAX} -25).
Note 4: Sample tested at +25°C by Quality Assurance to ensure compliance.

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, MODE 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0–DB7, $\overline{INT}$; I_{OUT} = -360μA	4.0			V
Output LOW Voltage	V_{OL}	DB0–DB7, $\overline{INT}$; I_{OUT} = 1.6mA RDY; I_{OUT} = 2.6mA			0.4 0.4	V
Three-state Output Current		DB0–DB7, RDY; V_{OUT} = 0V to V_{DD}			±3	μA
Output Capacitance (Note 8)	C_{OUT}			5	8	pF
POWER SUPPLY						
Supply Voltage	V_{DD}	5V ±5% for Specified Performance	+4.75		+5.25	V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = +2.4V			15	mA
Power Dissipation				25	75	mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

TIMING CHARACTERISTICS (Note 4, 5)

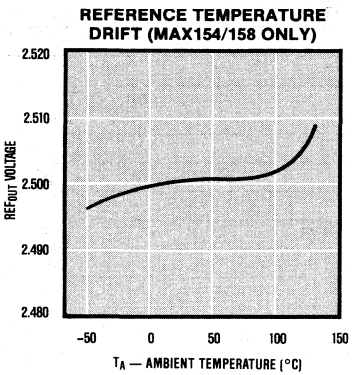
(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

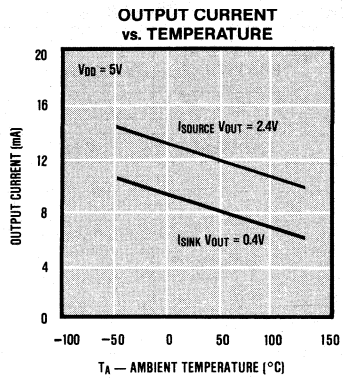
PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX15XC/E AD782XK/L/B/C		MAX15XM AD782XT/U		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, Hold Time	t_{CSH}		0			0		0		ns
Multiplexer Address Setup Time	t_{AS}		0			0		0		ns
Multiplexer Address Hold Time	t_{AH}		30			35		40		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R = 5kΩ		30	40		60		60	ns
Conversion Time (Mode 0)	t_{CRD}			1.6	2.0		2.4		2.8	μs
Data Access Time After $\overline{RD}$	t_{ACC1}	(Note 6)			85		110		120	ns
Data Access Time After INT, Mode 0	t_{ACC2}	(Note 6)		20	50		60		70	ns
$\overline{RD}$ to $\overline{INT}$ Delay (Mode 1)	t_{INTH}	C_L = 50pF		40	75		100		100	ns
Data Hold Time	t_{DH}	(Note 7)			60		70		70	ns
Delay Time Between Conversions	t_P		500			500		600		ns
$\overline{RD}$ Pulse Width (Mode 1)	t_{RD}		60		600	80	500	80	400	ns

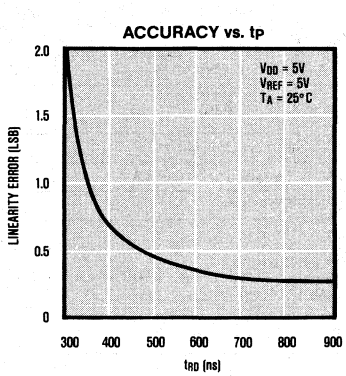
Note 5: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 6: Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4 V.
Note 7: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Note 8: Guaranteed by design.

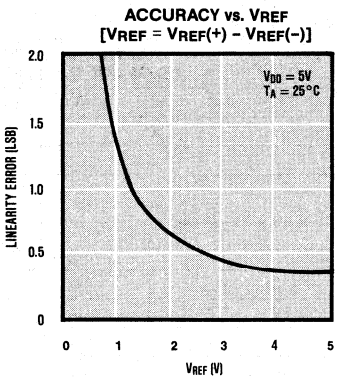
CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

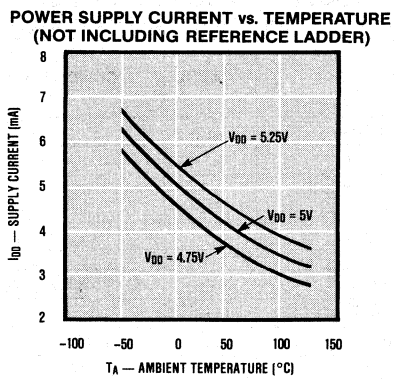
Typical Operating Characteristics











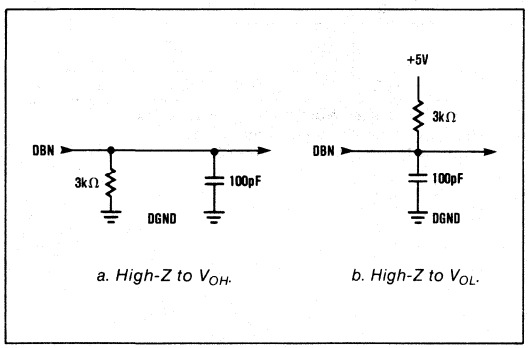


Figure 1. Load Circuits for Data Access Time Test

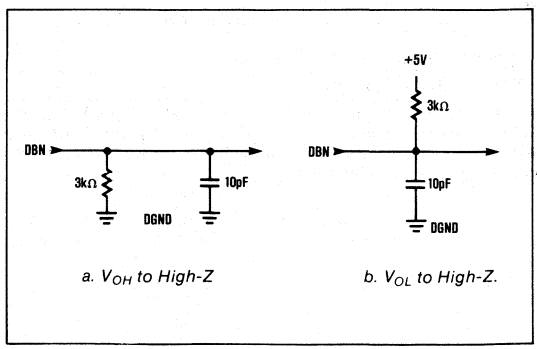


Figure 2. Load Circuits for Data Hold Time Test

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

MAX154/AD7824 Pin Description

PIN	NAME	FUNCTION
1	AIN4	Analog input channel 4
2	AIN3	Analog input channel 3
3	AIN2	Analog input channel 2
4	AIN1	Analog input channel 1
5	REFOUT TP	Reference output (2.5V) for MAX154 Test Point for AD7824. Do not connect.
6	DB0	Three-state data output, bit 0 (LSB)
7	DB1	Three-state data output, bit 1
8	DB2	Three-state data output, bit 2
9	DB3	Three-state data output, bit 3
10	$\overline{RD}$	READ input. $\overline{RD}$ controls conversions and data access. See Digital Interface section.
11	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
12	GND	Ground
13	$V_{REF}(-)$	Lower limit of reference span. Sets the zero code voltage. Range: GND to $V_{REF}(+)$
14	$V_{REF}(+)$	Upper limit of reference span. Sets the Full Scale input voltage. Range: $V_{REF}(-)$ to V_{DD}.
15	RDY	READY Output. Open drain output with no active pull-up device. Goes low when $\overline{CS}$ goes low and high impedance at the end of a conversion.
16	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to be selected.
17	DB4	Three-state data output, bit 4
18	DB5	Three-state data output, bit 5
19	DB6	Three-state data output, bit 6
20	DB7	Three-state data output, bit 7 (MSB)
21	A1	Channel Address 1 Input
22	A0	Channel Address 0 Input
23	NC	No Connect
24	V_{DD}	Power supply voltage, +5V

MAX158/AD7828 Pin Description

PIN	NAME	FUNCTION
1	AIN6	Analog input channel 6
2	AIN5	Analog input channel 5
3	AIN4	Analog input channel 4
4	AIN3	Analog input channel 3
5	AIN2	Analog input channel 2
6	AIN1	Analog input channel 1
7	REFOUT TP	Reference output (2.5V) for MAX158 Test Point for AD7828. Do not connect.
8	DB0	Three-state data output, bit 0 (LSB)
9	DB1	Three-state data output, bit 1
10	DB2	Three-state data output, bit 2
11	DB3	Three-state data output, bit 3
12	$\overline{RD}$	READ input. $\overline{RD}$ controls conversions and data access. See Digital Interface section.
13	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
14	GND	Ground
15	$V_{REF}(-)$	Lower limit of reference span. Sets the zero code voltage. Range: GND to $V_{REF}(+)$
16	$V_{REF}(+)$	Upper limit of reference span. Sets the Full Scale input voltage. Range: $V_{REF}(-)$ to V_{DD}.
17	RDY	READY Output. Open drain output with no active pull-up device. Goes low when $\overline{CS}$ goes low and high impedance at the end of a conversion.
18	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to be selected.
19	DB4	Three-state data output, bit 4
20	DB5	Three-state data output, bit 5
21	DB6	Three-state data output, bit 6
22	DB7	Three-state data output, bit 7 (MSB)
23	A2	Channel Address 2 Input
24	A1	Channel Address 1 Input
25	A0	Channel Address 0 Input
26	V_{DD}	Power supply voltage, +5V
27	AIN8	Analog input channel 8
28	AIN7	Analog input channel 7

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

Detailed Description

Converter Operation

The MAX154/MAX158/AD7824/AD7828 uses what is commonly called a "half-flash" conversion technique (see Figure 3). Two 4-bit flash A/D converter sections are used to achieve an 8-bit result. Using 15 comparators, the upper four bit MS (most significant) flash A/D compares the unknown input voltage to the reference ladder and provides the upper four data bits.

An internal DAC uses the MS bits to generate an analog signal from the first flash conversion. A residue voltage representing the difference between the unknown input and the DAC voltage is then compared to the reference ladder by 15 LS (least significant) flash comparators to obtain the lower four output bits.

Operating Sequence

The operating sequence is shown in Figure 4. A conversion is initiated by a falling edge of RD and CS. The comparator inputs track the analog input voltage for approximately 1μs. After this first cycle the MS flash result is latched into the output buffers and the LS conversion begins. INT goes low approximately 600ns later, indicating the end of the conversion, and that the lower 4 bits are latched into the output buffers. The data can then be accessed using the CS and RD inputs.

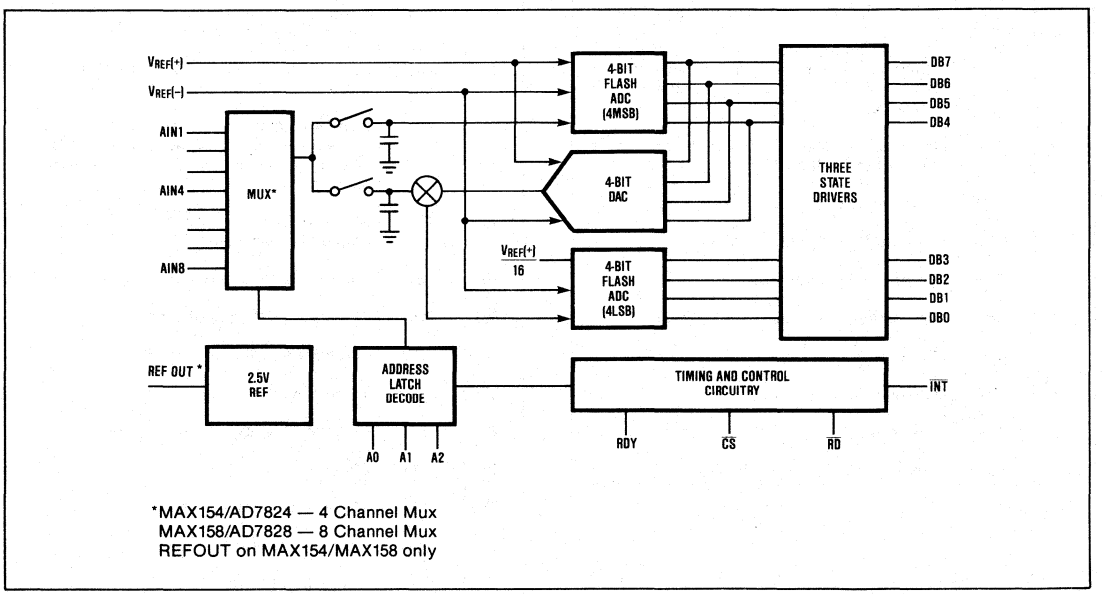
Digital Interface

The MAX154/MAX158 and AD7824/AD7828 use only Chip Select (CS) and Read (RD) as control inputs. A READ operation, taking CS and RD low, latches the multiplexer address inputs and starts a conversion (See Table 1).

Table 1.
Truth Table For Input Channel Selection

MAX154/AD7824 A1	MAX154/AD7824 A0	MAX158/AD7828 A2	MAX158/AD7828 A1	MAX158/AD7828 A0	SELECTED CHANNEL
0	0	0	0	0	AIN1
0	1	0	0	1	AIN2
1	0	0	1	0	AIN3
1	1	0	1	1	AIN4
		1	0	0	AIN5
		1	0	1	AIN6
		1	1	0	AIN7
		1	1	1	AIN8

There are two interface modes which are determined by the length of the RD input. Mode 0, implemented by keeping RD low until the conversion ends, is designed for microprocessors that can be forced into a WAIT state. In this mode, a conversion is started with a READ operation (taking CS and RD low) and data is read when the conversion ends. Mode 1 on the other hand does not require microprocessor WAIT states. A READ operation simultaneously initiates a conversion and reads the previous conversion result.



*MAX154/AD7824 — 4 Channel Mux
MAX158/AD7828 — 8 Channel Mux
REFOUT on MAX154/MAX158 only

Figure 3. Functional Diagram

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

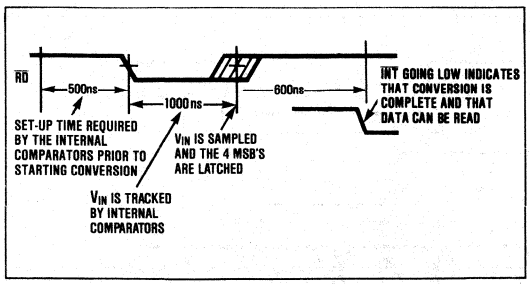


Figure 4. Operating Sequence

Interface Mode 0

Figure 5 shows the timing diagram for Mode 0 operation. This is used with microprocessors that have WAIT state capability, whereby a READ instruction is extended to accomodate slow memory devices. Taking $\overline{CS}$ and $\overline{RD}$ low latches the analog multiplexer address and starts a conversion. Data outputs DB0-DB7 remain in the high impedance condition until the conversion is complete.

There are two status outputs, Interrupt ($\overline{INT}$) and Ready (RDY). RDY, an open drain output (no internal pull-up device), is connected to the processor's READY/WAIT input. RDY goes low on the falling edge of $\overline{CS}$ and goes high impedance at the end of the conversion, when the conversion result appears on the data outputs. If the RDY output is not required, its external pull-up resistor can be omitted. $\overline{INT}$ goes low when the conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Interface Mode 1

Mode 1 is designed for applications where the microprocessor is not forced into a WAIT state. Taking $\overline{CS}$ and $\overline{RD}$ low latches the multiplexer address and starts a conversion (See Figure 6). Data from the previous conversion is immediately read from the outputs (DB0-DB7).

$\overline{INT}$ goes high at the rising edge of $\overline{CS}$ or $\overline{RD}$ and goes low at the end of the conversion. A second READ operation is required to read the result of this conversion. The second READ latches a new multiplexer address and starts another conversion. A delay of 2.5μs must be allowed between READ operations. RDY goes low on the falling edge of $\overline{CS}$ and goes high impedance at the rising edge of $\overline{CS}$. If RDY is not needed, its external pull-up resistor can be omitted.

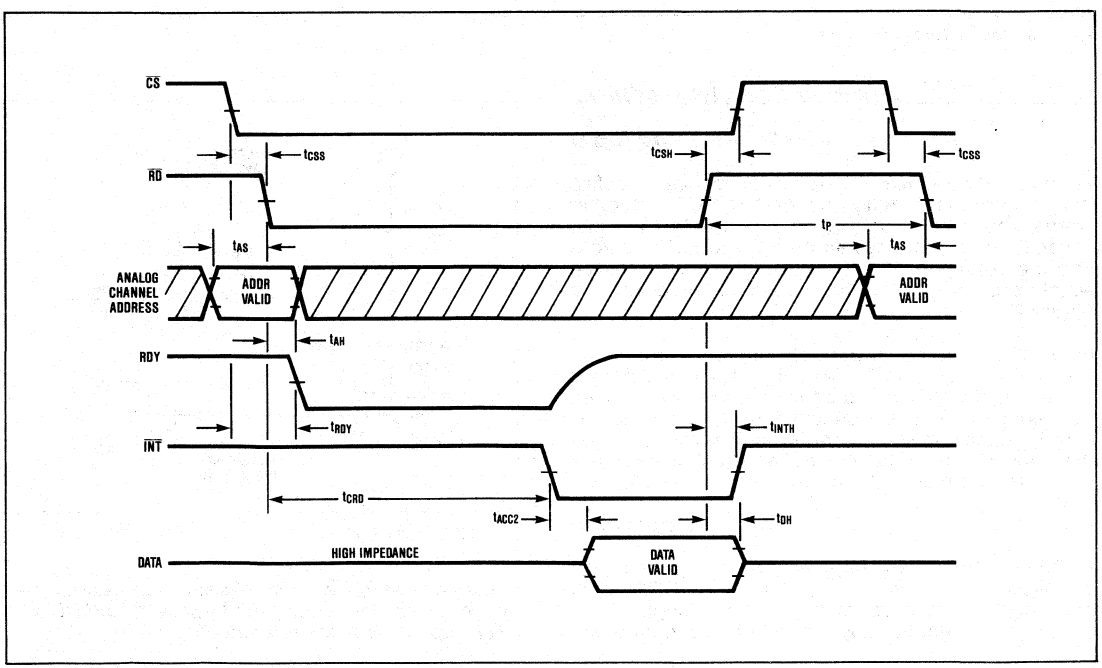


Figure 5. Mode 0 Timing Diagram

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

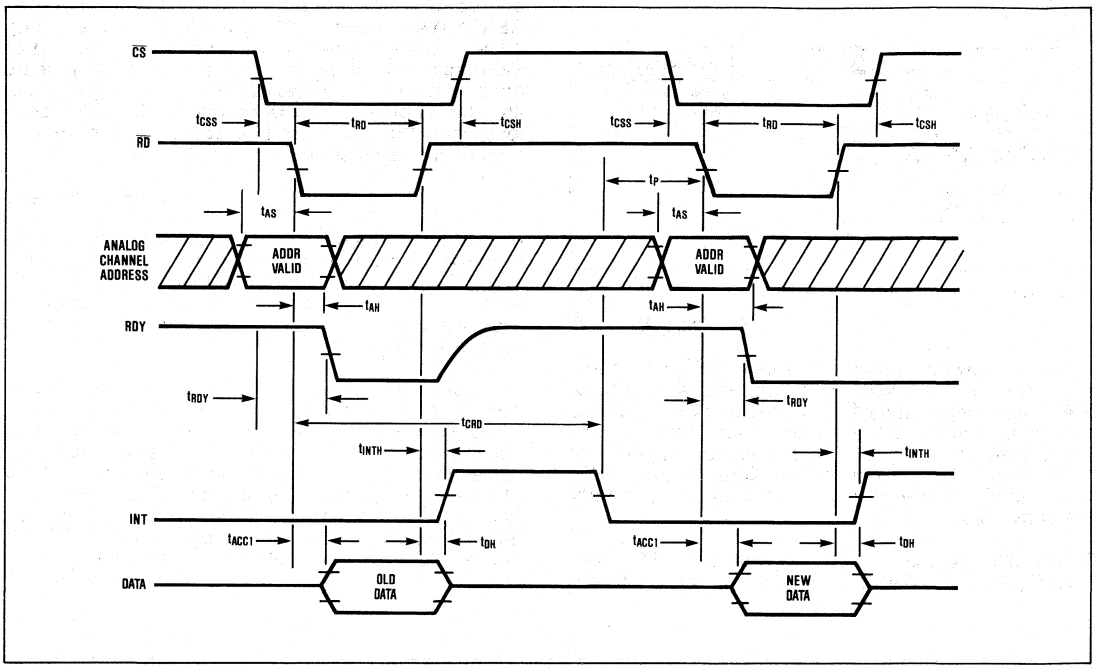


Figure 6. Mode 1 Timing Diagram

Analog Considerations

Reference and Input

The $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the converter define the zero and the full-scale of the ADC. In other words, the voltage at $V_{REF}(-)$ is equal to the input voltage which produces an output code of all zeroes and the voltage at $V_{REF}(+)$ is equal to input voltage which produces an output code of all ones (see Figure 7).

Figure 8 shows some possible reference configurations. For the MAX154/MAX158, a 0.01μF bypass capacitor to GND should be used to reduce the high frequency output impedance of the internal reference. Larger capacitors should not be used as this degrades the stability of the reference buffer. The 2.5V reference output is with respect to the GND pin.

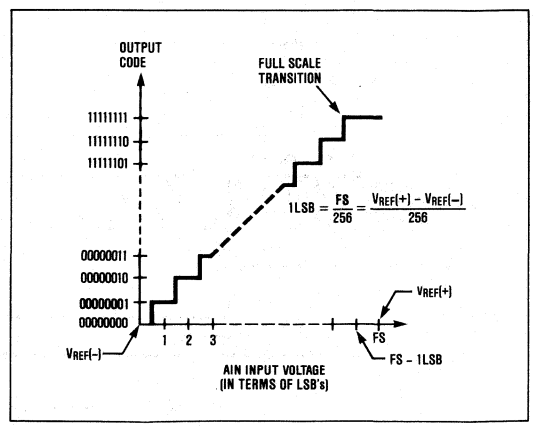


Figure 7. Transfer Function

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. These capacitors must have minimum lead length since excess lead length may contribute to conversion errors and instability. If the reference inputs are driven by long lines, they should be bypassed to GND with 0.1μF capacitors at the reference input pins.

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

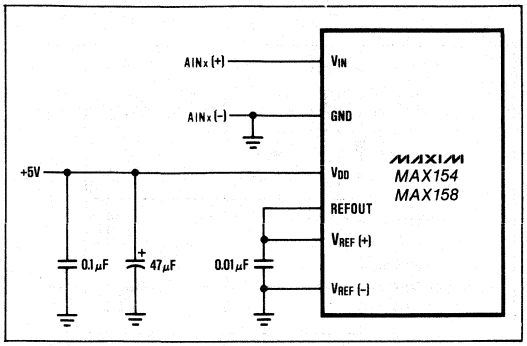


Figure 8a. Internal Reference (MAX154/MAX158 only)

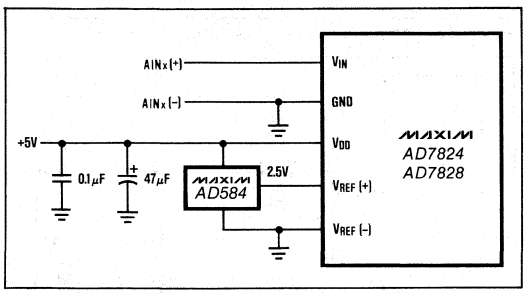


Figure 8b. External Reference +2.5V Full-Scale

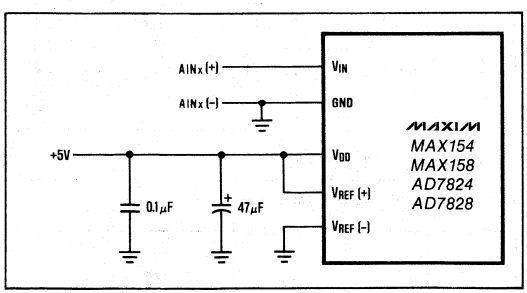


Figure 8c. Power Supply as Reference

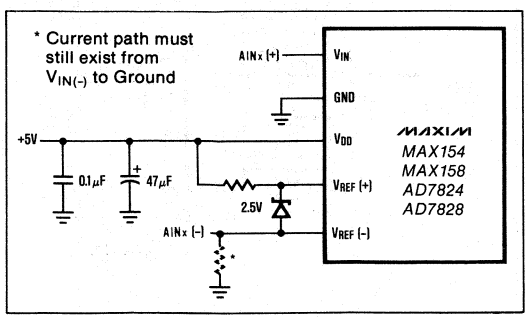


Figure 8d. Inputs Not Referenced to GND

Input Current

The converters' analog inputs behave somewhat differently from conventional ADCs. The sampled data comparators take varying amounts of current from the input depending on the cycle they are in. The equivalent circuit of the converter is shown in Figure 9a. When the conversion starts AIN(n) is connected to the MS and LS comparators. Thus, AIN(n) is connected to thirty-one 1pF capacitors.

To acquire the input signal in approximately 1µs, the input capacitors must charge to the input voltage through the on resistance of the multiplexer (about 600Ω) and the comparator's analog switches (2kΩ to 5kΩ per comparator). In addition, about 12pF of stray capacitance must be charged. The input can be modelled as an equivalent RC network shown in Figure 9b. As R_S (source impedance) increases, the capacitors take longer to charge.

Since the length of the input acquisition time is internally set, large source resistances (greater than 100Ω) will cause settling errors. The output impedance of an op-amp is its open loop output impedance divided by the loop gain at the frequency of interest. It is important that the amplifier driving the converter input have sufficient loop gain at approximately 1MHz to maintain low output impedance.

Input Filtering

The transients in the analog input caused by the sampled data comparators do not degrade the converter's performance since the A/D does not "look" at the input when these transients occur. The comparator's outputs track the input during the first 1µs of the conversion, and are then latched. Therefore, at least 1µs will be provided to charge the ADC's input capacitance. It is not necessary to filter these transients with an external capacitor on the AIN terminals.

Sinusoidal Inputs

The MAX154/MAX158 and AD7824/AD7828 can measure input signals with slew rates as high as 157mV/µs to the rated specifications. This means that the analog input frequency can be as high as 10kHz without the aid of an external track-and-hold. The maximum sampling rate is limited by the conversion time (typical t_{CRD} = 2µs) plus the time required between conversions (t_P = 500ns). It is calculated as:

$$f_{MAX} = \frac{1}{t_{CRD} + t_P} = \frac{1}{(2.0 + 0.5)\ \mu s} = 400kHz$$

f_{MAX} permits a maximum sampling rate of 50kHz per channel when using the MAX158/AD7828 and 100kHz per channel when using the MAX154/AD7824. These rates are well above the Nyquist requirement of 20kHz sampling rate for a 10kHz input bandwidth.

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

Bipolar Input Operation

The circuit in Figure 10a. can be used for bipolar input operation. The input voltage is scaled by an amplifier so that only positive voltages appear at the ADC's inputs. An external reference should be used for the AD7824/AD7828 but is not needed with the MAX154/MAX158. The analog input range is ±4V and the output code is complementary offset binary. The ideal input/output characteristic is shown in Figure 10b.

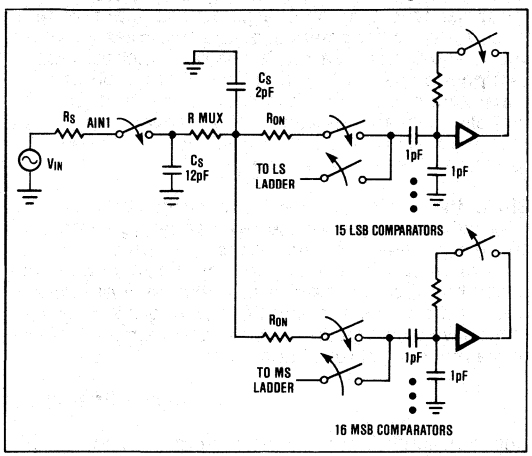


Figure 9a. Equivalent Input Circuit

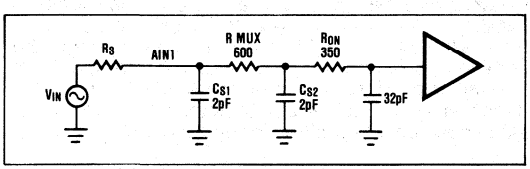


Figure 9b. RC Network Model

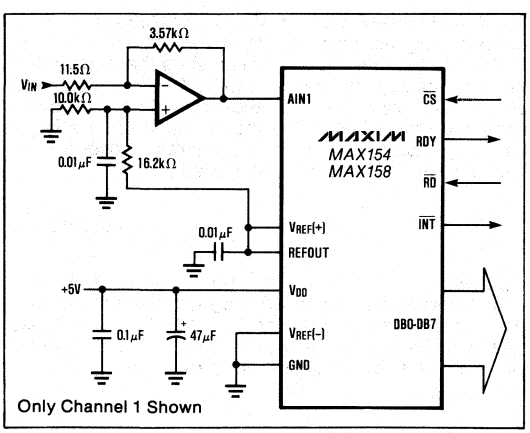


Figure 10a. Bipolar ±4V Input Operation

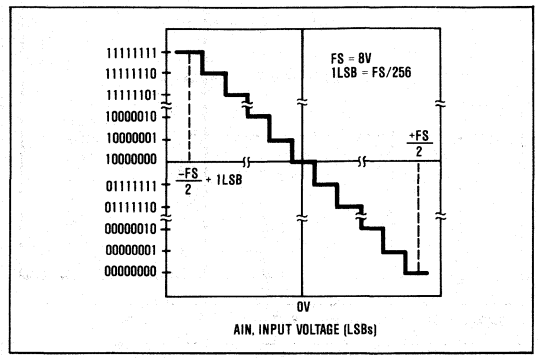


Figure 10b. Transfer Function for ±4V Input Operation

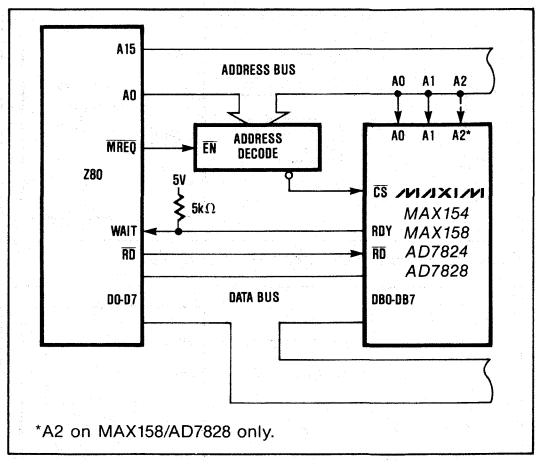


Figure 11. Simple Mode 0 Interface

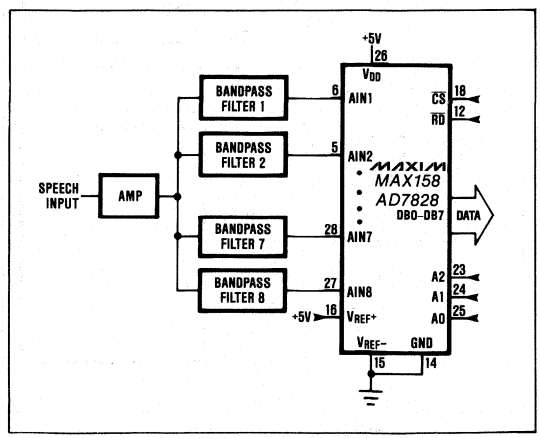


Figure 12. Speech Analysis Using Real Time Filtering

MAXIM

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

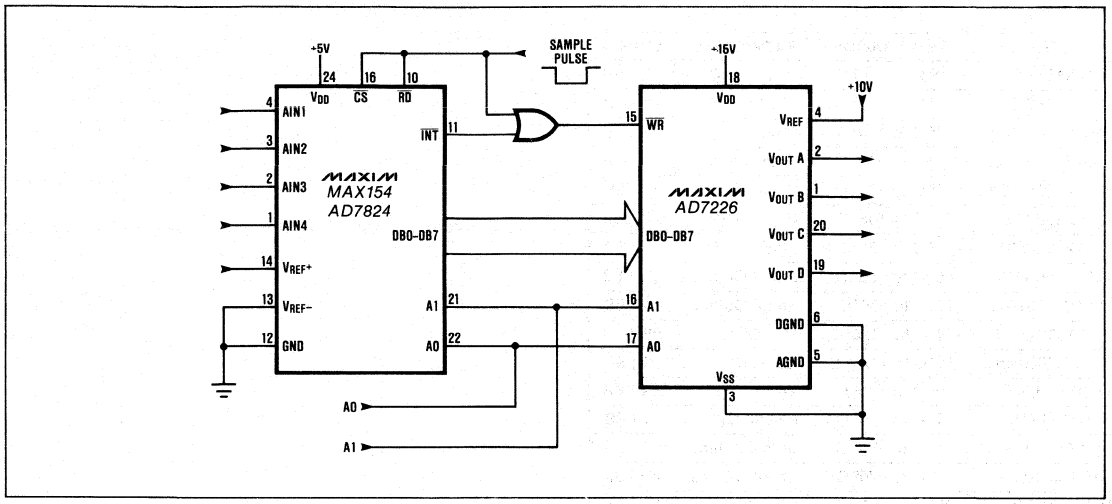
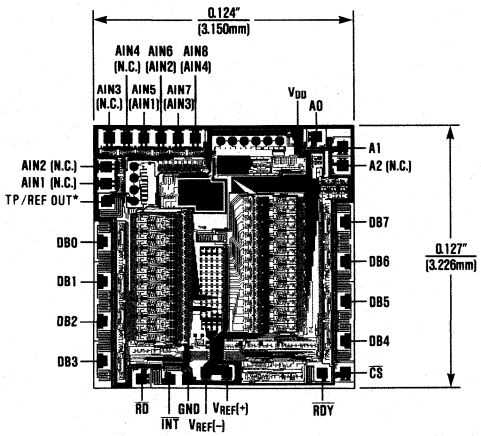


Figure 13. 4-Channel Fast Sample and Infinite Hold

Chip Topography



Note: Connections in parentheses ( ) are for MAX154/AD7824
* REFOUT on MAX154/MAX158 only

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

Ordering Information (continued)

PART	TEMP RANGE	PACKAGE*	ERROR
MAX158ACPI	0° C to +70° C	Plastic DIP	±½ LSB
MAX158BCPI	0° C to +70° C	Plastic DIP	±1 LSB
MAX158BC/D	0° C to +70° C	Dice	±1 LSB
MAX158ACWI	0° C to +70° C	Small Outline	±½ LSB
MAX158BCWI	0° C to +70° C	Small Outline	±1 LSB
MAX158AEPI	-40° C to +85° C	Plastic DIP	±½ LSB
MAX158BEPI	-40° C to +85° C	Plastic DIP	±1 LSB
MAX158AEWI	-40° C to +85° C	Small Outline	±½ LSB
MAX158BEWI	-40° C to +85° C	Small Outline	±1 LSB
MAX158AMJI	-55° C to +125° C	CERDIP	±½ LSB
MAX158BMJI	-55° C to +125° C	CERDIP	±1 LSB
AD7824LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7824KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7824LCWG	0° C to +70° C	Small Outline	±1 LSB
AD7824KCWG	0° C to +70° C	Small Outline	±½ LSB
AD7824CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7824BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7824UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7824TQ	-55° C to +125° C	CERDIP	±1 LSB
AD7828LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7828KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7828LCWI	0° C to +70° C	Small Outline	±1 LSB
AD7828KCWI	0° C to +70° C	Small Outline	±½ LSB
AD7828CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7828BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7828UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7828TQ	-55° C to +125° C	CERDIP	±1 LSB

* *MAX154/AD7824 — 24 lead package, MAX158/AD7828 — 28 lead package*

µP Compatible 8 Bit A/D Converter

General Description

The MAX160 and AD7574 are low cost, microprocessor compatible 8 bit analog-to-digital converters which use the successive-approximation technique to achieve conversion times of 4µs (MAX160) and 15µs (AD7574).

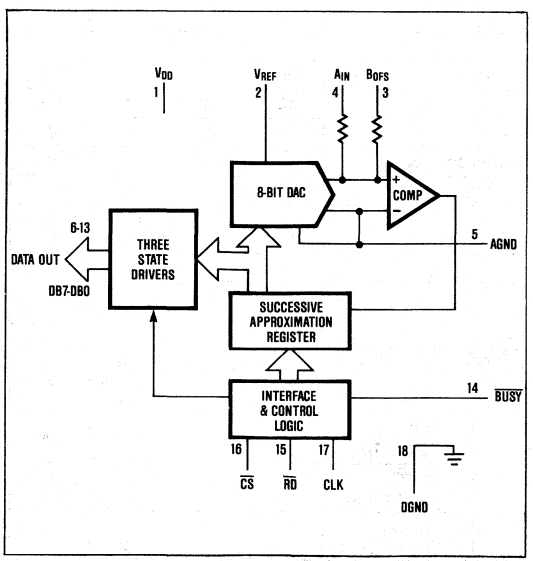
The A/Ds are designed to easily interface with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. Data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port. Operation is simplified by an on-chip clock, +5V power supply requirement, and low supply current (5mA max).

The MAX160 provides major performance improvements over the AD7574 in accuracy and speed specifications as well as compatibility with TTL logic levels.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
Process Automation
Instrumentation
Avionics

Functional Diagram



Features

- Improved Second Source (MAX160)
- Fast Conversion Time: 4µs (MAX160)
  15µs (AD7574)
- No Missing Codes Over Temperature
- Single +5V Supply
- Ratiometric Operation
- No External Clock Necessary
- Easy Interface To Microprocessors

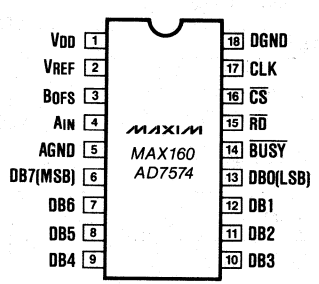
Ordering Information

PART	TEMP. RANGE	PACKAGE†	ERROR
MAX160CPN	0°C to +70°C	Plastic DIP	±½ LSB
MAX160CC/D	0°C to +70°C	Dice*	±½ LSB
MAX160CWN	0°C to +70°C	Small Outline	±½ LSB
MAX160EPN	-40°C to +85°C	Plastic DIP	±½ LSB
MAX160EWN	-40°C to +85°C	Small Outline	±½ LSB
MAX160MJN	-55°C to +125°C	CERDIP**	±½ LSB
AD7574KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7574JN	0°C to +70°C	Plastic DIP	±¾ LSB
AD7574KCWN	0°C to +70°C	Small Outline	±½ LSB
AD7574JCWN	0°C to +70°C	Small Outline	±¾ LSB

† *All devices — 18 lead packages*
* *Consult factory for dice specifications.*
** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP packages.*
Ordering Information continued on last page

Pin Configuration

Top View



μP Compatible 8 Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS — MAX160, AD7574

Supply Voltage, V_{DD} to AGND ..... 0V, +7V
V_{DD} to DGND ..... 0V, +7V
AGND to DGND ..... -0.3V, V_{DD}
Digital Inputs/Outputs (Pins 6-17) .... DGND - 0.3V, V_{DD}+ 0.3V
Analog Inputs (Pins 2-4) ..... -20V, +20V
Power Dissipation (Any Package) to +70°C 670mW
Derate Above +70°C by ..... 8.3mW/°C

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Ranges
MAX160CPN, AD7574JN/KN/JCWN/KCWN ... 0°C to +70°C
AD7574AD/BD/AQ/BQ ..... -25°C to +85°C
MAX160EPN ..... -40°C to +85°C
MAX160MDN/MJN ..... -55°C to +125°C
AD7574SD/TD/SQ/TQ ..... -55°C to +125°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS — MAX160, AD7574

(V_{DD} = +5V, V_{REF} = -10V, Unipolar Configuration, Slow Memory Mode using External Clock f_{CLK} = 2.0MHz for MAX160 and 0.5MHz for AD7574 (Fig. 9), T_A = T_{MIN} to T_{MAX}, unless specified otherwise.)

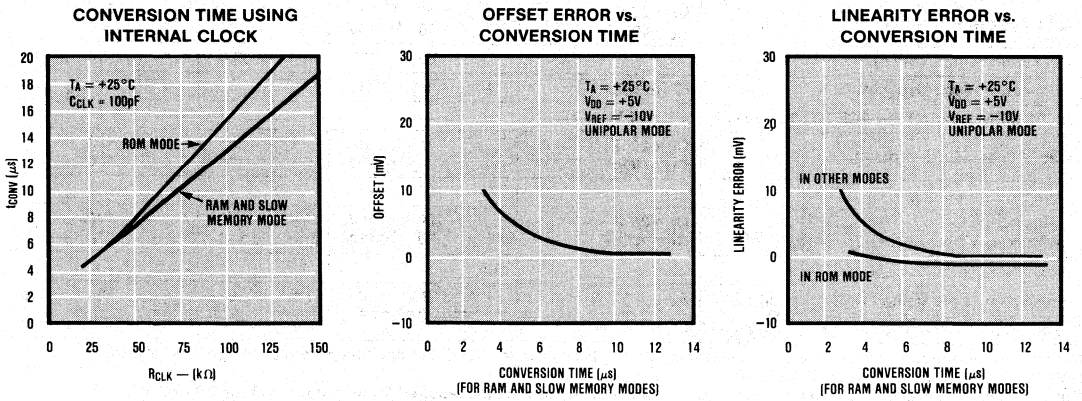
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY (f_{CLK} = 2.0MHz for MAX160 and 0.5MHz for AD7574)						
Resolution			8			bits
Relative Accuracy Error		MAX160, AD7574K/B/T AD7574J/A/S			±½ ±¾	LSB
Differential Non-Linearity		MAX160, AD7574K/B/T AD7574J/A/S			±¾ ±⅞	LSB
Full Scale Error (Note 1) (Gain Error)		MAX160, AD7574K/B/T; T_A = +25°C MAX160, AD7574K/B/T; T_A = T_{MIN} to T_{MAX}			±3 ±4.5	LSB
		AD7574J/A/S; T_A = +25°C AD7574J/A/S; T_A = T_{MIN} to T_{MAX}			±5 ±6.5	
Offset Error (Note 2)		**MAX160; T_A = +25°C MAX160; T_A = T_{MIN} to T_{MAX}**			**±20 ±30**	mV
		AD7574K/B/T; T_A = +25°C AD7574K/B/T; T_A = T_{MIN} to T_{MAX}			±30 ±50	
		AD7574J/A/S; T_A = +25°C AD7574J/A/S; T_A = T_{MIN} to T_{MAX}			±60 ±80	
Mismatch Between B_{OFS} and A_{IN} Resistances (Note 3)					±1.5	%
ANALOG INPUTS						
V_{REF} Input Resistance			5	10	15	kΩ
A_{IN} Input Resistance			10	20	30	kΩ
B_{OFS} Input Resistance			10	20	30	kΩ
Reference Voltage	V_{REF}	±5% for specified transfer accuracy		-10		V
Reference Voltage Range (Note 4)			-5		-15	V
Nominal Analog Input Range		Unipolar Mode Bipolar Mode	0 $-\|V_{REF}\|$		$\|V_{REF}\|$ $+\|V_{REF}\|$	V
LOGIC INPUTS						
Logic Input High Voltage	V_{INH}	MAX160; $\overline{RD}$, $\overline{CS}$ AD7574; $\overline{RD}$, $\overline{CS}$ MAX160, AD7574; CLK	2.4 3.0 3.0			V
Logic Input Low Voltage	V_{INL}	MAX160, AD7574; $\overline{RD}$, $\overline{CS}$ MAX160; CLK AD7574; CLK			0.8 0.8 0.4	V
Logic Input Current	I_{IN}	$\overline{RD}$, $\overline{CS}$, V_{IN} = 0, V_{DD}; T_A = +25°C $\overline{RD}$, $\overline{CS}$, V_{IN} = 0, V_{DD}; T_A = T_{MIN} to T_{MAX}			1 10	μA
Clock Input High Current		V_{IN} = V_{DD}; T_A = +25°C V_{IN} = V_{DD}; T_A = T_{MIN} to T_{MAX}			2 3	mA
Clock Input Low Current		V_{IN} = 0V; T_A = +25°C V_{IN} = 0V; T_A = T_{MIN} to T_{MAX}			1 10	μA
Input Capacitance (Note 5)	C_{IN}	$\overline{RD}$, $\overline{CS}$		5	7	pF

ELECTRICAL CHARACTERISTICS — MAX160, AD7574 (continued)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
LOGIC OUTPUTS							
Logic Output High Voltage	V_{OH}	$\overline{BUSY}$, DB0-DB7 I_{SRC} = 200μA		4.0			V
Logic Output Low Voltage	V_{OL}	$\overline{BUSY}$, DB0-DB7, I_{SINK} = 1.6mA	T_A = +25°C			0.4	V
			T_A = T_{MIN} to T_{MAX} MAX160 AD7574			 0.4 0.8	
Floating State Leakage	I_{LKG}	DB0-DB7, V_{OUT} = 0, V_{DD}	T_A = +25°C T_A = T_{MIN} to T_{MAX}			1 10	μA
Floating State Capacitance (Note 5)		DB0-DB7			5	7	pF
POWER REQUIREMENTS							
Power Supply Requirement	V_{DD}	+5V ±5% for specified performance		4.75		5.25	V
Power Supply Current	I_{DD}	A_{IN} = 0V, ADC in reset condition			1	5	mA
Reference Current	I_{REF}	Conversion complete, before reset				$V_{REF}/5$	V/kΩ

Note 1: Full scale error is measured after correcting for offset error. Max full-scale change from +25°C to T_{MIN} or T_{MAX} is ±1LSB.
Note 2: Maximum offset change from +25°C to T_{MIN} or T_{MAX} is ±10mV. Typical offset temperature coefficient is 50μV/°C.
Note 3: R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive full scale. The effect is an offset and gain term when using the circuit of Figure 9b.
Note 4: Typical value, not guaranteed or subject to test.
Note 5: Guaranteed but not tested.

Typical Operating Characteristics



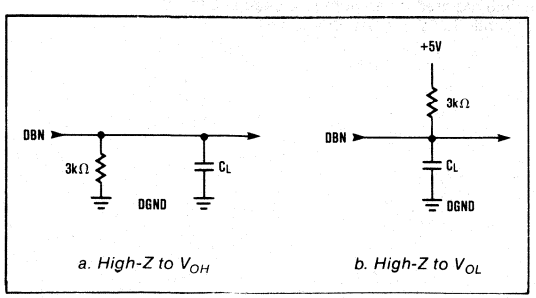


Figure 1. Load Circuits for Data Access Time Test

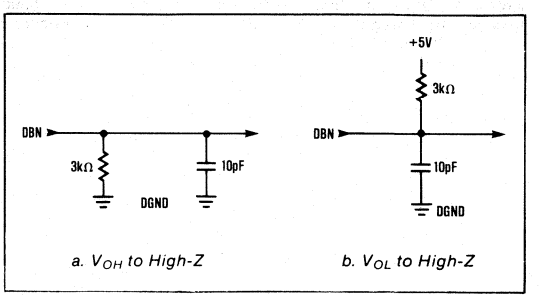


Figure 2. Load Circuits for Data Hold Time Test

µP Compatible 8 Bit A/D Converter

TIMING CHARACTERISTICS (Note 1, 2) — MAX160

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 22kΩ, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN}		T_A = T_{MAX}		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
STATIC RAM INTERFACE MODE (See Figure 5 and Table 5)										
$\overline{CS}$ Pulse Width Requirement	t_{CS}		100			150		150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}		0			0		0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		60 70	100 110		100 110		130 150	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		0			0		0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		0			0		0		ns
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		50 60	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHCS}				250		230		500	ns
Reset Time Requirement	t_{RESET}		1.5			1.5		1.5		µs
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	µs
Internal Clock Temperature Drift				250						ppm/°C
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 2.0MHz	4			4		4		µs
ROM INTERFACE MODE (See Figure 6 and Table 6)										
$\overline{RD}$ HIGH to $\overline{BUSY}$ Delay (Note 2)	t_{WBPD}	C_L = 20pF		800	1200		1200		1200	ns
$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	t_{BSR}	(Note 5)								
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		50 60	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	µs
SLOW MEMORY INTERFACE MODE (See Figure 7 and Table 7)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		0 0	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		60 70	100 110		100 110		130 150	ns
Reset Time Requirement			1.5			1.5		1.5		µs
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	µs
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 2.0MHz	4			4		4		µs

Note 1: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 2: Busy output crosses 0.8V or 2.4V.
Note 3: Outputs are loaded with circuits in Figure 1 and defined as the time required for an output to cross 0.8 or 2.4V.
Note 4: Outputs are loaded with circuits in Figure 2 and defined as the time required for an output to change 0.5V.
Note 5: $\overline{RD}$ can go low prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table 6.

TIMING CHARACTERISTICS (Note 1, 2) — AD7574

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 180kΩ, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN}		T_A = T_{MAX}		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
STATIC RAM INTERFACE MODE (See Figure 5 and Table 5)										
$\overline{CS}$ Pulse Width Requirement	t_{CS}		100			150		150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}		0			0		0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propogation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		50 70	120 150		120 150		180 200	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		0			0		0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		0			0		0		ns
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	AD7574S/T AD7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHCS}				250		200		500	ns
Reset Time Requirement			3			3		3		μs
Conversion Time Using Int CLK	t_{CONV}	See Graph		23						μs
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 500kHz	15			15		15		μs
ROM INTERFACE MODE (See Figure 6 and Table 6)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	AD7574S/T AD7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{RD}$ HIGH to $\overline{BUSY}$ Delay (Note 2)	t_{WBPD}	C_L = 20pF		700	1500		1000		2000	ns
$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	t_{BSR}	(Note 5)								
Conversion Time Using Int CLK	t_{CONV}	See Graph		25						μs
SLOW MEMORY INTERFACE MODE (See Figure 7 and Table 7)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	AD7574S/T AD7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		40 60	120 150		120 150		180 200	ns
Reset Time Requirement			3			3		3		μs
Conversion Time Using Int Clk	t_{CONV}	See Graph		23						μs
Conversion Time Using Ext Clk	t_{CONV}	f_{CLK} = 500kHz	15			15		15		μs

Note 1: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 2: Busy output crosses 0.8V or 2.4V.
Note 3: Outputs are loaded with circuits in Figure 1 and defined as the time required for an output to cross 0.8 or 2.4V.
Note 4: Outputs are loaded with circuits in Figure 2 and defined as the time required for an output to change 0.5V.
Note 5: $\overline{RD}$ can go low prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table 6.

µP Compatible 8 Bit A/D Converter

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power supply voltage, +5V.
2	V_{REF}	Reference Input, nominal -10V.
3	B_{OFS}	Bipolar Offset Input, +10V for bipolar mode, connect to A_{IN} for unipolar mode.
4	A_{IN}	Analog input, 0 to +10V for unipolar mode, -10V to +10V for bipolar mode.
5	AGND	Analog Ground.
6	DB7	Three-state data output, bit 7 (MSB).
7	DB6	Three-state data output, bit 6.
8	DB5	Three-state data output, bit 5.
9	DB4	Three-state data output, bit 4.
10	DB3	Three-state data output, bit 3.

PIN	NAME	FUNCTION
11	DB2	Three-state data output, bit 2.
12	DB1	Three-state data output, bit 1.
13	DB0	Three-state data output, bit 0 (LSB).
14	$\overline{BUSY}$	BUSY output, $\overline{BUSY}$ goes low at the start of a conversion and returns high when the conversion is complete.
15	$\overline{RD}$	READ input, $\overline{RD}$ must be low to access data. See Digital Interface section.
16	$\overline{CS}$	CHIP-SELECT input. Used for conversion control or device addressing. See Digital Interface section.
17	CLK	External clock input/Internal clock frequency set input.
18	DGND	Digital Ground.

Detailed Description

Converter Operation

The MAX160/AD7574 uses the successive approximation technique to convert an unknown analog input to an 8 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only passive clock components, a -10V reference, and a +5V power supply.

Figure 3 shows the MAX160/AD7574 functional diagram. When a start command is received from $\overline{CS}$ or $\overline{RD}$ (see Digital Interface Section), $\overline{BUSY}$ goes low indicating that the conversion is in progress. Successive bits, starting with the most significant bit (MSB), are applied to the input of a DAC. The comparator determines whether the addition of the bit causes the DAC output to be larger or smaller than the analog input, A_{IN}. If the DAC output is greater than A_{IN}, the trial bit is turned OFF, otherwise it is kept ON. Each successively smaller bit is tried and compared to A_{IN} in this manner until the least significant bit (LSB) decision has been made.

When all bits have been tried, $\overline{BUSY}$ goes high, indicating that the conversion is complete and the successive approximation register contains a valid representation of the analog input. The data can then be read using the $\overline{RD}$ input (see Digital Interface Section).

DAC Circuit Details

A thin film R-2R resistor network provides binarily weighted currents for each bit in the internal multiplying DAC (see Figure 4). N-channel MOS switches are used to steer current to either the summing junction or AGND depending on the DAC digital code. The A_{IN} and B_{OFS} input resistors also use series MOS switches (always ON) that match the DAC switches to maintain gain temperature tracking.

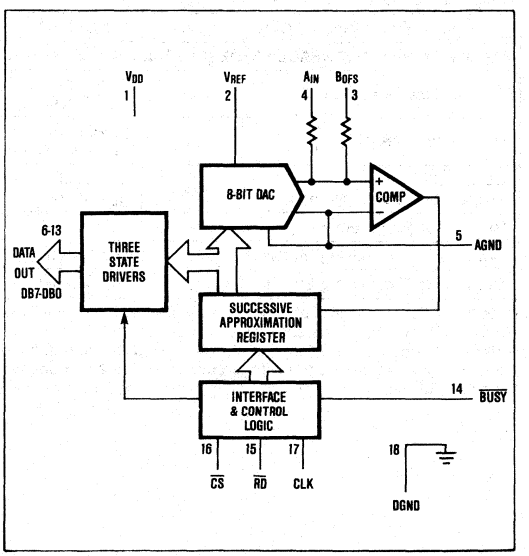


Figure 3. MAX160/AD7574 Functional Diagram

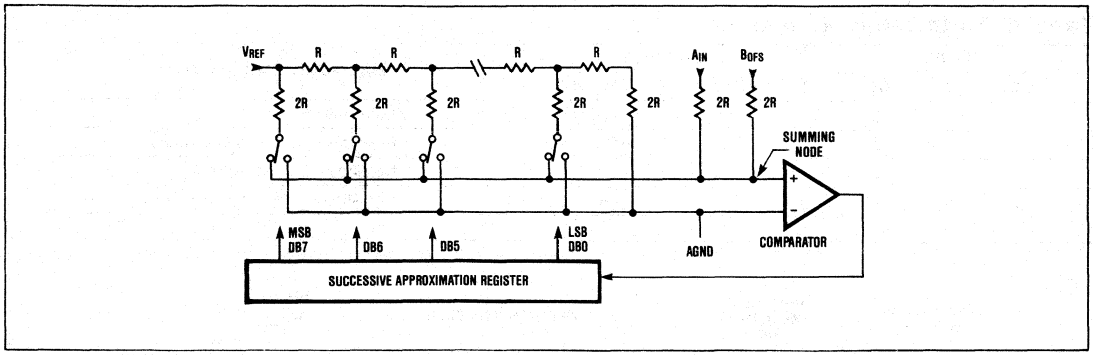


Figure 4. D/A Converter Used in the MAX160/AD7574

Table 5. Truth Table, Static Ram Mode

INPUTS		OUTPUTS		MAX160/AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
L	H	H	HI-Z	Write Cycle (Start Convert)
L	↓	H	HI-Z to DATA	Read Cycle (Data Read)
L	↑	H	DATA to HI-Z	Reset Converter
H	X (Note 1)	X	HI-Z	Not Selected
L	H	L	HI-Z	No Effect (Converter Busy)
L	↓	L	HI-Z	No Effect (Converter Busy)
L	↑	L	HI-Z	Not Allowed, Conversion Error

Note 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the state of $\overline{CS}$ or $\overline{BUSY}$.

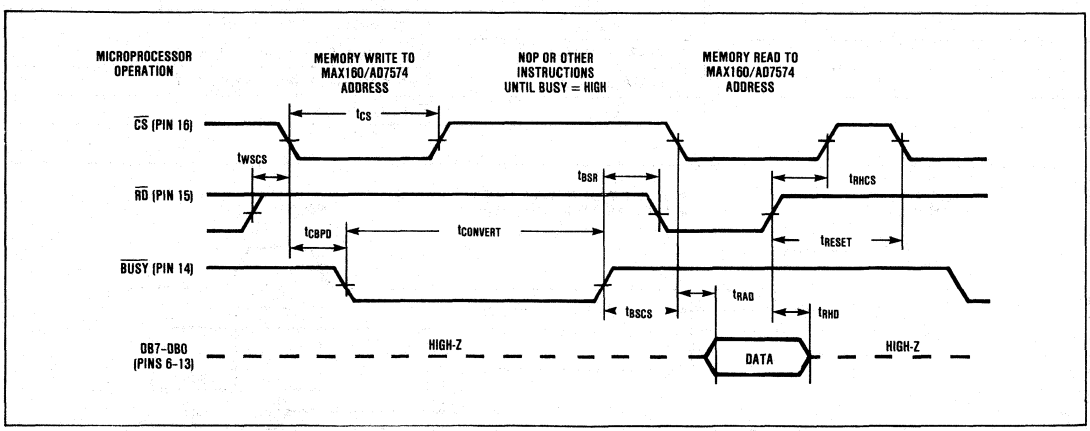


Figure 5. Static RAM Mode Timing Diagram

μP Compatible 8 Bit A/D Converter

Table 6. Truth Table, Rom Mode

INPUTS		OUTPUTS		MAX160/AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
L	⌐	H	HI-Z to DATA	Data Read
L	⌐	⌐	DATA to HI-Z	Reset and Start New Conversion
L	⌐	L	HI-Z	No Effect (Converter Busy)
L	⌐	L	HI-Z	Not Allowed, Conversion Error

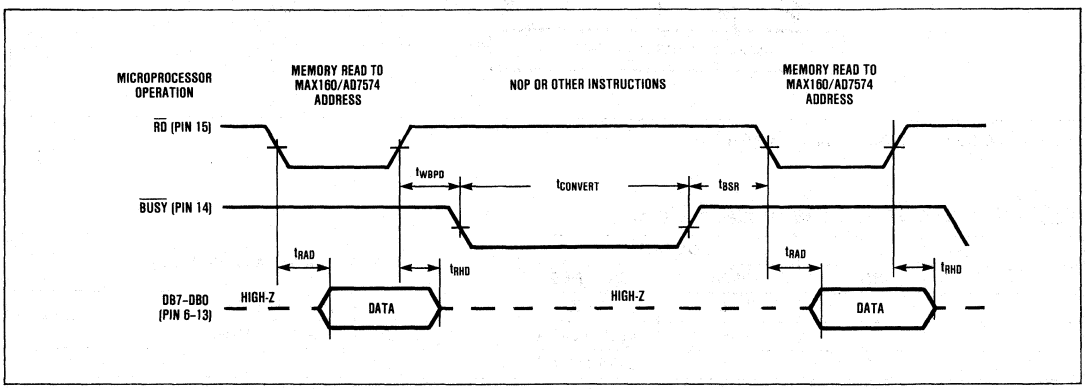


Figure 6. ROM Mode Timing Diagram ($\overline{CS}$ Held Low)

Table 7. Truth Table, Slow Memory Mode

INPUTS	OUTPUTS		MAX160/AD7574 OPERATION
$\overline{CS}$ & $\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
H	H	HI-Z	Not Selected
⌐	H → L	HI-Z	Start Conversion
L	L	HI-Z	Conversion in Progress. μP in WAIT State
L	⌐	HI-Z to DATA	Conversion Complete. μP READS Data
⌐	H	DATA to HI-Z	Converter Reset and Deselected
H	H	HI-Z	Not Selected

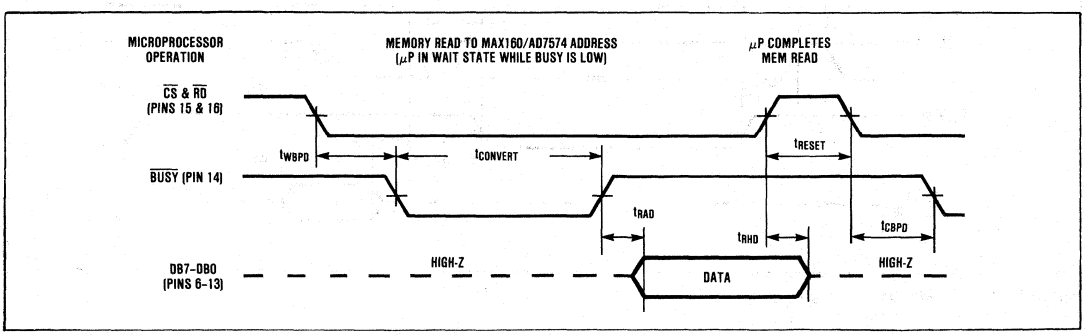


Figure 7. Slow Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)

Digital Interface

The MAX160/AD7574 has three interface modes which are determined by the timing of the CS and RD inputs.

Static RAM Interface Mode

Table 5 and Figure 5 show the truth table and timing requirements for interfacing the MAX160/AD7574 as a static RAM.

A conversion is started by executing a memory WRITE instruction to the MAX160/AD7574 address. Once a conversion is in progress, subsequent WRITE operations have no effect. Data is read by executing a memory READ operation to the A/D's address.

$\overline{BUSY}$ must be high before a READ is attempted. In other words, the elapsed time between WRITE and READ must be greater than the conversion time. Once $\overline{BUSY}$ is HIGH (end of conversion) the data READ can be performed. The data readout is destructive, since the MAX160/AD7574 is internally reset when $\overline{RD}$ goes high. Note that $\overline{CS}$ remaining LOW longer than the hold time (t_{RHCS}) will initiate a new conversion.

ROM Interface Mode

Table 6 and Figure 6 show the truth table and timing requirements for interfacing the MAX160/AD7574 as Read Only Memory.

In this mode the $\overline{CS}$ input is not used and is held low. The $\overline{RD}$ input is derived from the decoded device address. A data READ is initiated by executing a memory READ instruction to the MAX160/AD7574 address location. A conversion automatically starts when $\overline{RD}$ returns HIGH. Similar to the RAM mode, attempting a READ before $\overline{BUSY}$ goes HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is poorly defined in time since the conversion is performed at the end of a previous READ operation. This problem can be overcome by performing two READ operations back to back and only using the data from the second read.

Slow-Memory Interface Mode

Table 7 and Figure 7 show the truth table and timing requirements for interfacing the MAX160/AD7574 as slow memory. This mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX160/AD7574 conversion time.

In this mode $\overline{CS}$ and $\overline{RD}$ are tied together. The decoded device address is used to drive $\overline{CS}/\overline{RD}$. The $\overline{BUSY}$ output is connected to the processor's READY input. A conversion is initiated by executing a memory READ to the MAX160/AD7574 address. $\overline{BUSY}$ then goes LOW and forces the processor into a WAIT state. At the end of the conversion, $\overline{BUSY}$ returns high and the data is available at the data outputs.

The major advantage of the slow memory mode is that it allows the processor to start and end a conversion and read the result with a single READ instruction.

Do not attempt a memory WRITE in this mode, since a three-state bus conflict will arise.

Interface Application Hints

Timing and Control

Failure to observe the timing restrictions of Figures 5-7 may cause the MAX160/AD7574 to change interface modes. For example, in the RAM mode, if $\overline{CS}$ is held low for too long, the converter moves into the ROM mode since a new conversion starts.

Logic Deglitching in μP Applications

Unspecified states in the address bus can cause glitches at the MAX160/AD7574 $\overline{CS}$ or $\overline{RD}$ inputs. Such glitches can cause undesired conversion starts, resets or data reads. The best method for avoiding these problems is to gate the address decode with $\overline{WR}$ or $\overline{RD}$ when in the RAM or ROM modes. In the slow memory mode use latched address inputs.

Initialization After Power-Up

To initialize the MAX160/AD7574 at power-up, perform a memory READ to its address location and ignore the data.

Clock

Internal Oscillator

The MAX160/AD7574 has in internal asynchronous clock oscillator which starts when a convert command is received and stops at the end of a conversion.

The oscillator requires an external resistor and capacitor connected as shown in Figure 8. The internal oscillator has good initial accuracy and stability over temperature and supply voltage. See Typical Operating Characteristics for typical conversion times versus R_{CLK} with C_{CLK} set at 100pF.

To prevent false triggering of the internal clock, R_{CLK} and C_{CLK} must be placed close to the CLK pin and coupling from the $\overline{CS}$ and $\overline{RD}$ inputs must be minimized.

µP Compatible 8 Bit A/D Converter

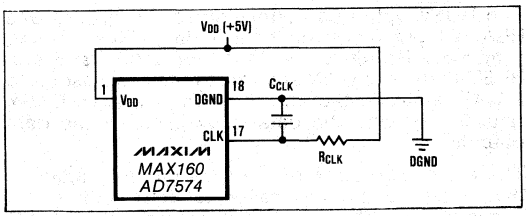


Figure 8. Connecting R_{CLK} and CLK to CLK Oscillator

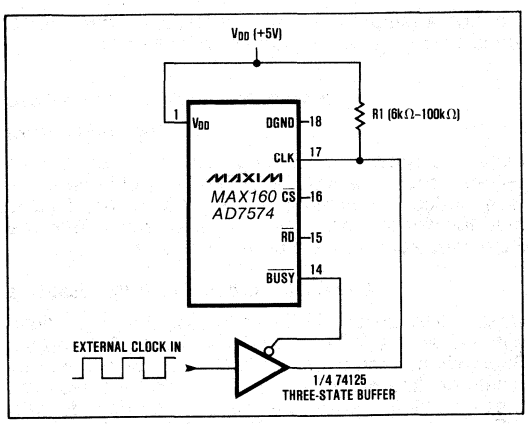


Figure 9. External Clock Operation (Static RAM and Slow Memory Mode)

Operation With External Clock

For applications where synchronous operation is required or the conversion time must be accurately controlled, an external clock can be used.

Figure 9 shows how an external clock is connected. The BUSY output is connected to the three-state enable input of a 74125 buffer. A 500kHz clock provides a conversion time of 15µs.

The external clock should be used only in the static-RAM or slow-memory modes and *not* in the ROM mode. Timing constraints for the external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go low on a positive clock edge to provide optimum settling time for the MSB.

2. A data READ can be performed at any time after BUSY = HIGH.

SLOW MEMORY MODE

1. When starting a conversion, $\overline{CS}$ and $\overline{RD}$ should go low on a positive clock edge to provide optimum settling time for the MSB.

Analog Considerations

Application Hints

Input Loading at V_{REF}, A_{IN}, and B_{OFS}

To prevent input loading effects due to the finite input resistance of these pins, low impedance driving sources must be used (i.e. op-amp buffers, or low output impedance references).

Ratiometric Operation

Ratiometric operation is inherent for the multiplying DAC scheme used on the MAX160/AD7574. However, the user must recognize that comparator limitations such as offset voltage, input noise and gain degrade the transfer function at reference voltages less than -10V.

Offset Correction

Offset error in the transfer function can be trimmed by offsetting the buffer that drives the A_{IN} input. This can be achieved either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between V_{DD} and V_{REF} and applying the tap voltage to the amplifier's non-inverting input. An example of the latter method can be seen in Figure 12.

Analog and Digital Ground

It is recommended that the AGND and DGND pins be connected locally to prevent noise injection into the A/D converter. In systems where the AGND-DGND connection is not local, clamp diodes should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other.

Unipolar Binary Operation

Figures 10 shows the analog circuit connections and nominal transfer characteristic for unipolar operation. Calibration is as follows:

Offset

If offset trimming is required, it must be done in the signal conditioning circuitry used to drive the A_{IN} input in Figure 10. See also the offset trim example shown in Figure 12.

1. Apply -39.1mV (1 LSB) to the input of the buffer amplifier used to drive R1 (i.e. +39.1 mV at R1).

2. Adjust the offset potentiometer until DB7-DB1 are LOW and DB0 flickers.

Gain (Full Scale)

Offset adjustment must be performed prior to gain adjustment. To trim gain:

1. Apply -9.961V to the input of the buffer that drives R1 (i.e. +9.961V at R1).

2. Adjust trimpot R2 until DB7-DB1 are HIGH and DB0 flickers.

Bipolar (Offset Binary) Operation

Figure 11 illustrates the analog circuitry and transfer function for bipolar operation. The output coding is offset binary. Offset correction can be performed at the buffer amplifier used to drive the signal input terminals of the MAX160/AD7574. See Figure 12 for an example of how offset trimming can be performed. Calibration is as follows:

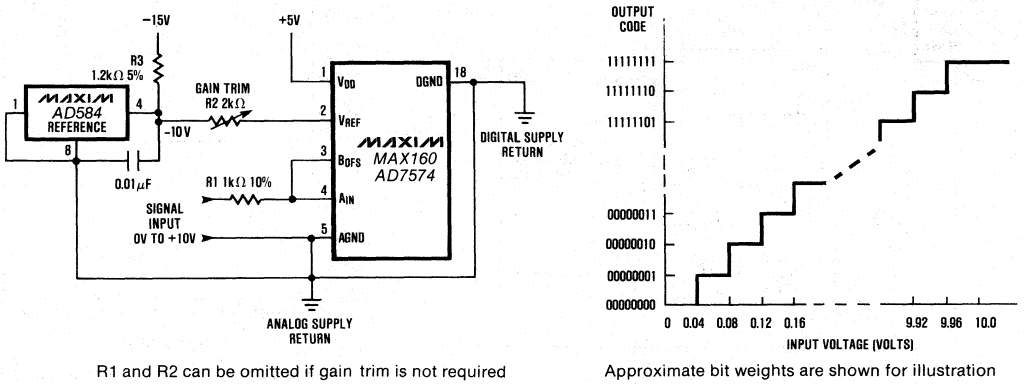
1. Adjust R6 and R7 for minimum resistance across the potentiometers.

2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at R6). Then trim R6 or R7 (whichever is required) until DB7-DB1 are LOW and DB0 flickers.

3. Apply 0V to the buffer amplifier used to drive the signal input terminals. Then trim the offset circuit of the buffer amplifier until the ADC output flickers between 01111111 and 10000000.

4. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to R6). Then trim R2 until DB7-DB1 are LOW and DB0 flickers.

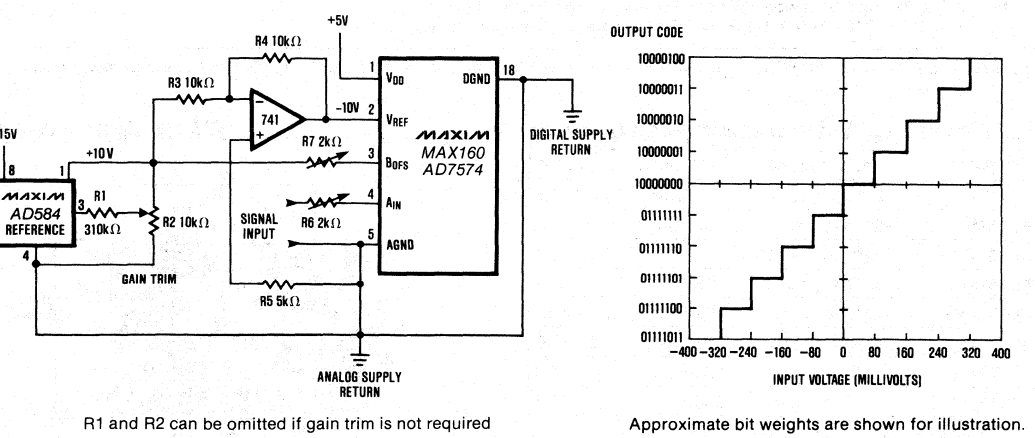
5. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of R6). If the ADC output code is not 11111110 ± 1 bit, repeat the calibration procedure.



R1 and R2 can be omitted if gain trim is not required

Approximate bit weights are shown for illustration

Figure 10. Unipolar (0V to +10V) Operation and Nominal Transfer Characteristic (Output Code is Straight Binary)



R1 and R2 can be omitted if gain trim is not required

Approximate bit weights are shown for illustration.

Figure 11. Bipolar (-10V to +10V) Operation and Nominal Transfer Characteristic Around Major Carry (Output Code is Offset Binary)

μP Compatible 8 Bit A/D Converter

Bipolar (Complementary Offset Binary) Operation

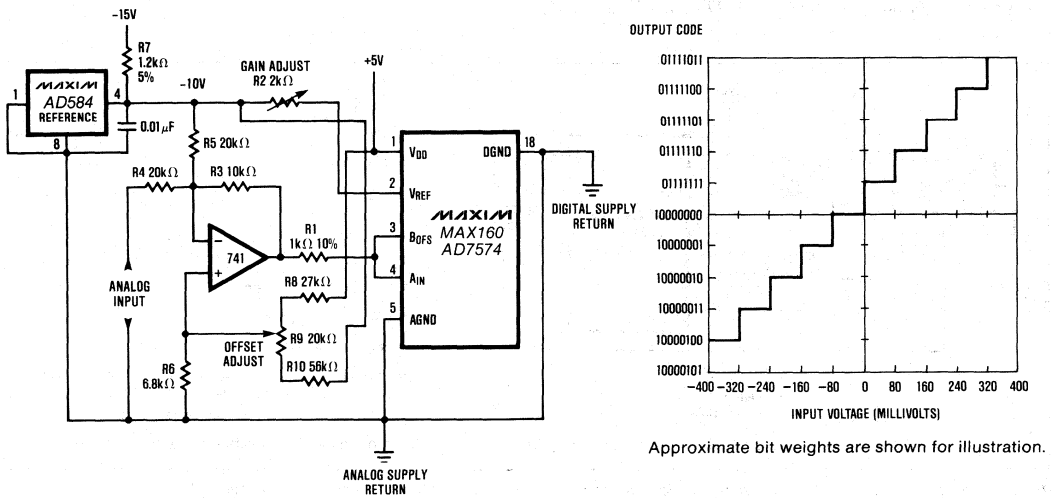
Figure 12 shows the analog connections for offset binary operation. The typical transfer characteristic is also shown. In this bipolar mode, the input signal (-10 to +10V) is conditioned and the A/D basically operates in unipolar mode (0 to +10V). Calibration is as follows (offset adjusted before gain):

Offset

1. Apply 0V to the analog input shown in Figure 12.
2. Adjust R9 until the converter output flickers between codes 01111111 and 10000000.

Gain (Full Scale)

1. Apply -9.922V across the analog input terminals shown in Figure 12.
2. Adjust R2 until DB7-DB1 are HIGH and DB0 flickers between HIGH and LOW.



Approximate bit weights are shown for illustration.

Note 1: R1 and R2 can be omitted if gain trim is not required.
Note 2: R8, R9 and R10 can be omitted if offset trim is not required.
Note 3: R6||R8||R10 = 5kΩ. If R8, R9 and R10 are not used, make R_6 = 5kΩ.

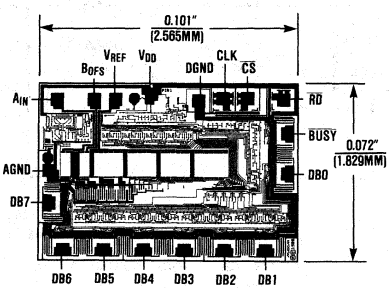
Figure 12. Bipolar (-10V to +10V) Operation and Nominal Transfer Characteristic Around Major Carry (Output Code is Complimentary Offset Binary)

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE†	ERROR
AD7574AQ	-25°C to +85°C	CERDIP**	±¾ LSB
AD7574BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7574SQ	-55°C to +125°C	CERDIP**	±¾ LSB
AD7574TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7574AD	-25°C to +85°C	Ceramic	±¾ LSB
AD7574BD	-25°C to +85°C	Ceramic	±½ LSB
AD7574SD	-55°C to +125°C	Ceramic	±¾ LSB
AD7574TD	-55°C to +125°C	Ceramic	±½ LSB

† *All devices — 18 lead packages*
** Maxim reserves the right to ship Ceramic Packages in lieu of *CERDIP packages.*

Chip Topography



MAXIM

CMOS 8-Bit 8-Channel Data Acquisition System

General Description

The MAX161 and AD7581 are CMOS single-chip 8-bit, 8-channel data acquisition systems (DAS). Each chip includes an 8-bit A/D converter, 8-channel multiplexer, 8 x 8 dual port RAM with contention logic, and microprocessor compatible I/O logic. When combined with a voltage reference, a complete data acquisition system is produced that interfaces with the majority of microprocessors.

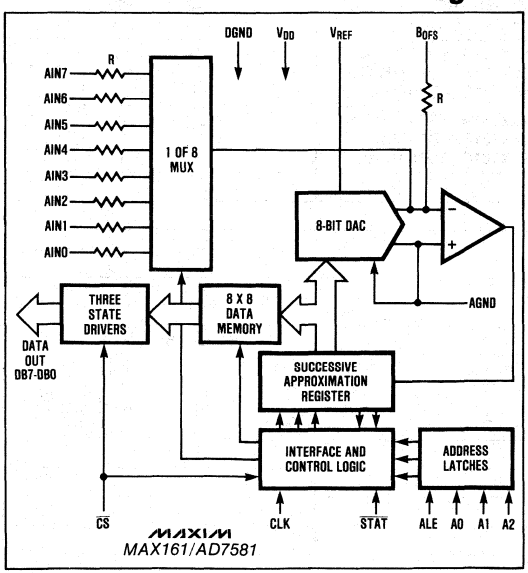
Conversions take place on a continuous, channel sequencing basis using a microprocessor clock or control signal. Data is stored automatically in dual port RAM so that any channel can be read at any time under microprocessor control.

The MAX161 is an enhanced, pin-compatible version of the AD7581. Improvements include faster conversion and interface timing, lower zero error and drift, reduced power dissipation, and availability in military temperature grades. All devices are available in 28 pin DIP and Small Outline (SO) packages.

Applications

Digital Signal Processing
Data Loggers
Automatic Test Equipment
Robotics
Process Control

Functional Diagram



Features

- ◆ Fast Conversion Time: 20μsec (MAX161)
- ◆ No Missing Codes Over Temperature
- ◆ On Chip 8 x 8 Dual Port RAM
- ◆ Interfaces Directly To Z80/8085/6800
- ◆ Ratiometric Capability
- ◆ Interleaved DMA Operation

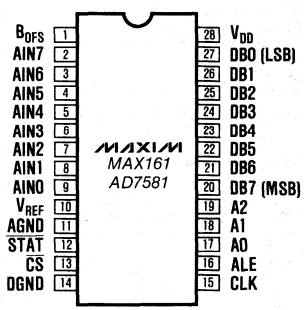
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX161ACPI	0° C to +70° C	Plastic DIP	1 7/8 LSB
MAX161BCPI	0° C to +70° C	Plastic DIP	3/4 LSB
MAX161CCPI	0° C to +70° C	Plastic DIP	1/2 LSB
MAX161ACWI	0° C to +70° C	Small Outline	1 7/8 LSB
MAX161BCWI	0° C to +70° C	Small Outline	3/4 LSB
MAX161CCWI	0° C to +70° C	Small Outline	1/2 LSB
MAX161CC/D	0° C to +70° C	Dice	1 7/8 LSB
MAX161AEPI	-40° C to +85° C	Plastic DIP	1 7/8 LSB
MAX161BEPI	-40° C to +85° C	Plastic DIP	3/4 LSB
MAX161CEPI	-40° C to +85° C	Plastic DIP	1/2 LSB
MAX161AEWI	-40° C to +85° C	Small Outline	1 7/8 LSB
MAX161BEWI	-40° C to +85° C	Small Outline	3/4 LSB
MAX161CEWI	-40° C to +85° C	Small Outline	1/2 LSB
MAX161AMJI	-55° C to +125° C	CERDIP**	1 7/8 LSB
MAX161BMJI	-55° C to +125° C	CERDIP**	3/4 LSB
MAX161CMJI	-55° C to +125° C	CERDIP**	1/2 LSB

* *All devices — 28 lead packages*
** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages.*
Ordering Information continued on last page.

Pin Configuration

Top View



CMOS 8-Bit 8-Channel Data Acquisition System

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... +7V
V_{DD} to DGND ..... +7V
AGND to DGND ..... -0.3V, V_{DD}
Digital Input Voltage to DGND
(pins 13,16-19) ..... -0.3V, V_{DD}
Digital Output Voltage to DGND
(pins 12,20-27) ..... -0.3V, V_{DD}
CLK (pin 15) input voltage to DGND ..... -0.3V, V_{DD}
V_{REF} (pin 10) to AGND ..... ±25V
V_{BOFS} (pin 1) to AGND ..... ±17V
AIN (0-7) (pins 9-2) ..... ±17V

Operating Temperature Range
MAX161XC, AD7581J/K/L ..... 0°C to +70°C
AD7581A/B/C ..... -25°C to +85°C
MAX161XE ..... -40°C to +85°C
MAX161XM, AD7581S/T/U ..... -55°C TO +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Package)
Plastic DIP (Derate 12mW/°C above +50°C) 1200mW
Ceramic (Derate 10mW/°C above +50°C) 1000mW
CERDIP (Derate 10mW/°C above +50°C) 1000mW
Small Outline (Derate 12mW/°C above +50°C) 1000mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = -10V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
ACCURACY (at f_{CLK} = 4.0MHz for MAX161, 1.2MHz for AD7581)							
Resolution				8			Bits
Relative Accuracy		MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U			±¾ ±½ ±¼	±1⅞ ±¾ ±½	LSB
Differential Nonlinearity		MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U			±¾ ±½ ±¼	±1⅞ ±⅞ ±¾	LSB
Offset Error (See Figure 5, Note 1)		**Adjustable to zero**	**MAX161A** **MAX161B** **MAX161C**		**±60** **±40** **±20**	**±120** **±60** **±40**	mV
			AD7581J/A/S AD7581K/B/T AD7581L/C/U		±60 ±40 ±20	±200 ±80 ±50	
Gain Error, Worst Channel (See Figure 5, Note 2)		Adjustable to zero	MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U		±3 ±2 ±1	±6 ±4 ±2	LSB
Gain Match Between Channels (See Figure 5)		Adjustable to zero	MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U		2 1 ½	3 2 1	LSB
B_{OFS} Gain Error (Note 3)					±1		LSB
ANALOG INPUTS							
Input Resistance at V_{REF}, B_{OFS}, and AIN7-AIN0	R_{IN}	Pins 1 to 10 (Note 4)		10	20	30	kΩ
V_{REF} (For Specified Performance)	V_{REF}			-10.5		-9.5	V
V_{REF} Range				-5V to -15V			V
Nominal Analog Input Range		+Unipolar Mode (See Figure 5) -Unipolar Mode (See Figure 7) Bipolar Mode (See Figure 9)		0 $-V_{REF}$ $-V_{BOFS}$		+V_{REF} 0 $\lvert V_{REF}\rvert$ - V_{BOFS}	V
DIGITAL INPUTS ($\overline{CS}$, ALE, CLK, A0-A2)							
Logic HIGH Threshold	V_{INH}			+2.4	+2.0		V
Logic LOW Threshold	V_{INL}				+1.2	+0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			0.01	1	μA
Input Capacitance	C_{IN}	(Note 5)			4	5	pF

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{REF} = -10V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DIGITAL OUTPUTS ($\overline{STAT}$, DB0-DB7)						
Output HIGH Voltage	V_{OH}	I_{SOURCE} = 40µA	4.5	4.8		V
Output LOW Voltage	V_{OL}	I_{SINK} = 1.6mA		0.2	0.6	V
Floating State Leakage	I_{LKG}	DB0-DB7		0.3	10	µA
Floating State Capacitance		DB0-DB7, V_{OUT} = 0V to V_{DD}		5	10	pF
Output Code		See Figure 5 See Figure 7 See Figure 9	Unipolar Binary Complementary Binary Offset Binary			
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		+4.5	+5.0	+5.5	V
Supply Current	I_{DD}	MAX161, AD7581 Static		3	5	mA
		MAX161 Dynamic (f_{CLK} = 4.0MHz)		**3**	**5**	
		AD7581 Dynamic (f_{CLK} = 1.2MHz)		3	8	

Note 1. Typical offset temperature coefficient is **±25µV/°C for the MAX161** and ±150µV/°C for the AD7581.
Note 2. Gain error is measured after offset calibration. Maximum full scale change for any channel from +25°C to T_{MIN} or T_{MAX} is ±2LSBs.
Note 3. Typical change in B_{OFS} gain from +25°C to T_{MIN} or T_{MAX} is ±2LSBs.
Note 4. R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 7 and 9.
Note 5. Guaranteed but not 100% tested.

TIMING CHARACTERISTICS — MAX161 (C_L = 100pF, See Figure 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
ALE Pulse Width	t_H	**50**	**35**		**ns**
Address Valid to Latch Set-Up Time	t_{ALS}	**45**	**30**		**ns**
Address Valid to Latch Hold Time	t_{ALH}	**10**	**0**		**ns**
Address Latch to $\overline{CS}$ Set-Up Time	t_{LCS}	**10**	**0**		**ns**
$\overline{CS}$ to Output Propagation Delay	t_{ACC}		**125**	**200**	**ns**
$\overline{CS}$ Pulse Width	t_{CW}	**250**	**175**		**ns**
$\overline{CS}$ to Output Float Propagation Delay	t_{CF}		**30**	**50**	**ns**
$\overline{CS}$ to Low Impedance Bus	t_{CLZ}		**70**	**100**	**ns**
Clock Frequency (Note 6)	f_{CLK}		**6**	**4.0**	**MHz**

TIMING CHARACTERISTICS — AD7581 (C_L = 100pF, See Figure 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
ALE Pulse Width	t_H	80	50		ns
Address Valid to Latch Set-Up Time	t_{ALS}	70	45		ns
Address Valid to Latch Hold Time	t_{ALH}	20	10		ns
Address Latch to $\overline{CS}$ Set-Up Time	t_{LCS}	20	10		ns
$\overline{CS}$ to Output Propagation Delay	t_{ACC}		200	250	ns
$\overline{CS}$ Pulse Width	t_{CW}	280	250		ns
$\overline{CS}$ to Output Float Propagation Delay	t_{CF}		50	80	ns
$\overline{CS}$ to Low Impedance Bus	t_{CLZ}		100	150	ns
Clock Frequency (Note 6)	f_{CLK}		1.6	1.2	MHz

Note 6. Guaranteed conversion time for stated accuracy of 20µs/channel with 4.0MHz clock for MAX161, and 66.7µs/channel with 1.2MHz clock for the AD7581.

CMOS 8-Bit 8-Channel Data Acquisition System

Detailed Description

Basic Operation

The MAX161 and AD7581 sequentially convert analog signals on 8 input channels into separate 8-bit data words. The data is continually updated in on-chip RAM, with each channel's conversion result assigned to a separate RAM address. Consequently, the conversion process is user transparent in that output data is read directly from RAM. The device can run directly from a microprocessor clock (6800 type systems) or control signal (ALE in 8085 type systems). A functional diagram of the MAX161 and AD7581 is shown on the front page.

A/D Conversion

Internally, the conversion process is divided into 10 phases, each 8 clock periods long. In the first phase, the input multiplexer is decremented and the control logic is reset. STAT (pin 12) goes low for 8 clock cycles at the beginning of this period. (STAT also goes low for 72 clock periods after channel 1 is converted). The successive approximation A/D conversion then takes place during phases 2 through 9. Finally, data is loaded into RAM during phase 10.

A single channel conversion takes 80 input clock periods while a complete scan through all channels requires 640 clock periods. Internal start-up logic initializes the converter within 800 clock periods after power is applied.

Digital Interface

Channel Selection

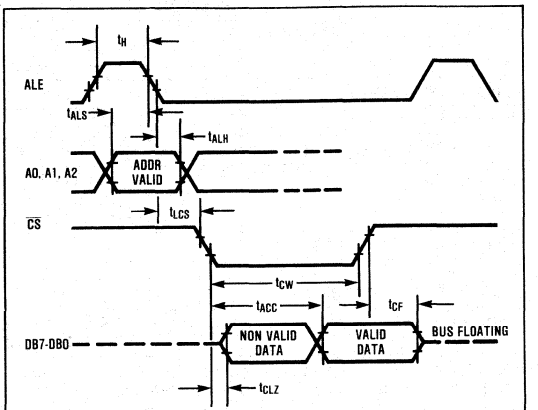
Table 1 shows the truth table for channel selection. RAM locations are addressed by AO-A2. In systems with a multiplexed address/data bus, the address is latched by ALE (pin 16). Alternatively, when address and data busses are separate, the address latches can be made transparent by tying ALE HIGH.

Table 1:
Channel Selection Truth Table

A2	A1	A0	ALE	CHANNEL DATA TO BE READ
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Timing And Control

Control timing for the MAX161 and AD7581 is shown in Figure 1. When CS (pin 13) is HIGH, the three-state data drivers are in their high impedance state. The drivers switch to the active state when CS goes LOW. Output data is valid after time t_{ACC}.



SWITCHING TERMINOLOGY

t_H: ALE pulse width requirement.
t_{ALH}: Address Valid to latch hold time.
t_{ALS}: Address Valid to latch set-up time.
t_{LCS}: Address latch to Chip Select set-up time.
t_{CW}: Chip Select pulse width requirement.
t_{ACC}: Chip Select to valid data propagation delay.
t_{CF}: Chip Select to output data float propagation delay.
t_{CLZ}: Chip Select to low impedance data bus.

Figure 1. Interface Timing Diagram

Data Read Operation

The MAX161 and AD7581 continuously scan and convert analog input signals without regard to the channel being selected for data output. The on-chip RAM and contention logic allow data to be read asynchronously with respect to the conversion process. The output data (RAM contents) is simply the most recent conversion result for the selected channel.

Automatic Interleaved DMA is provided by internal logic to ensure that memory updates do not take place when the memory is being addressed by a microprocessor. RAM is normally updated on a rising clock edge, 6 clock periods prior to STAT going LOW, provided CS is HIGH (i.e. data is not being read). If CS is LOW (read operation in progress), then the memory update is delayed by 3 clock periods. By delaying the update, data will not be written in RAM during a READ as long as CS is kept shorter than 3 clock periods. The possibility of a "contention" error with an asynchronous READ is therefore eliminated if CS is less than 3 clock periods long. Although asynchronous reading errors are eliminiated with this feature, it in no way restricts compatibility with other manufacturers' AD7581s.

Channel Identification

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To do this, the channel that is currently converting must be identified. $\overline{STAT}$ provides an identifying signal by staying low for an extended time (72 vs. 8 clock periods) when channel 0 is active (see Figure 2). Note that input channels are scanned in reverse order, i.e. AIN7,6...1,0.

A simple circuit for channel identification using $\overline{STAT}$ is shown in Figure 3. The time constant, RC, is chosen such that X2 ignores the short $\overline{STAT}$ pulses but responds to the wider (72 clock periods) pulse width occuring during channel 0 conversion. With a 1μs clock period, use 0.022μF for C and 1.8kΩ for R. An alternate means of channel identification uses the microprocessor to periodically interrogate the $\overline{STAT}$ output. A simple routine is shown in Figure 4.

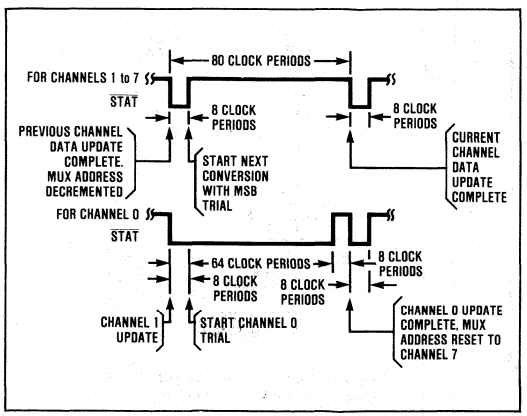


Figure 2. $\overline{STAT}$ Timing Diagram

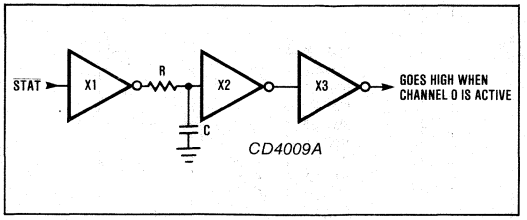


Figure 3. Hardware Channel Identification

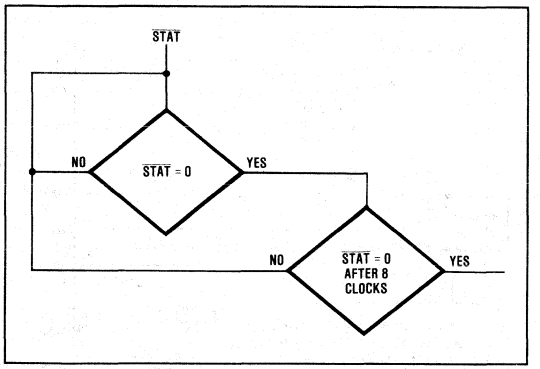


Figure 4. Software Channel Identification

Operating Circuits

For the following circuits, the offset and gain adjustments shown in Figures 5, 7 and 9 are often not needed (The offset and gain error of the MAX161C are 1LSB and 2LSB respectively). In those cases, A1 and R1–R12 can be omitted. Note that in all cases where full scale is adjusted, offset must be trimmed first.

Unipolar Binary Operation

Figures 5 and 6 show the analog circuit connections and the resulting transfer characteristic for basic unipolar operation (0 to +10V input). A –10V reference is connected to pin 10 through resistor R9 and a clock is connected to pin 15. Calibration is as follows:

Offset

Offset (zero error) is trimmed using the bipolar offset pin, B_{OFS}. Resistors R10–R12 form a voltage divider buffered by A1 which drives B_{OFS}. A0–A2 are taken LOW and latched using ALE so that channel 0 is continuously monitored. With AIN0 = +19.5mV (i.e. 1/2 LSB for 10V full scale) adjust R11 until DB7–DB1 are LOW and DB0(LSB) flickers. The offset of all channels is identical so one adjustment takes care of all eight inputs.

Full Scale

Apply +9.941V (F.S.–3/2LSB) to all inputs (AIN0–AIN7), then select one channel using A0–A2, and latch the address with ALE. Adjust trimmer RN of the selected input so that DB7–DB1 are HIGH and DB0 (LSB) flickers. Repeat for other channels.

CMOS 8-Bit 8-Channel Data Acquisition System

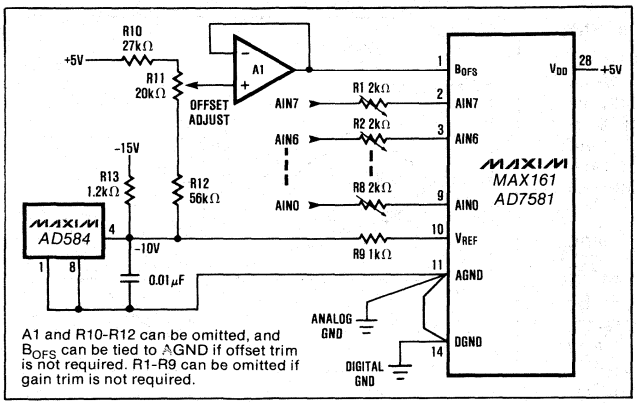


Figure 5. Unipolar (0 to +10V) Operation

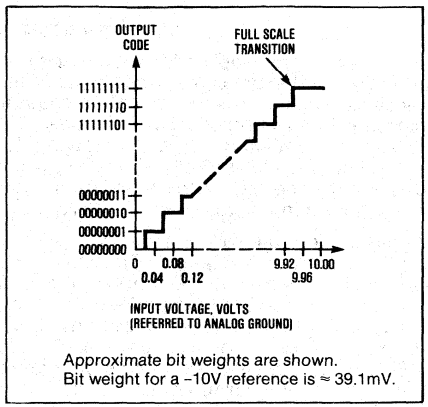


Figure 6. Unipolar (0 to +10V) Transfer Characteristic

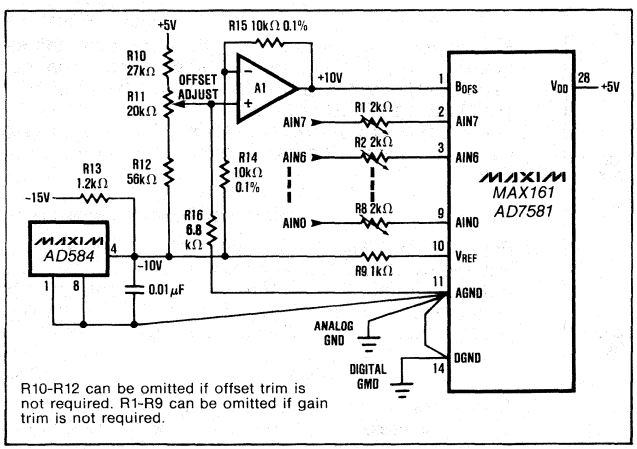


Figure 7. Unipolar (0 to -10V) Operation

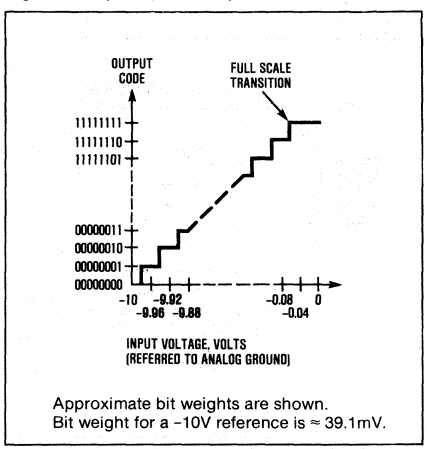


Figure 8. Unipolar (0 to -10V) Transfer Characteristic

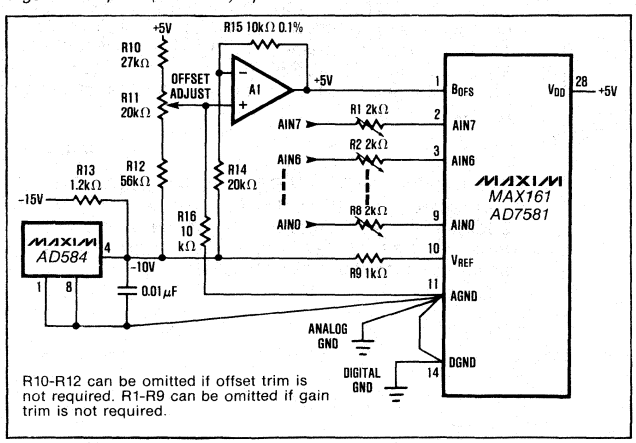


Figure 9. Bipolar (-5V to +5V) Operation

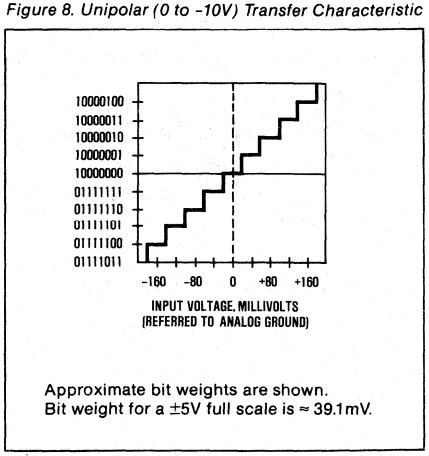


Figure 10. Bipolar Transfer Characteristic Around 0V

Unipolar (Complimentary Binary) Operation

Figures 7 and 8 show the analog circuit connections and typical transfer characteristic for unipolar (0 to -10V input) complementary binary operation. Calibration is as follows:

Offset

A0-A2 are taken LOW and latched using ALE, activating channel 0. The offset voltage is identical for all channels so only one trim is needed. With AIN0 = -9.98V (i.e. -F.S.+1/2LSB), adjust R11 so that DB7-DB1 are LOW and DB0 (LSB) flickers.

Full Scale

Apply -58.6mV (3/2 LSB) to all channels (AIN0-AIN7) and select the required channel using A0-A2 and latch the address with ALE. Adjust trimmer RN of the selected channel until DB7-DB1 are HIGH and the DB0 (LSB) flickers. Repeat for other channels.

Bipolar (Offset Binary) Operation

Figures 9 and 10 show the analog circuit connections and typical transfer characteristic for ±5V bipolar operation. Calibration is as follows:

Offset

A0-A2 are taken LOW and latched using ALE, selecting channel 0. The offset error is identical for all channels so only one trim is needed. With AIN0 = -4.980V (i.e. -F.S.+1/2LSB), adjust R11 so that DB1-DB7 are LOW and DB0 (LSB) flickers.

Full Scale

Apply +4.941V (+F.S.-3/2LSB) to all channels (AIN0-AIN7) and select the required channel using A0-A2 and latch the address with ALE. Adjust trimmer RN of the selected channel until DB1-DB7 are HIGH and DB0 (LSB) flickers. Apply -19.5mV to each gain trimmed channel. If the output code does not flicker between 01111111 and 1000000, repeat the calibration procedure.

Application Hints

Analog and Digital Ground

AGND and DGND should be connected together at the device to prevent the possibility of injecting noise into the A/D converter. In systems where the AGND-DGND connection is not local, connect clamp diodes (1N914 or equivalent) between the AGND and DGND pins.

VDD (pin 28) should be bypassed to AGND using a 10µF electrolytic and 0.1 µF ceramic capacitor. Lead lengths should be kept as short as possible.

Logic Deglitching In µP Applications

Unspecified states on the address bus (due to different rise and fall times) can cause glitches at the $\overline{CS}$ pin, initiating unwanted reads. These glitches can be avoided by gating the address decoding logic with $\overline{RD}$ (8085A) or VMA (6800) as shown in Figures 11 and 12.

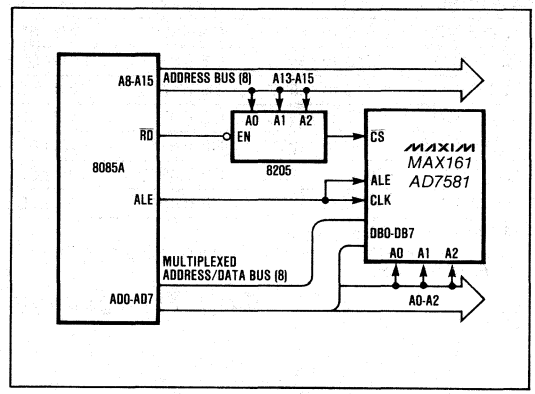


Figure 11. 8085A Interface

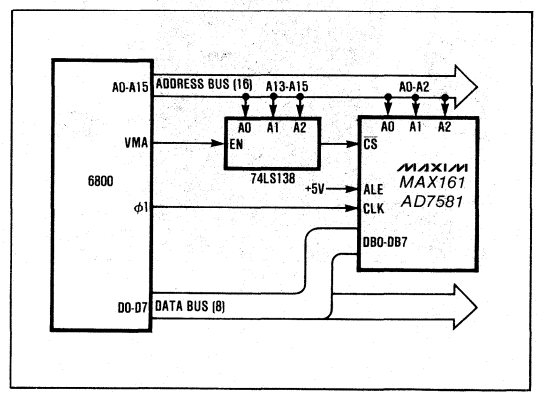


Figure 12. 6800 Interface

CMOS 8-Bit 8-Channel Data Acquisition System

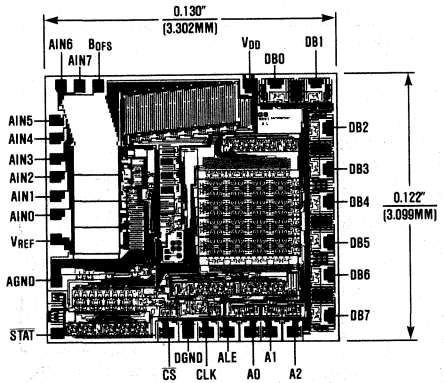
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7581JN	0°C to +70°C	Plastic DIP	1 7/8 LSB
AD7581KN	0°C to +70°C	Plastic DIP	3/4 LSB
AD7581LN	0°C to +70°C	Plastic DIP	1/2 LSB
AD7581JCWI	0°C to +70°C	Small Outline	1 7/8 LSB
AD7581KCWI	0°C to +70°C	Small Outline	3/4 LSB
AD7581LCWI	0°C to +70°C	Small Outline	1/2 LSB
AD7581JC/D	0°C to +70°C	Dice	1 7/8 LSB
AD7581AD	-25°C to +85°C	Ceramic	1 7/8 LSB
AD7581BD	-25°C to +85°C	Ceramic	3/4 LSB
AD7581CD	-25°C to +85°C	Ceramic	1/2 LSB
AD7581AQ	-25°C to +85°C	CERDIP**	1 7/8 LSB
AD7581BQ	-25°C to +85°C	CERDIP**	3/4 LSB
AD7581CQ	-25°C to +85°C	CERDIP**	1/2 LSB
AD7581SQ	-55°C to +125°C	CERDIP**	1 7/8 LSB
AD7581TQ	-55°C to +125°C	CERDIP**	3/4 LSB
AD7581UQ	-55°C to +125°C	CERDIP**	1/2 LSB

* *All devices — 28 lead packages*

** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages.*

Chip Topography



Complete High-Speed CMOS 12-Bit ADC

General Description

The MAX162 and AD7572 are complete 12-Bit analog-to-digital converters (ADC's) that combine high speed, low power consumption, and an on-chip voltage reference. The conversion times are 3μs (MAX162) and 5 and 12μs (AD7572). The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX162/AD7572 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read ($\overline{RD}$) and Chip Select ($\overline{CS}$) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

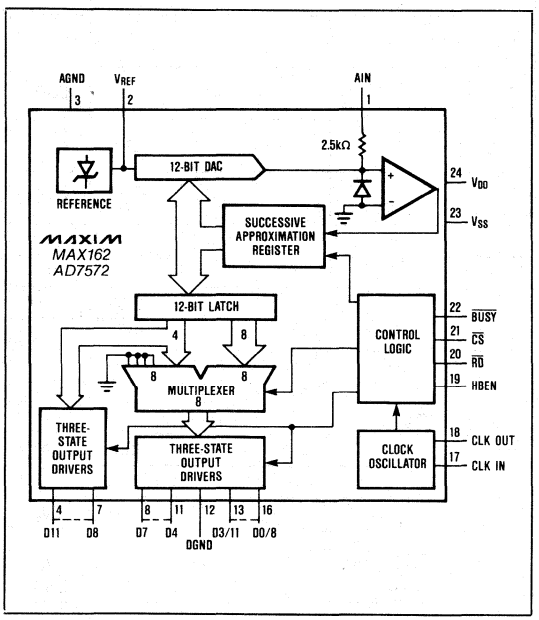
Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Functional Diagram



Features

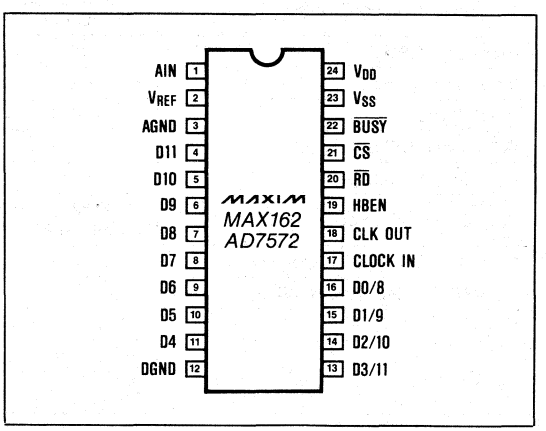
- 12-Bit Resolution and Linearity
- 3μs (MAX162), 5μs and 12μs (AD7572) Conversion Times
- No missing Codes
- On-Chip Voltage Reference
- 90ns Access Time
- 215mW Max Power Consumption
- 24-Lead Narrow DIP Package

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
3μs CONVERSION TIME			
MAX162ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX162BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162ACWG	0°C to +70°C	Wide S.O.	±½ LSB
MAX162BCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CC/D	0°C to +70°C	Dice**	±1 LSB
MAX162AING	-25°C to +85°C	Plastic DIP	±½ LSB
MAX162BING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162CING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX162BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX162CMRG	-55°C to +125°C	CERDIP	±1 LSB

* *All devices — 24 lead packages*
** *Consult factory for dice specifications*
Ordering Information continued on last page.

Pin Configuration



Complete High-Speed CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX162XC, AD7572JN, KN, LN,
JCWG, KCWG, LCWG ..... 0°C to +70°C
MAX162XI, AD7572AQ, BQ, CQ ..... -25°C to +85°C
MAX162XM, AD7572SQ, TQ, UQ .... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ± 5%, V_{SS} = -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for AD7572XX05 and 1MHz for AD7572XX12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL	MAX162A, AD7572L/C/U MAX162B/C, AD7572K/B/T/J/A/S				±1/2 ±1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Offset Error (Note 1)		MAX162C, AD7572J/A/S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±8	LSB
		MAX162B, AD7572K/B/T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±3 ±6	
		MAX162A, AD7572L/C/U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±4	
Full Scale Error (Note 2)		MAX162C, AD7572J/A/S	T_A = 25°C			±15	LSB
		MAX162B, AD7572K/B/T	T_A = 25°C			±10	
		MAX162A, AD7572L/C/U	T_A = 25°C			±10	
Full Scale Tempco (Notes 3, 4)		MAX162C, AD7572J/A/S MAX162B/A, AD7572K/B/T, AD7572L/C/U				±45 ±25	ppm/°C
ANALOG INPUT							
Input Voltage Range		For Bipolar Input see Figures 19-21		0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)		MAX162C, AD7572J/A/S MAX162B/A, AD7572K/B/T, AD7572L/C/U			40 20		ppm/°C
Output Current Sink Capability		(Note 6)				500	µA
POWER SUPPLY REJECTION							
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75V to 5.25V			±1/2		LSB
V_{SS} Only		FS Change, V_{DD} = 5V MAX162/AD7572 MAX162	V_{SS} = -14.25V to -15.75V V_{SS} = -11.4V to -12.6V		±1/8 ±1/8		LSB LSB

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ± 5%, V_{SS} = -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for AD7572XX05 and 1MHz for AD7572XX12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				10	pF
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN CLKIN	VIN = 0 to V_{DD}			±10 ±20	μA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SOURCE} = 200μA		4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	μA
Floating State Output Capacitance (Note 7)	C_{OUT}					15	pF
CONVERSION TIME							
MAX162	t_{CONV}	f_{CLK} = 4MHz	Synchronous (13 clock cycles) Asynchronous (12 to 13 clock cycles)	 3.0		3.25 3.25	μs
AD7572XX05	t_{CONV}	f_{CLK} = 2.5MHz	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	 4.8		5 5.2	μs
AD7572XX12	t_{CONV}	f_{CLK} = 1MHz	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	 12		12.5 13	μs
POWER REQUIREMENTS							
V_{DD}		±5% for Specified Performance		4.75	5	5.25	V
V_{SS} (Note 8)		±5% MAX162 ±5% AD7572			-12 or -15 -15		V
I_{DD}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V			145	215	mW

Note 1: Typical change over temp is ±1 LSB
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS - 3/2LSB
Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: V_{SS} = -12V ±5% for the MAX162 only. Functional operation is guaranteed by testing offset error and full scale error.

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TIMING CHARACTERISTICS (Note 9)

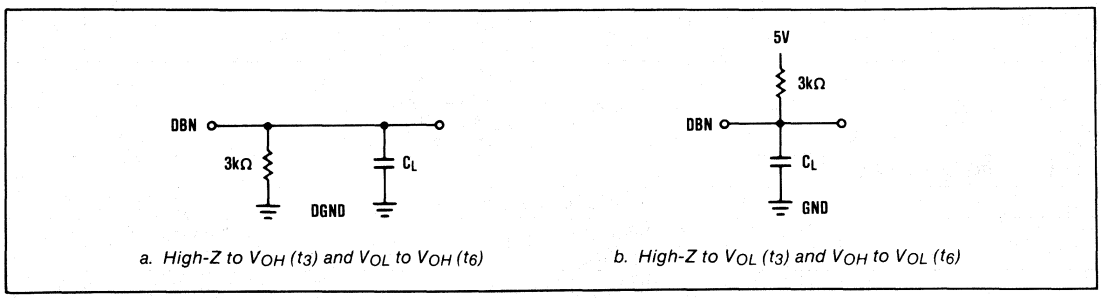
(V_{DD} = +5V, V_{SS} = -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX162C/I AD7572J/K/L AD7572A/B/C		MAX162M AD7572S/T/U		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t_3	C_L = 20pF C_L = 100pF		60 70	90 125		110 150		120 170	ns
$\overline{RD}$ Pulse Width	t_4		t_3			t_3		t_3		
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ Note (10)	t_6				70		90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

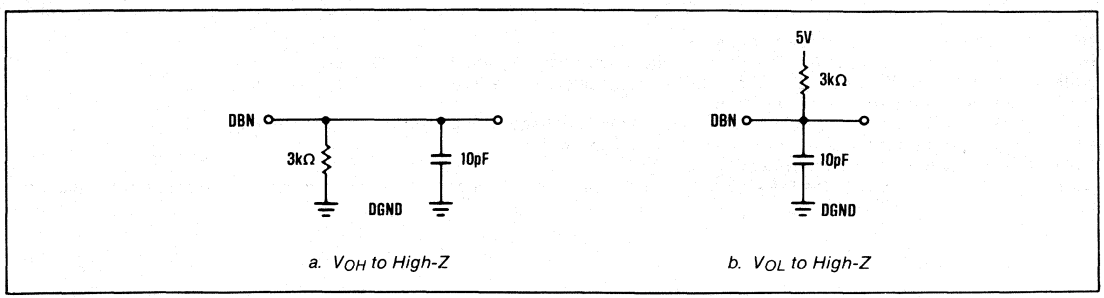
Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

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Pin Description

PIN	NAME	FUNCTION
1	AIN	Analog Input, 0 to +5V unipolar input
2	V_{REF}	-5.25V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLKIN	Clock Input. An external TTL/CMOS compatible clock may be applied to this pin or a crystal can be connected between CLKIN and CLKOUT.
18	CLKOUT	Clock Output. An inverted CLKIN signal appears at this pin.

PIN	NAME	FUNCTION
19	HBEN	High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). HBEN also disables conversion starts when HIGH.
20	$\overline{RD}$	READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.
21	$\overline{CS}$	The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.
22	$\overline{BUSY}$	The BUSY Output is low when a conversion is in progress.
23	V_{SS}	Negative Supply, -15V for AD7572 and -15V or -12V for MAX162.
24	V_{DD}	Positive Supply, +5V.

Data Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note:
* D11 . . . D0/8 are the ADC data output pins.
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB.

Converter Operation

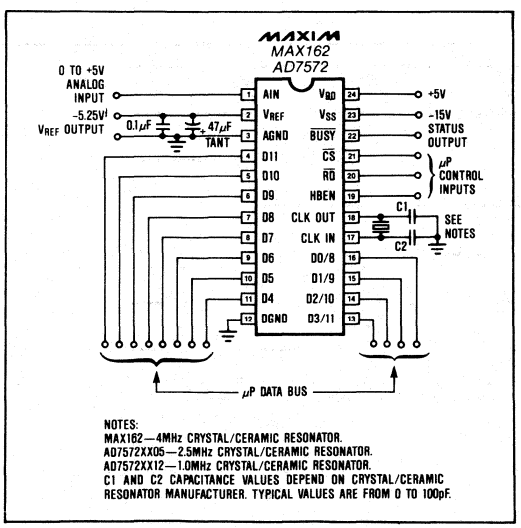

Figure 3. MAX162/AD7572 Operational Diagram

The MAX162 and AD7572 use a successive approximation technique to convert an unknown analog input to a 12 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital function. Figure 3 shows the MAX162/AD7572 in its simplest operational configuration.

Figure 4 shows the MAX162/AD7572 analog equivalent circuit. The internal voltage output DAC is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero crossing detector and its output is fed back to the SAR input.

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN digital inputs. A conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ while HBEN is low. Once started, conversion cannot be stopped. The $\overline{BUSY}$ output goes low as soon as the conversion starts. $\overline{BUSY}$ may be used to control an external sample-and-hold when wide bandwidth input signals are being measured.

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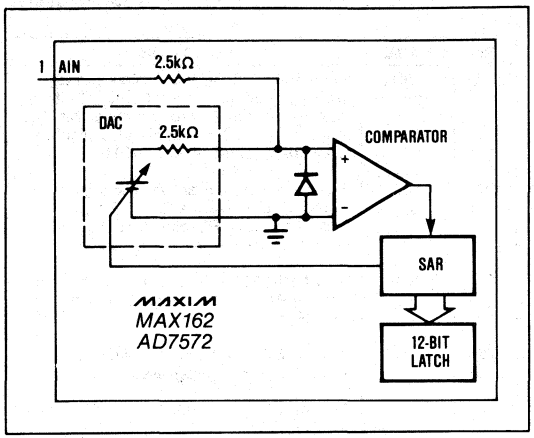

Figure 4. MAX162/AD7572 Analog Equivalent Circuit

The SAR is set to half scale as soon as the $\overline{CS}$ and $\overline{RD}$ inputs go low. This reset is asynchronous with the clock input. The analog input is then compared to one half of the full scale voltage. About 30ns after the second falling edge of CLKIN (or rising edge of CLKOUT), the output of the comparator is latched into the SAR MSB bit (see Figure 5). The bit is kept if the analog input is greater than half scale, or dropped if it is smaller. The next bit (bit 11) is then set with the DAC output either at 1/4 scale (if the MSB was dropped) or 3/4 scale (if the MSB was kept). The conversion continues in this manner until the LSB is tried. Following a falling CLKIN signal, the $\overline{BUSY}$ output goes high and the SAR result is latched into the three-state output buffers.

Clock Operation

Clock Oscillator

Figure 6 shows the MAX162/AD7572 clock circuitry. The capacitive load on the CLKOUT pin must be minimized for low power dissipation and to avoid digital coupling of the CLKOUT buffer currents to the comparator. If an external clock source is being used to drive CLKIN, CLKOUT should be left open. The external clock source must have a 50% duty cycle. If the internal oscillator is being used, a crystal/ceramic resonator should be connected between CLKOUT and CLKIN as shown in Figure 6.

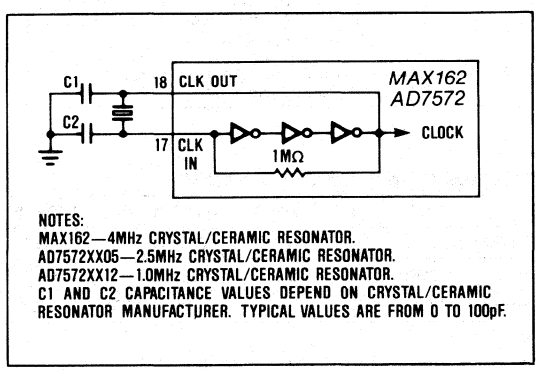

Figure 6. MAX162/AD7572 Internal Clock Circuit

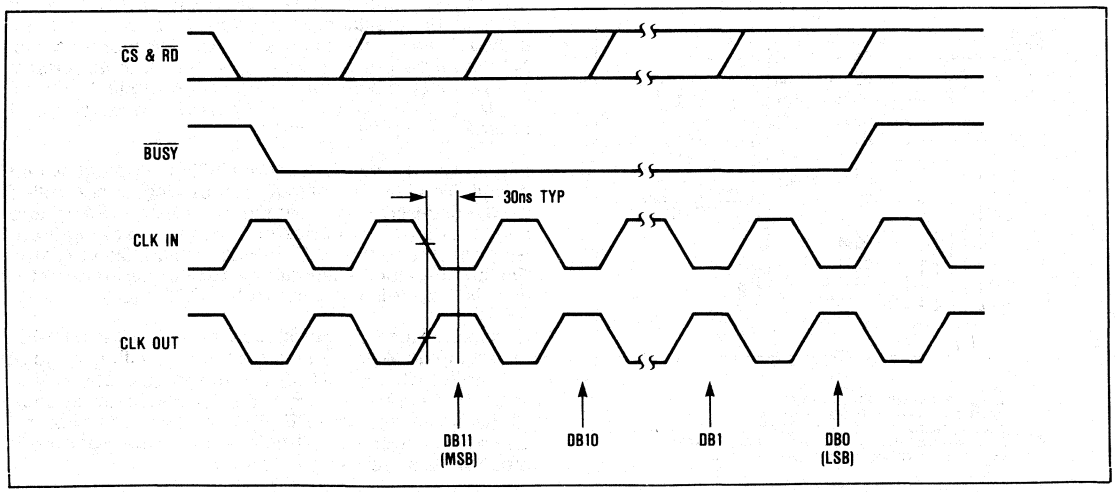

Figure 5. Operating Waveforms Using an External Clock Source for CLKIN.

Control Input Synchronization

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock, the conversion time can vary from 12 to 13 clock cycles. The SAR changes state on the falling edge of the CLKIN input (or rising edge on the CLKOUT pin). To ensure a fixed conversion time use the following guidelines for synchronization:

MAX162

For the MAX162 the $\overline{RD}$ input should go low at the falling edge of CLKIN. In this case the conversion lasts 13 clock cycles and the conversion time is 3.25μs when f_{CLK} = 4MHz. If the CLKIN and $\overline{RD}$ falling edges are skewed, the skew must not be more than 50ns to ensure the 13 period conversion time (See Figure 7). The MSB is tried at the second clock falling edge, leaving two clock cycles for the external sample-and-hold to settle from hold transients.

AD7572

The AD7572 $\overline{RD}$ input can go low at the rising edge of CLKIN. In this case the conversion lasts 12.5 clock cycles and the conversion time is 5μs when f_{CLK} = 2.5MHz and 12.5μs when f_{CLK} = 1MHz. The delay from the falling edge of RD to the falling edge of CLKIN must not be less than 180ns to ensure the 12.5 clock cycle conversion time (See Figure 8). This leaves the external sample-and-hold 1.5 clock cycles to settle from hold transients. An additional half clock cycle of settling can be allowed for driving the sample-and-hold by having RD go low at the falling edge of CLKIN, similar to the MAX162. This results in a 13 cycle conversion time (5.2μs when f_{CLK} = 2.5MHz, 13μs when f_{CLK} = 1MHz).

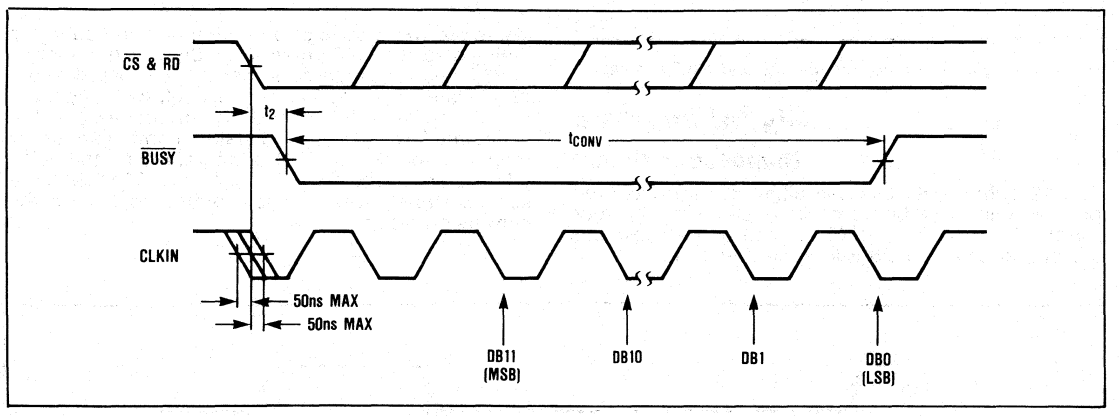

Figure 7. MAX162 $\overline{RD}$ and CLKIN For Synchronous Operation

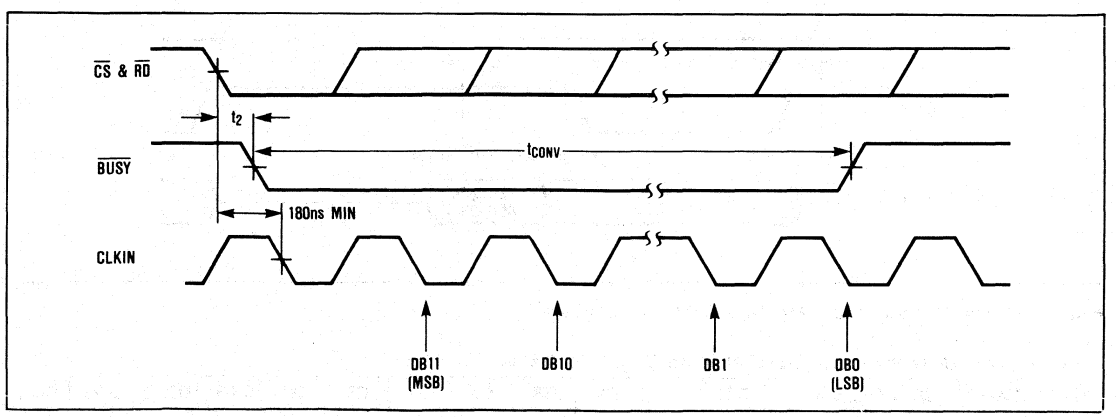

Figure 8. AD7572 $\overline{RD}$ and CLKIN For Synchronous Operation

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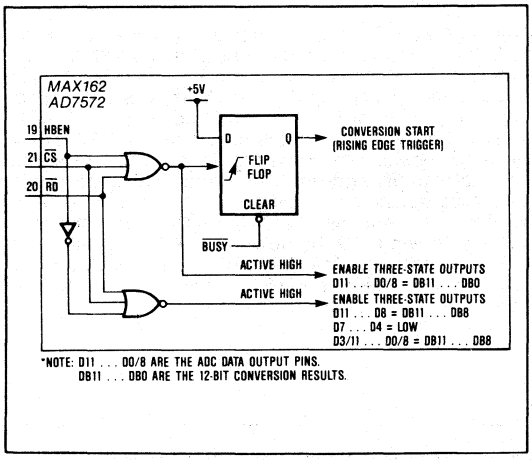


Figure 9. Logic Equivalent for $\overline{RD}$, $\overline{CS}$ and HBEN Inputs

Digital Interface

Output Data Format

The 12 output data bits can either be presented full parallel or in two 8 bit words. To obtain parallel output for 16 bit processors, HBEN should be kept low and the output data D11-D0 will be right justified.

For a two byte data read, outputs D7-D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented with the leading 4 bits being low for D7-D0/8.

Note that the 4 MSB's always appear at digital outputs D11-D8 whenever the digital drivers are enabled, regardless of the state of HBEN.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs; HBEN, CS and RD. Figure 9 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion. Once a conversion is in progress, it cannot be re-started. The BUSY output is low during the entire conversion cycle.

There are two modes of operation as outlined in the timing diagrams of Figures 10-13. Slow memory mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX162/AD7572 conversion time. ROM mode is for processors that cannot be forced into a wait state. In both operational modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation is required to access the conversion result.

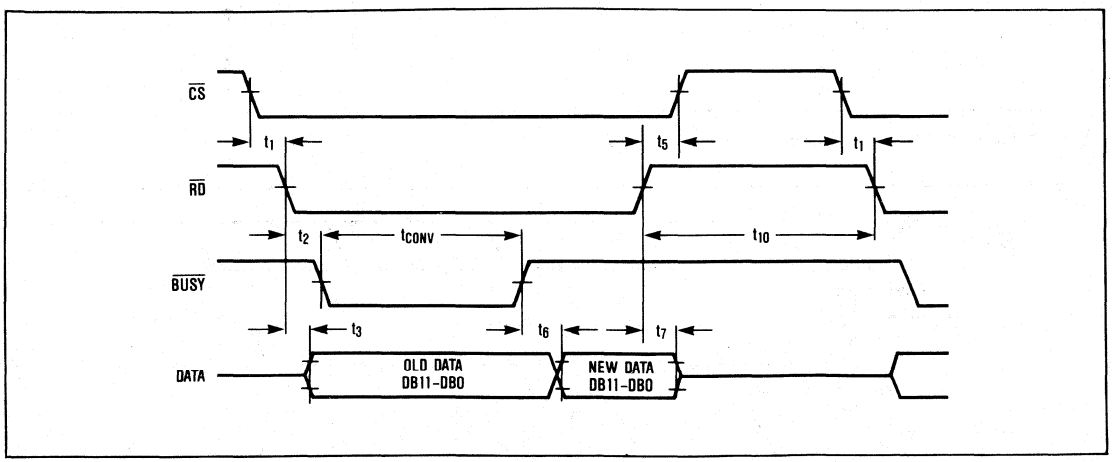


Figure 10. Slow Memory Mode, Parallel Read Timing Diagram

Table 1. Slow Memory Mode, Parallel Read Data Bus Status

MAX162/AD7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

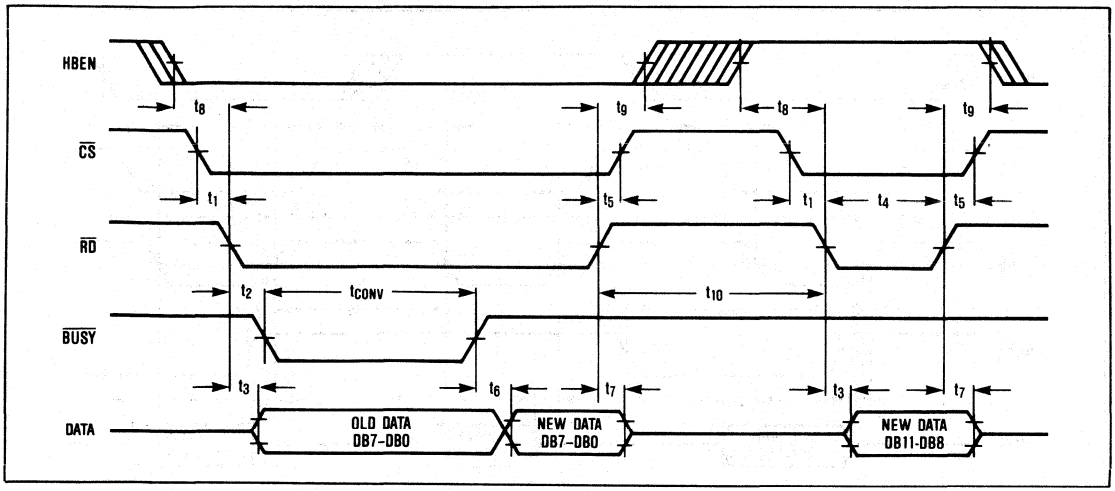


Figure 11. Slow Memory Mode, Two Byte Read Timing Diagram

Table 2. Slow Memory Mode, Two Byte Read Data Bus Status

MAX162/AD7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

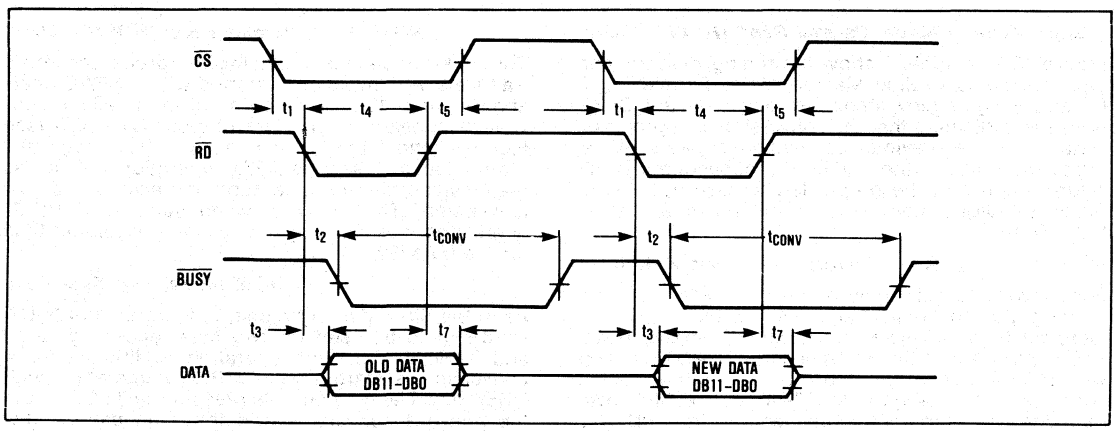


Figure 12. ROM Mode, Parallel Read Timing Diagram

Table 3. ROM Mode, Parallel Read Data Bus Status

MAX162/AD7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Complete High-Speed CMOS 12-Bit ADC

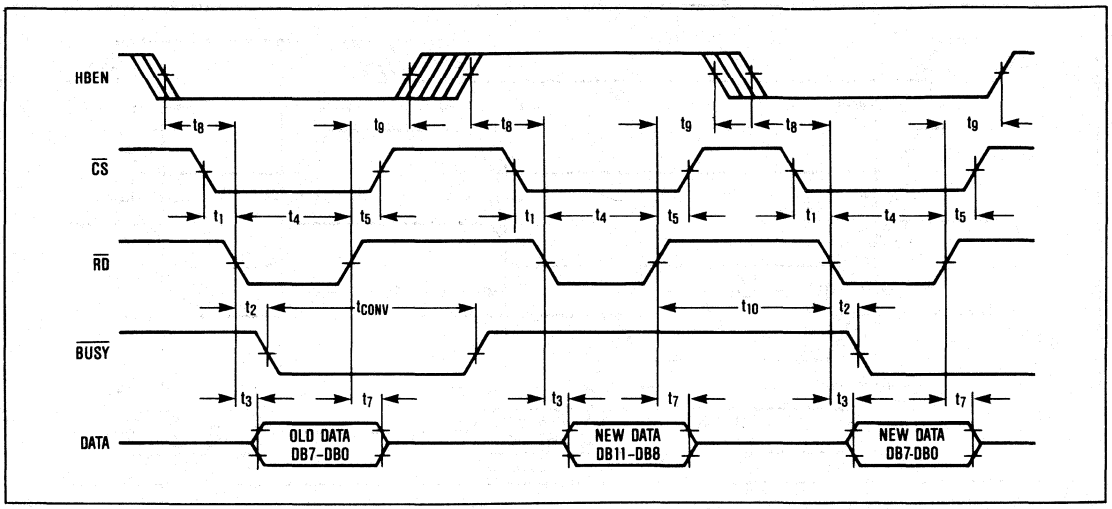


Figure 13. ROM Mode, Two Byte Read Timing Diagram

Table 4. ROM Mode, Two Byte Read Data Bus Status

MAX162/AD7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 10 and Table 1 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. CS and RD going low starts the conversion and BUSY goes low indicating that the conversion is in progress. Data from the previous conversion appears at the digital outputs. At the end of the conversion, BUSY returns high and the output latches are updated to place the digital conversion result on data outputs D11-D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only outputs D7-D0/8 are used. Starting the conversion and reading the 8 LSB's is identical to the Slow Memory Mode, Parallel Read. See Figure 11 and Table 2. A second READ operation with HBEN high places the 4 MSB's with 4 leading zeros on the data outputs D7-D0/8. The high byte read does not start another conversion since HBEN is high.

ROM Mode, Parallel Read (HBEN = LOW)

The ROM mode avoids placing the processor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion appears at the data outputs D11-D0/8 (see Figure 12 and Table 3). This data may be disregarded if not needed. A second READ operation will access the results of the first operation and also start a new conversion. The delay between successive READ operations must be longer than the conversion time for the MAX162/AD7572.

ROM Mode, Two Byte Read

As in the Slow Memory Mode, only data outputs D7-D0/8 should be used for two byte reads. Figure 13 and Table 4 show the operation in this mode. A conversion is started with a READ operation with HBEN low. The data outputs present the 8 LSB's from the previous conversion and this data can be disregarded if not required. Two more READ operations are needed to access the conversion result. The first READ must be with HBEN high, where the 4 MSB's with 4 leading zero's are accessed. The second READ is with HBEN low, which reads in the 8 LSB's and starts a new conversion.

Complete High-Speed CMOS 12-Bit ADC

Interface Application Hints

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, LSBs of error can be caused due to coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

ROM Mode

Considerable digital noise is generated in the ADC when RD or CS go high and the output data drivers are disabled after a conversion is started. This noise will feed into the ADC comparator and cause large errors if it coincides with the time the SAR is latching a decision to keep or drop a bit. To avoid this problem, RD and CS should be active for less than one clock cycle. In other words, the RD and CS low pulse should be shorter than 250ns for the MAX162, 400ns for the AD7572XX05 and 1μs for the AD7572XX12. If this cannot be done, the RD or CS signal must go high at a rising edge of CLKIN, since the comparator output is always latched at falling edges of CLKIN.

Analog Considerations

Application Hints

Physical Layout

For best system performance printed circuit boards should be used for the MAX162/AD7572. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX162/AD7572 package.

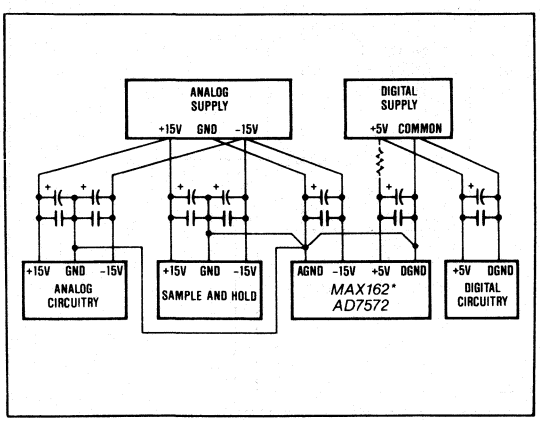


Figure 14. Power Supply Grounding Practice

Grounding

Figure 14 shows the recommended system ground connections. A single point analog STAR ground should be established at pin 3 (AGND) of the MAX162/AD7572 separate from the logic ground. All other analog grounds and pin 12 (DGND) of the MAX162/AD7572 should be connected to this STAR ground and no other digital grounds should be connected to this STAR point. The ground return to the power supply from this STAR ground should be low impedance for noise free operation of the ADC.

Power Supply Bypassing

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be by-passed to the analog STAR ground with 0.1μF and 10μF by-pass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small (10-20 ohms) resistor can be connected as shown in Figure 14 to filter external noise.

Internal Reference

The MAX162/AD7572 has an internal buried zener reference which provides the DAC reference voltage. The reference voltage is -5.25V ±1% and has a low temperature coefficient. The reference output is available at pin 2, and should be bypassed to analog ground (pin 3) with a 47μF tantalum capacitor in parallel with 0.1μF capacitor to minimize noise and provide low impedance at high frequencies. This by-pass capacitor must not be less than 4.7μF. The internal reference output buffer can sink upto 500μA.

Driving The Analog Input

The input signal leads to AGND and AIN should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion (4MHz for MAX162 and 2.5 or 1MHz for the AD7572). The output impedance of the driving amplifier is equal to its open loop output impedance divided by the loop gain at the frequency of interest.

AD7572 The AD7572 maximum clock rate of 2.5MHz makes it possible to drive it with amplifiers like the OP-42, AD711 or OP-27. At 1MHz clock rate a MAX400 or OP-07 can also be used.

MAX162 The MAX162 with a maximum 4MHz clock rate might cause settling problems with the above amplifiers. An LF356, LF400 or LT1056 can be used to drive the input. Alternatively, an emitter follower buffer inside the feedback loop of a OP-42, AD711 or OP-27 can be used to improve high frequency output impedance.

Complete High-Speed CMOS 12-Bit ADC

MAX162/AD7572 to Sample-and-Hold Interface

The analog input to the ADC must be stable to within 1/2 LSB during the entire conversion for specified 12 bit accuracy. This limits the input signal bandwidth to less than 6Hz for sinusoidal inputs, even when using the faster MAX162. For higher bandwidth signals a sample-and-hold should be used.

The $\overline{BUSY}$ output from the MAX162/AD7572 may be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. However, since the ADC's DAC is switched at approximately the same time as the $\overline{BUSY}$ signal goes low, the switching transients at the output of the sample-and-hold caused by the DAC switching may result in code dependent errors due to the aperture delay of the sample-and-hold. A NAND gate may be used to ensure that the sample-and-hold switches to the hold mode BEFORE any disturbances as shown in Figures 15 & 16. The NAND gate solution works only if the width of the $\overline{RD}$ pulse is wider than the $\overline{RD}$ to $\overline{BUSY}$ delay in the MAX162/AD7572. If this is not the case, use a flip flop which is set by the falling edge of $\overline{RD}$ and reset by the rising edge of $\overline{BUSY}$.

For synchronous $\overline{RD}$ and CLKIN as described above, the hold settling time allowed for the sample-and-hold is 500ns, 600ns and 1.5μs for the MAX162, AD7572XX05 and AD7572XX12 respectively.

To achieve the maximum sampling rate, the MAX162/AD7572 data must be read within the time allowed for the sample-and-hold to acquire a new input voltage.

AD7572 Figure 15 shows an AD585 sample-and-hold to AD7572 interface. The AD7572 $\overline{RD}$ input and $\overline{BUSY}$ output are used to put the AD585 in hold mode when a conversion is in progress. In this example the analog input range is ±2.5V but other voltage ranges can be configured differently as explained later.

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3μs sample-and-hold acquisition time.

Although this circuit works quite well for the 1MHz clock rate, at the 2.5MHz clock rate a faster sample-and-hold amplifier such as the HA-5320 is recommended.

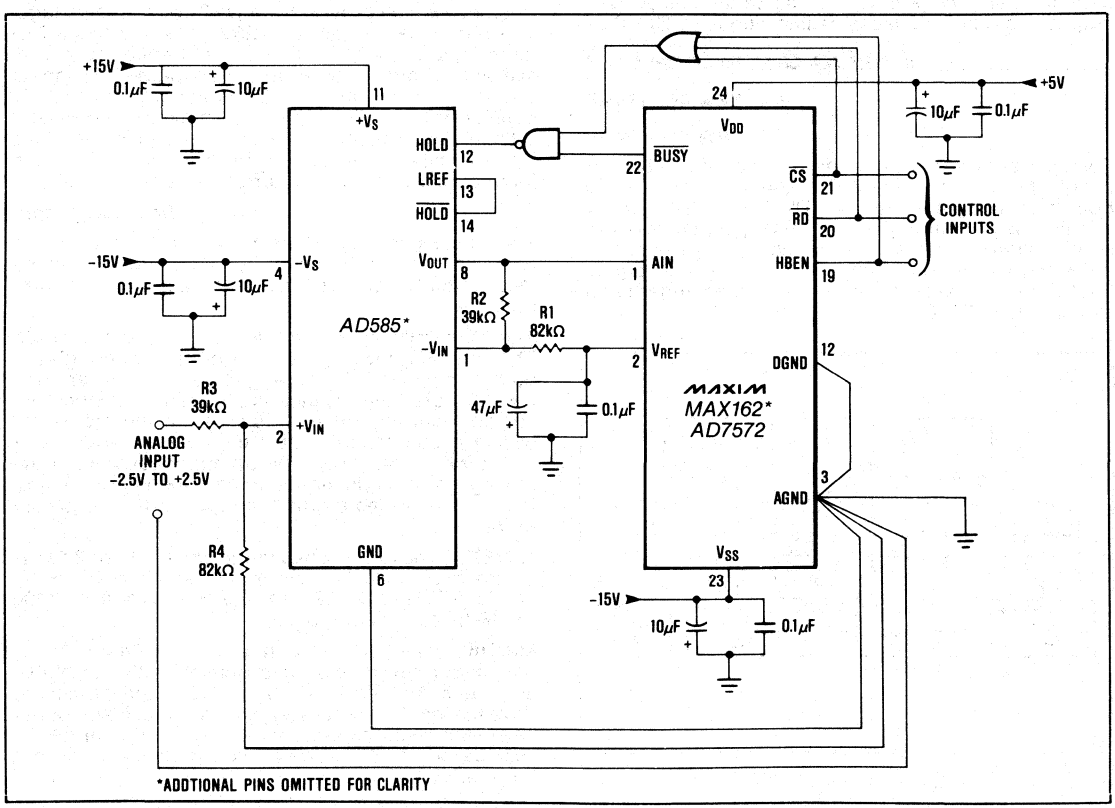


Figure 15. AD7572—AD585 Sample-and-Hold Interface

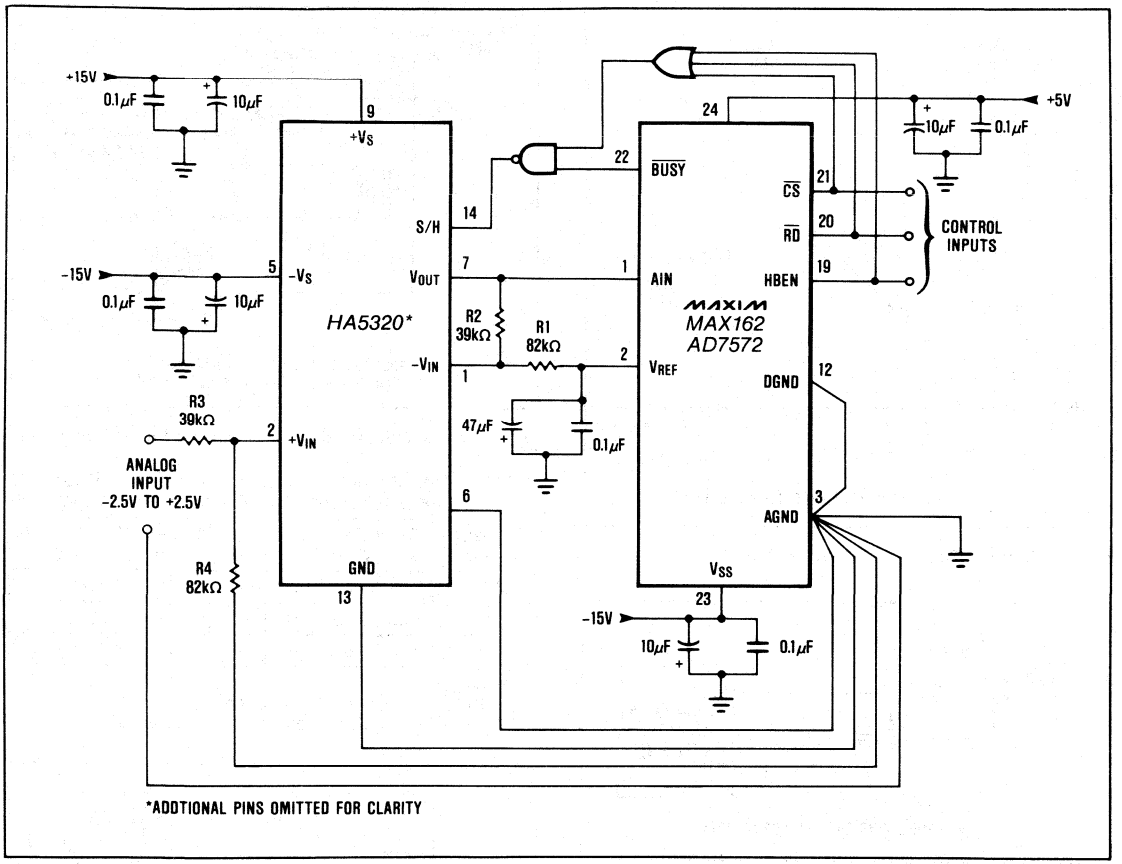


Figure 16. MAX162/AD7572—HA5320 Sample-and-Hold Interface

MAX162 Figure 16 shows the MAX162 to HA5320 interface. The maximum sampling rate is 210kHz with a 4MHz clock which allows for a 1.5μs acquisition time. The HA5320 can also be replaced by a HA5330 for higher throughput.

Unipolar Input Operation

Figure 17 shows the nominal input/output transfer function of the MAX162/AD7572. Code transitions occur half way between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 18. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS-3/2LSB (4.99817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 5 and 6.

Complete High-Speed CMOS 12-Bit ADC

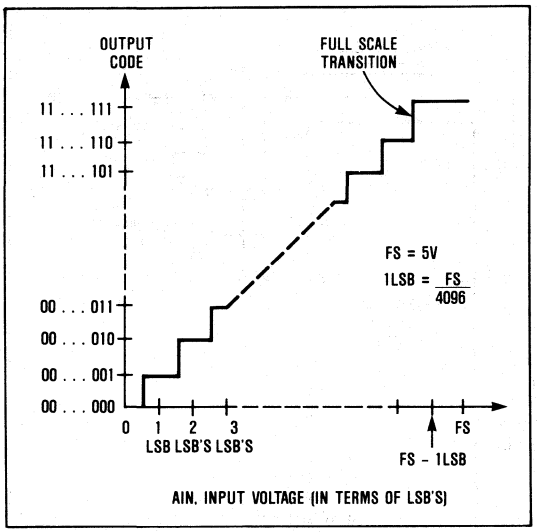


Figure 17. MAX162/AD7572 Transfer Function

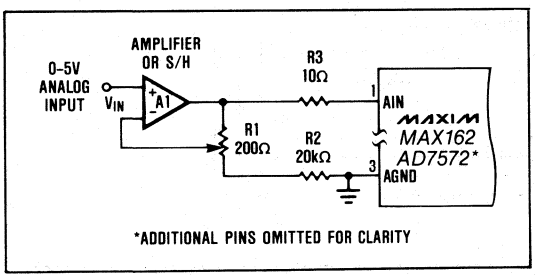


Figure 18. Full-Scale Adjustment

Figure 19 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 20 shows the ideal transfer function for this mode.

Figure 21 shows the bipolar operation in the inverting mode, where the output coding is complementary offset binary. Figure 20 shows the ideal transfer function for the circuit in Figure 21.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drifts. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

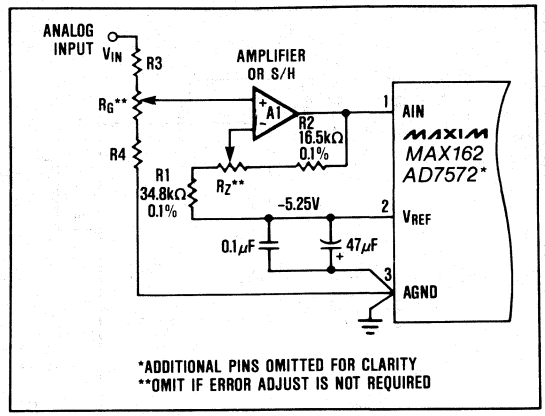


Figure 19. MAX162/AD7572 Non-inverting Bipolar Operation

Table 5. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 19

V_{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

Notes:
* R3 and R4 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

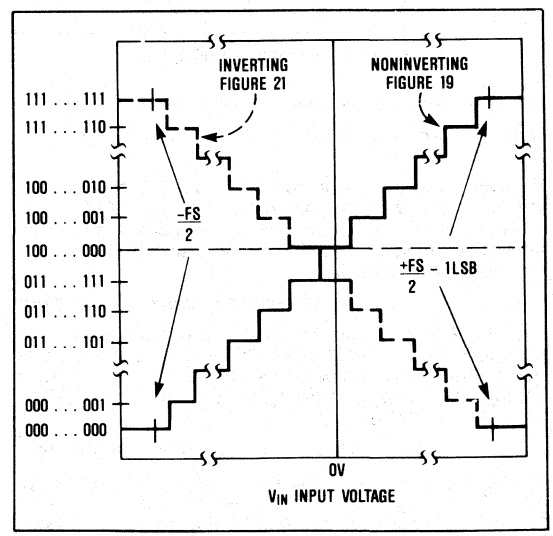


Figure 20. Ideal Input/Output Transfer Characteristic for the Bipolar circuits in Figures 19 and 21.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see tables 5 and 6) and adjust R_Z until the output code flickers between the following codes:

For Non-inverting (Figure 19)	1000 0000 0000 1000 0000 0001
For inverting (Figure 21)	0111 1111 1111 0111 1111 1110

Apply FS-3/2LSB (see tables 5 and 6) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-inverting (Figure 19)	1111 1111 1110 1111 1111 1111
For inverting (Figure 21)	0000 0000 0001 0000 0000 0000

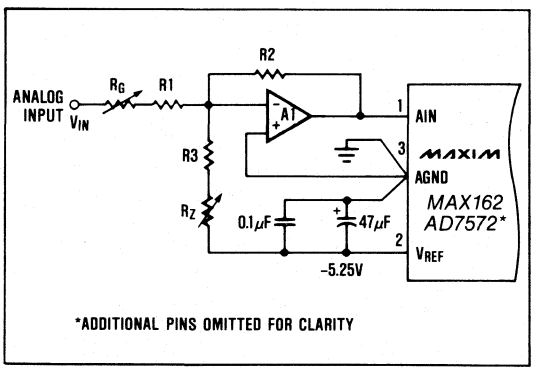


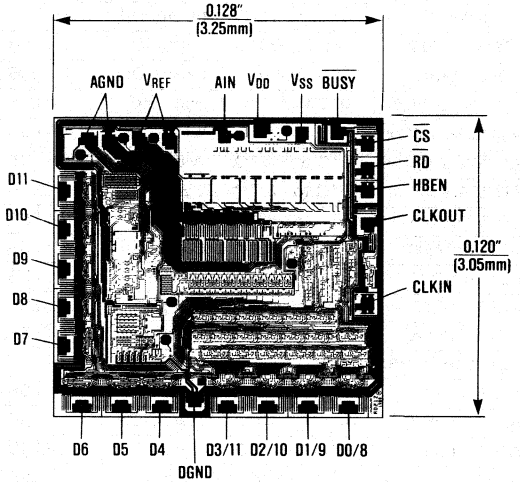
Figure 21. MAX162/AD7572 Inverting Bipolar Operation

Table 6. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 21

V_{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

Notes:
* R1, R2, and R3 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

Chip Topography



Complete High-Speed CMOS 12-Bit ADC

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
5μs CONVERSION TIME			
AD7572JN05	0°C to +70°C	Plastic DIP	±1 LSB
AD7572KN05	0°C to +70°C	Plastic DIP	±1 LSB
AD7572LN05	0°C to +70°C	Plastic DIP	±½ LSB
AD7572JCWG05	0°C to +70°C	Wide S.O.	±1 LSB
AD7572KCWG05	0°C to +70°C	Wide S.O.	±1 LSB
AD7572LCWG05	0°C to +70°C	Wide S.O.	±½ LSB
AD7572AQ05	-25°C to +85°C	CERDIP	±1 LSB
AD7572BQ05	-25°C to +85°C	CERDIP	±1 LSB
AD7572CQ05	-25°C to +85°C	CERDIP	±½ LSB
AD7572SQ05	-55°C to +125°C	CERDIP	±1 LSB
AD7572TQ05	-55°C to +125°C	CERDIP	±1 LSB
AD7572UQ05	-55°C to +125°C	CERDIP	±½ LSB
12μs CONVERSION TIME			
AD7572JN12	0°C to +70°C	Plastic DIP	±1 LSB
AD7572KN12	0°C to +70°C	Plastic DIP	±1 LSB
AD7572LN12	0°C to +70°C	Plastic DIP	±½ LSB
AD7572JCWG12	0°C to +70°C	Wide S.O.	±1 LSB
AD7572KCWG12	0°C to +70°C	Wide S.O.	±1 LSB
AD7572LCWG12	0°C to +70°C	Wide S.O.	±½ LSB
AD7572AQ12	-25°C to +85°C	CERDIP	±1 LSB
AD7572BQ12	-25°C to +85°C	CERDIP	±1 LSB
AD7572CQ12	-25°C to +85°C	CERDIP	±½ LSB
AD7572SQ12	-55°C to +125°C	CERDIP	+1 LSB
AD7572TQ12	-55°C to +125°C	CERDIP	±1 LSB
AD7572UQ12	-55°C to +125°C	CERDIP	±½ LSB

* *All devices — 24 lead packages*

Complete 10μs CMOS 12-Bit ADC

General Description

The MAX172 is a complete 12-Bit analog-to-digital converter (ADC) that combines high speed, low power consumption, and an on-chip voltage reference. The conversion time is 10μs. The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX172 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Features

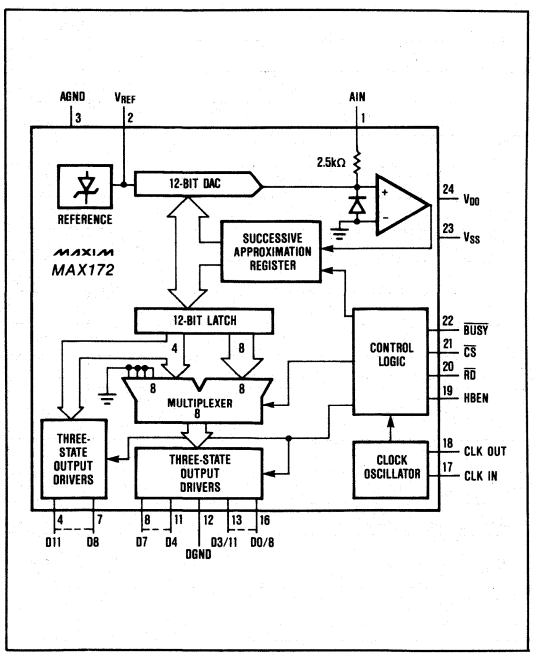
- **12-Bit Resolution and Linearity**
- **10μs Conversion Time**
- **No Missing Codes**
- **On-Chip Voltage Reference**
- **90ns Access Time**
- **215mW Max Power Consumption**
- **24-Lead Narrow DIP Package**
- **Pin-for-Pin AD7572 Replacement**

Ordering Information

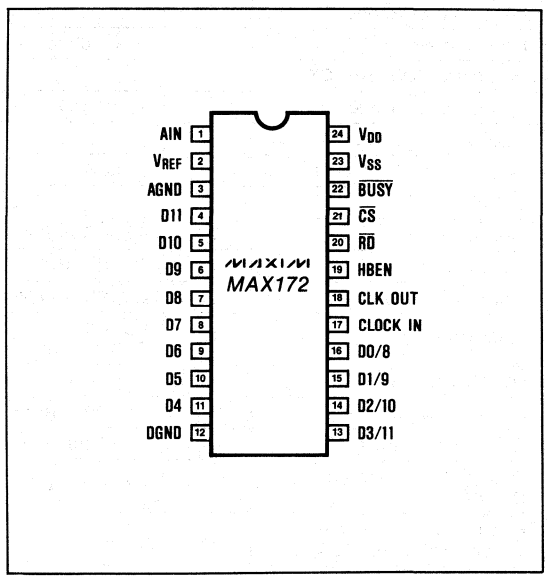
PART	TEMP. RANGE	PACKAGE*	ERROR
MAX172ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX172BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX172ACWG	0°C to +70°C	Wide S.O.	±½ LSB
MAX172BCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX172CC/D	0°C to +70°C	Dice**	±1 LSB
MAX172AING	-25°C to +85°C	Plastic DIP	±½ LSB
MAX172BING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX172AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX172BMRG	-55°C to +125°C	CERDIP	±1 LSB

* *All devices — 24 lead packages*
** *Consult factory for dice specifications*

Functional Diagram



Pin Configuration



Complete 10μs CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX172XC ..... 0°C to +70°C
MAX172XI ..... -25°C to +85°C
MAX172XM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 1.25MHz.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL	MAX172A MAX172B				±1/2 ±1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Offset Error (Note 1)		MAX172B	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±8	LSB
		MAX172A	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±4	
Full Scale Error (Note 2)		MAX172B	T_A = 25°C			±15	LSB
		MAX172A	T_A = 25°C			±10	
Full Scale Tempco (Notes 3, 4)						±45	ppm/°C
ANALOG INPUT							
Input Voltage Range				0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)					40		ppm/°C
Output Current Sink Capability		(Note 6)				500	μA
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				10	pF
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN CLKIN	VIN = 0 to V_{DD}			±10 ±20	μA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SOURCE} = 200μA		4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	μA
Floating State Output Capacitance (Note 7)	C_{OUT}					15	pF

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 1.25MHz.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION TIME						
MAX172	t_{CONV}	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	 9.6		10 10.4	µs
POWER SUPPLY REJECTION						
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75V to 5.25V		±1/2		LSB
V_{SS} Only		FS Change, V_{DD} = 5V, V_{SS} = -5% to +5%		±1/8		LSB
POWER REQUIREMENTS						
V_{DD}		±5% for Specified Performance		5		V
V_{SS} (Note 8)		±5% for Specified Performance		-12 or -15		V
I_{DD}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V		145	215	mW

Note 1: Typical change over temp is ±1 LSB.
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS - 3/2LSB.
Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: Functional operation at V_{SS} = -12V ± 5% is guaranteed by testing offset error and full scale error.

TIMING CHARACTERISTICS (Note 9)

(V_{DD} = +5V, V_{SS} = -12V or -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

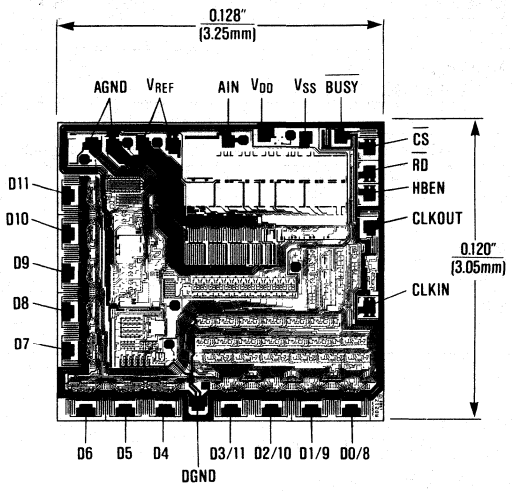
PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX172C/I		MAX172M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t_3	C_L = 20pF C_L = 100pF		60 70	90 125		110 150		120 170	ns
$\overline{RD}$ Pulse Width	t_4		t_3			t_3		t_3		
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ Note (10)	t_6				70		90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

For additional information on using the MAX172 please refer to MAX162 data sheet.

Complete 10μs CMOS 12-Bit ADC

Chip Topography



MAXIM

High Speed 12 Bit A/D Converter

General Description

The AD578 is a 12-bit successive approximation analog-to-digital converter complete with internal clock and reference. The combination of bipolar and CMOS technology optimizes accuracy, speed, and power in a convenient 32 pin ceramic DIP. Maximum conversion time is 3μS (L version) however the device may be operated at faster speeds with reduced resolution by short cycling.

Multiple input ranges are accommodated in both unipolar and bipolar modes using internal resistors. These resistors also track those in the reference for low gain drift with temperature. All data bits are available in both parallel and serial form using either the internal or an external clock.

Applications

High Speed Data Acquisition Systems
Transient Recorders
Multichannel Data Loggers
Digital Signal Processing

Features

- **Pin-for-Pin Second Source**
- **Fast Conversion: 3μs (AD578L)**
- **Internal +10V Reference**
- **Low Gain TC: 30ppm/°C Max**
- **Linearity Error: 0.012% Max**
- **No Missing Codes Over Temperature**
- **Parallel and Serial Outputs**
- **Adjustable Internal Clock**
- **Short Cycle Capability**

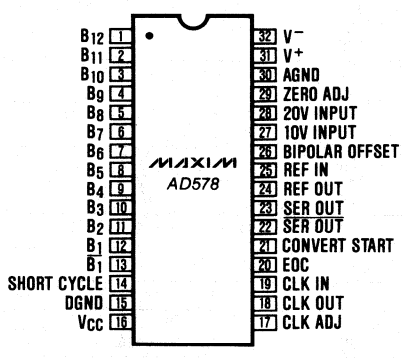
Ordering Information

PART	TEMP. RANGE	PACKAGE
AD578JN	0°C to +70°C	32 Lead Ceramic DIP
AD578KN	0°C to +70°C	32 Lead Ceramic DIP
AD578LN	0°C to +70°C	32 Lead Ceramic DIP
AD578SN	-55°C to +125°C	32 Lead Ceramic DIP
AD578TN	-55°C to +125°C	32 Lead Ceramic DIP

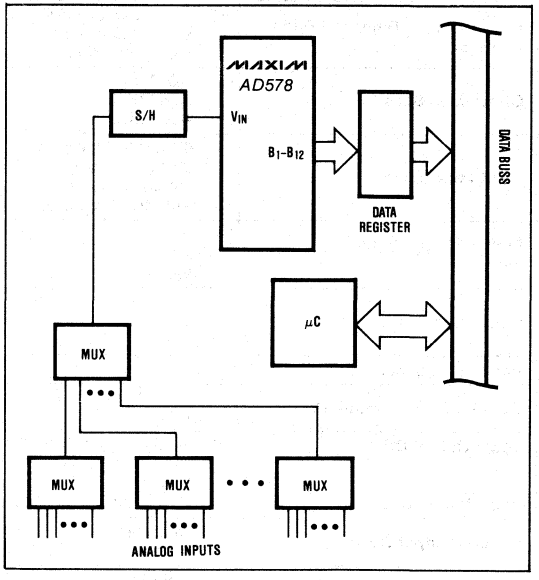
For ±12V Supplies, Order AD578ZXX
(For Hermetic Seal (D) Please Contact Factory.)

Pin Configuration

Top View



Typical Operating Circuit



High Speed 12 Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage, V^+ (pin 31 to GND) ..... +18V
Negative Supply Voltage, V^- (pin 32 to GND) ..... -18V
Digital Supply Voltage, V_{CC} (pin 16 to GND) ..... +7V
Digital Input Voltage
(pins 14, 17, 19, 21) ..... GND - 0.5V ≤ V_{IN} ≤ V_{CC} + 0.5V
Analog GND to Digital GND ..... ±0.5V

Analog Inputs (pins 25, 26, 27) ..... ±12V
(pins 28, 29) ..... ±24V
Ref Out ..... Indefinite Short to AGND
Momentary Short to V^+
Power Dissipation ..... 2W @ 100°C
Storage Temperature ..... -65°C ≤ T_A ≤ +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = -15V, V_{CC} = +5V, T_A = +25°C, unless noted—Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Offset (Note 1)	Unipolar, T_A = 25°C		±0.1	±0.25	%FSR
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J,T		±3	±10	ppm/°C
	AD578S		±3	±15	ppm/°C
	Bipolar (Note 1, 2), T_A = 25°C		±0.1	±0.25	%FSR
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J,T		±8	±20	ppm/°C
	AD578S		±8	±25	ppm/°C
Gain Error (Note 1, 3)	T_A = 25°C		±0.1	±0.25	%FSR
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J,T		±15	±30	ppm/°C
	AD578S		±15	±50	ppm/°C
Linearity	T_A = 25°C			½	LSB
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J		¾		
	AD578S,T			¾	
Differential Linearity Error	$T_{MIN} \le T_A \le T_{MAX}$	no missing codes			
Differential Linearity Drift	$T_{MIN} \le T_A \le T_{MAX}$		±2		ppm/°C
Reference Voltage Accuracy	$V_{nominal}$ = 10.000V		±10	±100	mV
Reference Voltage Drift	$T_{MIN} \le T_A \le T_{MAX}$		±10	±30	ppm/°C
Reference Output Current		±1			mA
Power Supply Rejection Ratio (Note 5)	V^+ = +13.5 to +16.5V			0.005	%/%ΔV
	V^- = -13.5 to -16.5V			0.005	
	V_{CC} = +4.5 to +5.5V			0.005	
Conversion Speed	AD578L	3.0			µs
	AD578K,T	4.5			
	AD578J,S	6.0			
Input Impedance	0V to +10V range		5		kΩ
	0V to +20V range		10		
	-5V to +5V range		5		
	-10V to +10V range		10		
Power Supply Range (Note 5)	V^+	13.5		16.5	V
	V^-	-13.5		-16.5	
	V_{CC}	4.75		5.25	
Power Supply Current	V^+		11	15	mA
	V^-		21	35	
	V_{CC}		45	80	
Power Dissipation			0.7	1.15	W
Operating Temperature Range	AD578L,K,J	0		+70	°C
	AD578S,T	-55		+125	
Logic Output Drive	B_1-B_{12}, $\overline{B_1}$, CLOCK OUT		2		LS TTL Loads
	SER OUT, $\overline{\text{SER OUT}}$		2		
	EOC		8		
Logic Input Load	CLOCK IN, CONVERT START		1		
Parallel Output Code	Unipolar	Binary			
	Bipolar	Offset Binary/Two's Complement			
Serial Output Code	Unipolar	Binary/Complementary Binary			
	Bipolar	Offset Binary/Complementary Offset Binary			

Note 1: Adjustable to zero.
Note 2: 50Ω, 1% resistor between pins 24 and 26.
Note 3: 50Ω, 1% resistor between pins 24 and 25.
Note 4: AD578ZXX models, V^+ = +12V, V^- + -12V
Note 5: 'Z' models, V+ = 11.6V to 12.6V,
V^- = -11.6V to -12.6V

High Speed 12 Bit A/D Converter

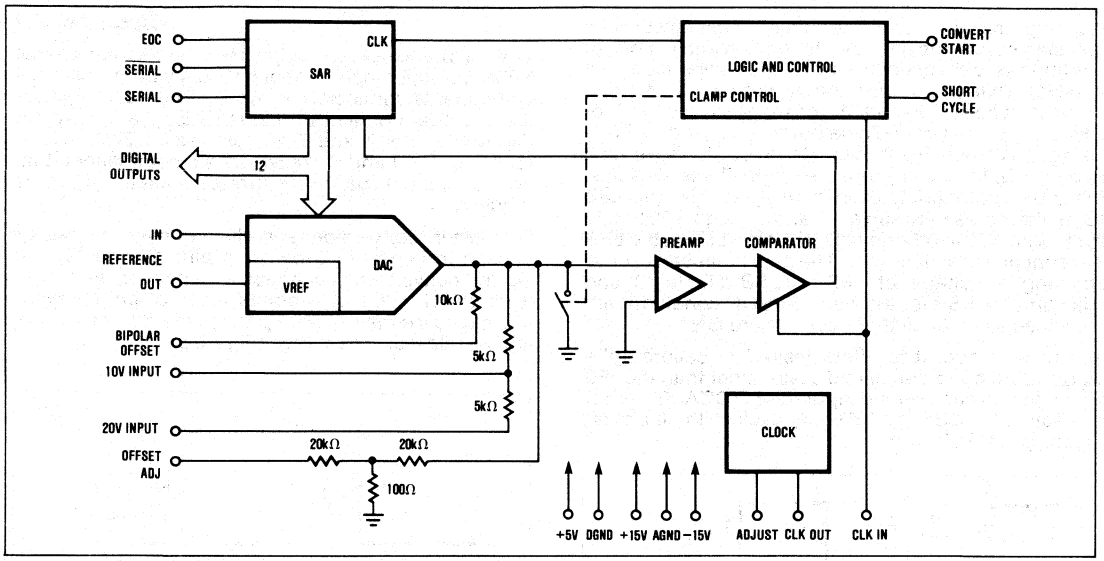


Figure 1. Maxim AD578 Block Diagram.

Detailed Description

The AD578 is a 12-bit successive approximation A/D converter in which the analog input is compared to the output of a high speed D/A converter (Figure 1). The D/A is binarily stepped until its output matches the analog input. The digital code from the successive approximation register (SAR) appears on the outputs as the binary value of the input voltage. The conversion processs consists of twelve successive tests, starting with the D/A set to half Full Scale (FS). The comparator determines whether the D/A output is higher or lower than the analog input and either sets or resets Bit 1 (MSB). On the next test, the D/A is incremented up or down ¼ FS, based on the last decision, and is again compared to the input. The result is stored as BIT 2. Each comparator decision is clocked into the SAR for the remaining bits until all twelve have been tested.

A positive going pulse on Convert Start resets the D/A Converter to ½ FS and sets the End-Of-Convert (EOC) high indicating that a conversion is in progress (Figure 7). The internal clock is enabled and the conversion begins on the trailing edge of the Start Convert (S) pulse. After the last bit has been tested, EOC goes LOW indicating that the output data is valid.

Calibration Procedure

For a large number of AD578 applications no user calibration is needed. The performance limits for an uncalibrated device are given in the Electrical Characteristics section. If more precision is required then offset and gain adjustments can be made as follows.

Table 1. Calibration Chart

	ANALOG INPUT VOLTAGE				OUTPUT CODE(1)	
	0 TO +10V	0 TO +20V	-5 TO +5V	-10 TO +10V	MSB	LSB
+FS -1LSB	+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1	1 1 1 1 1 1 1 1
+FS -1½LSB	+9.9964	+19.9927	+4.9964	+9.9927	1 1 1 1	1 1 1 1 1 1 1@
Mid Scale +½LSB	+5.0012	+10.0024	+0.0012	+0.0024	1 0 0 0	0 0 0 0 0 0 0@
Mid Scale	+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0	0 0 0 0 0 0 0 0
-FS +½LSB	+0.0012	+0.0024	-4.9988	-9.9976	0 0 0 0	0 0 0 0 0 0 0@
-FS	+0.0000	+0.0000	-5.0000	-10.0000	0 0 0 0	0 0 0 0 0 0 0 0

Note 1: The symbol "@" indicates a 0 or 1 with equal probability.

High Speed 12 Bit A/D Converter

Keeping in mind that the offset must always be adjusted before the gain, set the system into a mode of continuous conversions with a high repetition rate (>1kHz) while monitoring the output data lines using an oscilloscope, logic analyzer triggered on EOC, or LED's driven by latched data outputs clocked by EOC. Using a DVM, set the input voltage ½ LSB above -Full Scale (-FS) for the appropriate range (Table 1). Adjust the offset potentiometer (Figure 2) so that the LSB (B_{12}) alternates between a "0" and "1" with a 50% duty cycle with all the other bits OFF. Using LED's, the LSB will appear at half intensity. The gain is similarly set by applying a voltage of +FS -1½LSB (Table 1) and adjusting the LSB for the same 50% ON condition with the exception that all the other bits are ON.

In bipolar mode, it is often desired to calibrate the bipolar zero condition at mid scale rather than the -FS offset. In this case set the input to MID SCALE +½LSB and adjust the LSB for 50% duty cycle with all bits off except B_1 (MSB).

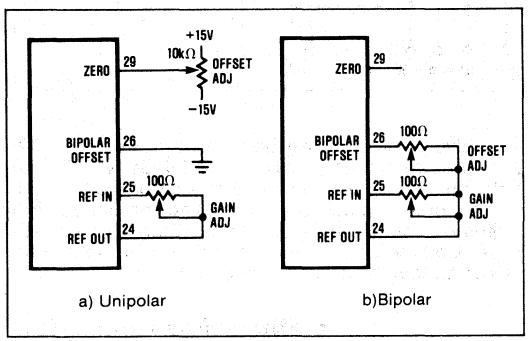


Figure 2. Unipolar and Bipolar Calibration Circuit.

Clock Adjust

The internal clock on all grades is set for a nominal 5.8μs with tolerance of about +0.2μs with no external components connected to pin 17. To obtain 3.0μs for the L grade, connect an 825Ω resistor as shown in Figure 5(a). For K and T grades, use a 3.3kΩ resistor for 4.5μs. For J and S grades, it is recommended that no adjustment be made unless exactly 6.0μs is required.

For faster conversion speeds, connect a resistor chosen from Figure 3 between pins 17 and 18. For slower conversions, connect a capacitor, Figure 4, from pin 17 to GND. A combination of both resistor and capacitor maybe used particularly for fine adjustment of slow clock settings (Figure 5).

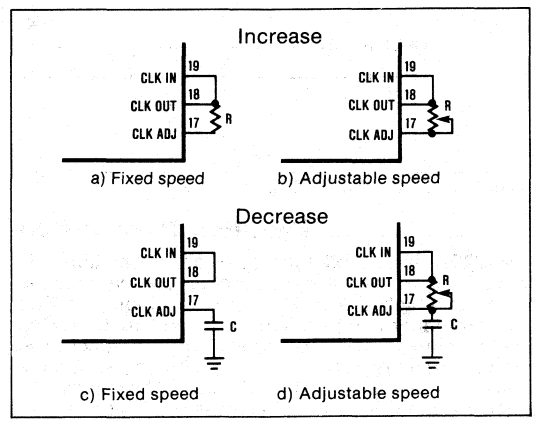


Figure 5. Adjusting the Internal Clock.

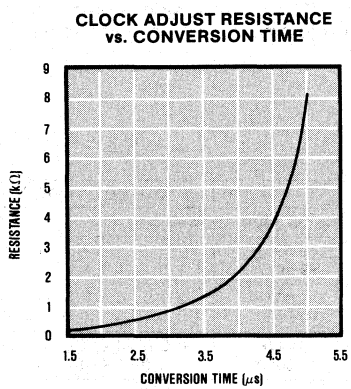


Figure 3. Speed vs. Resistance.

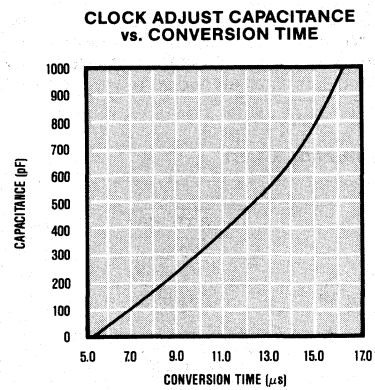


Figure 4. Speed vs. Capacitance.

High Speed 12 Bit A/D Converter

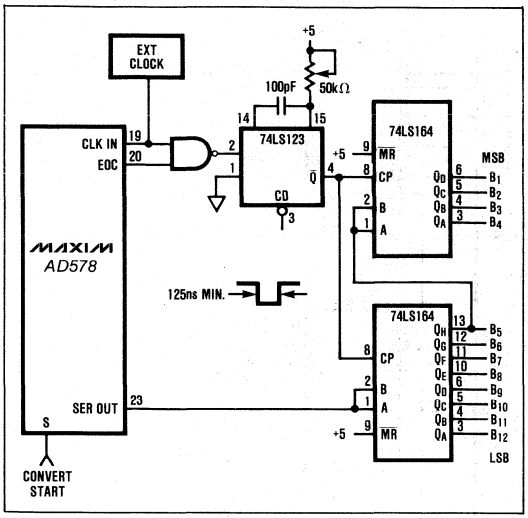
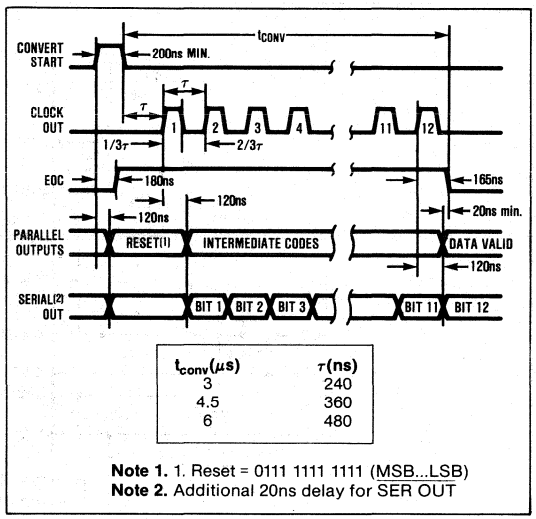


Figure 6. Serial Output with External Clock.



t_{conv}(μs)	τ(ns)
3	240
4.5	360
6	480

Note 1. 1. Reset = 0111 1111 1111 (MSB...LSB)
Note 2. Additional 20ns delay for SER OUT

Figure 7. Timing Diagram.

Short Cycle

For conversions of less than 12 bits, SHORT CYCLE, pin 14, must be connected to the next higher bit than the desired resolution. For example, connecting pin 14 to pin 2 will result in 10 bit conversions. When using an external clock, EOC must also be used to inhibit the CLK IN.

External Clock

The external clock can be used for synchronous applications, such as clocking the serial output data into a serial-to-parallel shift register (Figure 6). The clock should have a duty cycle between 30% and 70%. The main advantage of serial transmission is the reduction in the number of output lines from 12 to 1, which is particularly useful when using optical couplers or sending data over long distances.

Application Hints

Layout

The Analog and Digital Grounds should be directly connected together as close as possible to the package and then tied to a quiet analog ground with no switching transients taking place during the conversion. A ground plane works best, but is not necessary if large traces are used. It is advisable to filter the supplies with 10μF electrolytic capacitors on the PC board along with 0.1μF bypassing capacitors as close to the supply pins on the AD578 as possible. Above all, separate the analog circuit connections, pins 24 through 32, away from the digital section. If a digital signal must cross an analog connection, make sure it crosses at a ninety degree angle on different sides of the board if at all possible.

If using only the 20V input range, leave the 10V input (pin 27) completely unconnected since capacitance on this high impedance point can degrade dynamic performance. When relays or switches are used, mount them as close to the input pins as possible.

Although not necessary to achieve rated specifications, it is recommended that a 10μF electrolytic capacitor be connected on REF OUT to GND for improved noise on the code transitions.

Interfacing

The digital outputs of the AD578 should be latched since they are constantly changing during the conversion. Edge triggered, rather than transparent latches are preferred, such as the 74LS574 (Figure 8), to prevent changing data lines feeding back into the analog portions of the A/D converter. Capacitive loading above 30pF as well as connections more than a few inches long should be avoided on the digital outputs of the A/D.

Input Signal Conditioning

The analog input should be driven by a wide bandwidth, low output impedance op amp or a fast sample-hold. Although V_{IN} may not change during the conversion, the load current of the A/D abruptly changes with each clock cycle due to successive DAC codes (Figure 1). The amplifier must recover to the original value in time for the rest of the circuit to settle before the comparator can make a decision. An op amp which can settle to 0.01% in 50 to 100ns for a 0.5mA change in load current with no thermal tail and low offset voltage drift is recommended.

High Speed 12 Bit A/D Converter

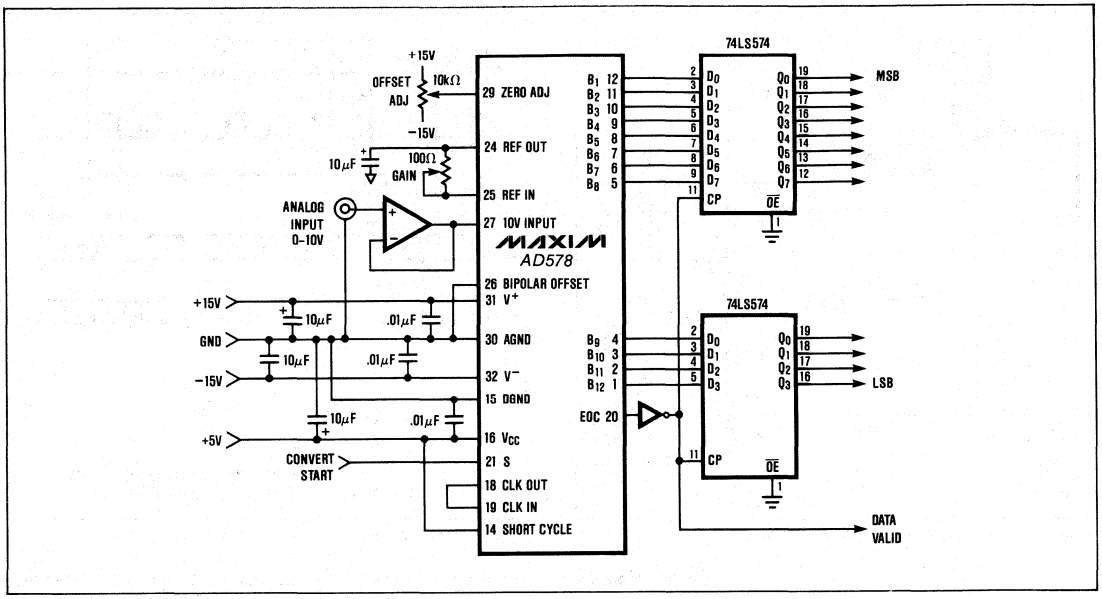


Figure 8. Typical Application for Unipolar 0-10V Range.

CMOS High Speed A/D Converter with Track/Hold Function

General Description

The ADC0820 is a high speed, microprocessor compatible, 8 bit analog-to-digital converter which uses a half-flash technique to achieve a conversion time of 1.4 μs. The converter has a 0V to +5V analog input range and uses a single +5V supply.

A built-in track-and-hold function is included, eliminating the need for an external track-and-hold for input slew rates up to 100mV/μs.

The A/D easily interfaces with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. Data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system I/O port. An over-flow output is also provided for cascading devices to achieve higher resolution.

Maxim's ADC0820 is pin-compatible with National Semiconductor's ADC0820 and provides improved specifications. It is packaged in 20-pin DIP and Small Outline packages.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Loops
Audio Systems

Features

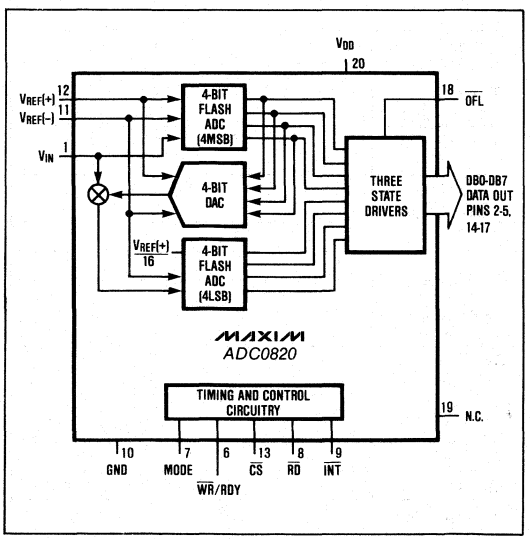
- **Fast Conversion Time: 1.4μs Max.**
- **Built-in Track-and-Hold Function**
- **No Missing Codes**
- **No User Adjustments Required**
- **Single +5V Supply**
- **No External Clock**
- **Easy Interface To Microprocessors**

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
ADC0820BCN	0° C to +70° C	Plastic	±½ LSB
ADC0820CCN	0° C to +70° C	Plastic	±1 LSB
ADC0820CC/D	0° C to +70° C	Dice	±1 LSB
ADC0820CCM	0° C to +70° C	Small Outline	±1 LSB
ADC0820BCJ	-40° C to +85° C	CERDIP	±½ LSB
ADC0820CCJ	-40° C to +85° C	CERDIP	±1 LSB
ADC0820BJ	-55° C to +125° C	CERDIP	±½ LSB
ADC0820CJ	-55° C to +125° C	CERDIP	±1 LSB

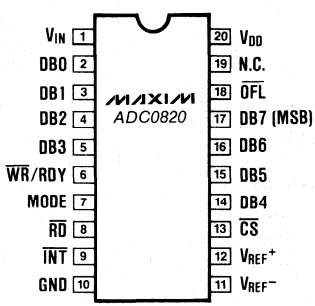
** All devices — 20 lead packages.*

Functional Block Diagram



Pin Configuration

Top View



CMOS High Speed A/D Converter with Track/Hold Function

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins
(Pins 1-9, 11-19) ..... GND - 0.3V, V_{DD} +0.3V
Output current (Pin 19) 30mA
Power Dissipation (Any Package) to +75°C 450mW
Derate Above +25°C by ..... 6mW/°C

Operating Temperature Ranges
ADC0820CCN/BCN/CCM ..... 0°C to +70°C
ADC0820BCJ/CCJ ..... -40°C to +85°C
ADC08020BJ/CJ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		ADC0820B ADC0820C			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
REFERENCE INPUT						
Reference Resistance		T_A = +25°C T_A = T_{MIN} to T_{MAX}	1.4 1.25	2.2	4.0 4.0	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD} + 0.1	V
V_{REF}^- Input Voltage Range			GND - 0.1		V_{REF}^+	V
ANALOG INPUT						
Analog Input Voltage Range	V_{INR}		GND - 0.1		V_{DD} + 0.1	V
Analog Input Capacitance	C_{VIN}			45		pF
Analog Input Current	I_{VIN}	V_{IN} = 0V to +5V; T_A = +25°C; T_{MIN} to T_{MAX}			±0.3 ±3	μA
Slew Rate, Tracking (Note 2)	SR			0.2	0.1	V/μs
LOGIC INPUTS						
Input HIGH Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE	2.0 3.5			V
Input LOW Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE			0.8 1.5	V
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$; T_A = +25°C; T_{MIN} to T_{MAX}			0.1 1	μA
		$\overline{WR}$; T_A = +25°C; T_{MIN} to T_{MAX}			0.3 3	
		MODE; T_A = +25°C; T_{MIN} to T_{MAX}		50	150 200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE; T_A = 25°C; T_{MIN} to T_{MAX}			-0.3 -1	μA
Input Capacitance (Note 3)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$ V_{DD} = +4.75V; I_{OUT} = -360μA V_{DD} = +4.75V; I_{OUT} = -10μA	4.0 4.5			V
Output LOW Voltage	V_{OL}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY V_{DD} = +4.75V; I_{OUT} = 1.6mA			0.4	V
Three-state Output Current		DB0-DB7, RDY; T_A = +25°C; T_{MIN} to T_{MAX}	-0.3 -3		+0.3 +3	μA
Output Capacitance (Note 3)	C_{OUT}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		5	8	pF
Output Source Current	I_{SRC}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$; V_{OUT} = 0		-25	-10	mA
Output Sink Current	I_{SINK}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{OUT} = V_{DD}		40	15	mA

CMOS High Speed A/D Converter with Track/Hold Function

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY						
Supply Voltage	V_{DD}	±5% for Specified Performance		5		V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 T_A = +25°C T_{MIN} to T_{MAX}		5	10 15	mA
Power Dissipation		$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0		25		mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. See Note 2, 4.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			ADC0820BCX ADC0820CCX		ADC0820BJ ADC0820CJ		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R = 3kΩ		35	70		90		100	ns
Conversion Time (RD Mode)	t_{CRD}	(Note 7)		1.2	1.6		2.0		2.5	μs
Data Access Time (RD Mode) (See Figure 1)	t_{ACC0}	(Note 5)		t_{CRD} + 10	t_{CRD} + 35		t_{CRD} + 50		t_{CRD} + 70	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		60	125		175		225	ns
Data Hold Time	t_{DH}	(Note 6)		40	90		120		150	ns
Delay Time Between Conversions	t_P		500			600		600		ns
Write Pulse Width	t_{WR}		600		50,000	600	50,000	600	50,000	ns
Conversion Time (WR-RD Mode)	t_{CWR-RD}		1.4			1.56		1.62		μs
Delay between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		600			700		700		ns
Data Access Time (WR-RD Mode) (See Figure 3)	t_{ACC1}	$t_{RD} < t_{INTL}$		110	220		280		350	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}			100	200		260		320	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}			600	1000		1400		1700	ns
Data Access Time (WR-RD Mode) (See Figure 2)	t_{ACC2}	$t_{RD} > t_{INTL}$, (Note 6)		60	100		130		160	ns
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone)	t_{IHWR}	C_L = 50pF		70	100		130		150	ns
Data Access Time After $\overline{INT}$	t_{ID}			10	50		65		75	ns

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Sample tested at +25°C by Quality Assurance to ensure compliance.
Note 3: Guaranteed by design.
Note 4: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 5: Defined as the time required for an output to cross 0.8V or 2.4 V.
Note 6: Defined as the time required for the data lines to change 0.5V.
Note 7: For faster conversions use WR-RD Mode.

CMOS High Speed A/D Converter with Track/Hold Function

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog input; range = GND < V_{IN} < V_{DD}.
2	DB0	Three-state data output, bit 0 (LSB).
3	DB1	Three-state data output, bit 1.
4	DB2	Three-state data output, bit 2.
5	DB3	Three-state data output, bit 3.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode selection input. This input is internally pulled low with a 50μA current source. RD Mode: MODE low/open. WR-RD Mode: MODE high.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
10	GND	Ground.
11	V_{REF}^-	Lower limit of reference span. Sets the zero code voltage. Range: GND to V_{REF}^+.
12	V_{REF}^+	Upper limit of reference span. Sets the Full Scale input voltage. Range: V_{REF}^- to V_{DD}.
13	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs
14	DB4	Three-state data output, bit 4.
15	DB5	Three-state data output, bit 5.
16	DB6	Three-state data output, bit 6.
17	DB7	Three-state data output, bit 7 (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is greater than V_{REF}^+, $\overline{OFL}$ will be high at the end of the conversion. It can be used to cascade two or more devices to increase resolution.
19	N.C.	Test Pin. Do not connect.
20	V_{DD}	Power supply voltage, +5V.

Digital Interface

RD Mode (Pin 7 Low)

A conversion is started by taking $\overline{RD}$ low and keeping it low until output data appears (Figure 1). Pin 6 ($\overline{WR}$/RDY) is configured as a status output (RDY) in this mode, and is used with microprocessors which can be forced into a WAIT state. The processor starts a conversion, waits, and then reads data with a single READ instruction. RDY, an open collector output, goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of the conversion. $\overline{INT}$ goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

WR-RD Mode (Pin 7 High)

In the WR-RD mode, pin 6 ($\overline{WR}$/RDY) is the WRITE input for the converter. With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{WR}$. There are several options for reading data:

Using the Internal Delay

The processor waits for $\overline{INT}$ to go low before reading data (Figure 2). $\overline{INT}$ typically goes low 600ns after the rising edge of $\overline{WR}$, indicating that the conversion is complete. With $\overline{CS}$ low, DB0-DB7 are read by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Reading Before Delay

The conversion time is externally controlled with $\overline{RD}$ (Figure 3). The status of $\overline{INT}$ is ignored and $\overline{RD}$ is taken low as soon as 600ns after the rising edge of $\overline{WR}$. This completes the conversion and enables DB0-DB7. $\overline{INT}$ goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$.

Pipelined Operation

"Pipelined" operation is achieved by tying $\overline{WR}$ and $\overline{RD}$ together (Figure 4). With $\overline{CS}$ low, taking $\overline{WR}$ and $\overline{RD}$ low starts a new conversion and, at the same time, reads the result of the previous conversion.

Stand-Alone Operation

In stand-alone operation, $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by pulling $\overline{WR}$ low (Figure 5). Output data is valid approximately 600ns after the rising edge of $\overline{WR}$.

Analog Considerations

Reference Input

The $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the converter set the full-scale and zero input voltages. The voltage at $V_{REF}(-)$ defines the input level which produces an output code of all zeroes, and the voltage at $V_{REF}(+)$ defines the input which produces an output code of all ones (see Figure 6). Figure 7 shows some reference configurations.

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. The lead length of these capacitors should be as short as possible. If the reference inputs (pins 11, 12) are driven by long lines, they also should be bypassed to GND with 0.1 μF capacitors at the reference input pins.

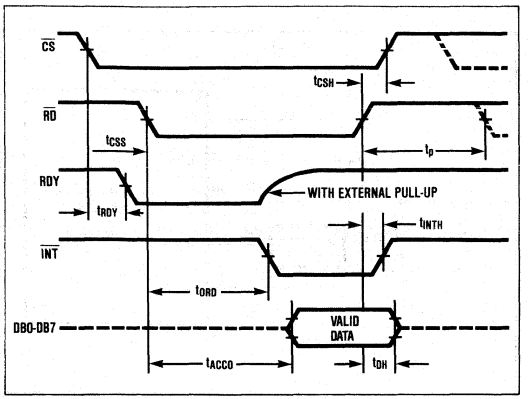


Figure 1. RD Mode Timing

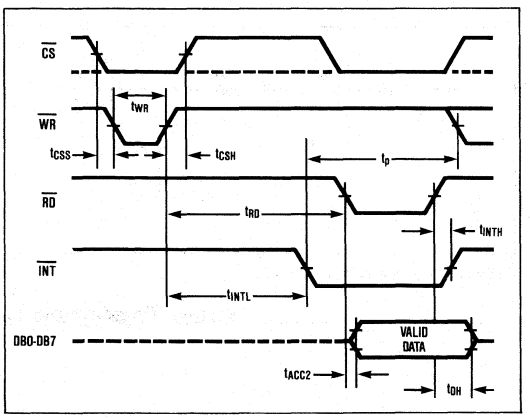


Figure 2. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

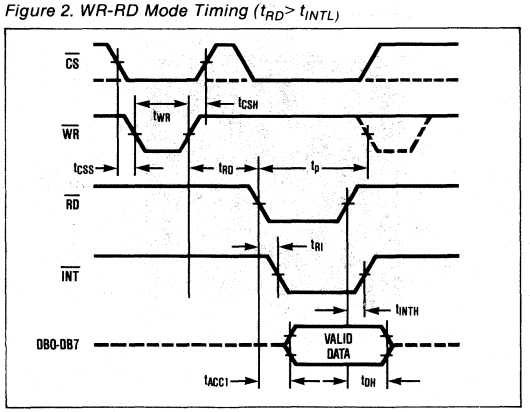


Figure 3. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

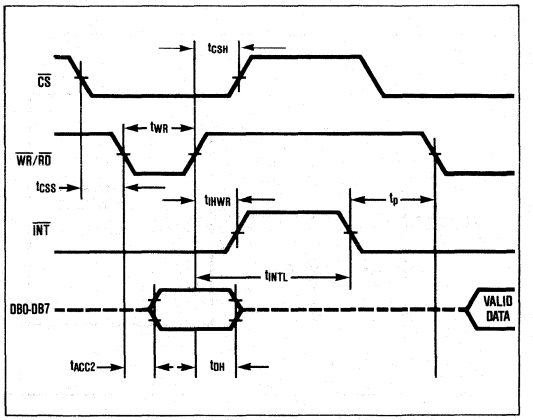


Figure 4. WR-RD Mode Pipe-Lined Timing, $\overline{WR} = \overline{RD}$

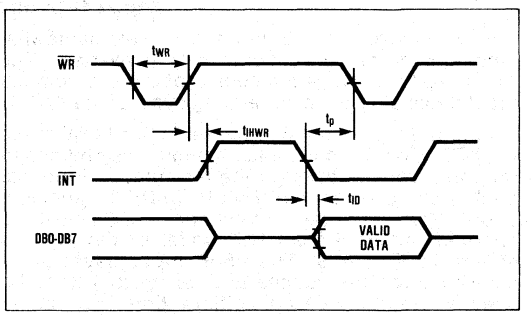


Figure 5. WR-RD Mode Stand-Alone Timing, $\overline{CS} = \overline{RD} = 0$

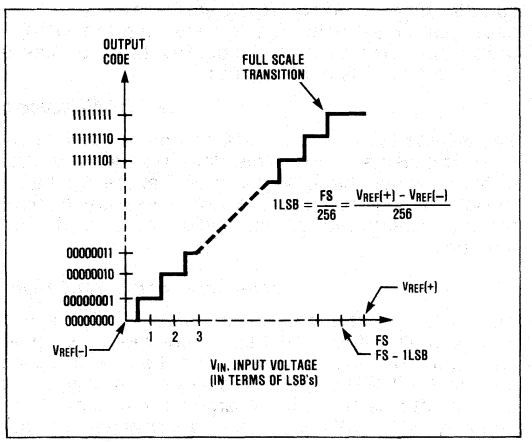


Figure 6. Transfer Function

CMOS High Speed A/D Converter with Track/Hold Function

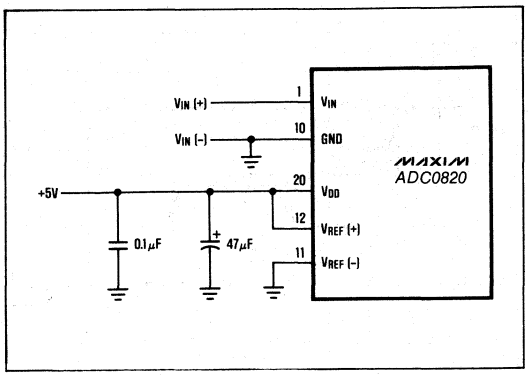


Figure 7a. Power Supply as Reference

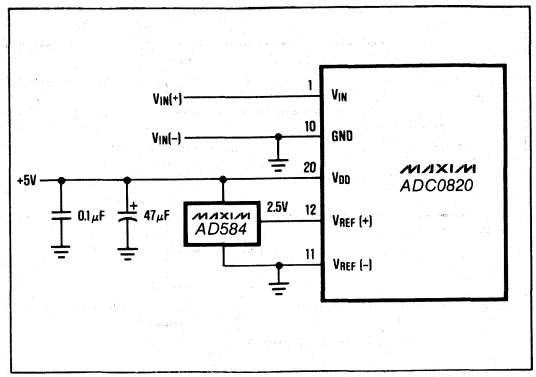


Figure 7b. External Reference 2.5V Full Scale

Input Current

The ADC0820 analog input behaves somewhat differently from conventional A/D converters. The ADC0820 takes varying amounts of current from the input depending on the operating cycle of the A/D.

During the input sampling phase ($\overline{WR}$ = LOW in the (WR-RD Mode) input capacitors must be charged to the input voltage through the resistance of internal analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of stray capacitance (C_S) must be charged. An equivalent RC model of the input is shown in Figure 8. The 45pF input capacitance allows source resistances (R_S) of up to 1kΩ to be used without increased settling time. For larger resistances, the width of the $\overline{WR}$ pulse must be increased from 600ns. In the RD mode, where the sample time is fixed, R_S greater than 1kΩ may cause settling errors. In this case, use the WR-RD mode and greater than 600ns $\overline{RD}$ time, or use a buffer to drive the analog input.

Input Filtering

The ADC0820's sampled data comparators generate input transients at V_{IN}. This does not degrade performance since the A/D only "looks" at the input after these transients occur. It is not necessary to filter these transients with an external capacitor at the V_{IN} terminal.

Inherent Track-and-Hold

The ADC0820 can measure a variety of high speed input signals without the help of an external sample-and-hold. The input is tracked from the time $\overline{WR}$ goes low (in the WR-RD mode) to approximately 100ns after it returns high. Input signals with slew rates typically up to 200mV/μs can be converted without error.

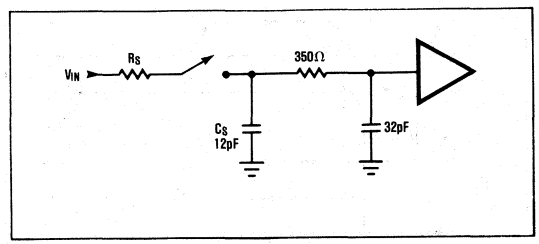
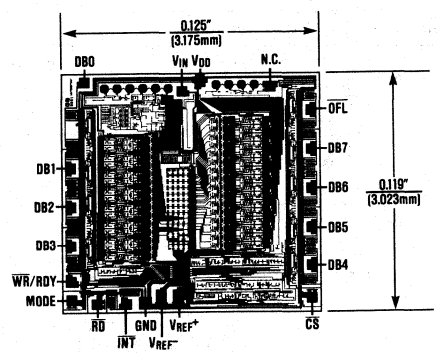


Figure 8. Equivalent Input Model

Chip Topography



MAXIM

3½ Digit A/D Converter

General Description

The Maxim ICL7106 and ICL7107 are monolithic analog to digital converters. They have very high input impedances and require no external display drive circuitry. On-board active components include polarity and digit drivers, segment decoders, voltage reference and a clock circuit. The ICL7106 will directly drive a non-multiplexed liquid crystal display (LCD) whereas the ICL7107 will directly drive a common anode light emitting diode (LED) display.

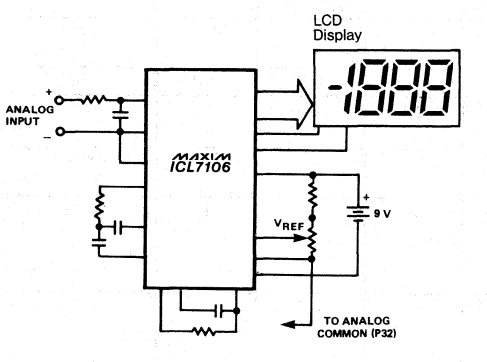
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7106 and ICL7107, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

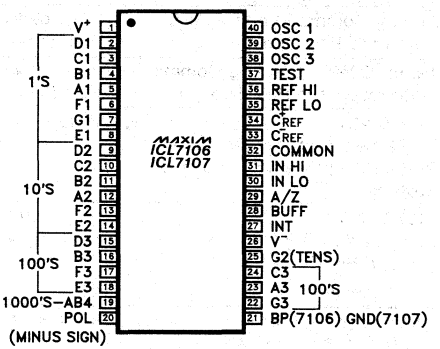
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™")**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required**
  LCD-ICL7106
  LED-ICL7107
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **True Differential Reference and Input**
- **True Polarity Indication for Precision Null Applications**
- **Monolithic CMOS design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7106CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7106CJL	0°C to +70°C	40 Lead CERDIP
ICL7106CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7106C/D	0°C to +70°C	Dice
ICL7107CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7107CJL	0°C to +70°C	40 Lead CERDIP
ICL7107CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7107C/D	0°C to +70°C	Dice

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Plastic Package 1000mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- supply current 7107 only			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{CLOCK} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

3½ Digit A/D Converter

- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 7)**
- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Negligible Hysteresis**
- **Maxim Quality and Reliability**
- **Increased Maximum Rating for Input Current (Note 8)**

ABSOLUTE MAXIMUM RATINGS:

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS:

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1; unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 6)	−000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**−000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 6)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV				
	T_A = 25°C (Note 6)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ 70°C (Note 10)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 6)		1	10	pA
	0° ≤ T_A ≤ 70°C		**20**	**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0				
	T_A = 25°C		0.6	1.8	mA
	0° ≤ T_A ≤ 70°C			**2**	
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply		75		ppm/°C
7106 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7107 Only—Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment Voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA
7106 Only—Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	**V**
Overload Recovery Time (Note 9)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	**Measurement Cycles**

Note 6: Test condition is V_{IN} applied between pin IH-HI and IN-LO through a 1MΩ series resistor as shown in Figures 1 and 2.

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 9: Number of measurement cycles for display to give accurate reading.

Note 10: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter

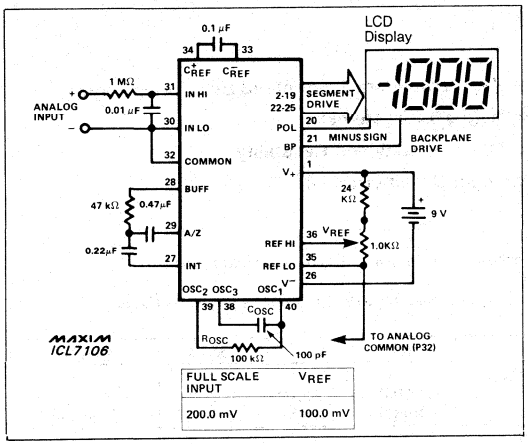


Figure 1. Maxim ICL7106 Typical Operating Circuit

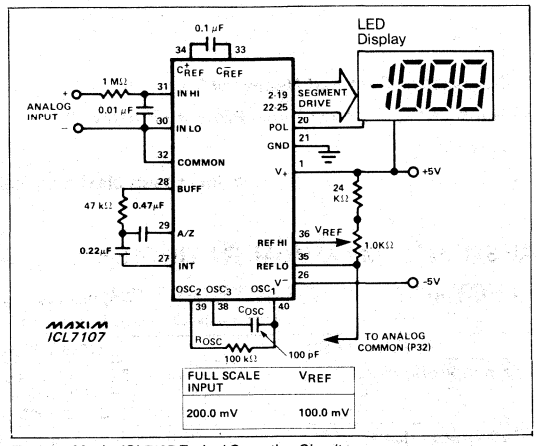


Figure 2. Maxim ICL7107 Typical Operating Circuit

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" overrange conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a rollover voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This happens during de-integration of a positive signal. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifer can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical

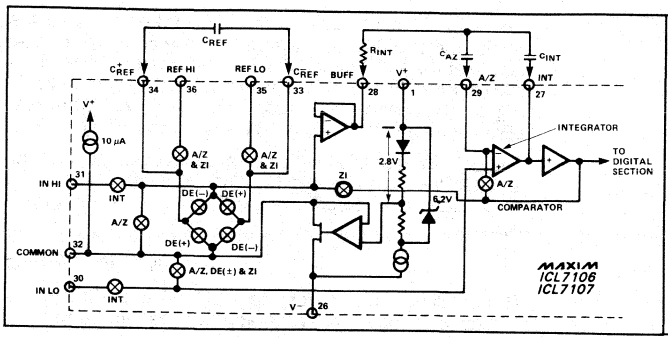


Figure 3. Analog Section of ICL7106/ICL7107

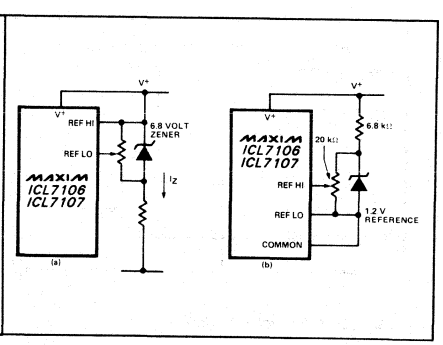


Figure 4. Using an External Reference

applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful when using the ICL7106, or for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The analog common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80ppm/°C, and a low voltage coefficient (.001%).

The internal heating of the ICL7107 by the LED display drivers degrades the stability of Analog Common. The power dissipated by the LED display drivers changes with the displayed count, thereby changing the temperature of the die, which in turn results in a small change in the Analog Common voltage. This combination of variable power dissipation, thermal resistance, and temperature coefficient causes a 25–80μV increase in noise near full scale. Another effect of LED display driver power dissipation can be seen at the transition between a full scale reading and an overload condition. Overload is a low power dissipation condition since the three least significant digits are blanked in overload. On the other hand, a near full scale reading such as 1999 has many segments turned on and is a high power dissipation condition. The difference in power dissipation between overload and full scale may cause a ICL7107 with a negative temperature coefficient reference to cycle between overload and a near full scale display as the die alternately heats and cools. An ICL7107 with a positive TC reference will exhibit hysteresis under these conditions: once put into overload by a voltage just barely more than full scale, the voltage must be reduced by several counts before the ICL7107 will come out of overload.

None of the above problems are encountered when using an external reference. The ICL7106, with its low power dissipation, has none of these problems with either an external reference or when using Analog Common as a reference.

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from analog-common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, REF-LO should be connected to analog common. This will remove the common-mode voltage from the reference system.

Analog Common is internally tied to an N-channel FET that can sink 30mA or more of current. This will hold the Analog Common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 10μA of source current, however, so COMMON may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD if left in this mode for several minutes.

3½ Digit A/D Converter

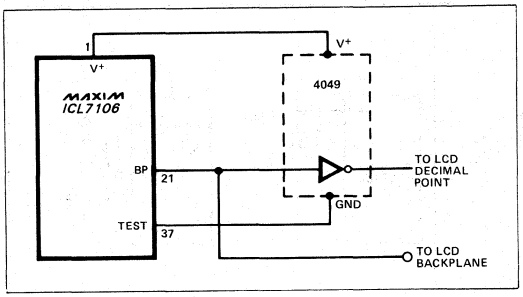


Figure 5A. Fixed Decimal Point Drivers

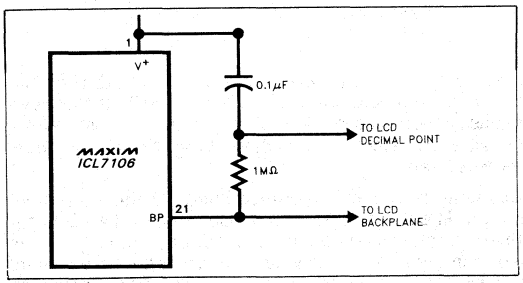


Figure 5B. Fixed Decimal Point Drivers

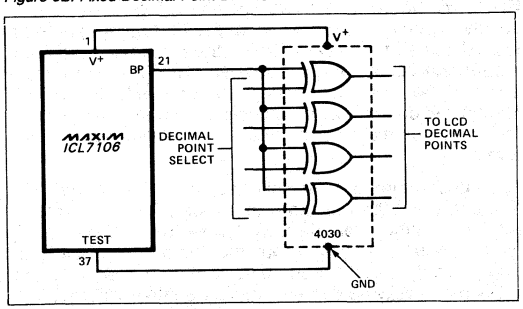


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Digital Section

The digital section for the ICL7106 and ICL7107 is illustrated in Figures 8 and 9. In Figure 8, an internal digital ground is generated from a 6V zener diode and a large P-channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the segment is ON and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The ICL7107 is identical to the ICL7106 except that the backplane and drivers have been replaced by N-channel segment drivers. The ICL7107 is designed to drive common anode LED's with a typical segment current of 8mA. Pin 19 (thousands digit output) sinks current from two LED segments, and has a 16mA drive capability.

The polarity indication is "on" for negative analog inputs, for both the ICL7106 and ICL7107. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7106 and ICL7107 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 30kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 48kHz would be used to obtain three readings per second.

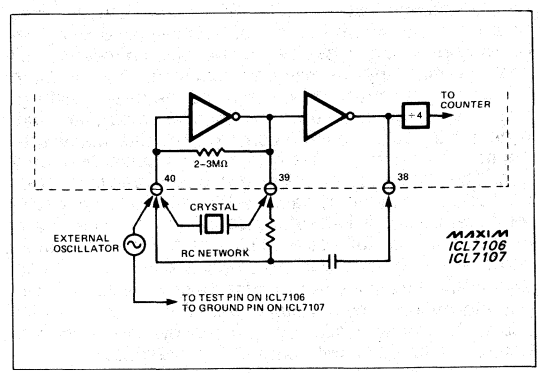


Figure 7. Clock Circuits

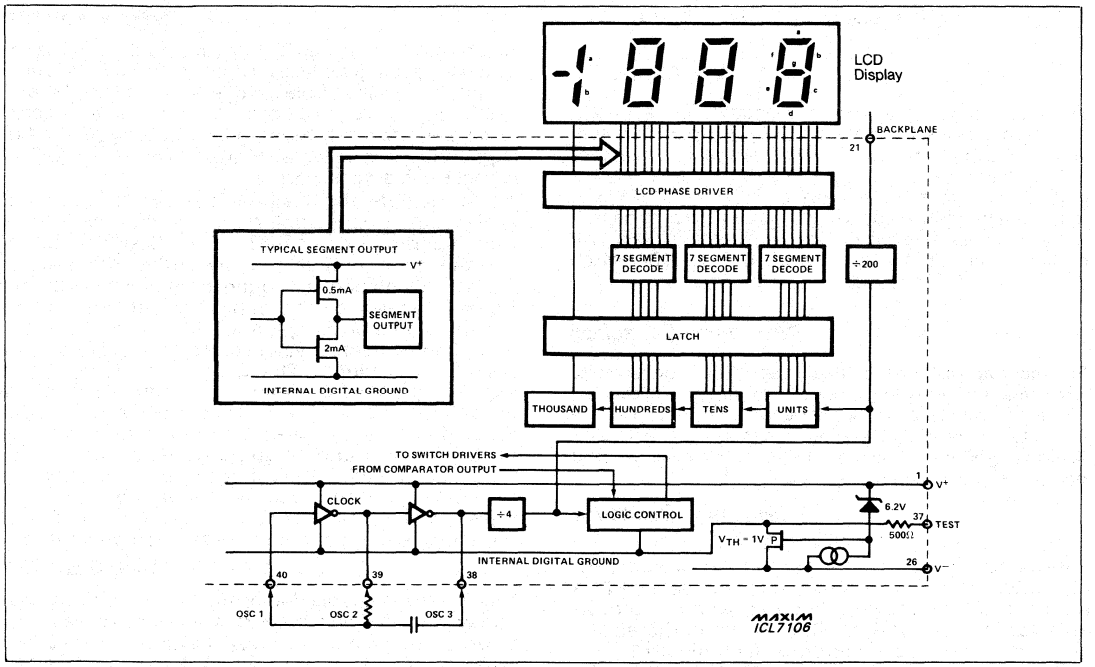


Figure 8. ICL7106 Digital Section

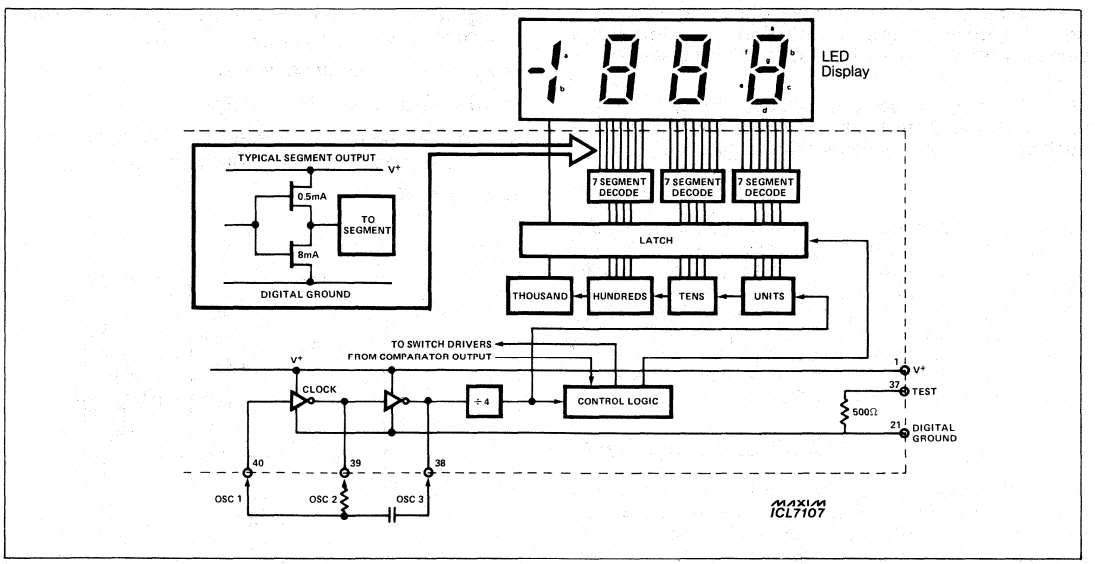


Figure 9. ICL7107 Digital Section

3½ Digit A/D Converter

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For the 2V scale, a 0.047μF capacitor is adequate. A capacitor size of 0.47μF is recommended for 200mV full scale where low noise operation is very important. Due to the ZI phase of Maxim's ICL7106/7, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems seen in other manufacturers' ICL7106/7 which do not have the ZI phase.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent rollover error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (at approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable for the ICL7106 or ICL7107 when the analog common is used as a reference. A nominal ±3.5 to 4 volt swing is acceptable for the ICL7107 with a ±5V supply and analog common tied to supply ground. The nominal values for C_{INT} is 0.22μF for three readings per second. (48kHz clock). These values should be changed in inverse proportion to maintain the same output swing if different oscillator frequencies are used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100μA of quiescent current. 20μA of drive current can be supplied with negligible non-linearity. This resistor should be large enough to maintain the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 47KΩ resistor is recommended; (2V scale/470KΩ).

Oscillator Components

A 100KΩ resistor is recommended for all ranges of frequency. By using the equation f = 0.45/RC, the capacitor value can be calculated. For 48kHz clock, (3 readings/second), the oscillator capacitor plus stray capacitance should equal 100pF.

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. Suitable values of the capacitor and integrating resistor would be 0.22μF and 120KΩ. This provides for a slightly quieter system and also avoids a divider network on the input. The ICL7107 can accept input signals up to ±3.5V with ±5V supplies. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset reading can be conveniently generated.

ICL7107 Power Supplies

The ICL7107 is designed to operate from ±5V supplies. However, when a negative supply is not available it can be generated from a clock output with two diodes, two capacitors, and an inexpensive IC. Refer to Figure 10. Alternatively a −5V supply can be generated using Maxim's ICL7660 and two capacitors.

A negative supply is not required in selected applications. The conditions to use a single +5V supply are:

- An external reference is used.
- The signal is less than ±1.5V.
- The input signal can be referenced to the center of the common-mode range of the converter.

See Figure 18.

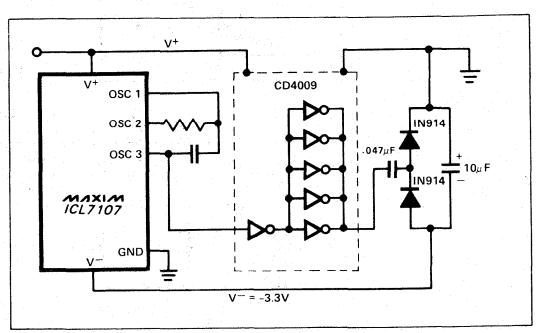


Figure 10. Generating Negative Supply from +5V

Applications Information

Heat is generated within the ICL7107 IC package due to the sinking of LED display current. Fluctuating chip temperature can cause a display to change reading if the internal voltage reference is used. By reducing the power being dissipated such variations can be reduced. The ICL7107 power dissipation is reduced by reducing the LED common anode voltage. The curve tracer illustration showing the relationship between the output current and the output voltage for typical ICL7107 is seen in Figure 11. Note that the typical ICL7107 output is 3.2V (point A), since the typical LED has 1.8V across it (8mA drive current) and its common anode is connected to +5V. Maximum power dissipation is:

$$8.1mA \times 3.2V \times 24 \text{ segments} = 622mW$$

Once the ICL7107 output voltage is above 2V, the LED current is essentially constant as output voltage increases. Point B illustrates that reducing the output voltage by 0.7V results in 7.7mA of LED current, (only 5% reduction). The maximum power dissipation is a reduction of 26% as calculated by:

$$7.7mA \times 2.5V \times 24 \text{ segments} = 462mW$$

As illustrated in Figure 12, reduced power dissipation is easy to obtain. This can be accomplished by placing either a 5.1Ω resistor or a 1 amp diode in series with the display (but not in series with the ICL7107). Point C of Figure 18 illustrates that a resistor will reduce the ICL7107 output voltage when all 24 segments are "On". The output voltage will increase when segments are turned "Off". On the other hand, the diode will result in a relatively steady output voltage, around Point B. The resistor not only reduces the change in power dissipation as the display changes, but also limits the maximum power dissipation. This is due to the fact that as fewer segments are "On", each "On" output drops more voltage and current. The resistor circuit will change about 230mW when changing from the best case of six segments, a "111" display, to worst-case of a "1888" display. If the resistor is removed, the power dissipation change will be 470mW. The resistor, therefore, will reduce the effect of display dissipation on reference voltage drift by about 50%.

As more segments are turned off, the change in LED brightness caused by the resistor is almost unnoticeable. A diode may be used instead of the resistor if it is important to maintain a steady level of display brightness.

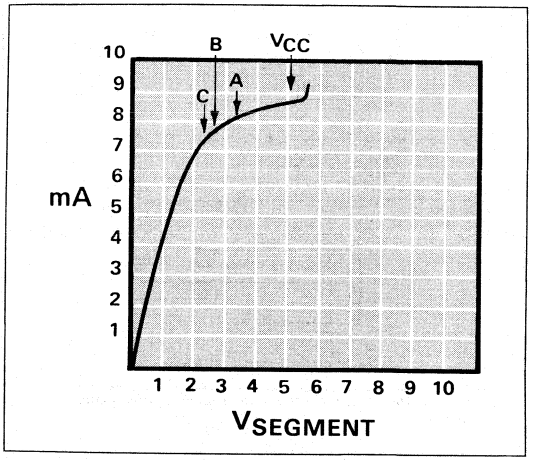


Figure 11. ICL7107 Output Current vs. Output Voltage

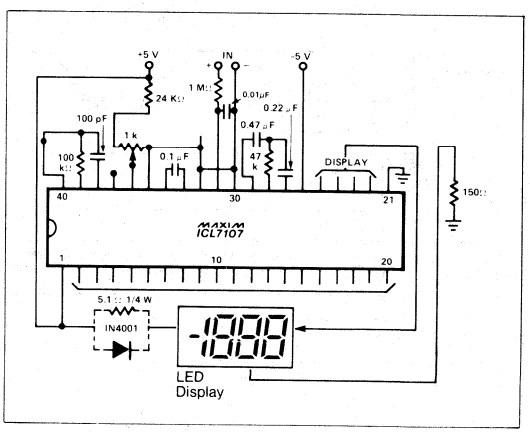


Figure 12. Diode or Resistor Limits Package Power Dissipation

3½ Digit A/D Converter

Typical Applications

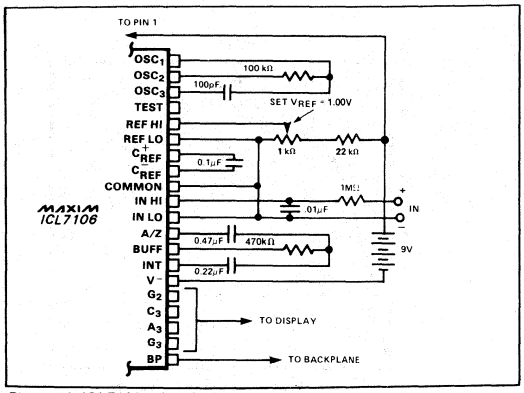


Figure 13. ICL7106 using the Internal Reference. 2V Full Scale; 3 Readings per Second.

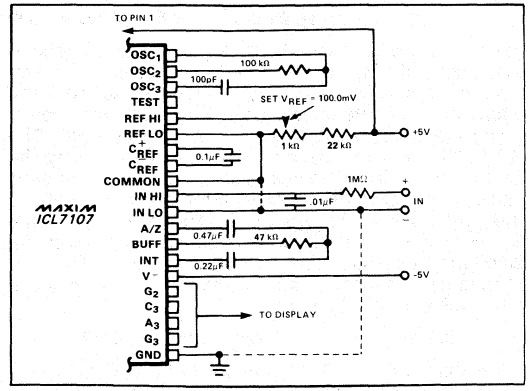


Figure 14. ICL7107 Internal Reference. 200mV Full Scale; 3 Readings per Second, V_{IN} Tied to GND for Single Ended Inputs. (See discussion under "Analog Common".)

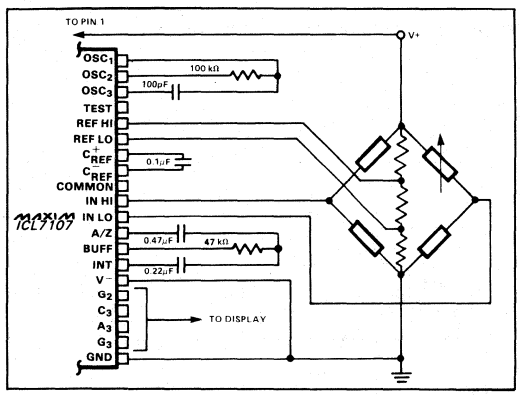


Figure 15. ICL7107 Measuring Ratiometric Values of a Load Cell. Desired Sensitivity is Determined by Resistor Values Within the Bridge.

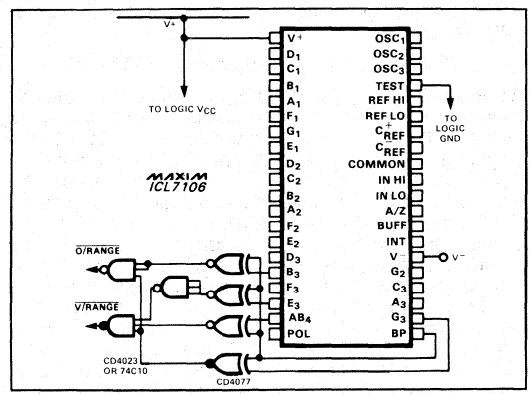


Figure 16. Circuit for Developing Under Range and Over Range Signals from ICL7106 Outputs.

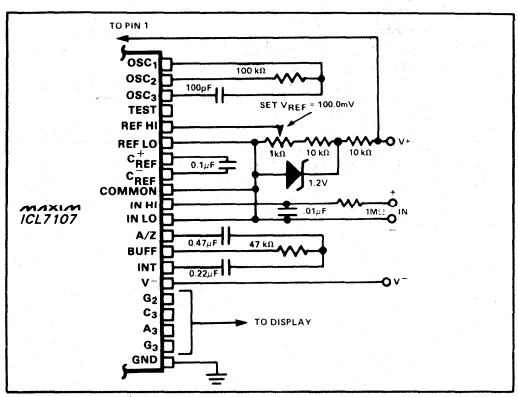


Figure 17. ICL7107 with a 1.2V External Band-Gap Reference V_{IN} tied to common.

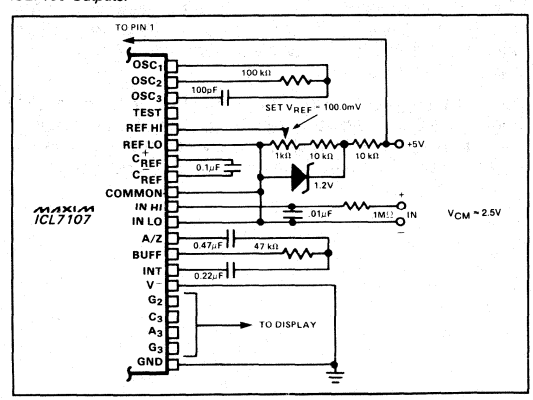


Figure 18. ICL7107 Operated from Single +5V Supply. An external Reference must be used in this application.

Typical Applications

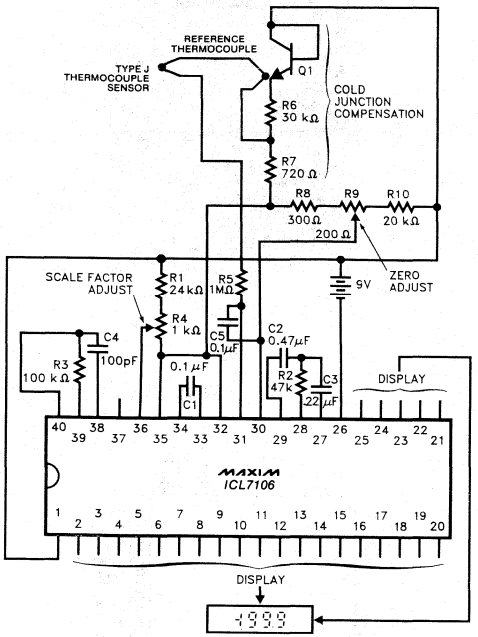


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 50.4μV/°C output of a Type J thermocouple results in 1 count/°C.

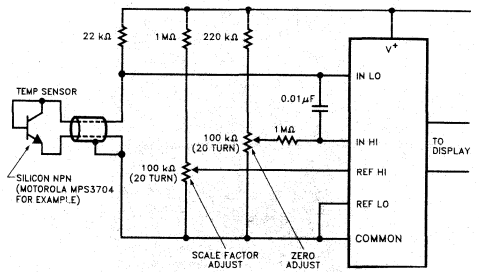


Figure 20. Digital Thermometer

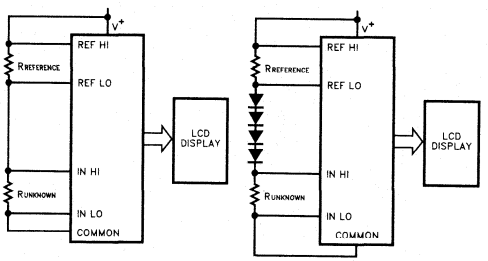
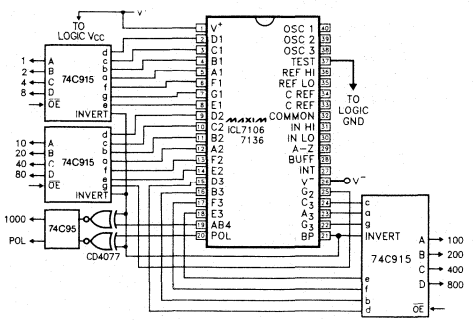
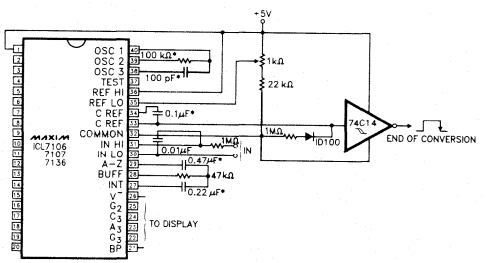


Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers

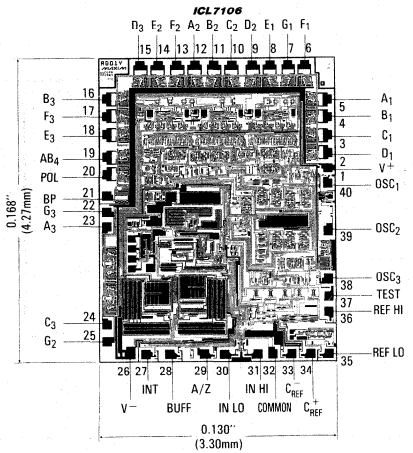


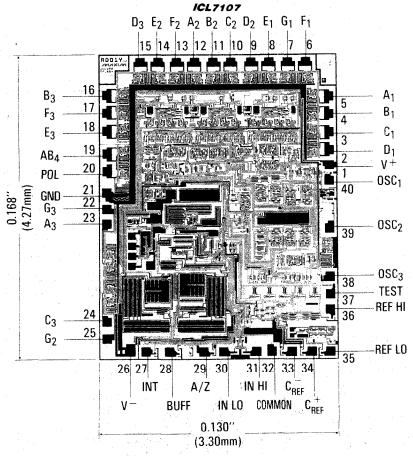
* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

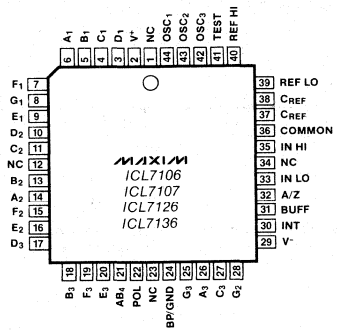
3½ Digit A/D Converter

Chip Topographies





Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

MAXIM

12 Bit A/D Converter With 3-State Binary Outputs

General Description

The ICL7109 is a monolithic 12 bit A/D converter designed for easy interface with microprocessors and UARTs. The 12 bit binary plus polarity and over-range outputs can be directly interfaced to a microprocessor bus. In this mode the ICL7109 is controlled by the microprocessor through the chip select and two byte enable inputs. For remote data logging applications the ICL7109 outputs are easily converted to a UART handshake mode, working with industry standard UARTs to provide serial data transmission.

This device offers high accuracy by lowering rollover error to less than 1 count and zero reading drift to less than 1 μV/°C. In many data acquisition systems the ICL7109 is an attractive, low cost, one-per-channel alternative to analog multiplexing due to its low power consumption and input bias current.

Maxim has added a zero-integrator phase to the ICL7109, eliminating overrange hangover, "crosstalk" and hysteresis effects. Maxim has also increased the current sourcing capabilities of the ICL7109, enabling it to rapidly drive the large capacitances often found on microprocessor busses.

Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Zero Integrator Phase for Fast Overload Recovery**
- **Hysteresis and "Crosstalk" Eliminated**
- **Enhanced Bus Driving Capability**
- **Byte Organized Three-state Outputs**
- **UART Handshake Mode for Serial Interfacing**
- **True Differential Input and Reference**
- **Up to 30 Conversions per Second**
- **Significantly Improved ESD Protection**
- **Monolithic, Low Power CMOS Design**

Applications

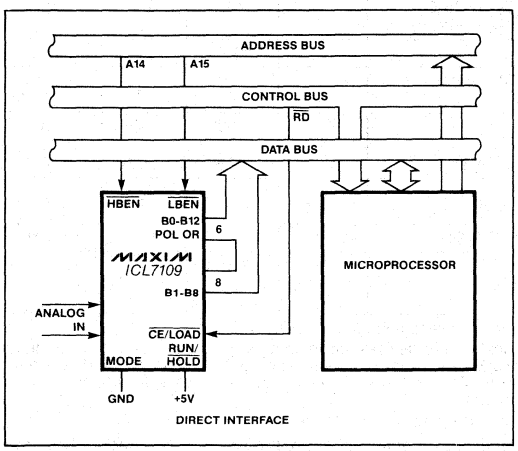
This device is used in a wide range of data acquisition and control applications. Most applications involve the measurement of analog data:

Pressure	Speed	Voltage
Resistance	Flow	Weight
Temperature	Power	Current

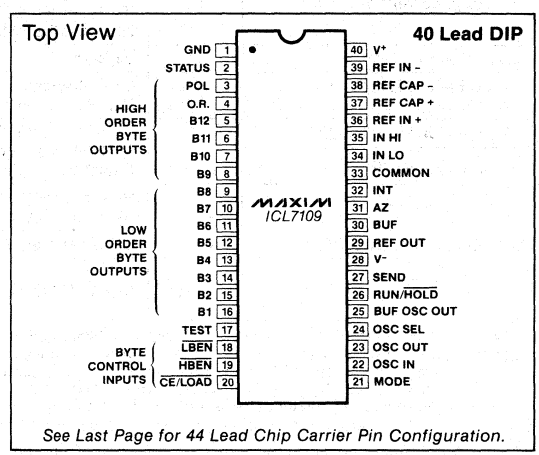
Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7109MJL	-55°C to +125°C	40 Lead CERDIP
ICL7109IJL	-20°C to +85°C	40 Lead CERDIP
ICL7109CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7109CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7109C/D	0°C to +70°C	Dice

Typical Operating Circuit



Pin Configuration



See Last Page for 44 Lead Chip Carrier Pin Configuration.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

12 Bit A/D Converter With 3-State Binary Outputs

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... -9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) .. V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) .... GND - 0.3V ≤ V_{IN} ≤ V^+ + 0.3V
Power Dissipation (Note 3)
Cerdip Package ..... 1W @ +85°C
Plastic Package ..... 500mW @ +70°C
Plastic Chip Carrier (Quad) ..... 400mW @ +70°C

Operating Temperature
Cerdip Package (MJL) ..... -55°C ≤ T_A ≤ +125°C
Cerdip Package (CJL) ..... -20°C ≤ T_A ≤ +85°C
Plastic Package (CPL) ..... 0°C ≤ T_A ≤ +70°C
Plastic Chip Carrier
(Quad) Package (Q) ..... 0°C ≤ T_A ≤ 70°C
Storage Temperature ..... -65°C ≤ T_A ≤ +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(All parameters with V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Low, Common	V^- +1.5		V^+ -1.5	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage current at Input	I_{ILK}	V_{IN} = 0 All devices 25°C ICL7109CPL 0°C ≤ T_A ≤ +70°C ICL7109IDC -25°C ≤ T_A ≤ +85°C ICL7109MDL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = > 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	V^- +1.5	V^+ -0.5 to V^- +1.0	V^+ -1.0	V

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100 μA.

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

12 Bit A/D Converter With 3-State Binary Outputs

- **Zero Integrator Phase ensures fast overload recovery**
- **"Crosstalk" and Hysteresis Eliminated**
- **Bus Driving Capability Enhanced**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 4)**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C; Test Circuit Figure 1; unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Recovery Time				**0**	**1**	**Measurement Cycles**
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 5)	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 2.048V Over full operating temperature range (Note 5)	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	V_{CMR}	Input Hi, Input Low, Common	V^- +1.5		V^+-1.5	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage Current at Input	I_{ILK}	V_{IN} = 0V All devices, T_A = 25°C ICL7109CPL CQ 0°C ≤ T_A ≤ +70°C ICL7109IJL -20°C ≤ T_A ≤ +85°C ICL7109MJL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} ≈ 408.9mV ≈ 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29 open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C

Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (test circuit per Mil Std 883, Method 3015.1).

Note 5: A 4.096V full scale voltage exceeds the Common Mode Voltage Range of the device. The full scale voltage has therefore been changed to 2.048V.

12 Bit A/D Converter With 3-State Binary Outputs

ELECTRICAL CHARACTERISTICS

(All parameters with $V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, unless noted.)

DIGITAL SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	$I_{OUT} = 100\mu A$ Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage	V_{OL}	$I_{OUT} = 1.6mA$		0.2	0.4	V
Output Leakage Current		Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current		Pins 18, 19, 20 $V_{OUT} = V^+ -3V$ MODE input at GND		5		μA
Control I/O Loading		HBEN Pin 19 LBEN Pin 18			50	pF
Input High Voltage	V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage	V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current		Pins 26, 27 $V_{OUT} = V^+ -3V$		5		μV
Input Pull-up Current		Pins 17, 24 $V_{OUT} = V^+ -3V$		25		μA
Input Pull-down Current		Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High O_{OH}	$V_{OUT} = 2.5V$		1		mA
	Low O_{OL}	$V_{OUT} = 2.5V$		1.5		mA
Buffered Oscillator Output Current	High BO_{OH}	$V_{OUT} = 2.5V$		2		mA
	Low BO_{OL}	$V_{OUT} = 2.5V$		5		mA
MODE Input Pulse Width	t_W		50			ns

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

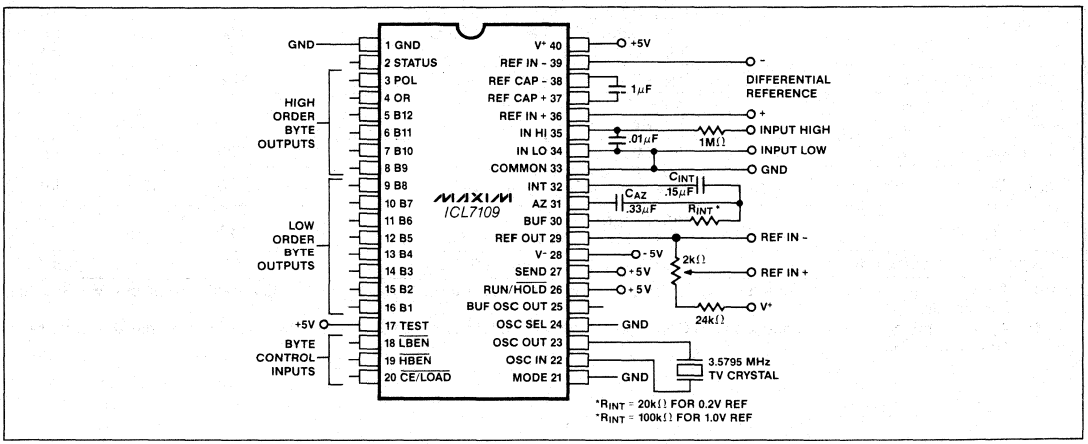


Figure 1. ICL7109 Test Circuit

12 Bit A/D Converter With 3-State Binary Outputs

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		**V_{OH}**	**Pins 2-16, 18-20. I_{OUT} = 1mA I_{OUT} = 100µA**	**3.5 4.0**	**4.3 4.5**		**V V**
Output Low Voltage		V_{OL}	I_{OUT} = -1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	µA
Control I/O Pullup Current			**Pins 18, 19, 20 V_{OUT} = V^+ -3V MODE input at GND**	**2**	**5**	**20**	**µA**
Control I/O Loading			HBEN Pin 19, LBEN Pin 18			50	pF
Input High Voltage		V_{IH}	Pins18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			**Pins 26, 27 V_{OUT} = V^+ -3V**	**2**	**5**	**20**	**µA**
Input Pull-up Current			**Pins 17, 24 V_{OUT} = V^+ -3V**	**5**	**100**	**300**	**µA**
Input Pull-down Current			**Pin 21 V_{OUT} = GND +3V**	**2**	**5**	**20**	**µA**
Oscillator Output Current	**High**	**O_{OH}**	**V_{OUT} = 2.5V**	**1**	**2**		**mA**
	Low	**O_{OL}**	**V_{OUT} = 2.5V**	**1.5**	**3**		**mA**
Buffered Oscillator Output Current	**High**	**BO_{OH}**	**V_{OUT} = 2.5V**	**2**	**4**		**mA**
	Low	**BO_{OL}**	**V_{OUT} = 2.5V**	**5**	**10**		**mA**
MODE Input Pulse Width		t_W	(Note 6)	50			ns
Byte Enable Width		t_{BEA}	(Note 6)	350	100		ns
Data Access Time from Byte Enable		t_{DAB}	(Note 6)		150	350	ns
Data Hold Time from Byte Enable		t_{DHB}	(Note 6)		100	300	ns
Chip Enable Width		t_{CEA}	(Note 6)	400	120		ns
Data Access Time from Chip Enable		t_{DAC}	(Note 6)		175	400	ns
Data Hold Time from Chip Enable		t_{DHC}	(Note 6)		150	400	ns

Note 6: Guaranteed by design; sample tested only.

12 Bit A/D Converter With 3-State Binary Outputs

Table 1. PIN FUNCTIONS

PIN	FUNCTION	TYPE	DESCRIPTION
1	GND		Ground return for digital logic, 0V
2	STATUS	Output	HI = Converter in integrate phase, or deintegrate phase until data is latched LO = Converter in zero-integrator phase, auto-zero phase, or deintegrate phase after data is latched.
3	POL	Three state data output bits	Polarity — HI = Positive input.
4	OR		Overrange — HI = Overranged
5	B12		Bit 12 = Most significant bit
6	B11		Bit 11
7	B10		Bit 10
8	B9		Bit 9
9	B8		Bit 8
10	B7		Bit 7
11	B6		Bit 6
12	B5		Bit 5
13	B4		Bit 4
14	B3		Bit 3
15	B2		Bit 2
16	B1		Bit 1 = Least significant bit.
17	TEST	Input	HI = Normal operation LO = All output bits high. MID = Counter output latches enabled. Connect to +5V if not used.
18	$\overline{LBEN}$	Input Output	Low Byte Enable. When MODE is low and $\overline{CE/LOAD}$ is low, taking Low Byte Enable low activates low order byte outputs B1-B8. In handshake mode (when MODE is HI) this pin becomes a low byte flag output.
19	$\overline{HBEN}$	Input Output	High Byte Enable. When MODE is low and $\overline{CE/LOAD}$ is low, taking High Byte Enable low activates high order byte outputs B9-B12, POL & OR. In handshake mode (when MODE is HI) this pin becomes a high byte flag output.
20	$\overline{CE/LOAD}$	Input Output	When MODE is low, taking Chip Enable/Load high disables B1-B12, POL & OR. Taking it low enables B1-B12, POL & OR if $\overline{HBEN}$ and $\overline{LBEN}$ are low. In handshake mode (when MODE is HI) this pin becomes a load strobe output.

PIN	FUNCTION	TYPE	DESCRIPTION
21	MODE	Input	LO = Converter in direct output mode. Makes $\overline{LBEN}$, $\overline{HBEN}$ & $\overline{CE/LOAD}$ act as inputs controlling byte outputs directly. HI = Converter in handshake mode. Makes $\overline{LBEN}$, $\overline{HBEN}$ & $\overline{CE/LOAD}$ act as outputs.
22	OSC IN	Input	Oscillator input.
23	OSC OUT	Output	Oscillator output.
24	OSC SEL	Input	Taking Oscillator Select high or leaving it open configures OSC IN, OSC OUT & BUF OSC OUT as an RC oscillator. Clock frequency = BUF OSC OUT frequency. Taking it low configures OSC IN & OSC OUT for crystal oscillators. Clock frequency = BUF OSC OUT frequency ÷ 58.
25	BUF OSC OUT	Output	Buffered Oscillator Output
26	RUN/$\overline{HOLD}$	Input	HI = Continuous conversions every 8192 clock pulses. LO = Converter stops in auto-zero after completing the conversion in progress.
27	SEND	Input	Indicates ability of external device to accept data when converter is in handshake mode. Connect to +5V if not used.
28	V^-		Negative supply. Nominally -5V from GND.
29	REF OUT	Output	Reference voltage output. Nominally 2.8V below V^+.
30	BUFFER	Output	Buffer Amplifier Output.
31	AUTO-ZERO		Inside foil of C_{AZ} connects here.
32	INTEGRATOR	Output	Outside foil of C_{INT} connects here.
33	COMMON		Analog Common.
34	INPUT LO		Low side of differential input.
35	INPUT HI		High side of differential input.
36	REF IN^+		Positive input of differential reference.
37	REF CAP^+		Positive side of reference capacitor.
38	REF CAP^-		Negative side of reference capacitor.
39	REF IN^-		Negative input of differential reference.
40	V^+	Input	Positive supply. Nominally +5V from GND.

Note: All digital levels are positive true.

12 Bit A/D Converter With 3-State Binary Outputs

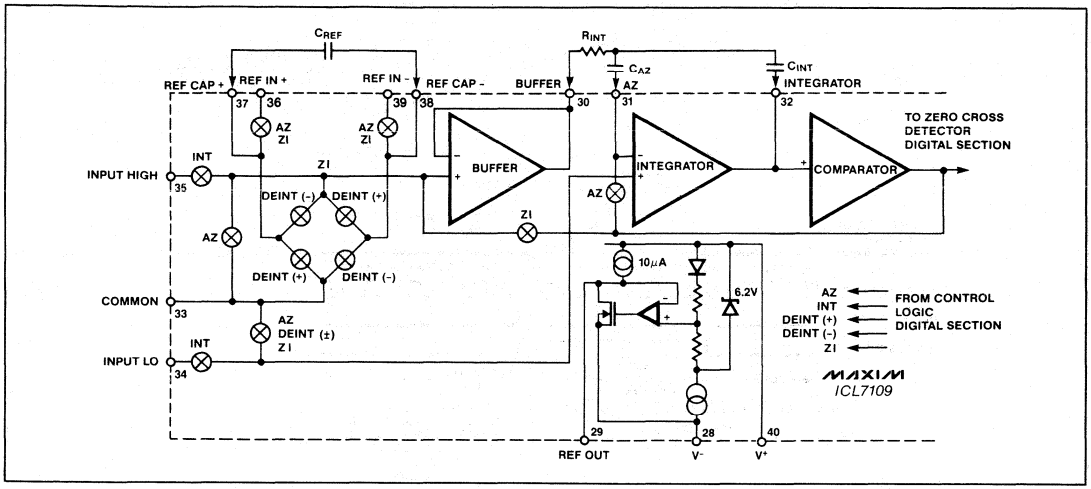


Figure 2. Analog Section

Detailed Description

Analog Section

The equivalent circuit of the Analog Section of the ICL7109 is shown in Figure 2. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle) when the RUN/HOLD input is left open or connected to V^+. Each measurement cycle is divided into four phases as shown in Figure 3. They are:

1. Auto-Zero (AZ)
2. Signal Integrate (INT)
3. De-integrate (DE)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during Auto-zero. The inputs, In-Hi and In-Lo, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. Lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy. In any event, the offset referred to the input is less than 10 μV.

Signal Integrate Phase

The internal input high (In-Hi) and input low (In-Lo) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between In-Hi and In-Lo for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. The polarity of the integrated signal is determined at the end of this phase.

De-integrate Phase

The third phase is De-integrate, also known as reference integrate. Input high is internally connected across the previously charged reference capacitor and input low is internally connected to analog Common. The polarity detection circuit connects the reference capacitor with the polarity such that the integrator output returns with a fixed slope to the zero level established in the Auto-Zero phase. The time required for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Zero Integrator Phase

Input low is shorted to analog Common and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return rapidly to zero (See Figure 3). This phase normally lasts between 16 and 32 clock pulses but is extended to 1552 clock pulses after an overrange conversion.

This phase will remove any residual charge left on the integrator capacitor after an overload reading. This Zero Integrator phase virtually eliminates the problem of interaction or "crosstalk" between the various channels of a Maxim ICL7109 based multiple channel data acquisition system. Without the zero integrator phase, an overload on one channel would leave charge on the integrator capacitor, which would then be transferred to the autozero capacitor during the autozero cycle, resulting in an erroneous reading for the next channel that is measured after the channel with the overload.

12 Bit A/D Converter With 3-State Binary Outputs

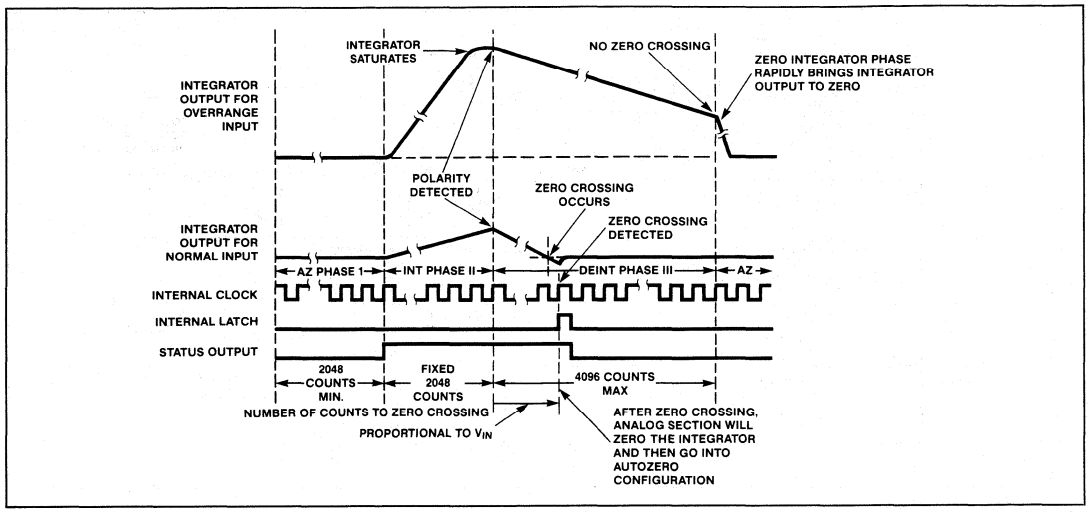


Figure 3. Conversion Timing (RUN/$\overline{HOLD}$ Pin High)

Differential Input

Differential input voltages anywhere within the common-mode range of the input amplifier can be accepted (specifically from 1.5V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB typical in this range. For optimum performance the input voltage at In-Lo and In-Hi should not come within 2 volts of either the positive or negative supply. Care must be exercised to ensure that the integrator output does not saturate, since the integrator also swings with the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator positive. The integrator output swing can be reduced to less than the recommended 4V full-scale swing with little loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

The ICL7109 has been optimized for operation with analog common near digital ground. This allows for a 4V full scale integrator swing positive or negative which maximizes performance of the analog section with ±5V power supplies.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Roll over error defines this difference in reference for positive or negative input voltages. This error can be held to less than one half count for worst-case condition by using an optimum reference capacitor. (See component value selection.)

By having the reference common mode voltage near or at analog COMMON, the roll-over error from these sources is minimized.

Component Value Selection

Care must be exercised in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate for optimum performance of the analog section. The optimum values must be selected for each application.

Integrating Resistor

Both the integrator and buffer amplifier have a class A output stage with a quiescent current of 100 μA, which can supply 20 μA with negligible non-linearity. The integrating resistor should be small enough that undue leakage requirements are not placed on the PC board, but large enough to keep the output current less than 40 μA. For 2.048 volt full scale, 100kΩ is optimum and similarly a 20kΩ is optimum for a 409.6mV scale. For other full scale voltages, R_{INT} should be selected by the relation

$$R_{INT} = \frac{\text{full scale voltage (mV)}}{20\ \mu A}\ k\Omega$$

12 Bit A/D Converter With 3-State Binary Outputs

Integrating Capacitor

C_{INT} (the integrating capacitor) should be selected for maximum integrator output voltage swing without saturation of the integrator (at 0.3 volt from either supply). A ±3.5 to ±4 volt integrator output swing is ideal for the ICL7109 with a ±5 volt supplies and analog common connected to GND. Nominal values for C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively, for 7½ conversions per second (61.44kHz clock frequency). These values should be changed to maintain the integrator output voltage swing, if different clock frequencies are used. The value of C_{INT} is generally given by

$$C_{INT} = \frac{(2048 \times \text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing (V)}}\ \mu F$$

To prevent roll-over and linearity errors a low dielectric absorption capacitor is required. Polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. Teflon™ capacitors are recommended for the military temperature range. Polypropylene and Teflon™ capacitors should give less than 0.5 count of error due to dielectric absorption even though their absorption characteristics vary somewhat from unit to unit.

Auto-Zero Capacitor

The Maxim ICL7109 has a zero integrator phase which ensures that any charge left on the integrator after an overrange reading is removed before the autozero phase is started. This zero integrator phase allows the use of larger values of autozero capacitors than allowed with other manufacturer's ICL7109s. Normally, the optimum value of the autozero capacitor is between 2 and 4 times the value of the integrator capacitor. The typical value of the autozero capacitor is 0.33 μF. Lower values of C_{AZ} increase the noise in the autozero loop; very large values will take a longer time to charge to the proper value after power-up.

The outer foil of C_{AZ} should be connected to the R_{INT}, C_{INT} summing junction and the inner foil to pin 31 for optimal rejection of stray pickup. Similarly, the inner foil of C_{INT} should be connected to the RC summing junction, and the outer foil of C_{INT} should be connected to pin 32. Above 85°C, Teflon™, or equivalent capacitors are recommended for their low leakage characteristics.

Reference Capacitor

Good results can be achieved in most applications with a 1 μF capacitor. A larger value is required to prevent roll-over error where a 409.6mV scale is used and a large common mode voltage exists (i.e., the reference low is not at analog common). The roll-over error can generally be held to one half count by 10 μF in this case. Above 85°C, Teflon™, or equivalent capacitors are again recommended for their low leakage characteristics.

Reference Voltage

An analog input of $V_{IN} = 2 \times V_{REF}$ generates a full scale output of 4096 counts. For a normalized scale, a reference of 204.8mV should be used for a 409.6mV full scale (100 μV per LSB), and 1.024V reference should be used for a 2.048V full scale (500 μV per LSB). There will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output in many applications where the A/D is sensing the output of a transducer. In a weighing system, for example, the designer could possibly want a full scale reading when the voltage from the transducer is 0.682V. The input voltage should be measured directly and a reference voltage of 0.341V should be used instead of dividing the input down to 409.6mV. 34kΩ and 0.15 μF are suitable values for the integrating resistor and capacitor. A divider on the input is thus avoided. When a zero reading is desired for non-zero input, another advantage of this system is realized. Examples might include temperature and weight measurements with an offset or tare. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. It may be more efficient, however, to perform this type of scaling or tare subtraction digitally using software in processor-based systems using the ICL7109.

Reference Sources

A major factor in the overall absolute accuracy of the converter is the stability of the reference voltage. The resolution of the ICL7109 at 12 bits is 244 ppm or one part in 4096. Therefore, a temperature difference of 3°C will introduce a one-bit error if the reference has a temperature coefficient of 80 ppm/°C (like the onboard reference). Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made, an external high quality reference should be used.

To generate a suitable reference voltage, the ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider. This output will sink up to about 20mA without a significant output variation. A pullup bias device which sources about 10 μA is also provided. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80 ppm/°C typical. REF^+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+, and REF OUT (Pin 29) should be connected to REF^- (pin 39) when using the onboard reference. Shown in the test circuit is the circuit for a 204.8mV reference. The fixed resistor should be removed for a 1V reference, and a 25kΩ precision

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potentiometer between REF OUT and V+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink sufficient current to destroy the device. By placing a 1kΩ resistor in series with pin 39, this can be avoided.

Detailed Description

Digital Section

The digital section (Figure 4) includes: 1) the clock oscillator and divider circuit; 2) a 12-bit binary counter with output latches and TTL-compatible three-state output drivers; 3) control logic; and 4) UART handshake logic.

Note: The term "clock cycles" as used in the following discussion relates to the internal clock, which is the oscillator output ÷ 58 when OSC SEL is low.

Three-State Outputs

The ICL7109 has 14 three-state outputs: 12 data bits, 1 polarity bit, and 1 overrange bit. These bits are enabled either by the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ control signals (see Table 2), or by entering the Handshake mode.

$\overline{CE/LOAD}$, $\overline{LBEN}$, and $\overline{HBEN}$

These three control pins can function as either inputs or outputs. In the Direct interface mode (see "Interfacing" below), these three pins are Chip Enable and Byte Enable inputs. In the Handshake mode these three pins become outputs that load data into the UART. These pins will be outputs while a handshake transfer is in progress or at any time that the Mode input is high.

Run/$\overline{Hold}$ Input

When the Run/$\overline{Hold}$ input is tied high, the ICL7109 continuously performs A/D conversions with a fixed length of 8192 clock cycles per conversion. When Run/$\overline{Hold}$ is taken low, the ICL7109 will complete the conversion in progress, then wait in the autozero phase. After the minimum autozero time has been completed, a high-going pulse on Run/$\overline{Hold}$ of at least 200 nanoseconds is required to start a new conversion; but any pulses during a conversion or up to 2048 clock cycles after Status goes low will be ignored. If the ICL7109 is holding at the end of the autozero phase, a new conversion will start and Status will go high within 7 clock cycles after Run/$\overline{Hold}$ goes high.

In addition to starting and stopping conversions, the Run/$\overline{Hold}$ pin can also be used to minimize conversion time. If Run/Hold is high, each conversion takes a full 8192 clock cycles, with the De-integrate phase taking 4096 clock cycles independent of input voltage. On the other hand, if Run/$\overline{Hold}$ is low at any time after Status goes low, the ICL7109 immediately jumps to the Auto-Zero phase rather than taking a full 4096 clock cycles for De-integrate. A simple way to ensure minimum conversion time is to drive the Run/$\overline{Hold}$ input with the Buffered Oscillator Output. When this is done, the conversion time is dependent on the input voltage: 4096 clock cycles for a zero voltage input, rising to 8192 clock cycles for full scale or overrange inputs.

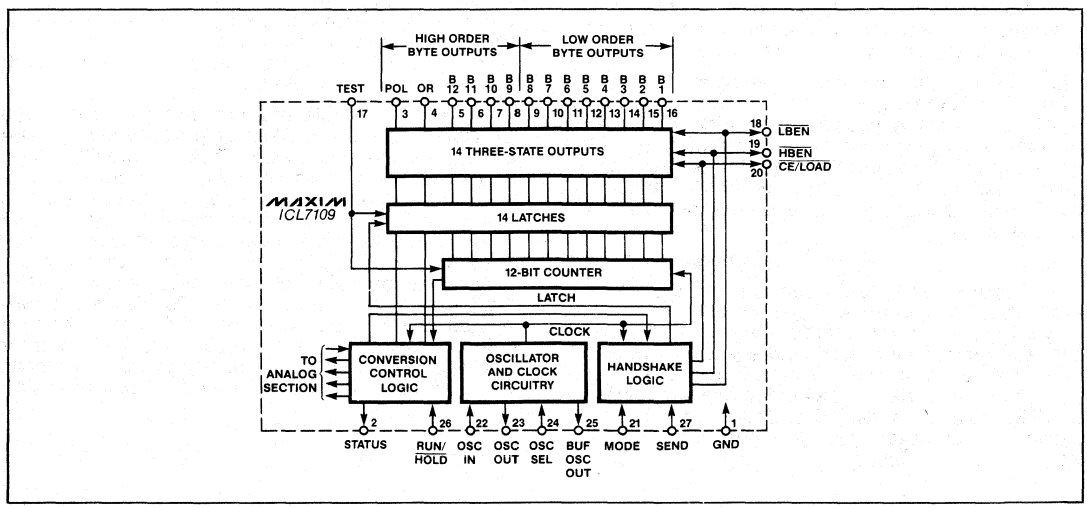

Figure 4. Digital Section

12 Bit A/D Converter With 3-State Binary Outputs

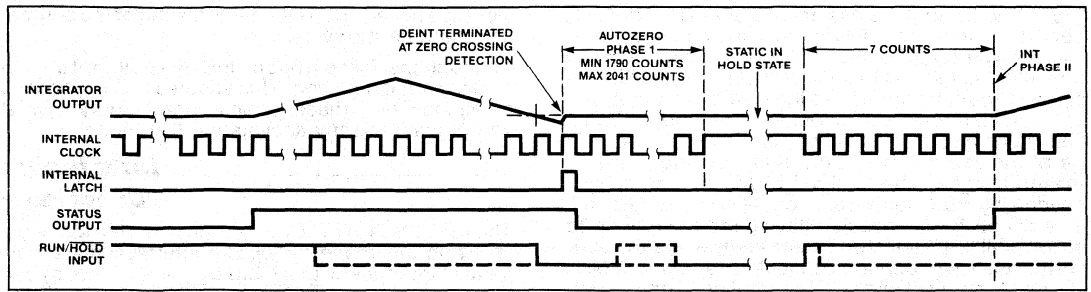

Figure 5. RUN/$\overline{HOLD}$ Operation

Mode Input

The Mode input is used to control the converter output mode. The converter is in its Direct output mode, where the output data is directly accessible under the control of the chip and byte enable inputs when the Mode pin is low or left open. (To ensure a low level when the pin is left open, this input is provided with an internal pulldown resistor.) When the Mode input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "Direct" mode. The converter will output data in the handshake mode at the end of every conversion cycle when the Mode input remains high. (See "Handshake Mode" section for more details.)

Send Input

The Send Input is a handshake control input used during handshake transfers. The use of Send to control a handshake interface is discussed in the "Interfacing" section, below.

The Maxim ICL7109 contains an improved power-up reset circuit that ensures that the ICL7109 powers up in the Direct mode if the Mode input is low, but other manufacturer's ICL7109s may power up in the Handshake mode even if the Mode input is held low. Although the Send input on the Maxim ICL7109 can be tied either high or low if only the Direct mode is used, other manufacturer's ICL7109s require that the Send input be tied high so that the ICL7109 will return to the Direct mode in 7 clock cycles if the Handshake mode is inadvertently entered on power-up.

Oscillator

The ICL7109 has a versatile three terminal oscillator that may be operated as a crystal or RC oscillator. It also may be overdriven by an external clock source. To optimize it for crystal or RC operation, the Oscillator Select input changes the internal configuration of the oscillator. The oscillator is configured for RC operation when the Oscillator Select input is high or left open (the input is provided with an internal pullup resistor), and the internal clock will be of the same phase and frequency as the signal at the Buffered Oscillator Output. (See Figure 6 for the resistor and capacitor connections.) Oscillation will occur in the circuit at a frequency given by f = 0.45/RC. The oscillator resistor should be 100kΩ. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60Hz period for optimum 60Hz line rejection, but the capacitor value should not be less than 50pF.

A feedback device and input and output capacitors are added to the oscillator when the Oscillator Select input is low. With no external components, the oscillator will function with most crystals in the 1 to 5MHz range. (See Figure 7.) A fixed ÷ 58 circuit is inserted between the Buffered Oscillator Output and the internal clock by taking the Oscillator Select input low. This division ratio provides 33.18ms integration time, by using a 3.58MHz TV crystal.

$$T = (2048 \text{ clock periods}) \times \frac{58}{3.58\text{MHz}} = 33.18\text{ms}$$

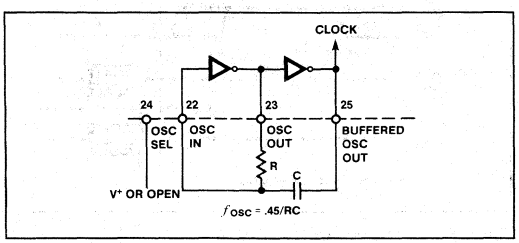

Figure 6. RC Oscillator

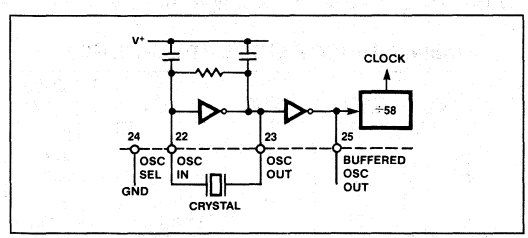

Figure 7. Crystal Oscillator

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This time is quite close to 33.33ms or two 60Hz periods. The error is lower than one percent, which will yield better than 40dB of 60Hz rejection. If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the Oscillator Input, and the Oscillator Output should be left open. When Oscillator Select is left open, the internal clock will be of the same duty cycle, frequency and phase as the input signal. The clock will be the input frequency divided by 58 when Oscillator Select is at Ground. The divide by 58 circuit will operate reliably up to about 5MHz (Oscillator Select low), while the converter itself will operate at clock rates up to 2 MHz (Oscillator Select high). This implies a conversion rate of 244 conversions/sec. To operate the converter at these rates the auto-zero and integrating capacitors must be scaled using the guidelines in the Component Selection section. As the conversion rate increases, the accuracy of the converter is compromised, primarily due to noise and the delay of the comparator. If the clock period is less than the comparator delay (typically 1-3 μsec.), the low order bits become meaningless. At 2 MHz, typical readings with the inputs shorted may be 4-10 counts, rendering the 4 LSBs meaningless.

Note: At 15 conversions per second, the integration time of 2048 clock pulses equals one complete period of 60 Hz. This is therefore the maximum conversion rate that will provide 60 Hz noise rejection.

Status Output

At the end of a conversion cycle the Status output goes low, one-half clock period after new data from the conversion has been stored in the output latches. Status goes high at the beginning of Signal Integrate (Phase II). Figure 3 shows the timing details. This signal may be utilized as a flag indicating "data valid" for monitoring the status of the converter or to drive interrupts since data never changes while Status is low.

Test Input

The counter output latches are enabled when the Test input is taken to a level halfway between V^+ and Ground, allowing the counter contents to be examined. When the Test input is grounded, the internal clock is disabled and the counter outputs are all forced into the high state. The counter outputs will be clocked to the low state when the input returns to the 1/2 (V^+ -Ground) voltage (or to V^+) and one clock is applied. This facilitates testing of the counter and the output drivers.

Although the Test pin has an internal pullup, it should be tied high if not used. This ensures that high speed transitions on adjacent pins (particularly LBEN) do not inadvertently activate the test mode.

Table 2. DIRECT MODE TRUTH TABLE

$\overline{CE}$/LOAD	$\overline{LBEN}$	$\overline{HBEN}$	B1-B8	B9-B12, POL,OR
1	X	X	Hi-Z	Hi-Z
0	1	1	Hi-Z	Hi-Z
0	0	1	Data Out	Hi-Z
0	1	0	Hi-Z	Data Out
0	0	0	Data Out	Data Out

Interfacing

Direct Mode

The ICL7109 is in the Direct mode when the Mode pin is low. In this mode the output interface is a simple parallel interface with a Chip Enable ($\overline{CE}$/Load) and two byte enables ($\overline{HBEN}$ and $\overline{LBEN}$). As shown in the truth table of Table 2, the least significant 8 bits of data are enabled when both $\overline{CE}$/Load and $\overline{LBEN}$ are low. The upper 4 bits of data, polarity, and overrange are enabled whenever $\overline{CE}$/Load and $\overline{HBEN}$ are low. The Maxim version of the ICL7109 has significantly enhanced current sourcing capability, which enables it to rapidly drive the large capacitances often found on microcomputer busses.

In Figure 12, an approach to interfacing several ICL7109s to a bus is shown. This is achieved by using the $\overline{CE}$/Load inputs (decoded from an address possibly) to select the desired converter, and tying the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together.

The ICL7109 can also be controlled through I/O peripheral ports, as shown in Figures 14, 15 and 16. Figures 13 through 16 are some practical circuits utilizing the parallel three-state output capabilities of the ICL7109. Shown in Figure 16 is a straightforward interface to the Intel MCS-48, -80 and -85 systems via an 8255 PPI, where the ICL7109 data outputs are active at all times. The 8155 I/O ports may be utilized in the same way. Although a read performed while the data latches are undergoing updates will lead to scrambled data, this interface can be used in a read-

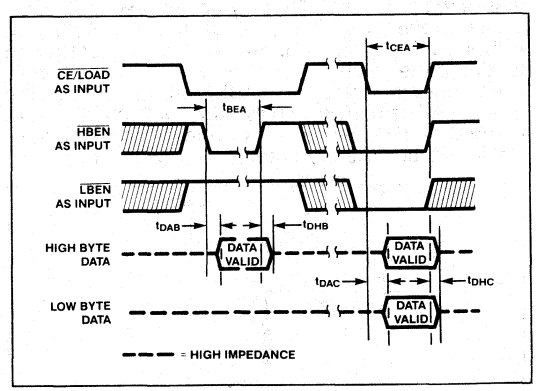

Figure 8. Direct Mode Output Timing

anytime mode. One way of solving this problem is to read the Status output as well. If it is high, read the data a second time after a delay of more than 1/2 converter clock period. If Status is still high, the first reading is correct. If Status is now low, the second reading is correct. On the other hand, the problem of timing is completely avoided by using a read-after-update sequence. (See Figure 14.) Data can be accessed by the high to low transition of the Status output driving an interrupt to the microprocessor. Figure 14 also demonstrates the Run/Hold input being used to initiate conversions under software control.

Figure 15 shows a similar interface to 650X or 680X systems. The transition of the Status output from high to low generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the Run/Hold pin through Control Register B. This application permits software-controlled initiation of conversions.

Direct interfacing to most microprocessor busses is allowed by the three-state output capability of the ICL7109. (See Figure 13 and the typical operating circuit on the first page.) It is important that the requirements for setup and hold times, and minimum pulse widths are met. There are also drive limitations on long busses that should be noted. In general, this type of interface is favored only if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can mandate several extra components. The use of interfacing devices will simplify the system in many cases.

Handshake Mode

Handshake Mode permits the interface with a number of external devices. For example, byte enables may be used as load enables or as byte identification flags, and external latches may be clocked by the rising edge of $\overline{CE}$/Load.

The handshake mode is specifically designed to directly interface the ICL7109 to industry standard UARTs, with no external logic required. The ICL7109 is in the handshake mode whenever the Mode input is high. In the handshake mode the $\overline{CE}$/Load, $\overline{LBEN}$ and $\overline{HBEN}$ pins are outputs and Send is an input. A typical UART to ICL7109 interface is shown in Figure 18, with the interface timing shown in Figures 9 through 11.

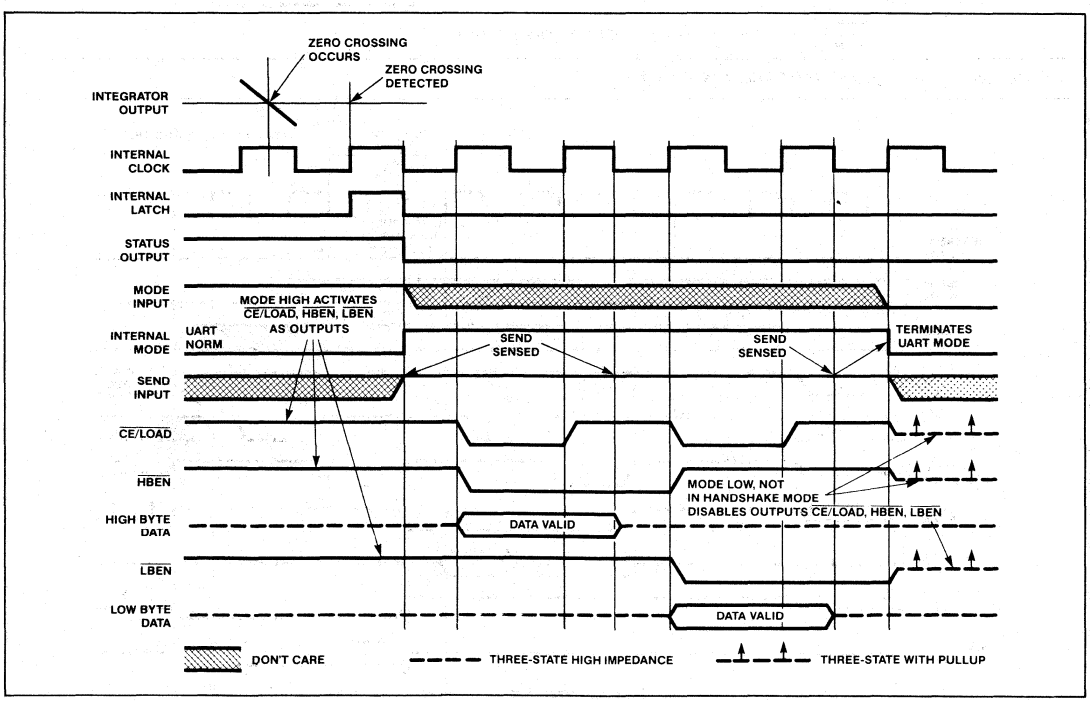

Figure 9. Handshake With Send Held Positive

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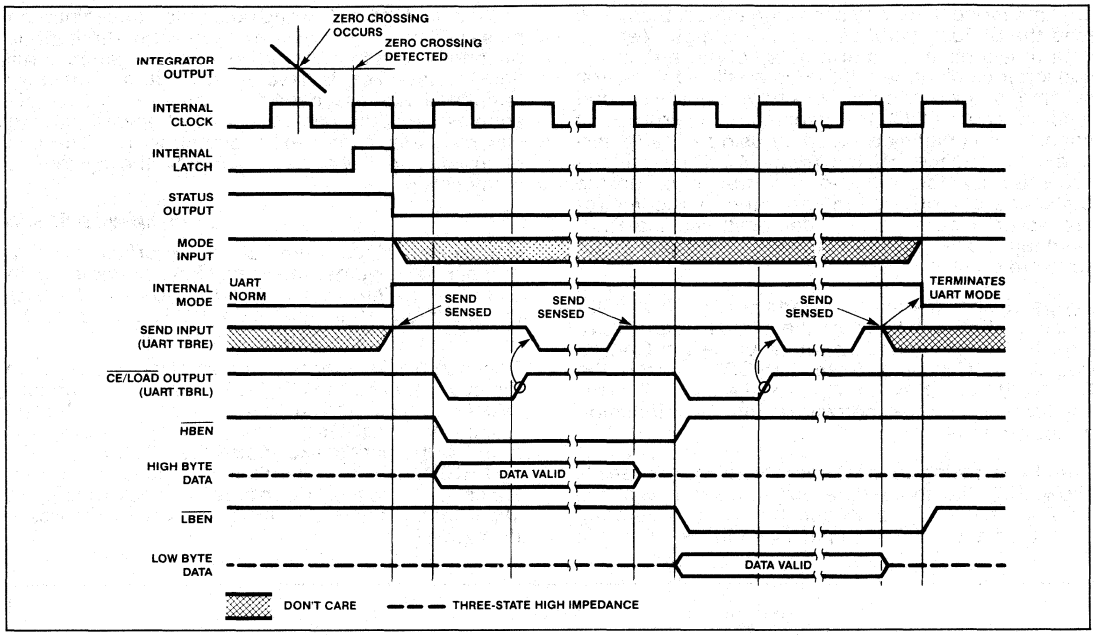


Figure 10. Handshake - Typical UART Interface Timing

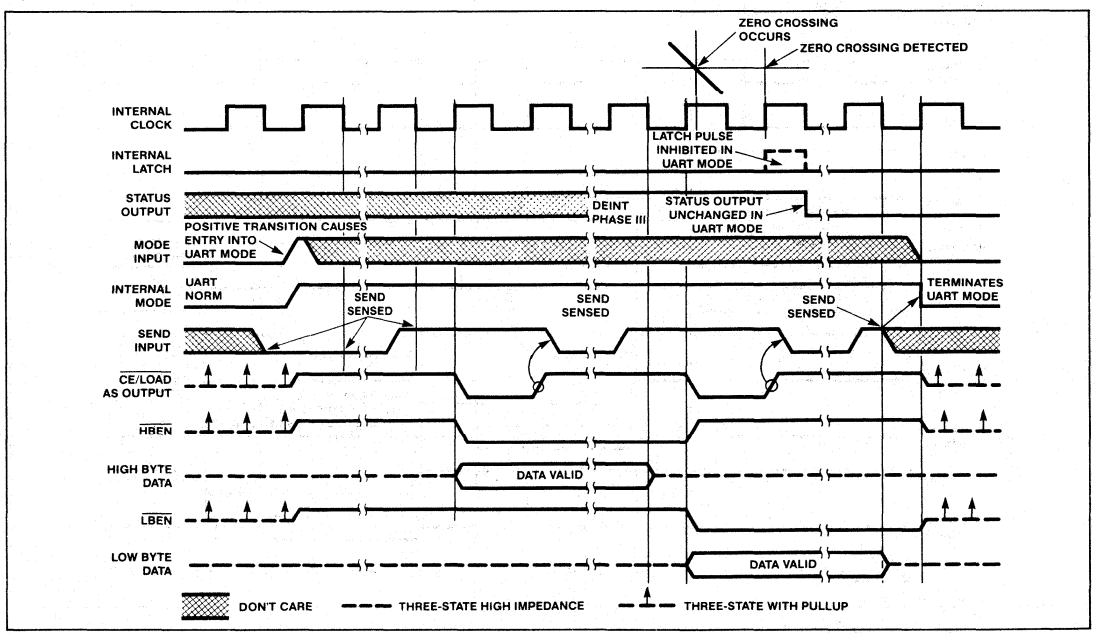


Figure 11. Handshake Triggered By Mode

When Mode is continuously held high, a new UART transmission will be started when Status goes low, provided Send is high at that time. As shown in Figure 10 the high byte of data will be written into the UART by the first pulse of $\overline{CE/Load}$. The $\overline{TBRE}$ signal of the UART will momentarily go low upon receiving the data. After the UART transfers the data to the transmitter register, the UART's $\overline{TBRE}$ output drives the ICL7109's Send input high. The ICL7109 senses the high level on the Send input and loads the low byte of data into the UART with a second pulse of $\overline{CE/Load}$. The ICL7109 continues its conversion cycles while this handshake takes place, and if the UART's $\overline{TBRE}$ has driven the ICL7109 Send input high by the end of the next conversion, the data transfer sequence will repeat. If the UARTs $\overline{TBRE}$ (and therefore the ICL7109's Send input) is low when the ICL7109 completes the next conversion, the internal latch pulse is inhibited and the data from that conversion is lost.

A handshake transfer can be initiated by a high-going pulse on the Mode pin. Upon receiving a high going pulse, the ICL7109 sets an internal Mode latch and will start a handshake transmission when Status goes low at the end of the next conversion. An alternate method of controlling the ICL7109 is to leave Mode high and initiate conversions via the Run/$\overline{Hold}$ input. With this method the ICL7109 will first make a conversion then transmit the data. Another method of initiating a transmission is shown in Figure 11. Here Mode is pulsed high while Send is low. A UART transmission is started when Send is taken high (at least 2 negative clock edges later).

The UART mode is also useful in interfacing the ICL7109 to I/O ports such as the 8255 and 6520. Figure 17 is an example of such an interface. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the Send input to the ICL7109, and using the $\overline{CE/Load}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1. The next conversion's result will be strobed into the port if the 8255 IBF flag is low and the ICL7109 is in handshake mode. The strobe will cause IBF to go high (Send goes low) which will prevent the ICL7109 from loading the second byte of data. The PPI will generate an interrupt. When executed, the result is that the data is read. The IBF will be reset low when the byte is read which causes the ICL7109 to sequence into the next byte. Figure 17 shows the PC7 line of the PPI connected to the Mode input of the ICL7109. If this input is tied high or left high, the data from every conversion will be sequenced into the system (provided the data access takes less time than a conversion). The output sequence can be obtained on demand by using the PC7 output to drive the Mode input. Note that the 8255 can service another peripheral device since only one port is used. The 8155 can utilize the same arrangement.

The ICL7109 is not limited to the applications described here. These examples show some of the many interfaces and uses of the ICL7109 and merely provide a point of departure for users to develop appropriate systems. Many of the suggestions made here may be combined. More specifically, the uses of the Mode, Status, and Run/$\overline{Hold}$ signals may be mixed.

Typical Applications

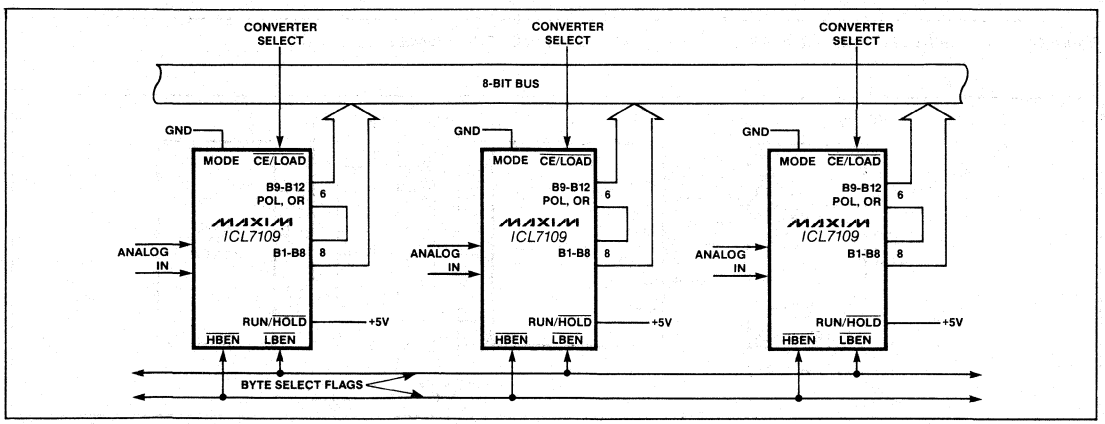


Figure 12. Three-stating several 7109 s to a Bus

12 Bit A/D Converter With 3-State Binary Outputs

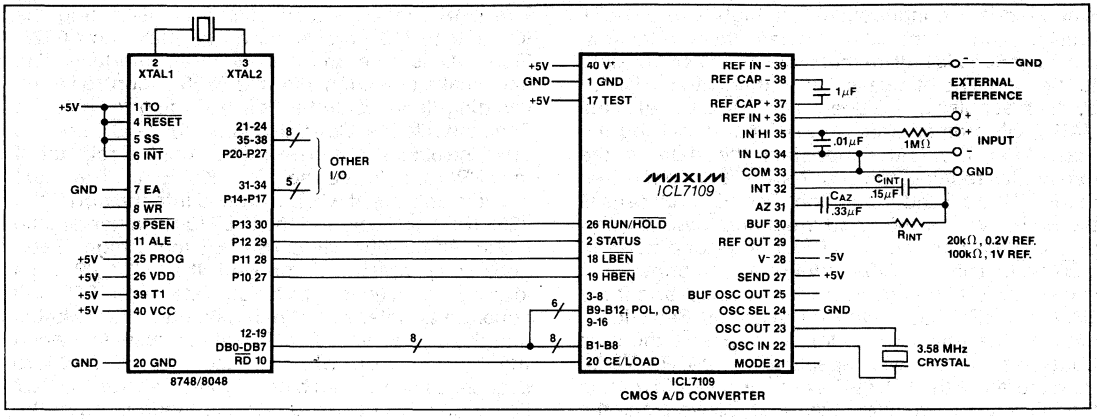


Figure 13. Typical Connection Diagram Parallel Interface with MCS-48 Microcomputer

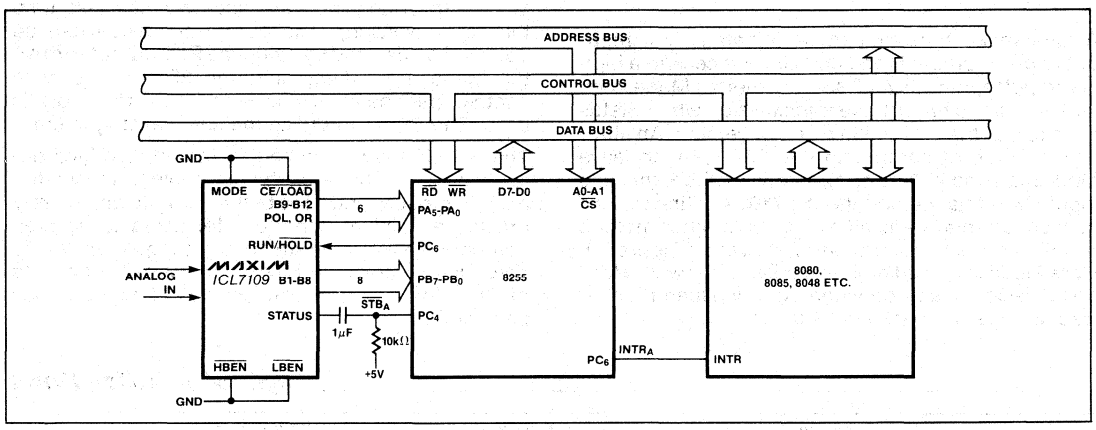


Figure 14. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

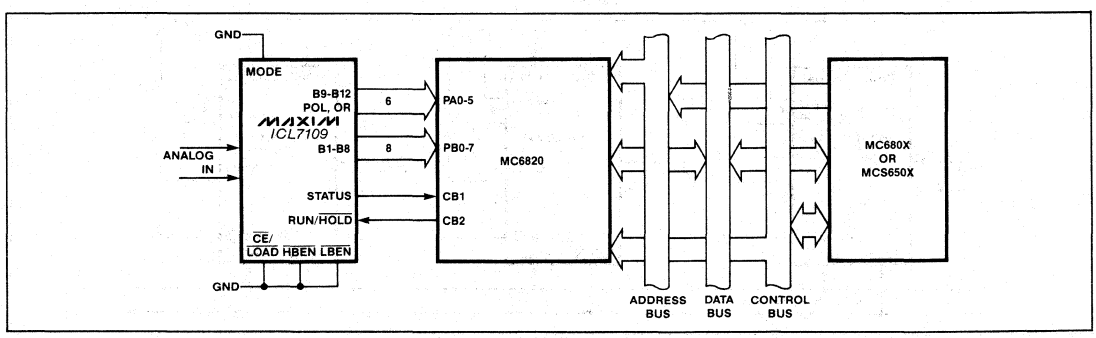


Figure 15. Full-time Parallel Interface to MS680X or MCS650X Microprocessors

12 Bit A/D Converter With 3-State Binary Outputs

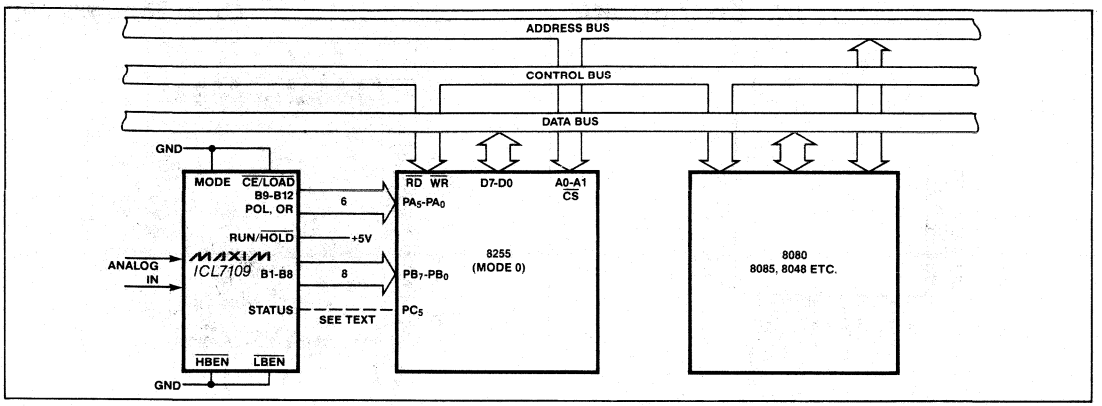


Figure 16. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

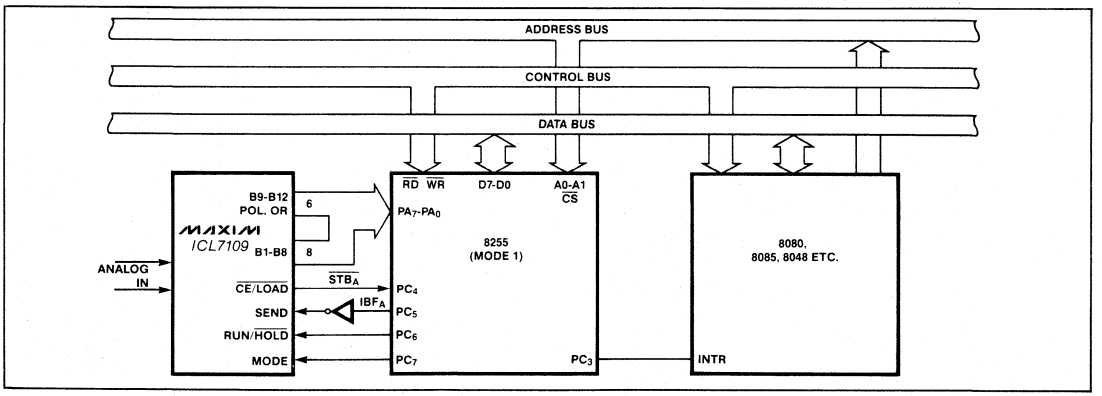


Figure 17. Handshake Interface - ICL7109 to MCS-48, -80, -85

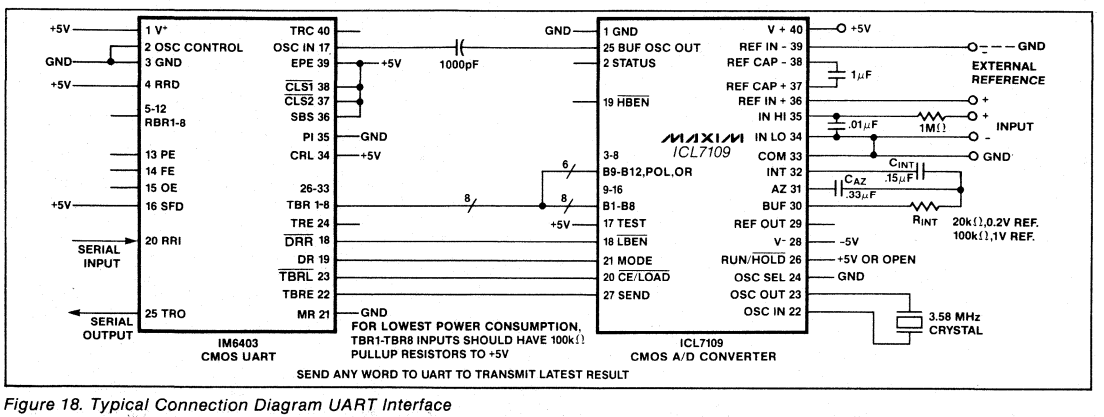
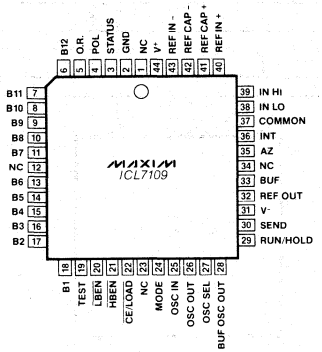


Figure 18. Typical Connection Diagram UART Interface

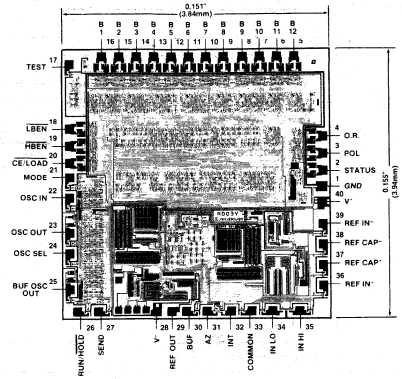
12 Bit A/D Converter With 3-State Binary Outputs

Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pak)

Chip Topography



MAXIM

3½ Digit A/D Converter With Display Hold

General Description

The Maxim ICL7116 and ICL7117 are 3½ digit monolithic analog to digital converters. They differ from the Maxim ICL7106 and ICL7107 in that the ICL7116 and ICL7117 have a Hold pin which makes it possible to hold or "freeze" a reading. These integrating A/D converters have very high input impedances and directly drive LCD (ICL7116) and LED (ICL7117) displays.

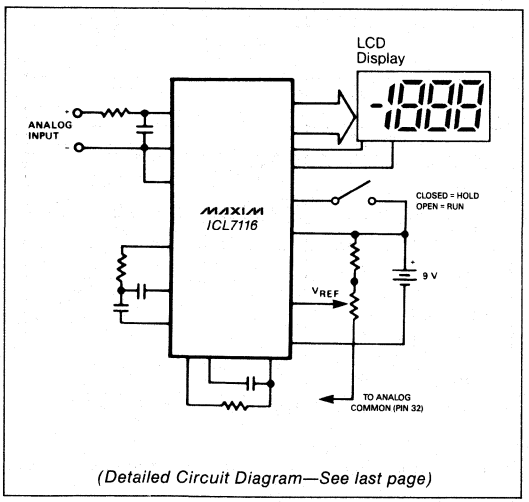
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input is particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7116 and ICL7117, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



(Detailed Circuit Diagram—See last page)

Features

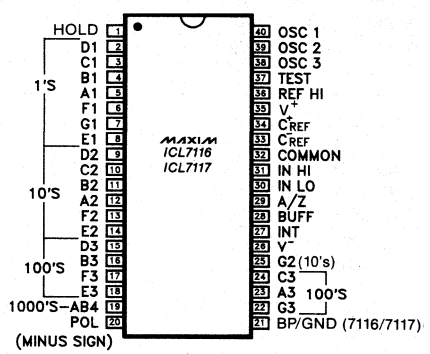
- **Improved 2nd Source! (See 3rd page of this data sheet for "Maxim Advantage™")**
- **Hold pin allows indefinite display hold.**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required: LCD-ICL7116, LED-ICL7117**
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **Zero Input Gives Zero Reading**
- **True Polarity Indication for Precision Null Applications**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7116CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7116CJL	0°C to +70°C	40 Lead CERDIP
ICL7116CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7116C/D	0°C to +70°C	Dice
ICL7117CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7117CJL	0°C to +70°C	40 Lead CERDIP
ICL7117CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7117C/D	0°C to +70°C	Dice

Pin Configuration

Top View



See last page for Plastic Chip Carrier Pin Configuration

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter With Display Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7116, V^+ to V^- 15V
- ICL7117, V^+ to GND ..... +6V
- ICL7117, V^- to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7116 ..... TEST to V^+
- ICL7117 ..... GND to V^+

Power Dissipation (Note 2)
- Cerdip Package 1000mW
- Plastic Package 800mW

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0, 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- supply current 7107 only			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ −1.5			V
7116 ONLY (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4 4	5 5	6 6	V
7117 ONLY (Except Pin 19) Segment Sinking Current (Pin 19 only)	V^+ = 5.0V Segment voltage = 3V	5 10	8.0 16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion. (See Maxim's ICL7106/ICL7107 data sheet).

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

3½ Digit A/D Converter With Display Hold

- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 8)**
- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Negligible Hysteresis**
- **Maxim Quality and Reliability**
- **Increased Maximum Rating for Input Current (Note 9)**

ABSOLUTE MAXIMUM RATINGS:

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS:

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1 (ICL7116), Figure 2 (ICL7117) unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 7) **0° ≤ T_A ≤ 70°C (Note 11)**	−000.0 **−000.0**	±000.0 **±000.0**	+000.0 **+000.0**	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 7) **0° ≤ T_A ≤ 70°C (Note 11)**	999 **998**	999/1000 **999/1000**	1000 **1001**	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV T_A = 25°C (Note 7) 0° ≤ T_A ≤ 70°C (Note 11)	−1	±.2 ±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0, T_A = 25°C (Note 7) **0° ≤ T_A ≤ 70°C**		1 **20**	10 **200**	pA
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 7)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 7)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7117)	V_{IN} = 0 T_A = 25°C **0° ≤ T_A ≤ 70°C**		0.6	1.8 **2**	mA
V^- Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply		75		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ −1.5			V
7116 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7117 Only—Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA mA
7116 Only—Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	**V**
Overload Recovery Time (Note 10)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	**Measurement Cycles**

Note 7: Test condition is V_{IN} applied between pins IN-HI and IN-LO. i.e., 1MΩ resistor in Figures 1 and 2.
Note 8: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std 883C, Method 3015 .2)
Note 9: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).
Note 10: Number of measurement cycles for display to give accurate reading.
Note 11: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter With Display Hold

Detailed Description

The Maxim ICL7116 and ICL7117 3½ digit A/D converter are similar to the Maxim ICL7106 and ICL7107, except for the addition of a Hold pin. For a detailed product description, package dimensions, and applications information (other than the operation of the Hold pin described below) refer to Maxim's ICL7106 and ICL7107 data sheet.

Hold Input

The Hold input is a digital input with a logic threshold approximately midway between V^+ and Test (ICL7116) or V^+ and Ground (ICL7117). The ICL7116/7117 continuously performs conversions, independent of the Hold input. When the Hold input is connected to V^+, however, the display latch pulse is inhibited, and the display latches are not updated. The Hold input has a 70 kilohm pulldown resistor to Test (ICL7116) or Ground (ICL7117) and the Hold input will be pulled low if it is left open. When Hold is low the ICL7116/ICL7117 updates the display at the end of each conversion. The Hold input is CMOS compatible, and can also be driven by a switch connected to V^+ (Figure 1 and 2) or by a PNP transistor.

Unlike the ICL7106 and ICL7107, the ICL7116 and ICL7117 do not have a Reference Low input. Apply the reference voltage between Reference High (REF HI) and Common.

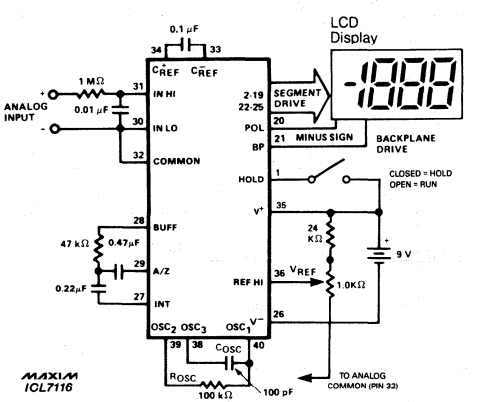


Figure 1. Maxim ICL7116 Typical Operating Circuit, 200mV Reference

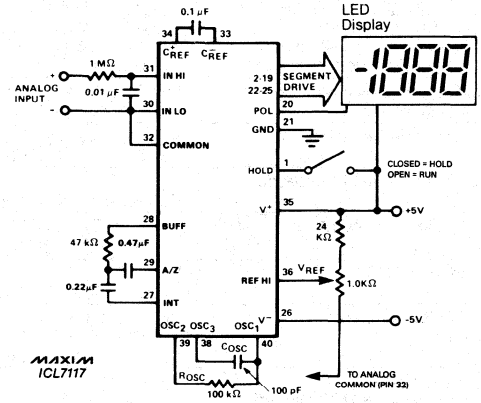
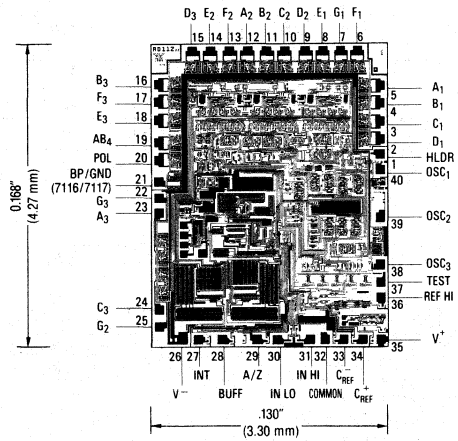
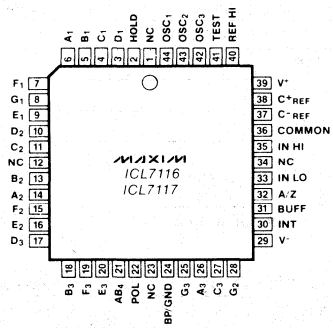


Figure 2. Maxim ICL7117 Typical Operating Circuit, 200mV Reference

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

MAXIM

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7126 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7126 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7126 a superior device, especially for portable systems.

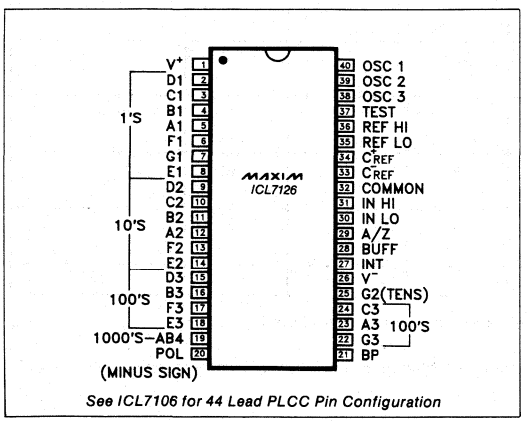
Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7126 eliminates overrange hangover and hysteresis effects. The Zero Integrator phase also allows the use of larger auto zero capacitors reducing noise further. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Pin Configuration



See ICL7106 for 44 Lead PLCC Pin Configuration

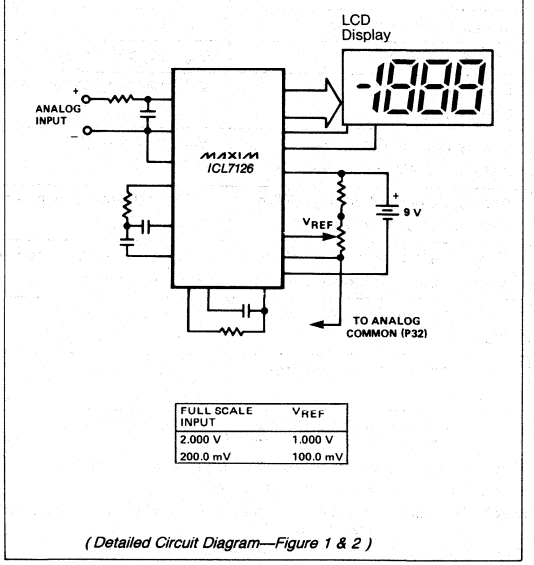
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Power dissipation guaranteed less than 1mW-9V battery life 3000 hours typical**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LCD Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7126CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7126CJL	0°C to +70°C	40 Lead CERDIP
ICL7126CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7126C/D	0°C to +70°C	Dice

Typical Operating Circuit



(Detailed Circuit Diagram—Figure 1 & 2)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 1000mW
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	-1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{CLOCK} = 16kHz and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 9)**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 10)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 8)	−000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**−000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 8)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ 200.0mV T_A = 25°C (Note 8) 0° ≤ T_A ≤ +70°C (Note 12)	−1	±.2 ±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		5		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		µV
Input Leakage Current	V_{IN} = 0 T_A = 25°C (Note 8)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0 T_A = 25°C		60	100	µA
	0° ≤ T_A ≤ +70°C			**120**	
Analog Common Voltage (with respect to Pos. Supply)	**250kΩ between Common & Pos. Supply**	**2.6**	**2.8**	**3.2**	**V**
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	**With respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	**V_{IN} changing from ± 10V to 0V**		**0**	**1**	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO through a 1MΩ series resistor as shown in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.

Low Power, 3½ Digit A/D Converter

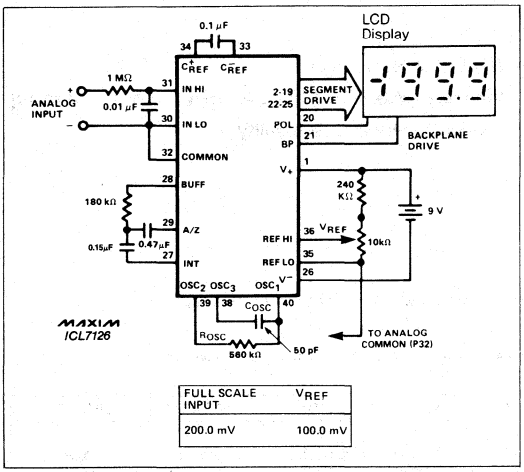


Figure 1. Maxim ICL7126 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)

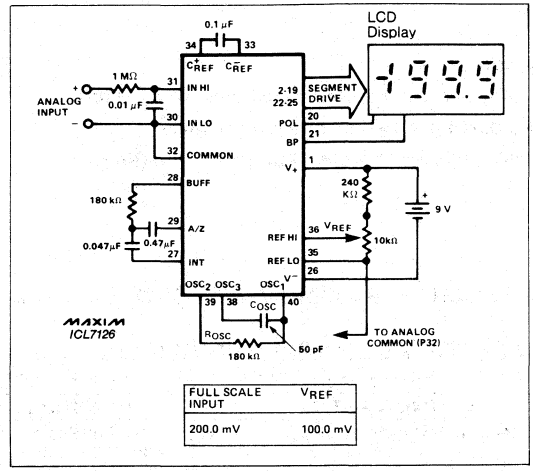


Figure 2. Maxim ICL7126 Typical Operating Circuit Clock Frequency 48kHz (3 readings/sec)

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

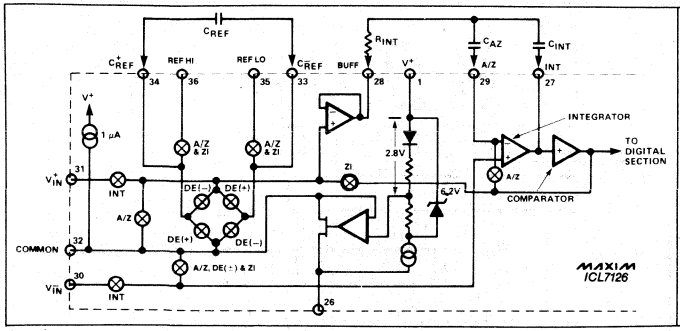


Figure 3. Analog Section ICL7126

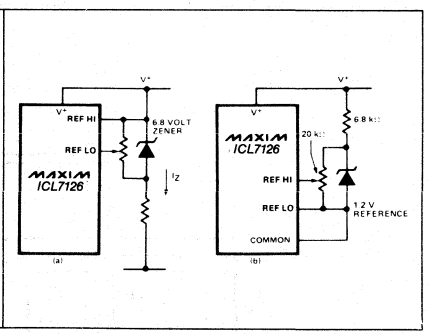


Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 µA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 µA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7126. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.

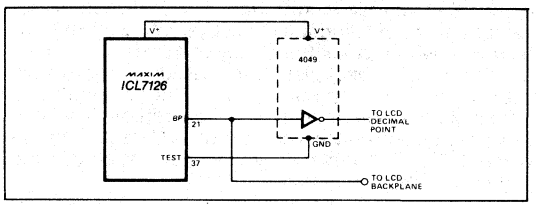


Figure 5. Simple Inverter for Fixed Decimal Point

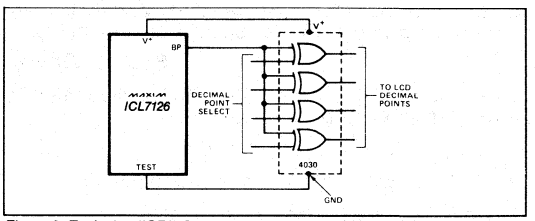


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Low Power, 3½ Digit A/D Converter

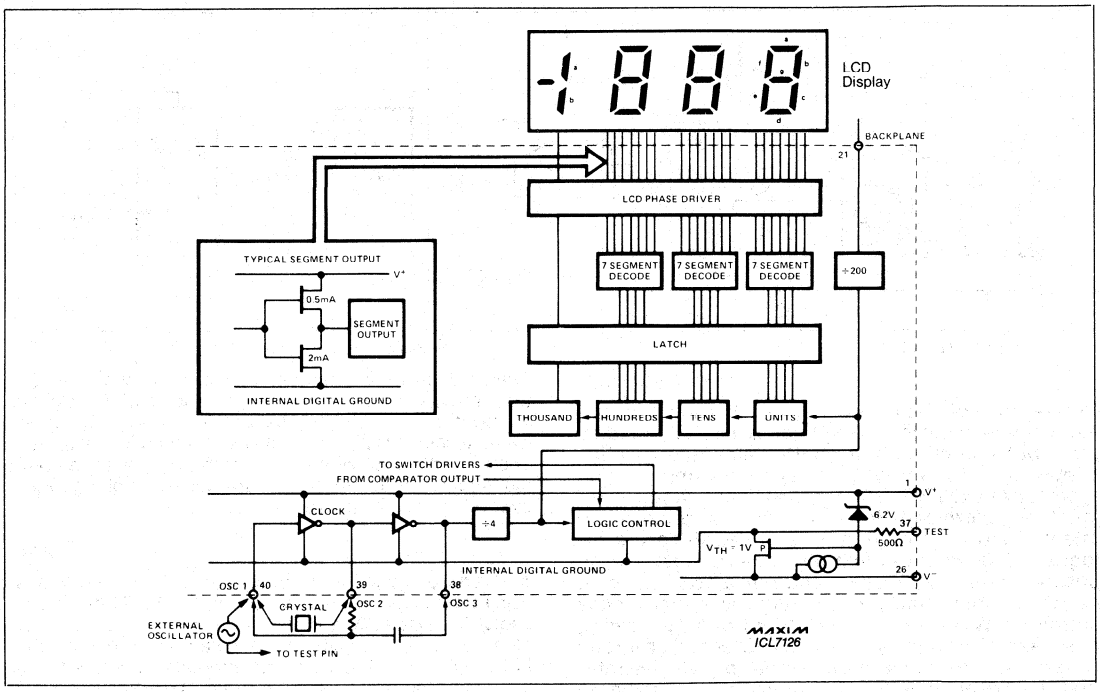


Figure 7. ICL7126 Digital Section

Digital Section

The digital section for the ICL7126 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7126. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7126 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80khZ, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000) clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a 0.1μF capacitor is adequate. While the Maxim ICL7126 will operate with a 0.33μF capacitor, a 0.47μF capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held to half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is 0.15μF at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 6μA of quiescent current and can supply 1μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 180kΩ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. A suitable value of the integrating resistor would be 330kΩ. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Typical Applications

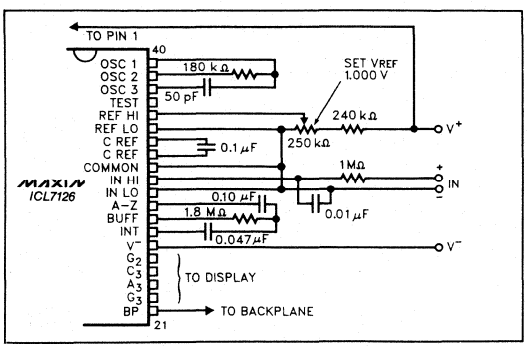


Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.

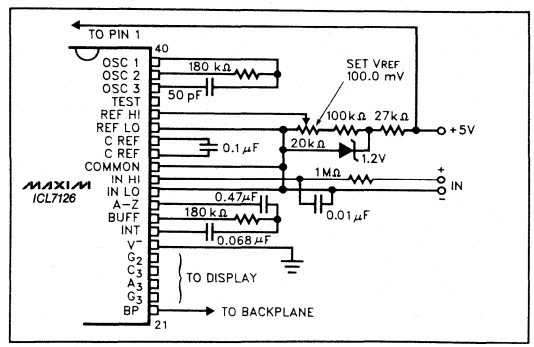


Figure 9. 7126 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V⁺ and V⁻ is insufficient for correct operation of the internal reference.

Low Power, 3½ Digit A/D Converter

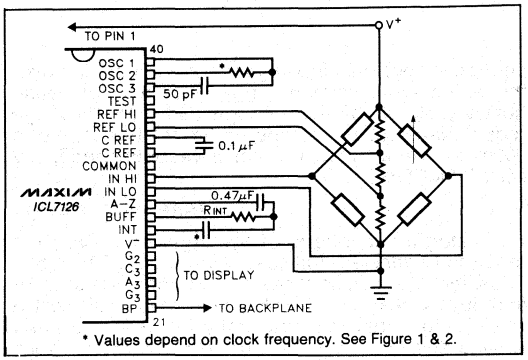


Figure 10. 7126 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

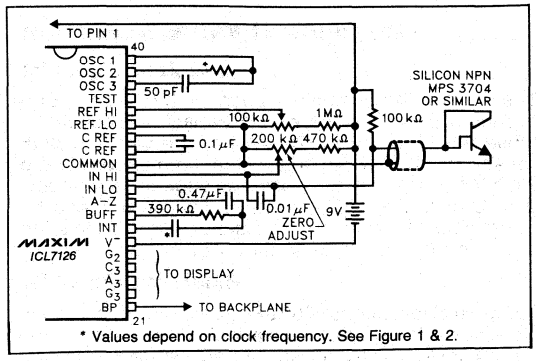
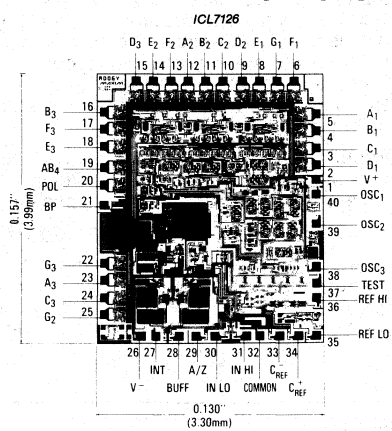


Figure 11. 7126 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/° C/. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

Chip Topography



MAXIM

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

General Description

The Maxim ICL7129A/MAX7129 is a high precision monolithic 4-1/2 digit A/D converter that directly drives a multiplexed liquid crystal display. Using a novel "successive integration" technique, the ICL7129A/MAX7129 has a ±20,000 count resolution on both 2.00000V and 200.00mV ranges. It features high impedance differential inputs, excellent differential linearity, true ratiometric operation and auto polarity. The only external active component required to make precision DVM/DPMs is a reference. The overrange and underrange outputs and the 10:1 range changing input facilitate the design of autoranging systems. The ICL7129A/MAX7129 detects and flags a LOW BATTERY condition and also checks for continuity, giving a visual indication and a logic level output which can be used to generate an audible signal.

The MAX7129 has a fullscale accuracy of 0.0005%, resolution of 10μV, zero reading drift of 0.5μV/°C, an input bias of 10pA max, and a rollover error of less than 1 count. Maxim has reduced the noise of the ICL7129A to 3μV—significantly lower than the MAX7129.

Applications

This device can be used for a wide range of precision digital voltmeter, multimeter and panelmeter applications. Most applications involve the measurement and display of analog data:

Pressure	Weight
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

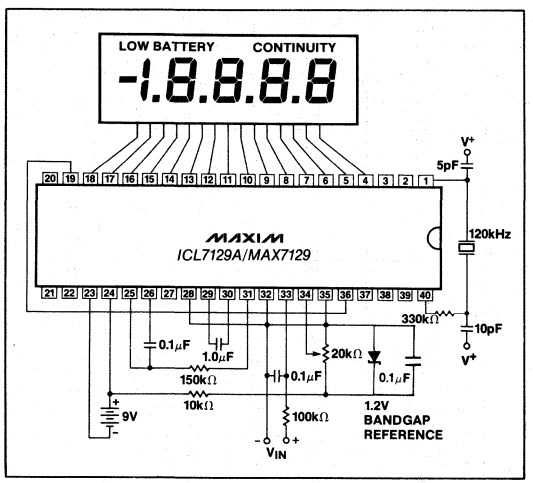
Features

- ±19,999 Count Resolution
- 10pA Max Input Bias Current (MAX7129)
- 3μV peak to peak noise (ICL7129A)
- Onboard Multiplexed LCD Display Driver
  4-1/2 Digits, 4 Decimal Points, 3 Annunciators
- Instant Continuity Detector
- Low Battery Detector and Indicator
- Overrange/Underrange Outputs
- Precise 10:1 Range Select
- 10μV Resolution
- Significantly improved ESD protection
- Monolithic, Low Power CMOS Design
- Eliminates Need for Compensation Capacitor

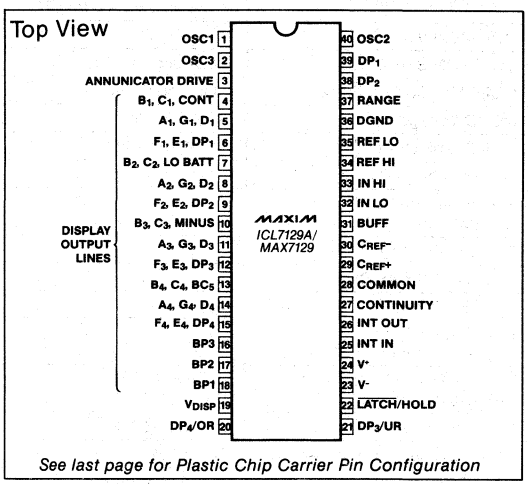
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX7129CPL	0°C to +70°C	40 Lead Plastic DIP
MAX7129CJL	0°C to +70°C	40 Lead CERDIP
MAX7129CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX7129C/D	0°C to +70°C	Dice
ICL7129ACPL	0°C to +70°C	40 Lead Plastic DIP
ICL7129ACJL	0°C to +70°C	40 Lead CERDIP
ICL7129ACQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7129AC/D	0°C to +70°C	Dice

Typical Operating Circuit



Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... V^+ to DGND - 0.3V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to V^+
Analog Input Pins
25, 29, 30 ..... V^+ to V^-

Power Dissipation (Note 2)
CERDIP package 1000mW
Plastic package 800mW
Plastic Chip Carrier
(Quad) Package 700mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Soldering Temperature (10 sec.) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX7129)

(V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C		±0.5		µV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 0.10000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN}$ = $+V_{IN}$ = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) - 0.5	V
Noise (p-p Value not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale		7.0		µV
Input Leakage Current	V_{IN} = 0V, IN HI V_{IN} = 0V, IN LO		1 3	10 40	pA pA
Scale Factor Tempco	V_{IN} = 199mV, 0°C ≤ T_A ≤ +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V	0.1	2.0		mA
COMMON Source Current	ΔCommon = -0.1V	1	9	15	µA
DGND Voltage	V^+ to Pin 36	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	0.5	1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current			1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate			100		Hz
V_{DISP} Resistance	V_{DISP} to V^+	20	50	100	kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	 400	mV mV
Pull-Down Current	Pins 37, 38, 39	0.25	2	10	µA
"Weak Output" Current	Pin 20, 21	0.25	3/3	10	µA
Sink, Source	Pin 27 Sink/Source	0.25	3/9	15	µA
Pin 22 Source Current Pin 22 Sink Current		1 0.25	40 3	100 10	µA µA

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS (ICL7129A)

(V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted. Test Circuit without C_C.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C		±0.5		µV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 0.10000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN}$ = $+V_{IN}$ = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) - 0.5	V
Noise (p-p Value not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale		3.0	(Note 4)	µV
Input Leakage Current	V_{IN} = 0V, IN HI V_{IN} = 0V, IN LO		13 15	20 40	pA
Scale Factor Tempco	V_{IN} = 199mV, 0°C ≤ T_A ≤ +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V	0.1	2.0		mA
COMMON Source Current	ΔCommon = -0.1V	1	9	15	µA
DGND Voltage	V^+ to Pin 36, V^+ to V^- = 9V	4.2	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	0.5	1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current	V^+ to V^- = 9V		1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate	f_{CLK} = 120kHz		100		Hz
V_{DISP} Resistance	V_{DISP} to V^+	20	50	100	kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	 400	mV mV
Pull-Down Current	Pins 37, 38, 39	0.25	2	10	µA
"Weak Output" Current	Pins 20, 21	0.25	3/3	10	µA
Sink, Source	Pin 27 Sink/Source	0.25	3/9	15	µA
Pin 22 Source Current Pin 22 Sink Current		1 0.25	40 3	100 10	µA µA

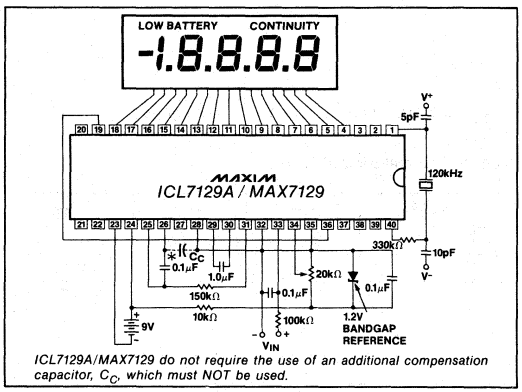
Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±400µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±mA.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Note 3: All pins on Maxim's MAX7129 and ICL7129A are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883, Method 3015.1)

Note 4: The Maxim ICL7129A uses innovative noise reduction techniques to achieve a 3µV noise level. This ensures that for any specific input voltage, the ICL7129A continuously displays one number or fluctuates between two adjacent numbers. In no case will the ICL7129A display three different numbers for a constant input voltage.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver



ICL7129A/MAX7129 do not require the use of an additional compensation capacitor, C_C, which must NOT be used.

Figure 1. MAX7129/ICL7129A Test Circuit

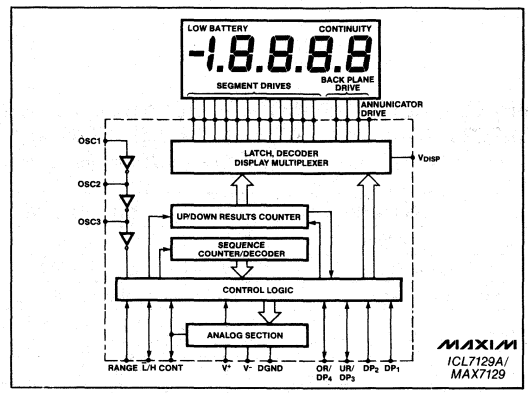


Figure 2. Simplified Block Diagram of MAX7129/ICL7129A Digital Section

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, G_4, D_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative supply for display drivers.
20	DP_4/OR	INPUT: Turns on most significant decimal point when HI. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: When floating, MAX7129/ICL7129 significant decimal point when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{LATCH}$/HOLD	INPUT: When floating, ICL7129 operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used as a converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive supply for display drivers.
25	INT IN	Integrator amplifier input.
26	INT OUT	Integrator amplifier output.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc.
29	$C_{REF}+$	Positive side of external reference capacitor.
30	$C_{REF}-$	Negative side of external reference capacitor.
31	BUFFER	Buffer amplifier output.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input.
35	REF LO	Negative reference voltage input.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. Turns on least significant decimal point when HI.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

Table 1. PIN ASSIGNMENTS AND FUNCTIONS

Detailed Description

Conversion Technique

The ICL7129A/MAX7129 differs from earlier integrating A/Ds in two ways. First, it uses a variant of the dual-slope method called "successive integration." Secondly, it uses digital autozeroing rather than an analog autozero loop requiring an external autozero capacitor. Earlier converters stored an offset correction voltage on the autozero capacitor. Although this method worked well for 100μV resolution A/Ds, the autozero loop resulted in greatly increased noise in the earlier generation of integrating A/Ds, making them unsuitable for 10μV resolution systems. The ICL7129A/MAX7129 eliminates the autozero capacitor and the noise associated with the autozero loop by performing two conversions with 5½ digit resolution. The first conversion is performed with the A/D connected to the external inputs, Input HI and Input LO. The second conversion is performed with the A/D inputs internally shorted together. The results of this second conversion, which is proportional to the A/D's offset, is digitally subtracted from the first reading to generate an offset-corrected, autozeroed measurement result.

The ICL7129A/MAX7129 enhances the dual slope conversion technique through multiple dual slope conversions, with each successive conversion having 10 times the resolution of the preceding conversion. The key to this "successive integration" technique is the multiplication of the residual voltage on the integrator capacitor after each conversion. The ICL7129A/MAX7129 first performs a 3½ digit dual slope conversion. The De-integration cycle terminates on the next positive clock edge after the integrator output crosses zero, leaving a small residue of voltage on the integrator capacitor. Unlike other A/D convertors, the ICL7129A/MAX7129 multiplies this residue by a factor of 10, then performs another dual slope conversion. Since the residue on the integrator capacitor has been multiplied by 10 the resolution of the second De-integration cycle is also increased by a factor of 10, and the ICL7129A/MAX7129 achieves 4½ digit resolution during the second De-integration cycle. The integrator capacitor residue left after the second De-integration cycle is again multiplied by 10, and the ICL7129A/MAX7129 performs a third De-integration cycle, this time with 5½ digit resolution.

Figure 2 shows a simplified block diagram of the ICL7129A/MAX7129 digital section. The sequence counter/decoder section keeps track of the many separate phases required for each conversion cycle and provides timing signals to the control logic. The sequence counter runs continuously and is independent of the up/down results counter, which is activated only when the integrator is De-integrating. The data remaining in the results counter at the end of a conversion is latched, decoded and multiplexed to the liquid crystal display.

Figure 3 shows a block diagram of the analog section including all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the conversion cycle. The reference switching and input schemes are very similar to those in other less accurate, integrating A/D converters. A typical waveform on the integrator output is illustrated

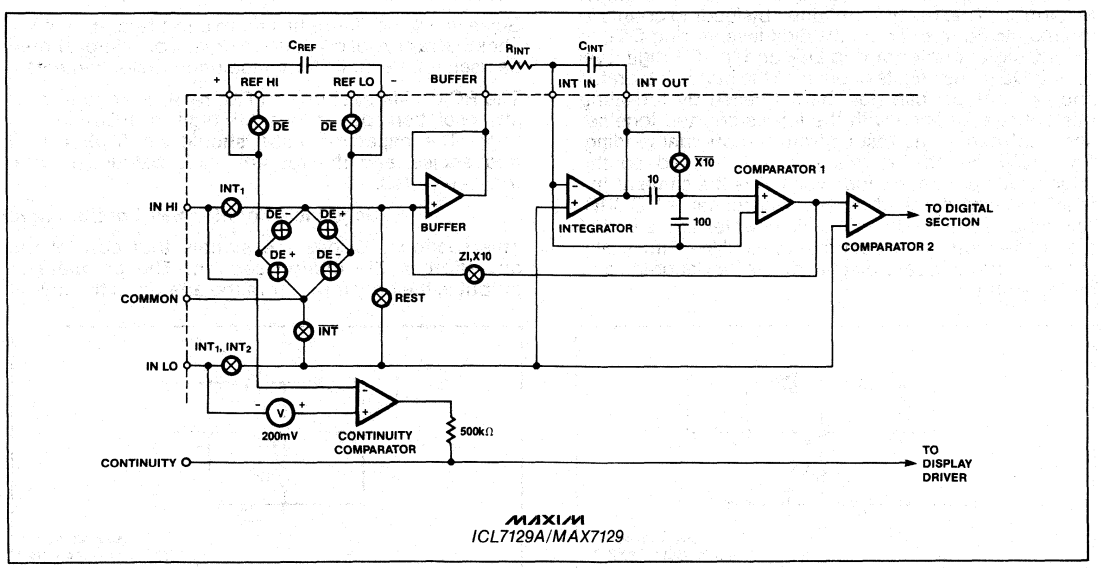


Figure 3. Analog Section Block Diagram

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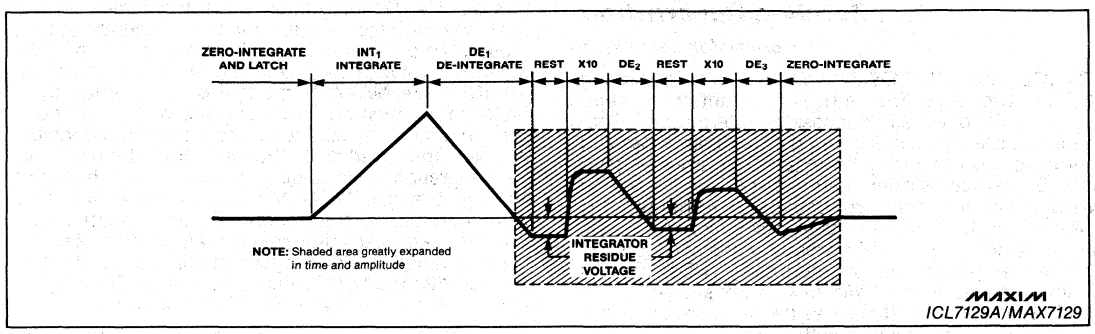

Figure 4. Integrator Waveform for a Negative Input Voltage

in Figure 4. INT_1 refers to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage. In the De-integrate phases, DE_1, DE_2, and DE_3, the reference capacitor is connected to the buffer amplifier and the integrator ramps back down towards Common, the level at which it started integrating. Since the De-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129A/MAX7129 amplifies this overshoot by -10 in the X10 phase and DE_2 begins. Similarly DE_2's overshoot is amplified by -10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This result is obtained by feeding counts to the results counter at the 3½ digit level during DE_1, to the 4½ digit counter during DE_2 and the 5½ digit level during DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted together and subtracting the results from the original reading. The INT_2 switch for this phase is closed so the integrator's common mode voltage is the same as the measurement cycle, thus ensuring excellent CMRR. The data in the up/down results counter at the end of the conversion cycle, accurate to 0.005% of full scale, is sent to the onboard display driver for decoding and multiplexing.

Digital Section

Oscillator and Clock Generator

The ICL7129A/MAX7129 has an oscillator suitable for either crystal or RC operation. The oscillator's output is internally divided by two to generate a system clock with a precise 50% duty cycle. All references to clock cycles in this data sheet refer to the system clock, which is half the frequency of the oscillator.

The crystal oscillator shown in Figure 5A is recommended for most applications. The crystal frequency should be 120kHz for maximum normal mode rejection at 60Hz, and 100kHz for maximum normal mode rejection at 50Hz.

Since an RC oscillator has more short term frequency jitter than a crystal oscillator, a crystal oscillator should be used for 4½ digit, 10μV resolution measurements.

The RC oscillator shown in Figure 5B is adequate for low resolution applications, (3½ digits at 100μV resolution). The capacitor value should be 51pF for all frequencies, and the resistor value calculated from $f_{OSC} = 0.45/RC$.

Sequence Counter and Control Logic

This section provides the signals that control the operation of the analog section. The comparator output is the only input from the analog to the digital

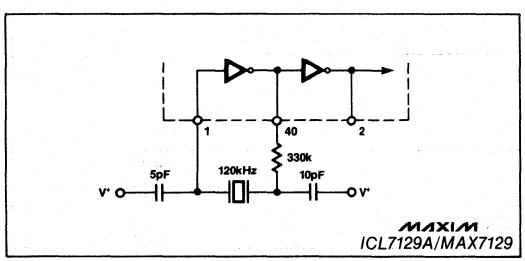

Figure 5A. Crystal Oscillator Circuits

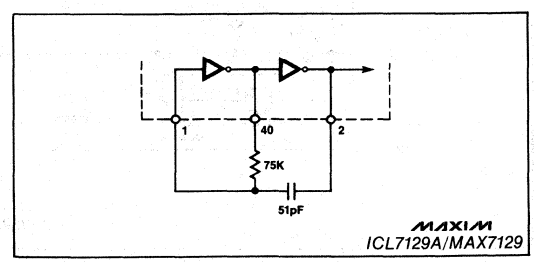

Figure 5B. RC Oscillator Circuit

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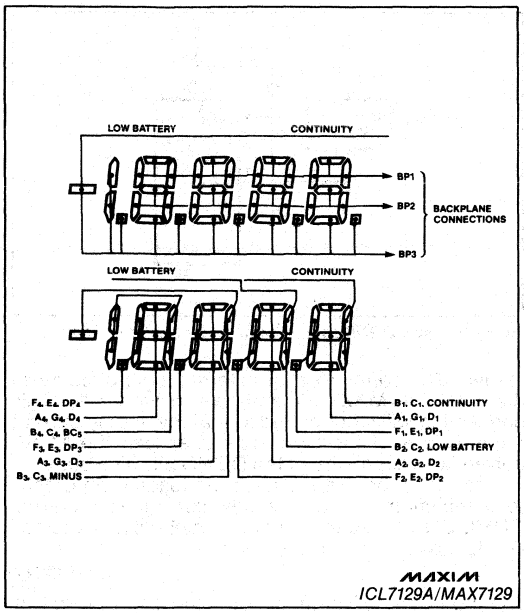


Figure 6. Triplexed Liquid Crystal Display Layout

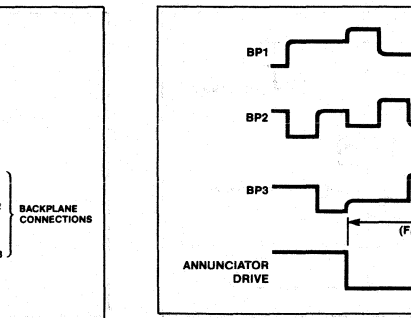


Figure 7. Backplane and Annunciator Drive Waveforms

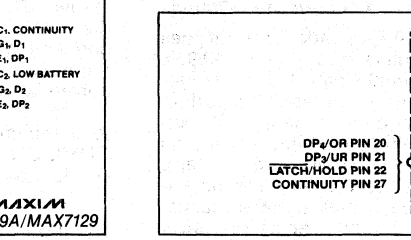


Figure 8. "Weak Output" Digital I/O Pins

section. The digital section uses the comparator output to determine the polarity of the integrator's output and to gate clock counts into the Up/Down Results Counter. The control logic also responds to the external digital inputs: Range, Hold, and Continuity. It also generates the digital outputs: Overrange, Underrange, Latch, and Continuity.

Display Driver

The ICL7129A/MAX7129 can be used to drive a triplexed liquid crystal display with three backplanes. In addition to driving 4½—7 segment digits, the ICL7129A/MAX7129 can directly drive the decimal points, polarity sign, "Continuity," and "Low Battery" annunciators. Figure 6 shows the assignment of the 36 display segments to the three backplanes and 12 segment drive lines. The ICL7129A/MAX7129 divides the oscillator frequency by 1200 to generate the backplane frequency, resulting in a backplane frequency of 100Hz with a 120kHz oscillator crystal or 83.3Hz with a 100kHz crystal. Figure 7 shows the backplane and annunciator output waveforms.

Range Input

With a 1V reference, the ICL7129A/MAX7129 has a 2V full scale when the Range input is high and a 200mV full scale when the Range input is low or open. The ICL7129A/MAX7129 achieves a precise 10:1 change in scale factor by reducing the integration period from 10,000 clock cycles on the 200mV range to 1000 clock cycles on the 2V range.

Digital I/O Pins

Four of the ICL7129A/MAX7129's pins are quasi-directional and can be used as either inputs or outputs. As shown in Table 1, DP4/OR, DP3/UR, Latch/Hold, and Continuity each have dual input/output functions. Figure 8 shows a simplified schematic of these input/output pins. Since there is approximately 500kΩ in series with these outputs, they can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. Since the output drive current is limited to only a few microamps, the outputs are easily overdriven by 4000 series CMOS when the pin is used as an input.

Latch/Hold

The Latch/Hold pin puts out a low-going pulse during the last 100 clock cycles of each conversion. This low-going pulse latches the conversion data into the onboard display driver section. The ICL7129A/MAX7129 will not update the display, and the display will continue to show the previous reading if the Latch/Hold pin is held high. If the Latch/Hold pin is held low, the display latches are transparent and the counting of the sequence counter can be observed during the de-integrating phases.

OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are valid on the falling edge of Latch/Hold and remain in that state until the end of the next conversion cycle.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

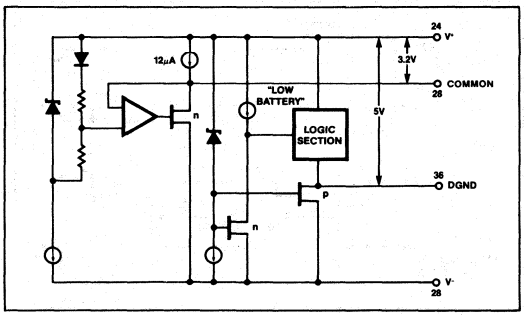


Figure 9. DGND and Common Outputs

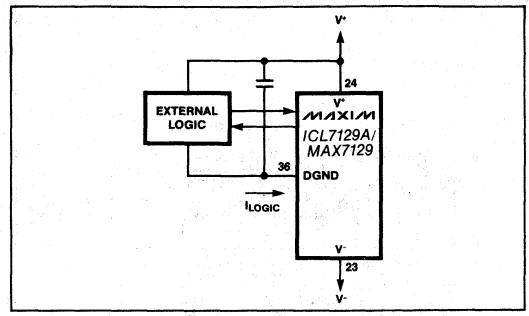


Figure 10. Using DGND as Supply Voltage for External Logic

Overrange and Underrange Outputs

The DP4/OR (Decimal Point 4/Overrange) output goes high if the measurement result is greater than ±19,999. Similarly, the DP3/UR (Decimal Point 3/Underrange) output goes high if the measurement result is less than ±1000. These signals are updated at the end of each conversion, unless Latch/Hold is held high. These pins are also inputs that control the decimal points, DP3 and DP4. A high level input on these pins turns on the decimal point segments of the display. If these decimal points are not required, they can be used as logic level controlled annunciators.

Continuity

An internal comparator with a 200mV threshold is connected directly between the INPUT HI and INPUT LO pins of the ICL7129A/MAX7129 (see Figure 3). The Continuity output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This activates the Continuity annunciator on the display. The Continuity annunciator can also be controlled by an external source if desired, since the Continuity pin is one of the four quasi-bidirectional pins of the ICL7129A/MAX7129. A pull-down resistor connected between Continuity and DGND (pin 36) disables the continuity function when it is not desired.

Analog Section

Common, Digital GrouND, and Low Battery

Figure 9 shows how the Common and DGND (Digital GrouND) outputs of the ICL7129A/MAX7129 are generated from internal zener diodes. Common can be used to set the common mode voltage in applications where the input signals float with respect to the ICL7129A/MAX7129's power supplies, which is typical for battery powered applications. Common can also function as a pre-regulator for an external precision reference voltage source.

The voltage between V^+ and DGND is the internal supply voltage for the logic section of the ICL7129A/MAX7129. Both Common and DGND are capable of sinking current from external loads, but care should be taken to ensure that these outputs are not overloaded. The connection of external logic circuitry to the ICL7129A/MAX7129 is shown in Figure 10. This connection will work provided that the supply current requirements of the logic do not exceed the 1.2mA current sink capability of the DGND pin. The buffer in Figure 10 can be used to keep the loading on DGND to a minimum if more supply current is required. COMMON can source approximately 12μA whereas DGND has no source capability.

Low Battery

The "Low Battery" annunciator of the display turns on when the supply voltage between V^+ and V^- drops below 7.2V. The exact point at which this occurs is determined by the 6.3V zener diode and threshold voltage of the n-channel transistor connected to the V^- rail shown in Figure 9.

Buffer

The ICL7129A/MAX7129 buffer has a common mode input voltage range of V^- + 1.5V to V^+ - 1.0V and can supply up to 20μA of output current.

Integrator

The integator can swing to within 0.3V of the supply rails while delivering 20μA of output current. It should also be noted that, unlike the ICL7129, Maxim's ICL7129A/MAX7129 provides stable operation without the need for an additional capacitor between the Integrator Output and Common pins. The compensation cap used with the ICL7129 must be omitted for correct operation of the ICL7129A/MAX7129.

X10 Amplifier

The X10 ("times ten") amplifier provides a precise gain of -10, without using any external components. This amplifier, unique to the "successive integrator" A/D, is used to multiply the residue left on the integrator capacitor after the DE_1 and DE_2 phases.

Comparator

The comparator has the high gain and bandwidth needed to rapidly detect zero crossing. The comparator's output is used by the digital control logic to select the correct polarity for De-integration, and to gate clock pulses into the up/down results counter during the De-integration phases.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

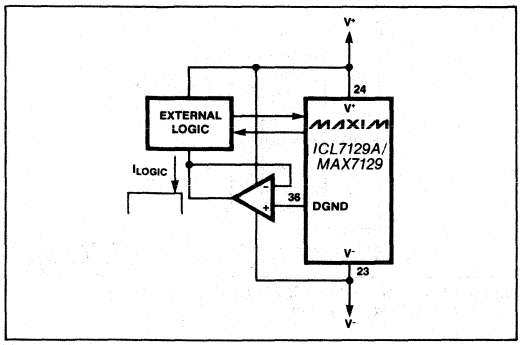


Figure 11. DGND Buffer

Component Selection

Integrating Resistor

Optimum linearity is obtained by choosing the integrating resistor value is chosen so that the buffer's maximum output current is between 5 and 20μA. The quiescent current of the buffer is 70μA, and can supply 13μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the optimum value of integrating resistor can be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{13\mu A} = \frac{2V}{13\mu A} = 150k\Omega$$

Too high a value for the integrating resistor increases the sensitivity to noise pickup and increases errors caused by stray leakage currents. Too low a value degrades integral linearity by attempting to draw more current from the buffer and integrator than they can provide without degrading linearity.

Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as

$$Vswing = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

where $I_{INT} = 13\mu A$ if R_{INT} is chosen as described above and T_{INT} = 1,000 clock periods (16.7ms for 120kHz oscillator frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. The integrator will not saturate unless its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. Since Common is a approximately 3V below V^+, the integrator swing should be 2V. Substituting these values in the above formula, C_{INT} can now be calculated as:

$$C_{INT} = \frac{13.3\mu A \times 16.7ms}{2V} = 0.1\mu F$$

Too low a value for C_{INT} increases integrator swing to the point where the integrator saturates and causes integral linearity errors. Too high a value for C_{INT} reduces the integrator swing range and increases the effect of comparator noise. If a positive common mode voltage is applied to IN LO the value of C_{INT} must be reduced to keep the integrator output voltage at least 1V below V^+.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the Input HI is a good indication of the amount of dielectric absorption in the integrator capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon™ capacitors. In less critical applications polystyrene and polycarbonate capacitors may also be used.

Reference Capacitor

The reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are required only where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in digital multimeters.

The reference capacitor must be a low leakage capacitor since it stores the reference voltage while floating during both the Integrate and De-integrate phases. Any leakage or charge loss during these phases causes a change in the scale factor of the ICL7129A/MAX7129. Low cost film capacitors such as polyester or polystyrene are suitable for most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. In most applications the Ref Lo Input terminal is connected to Common, and the Ref Hi Input is 1V above Common. During the integration and idle phases the reference capacitor is connected to the Reference Inputs (C_{REF}^+ to Ref Hi and C_{REF}^- to Ref Lo). At the end of the integration phase the comparator determines the polarity at the integrator output and the digital section closes analog switches so that the reference capacitor is connected to Common and the buffer input with a polarity such that the integrator output will return toward Common during the De-integrate phase. A negative input signal during the integrate phase drives the integrator output positive and the ICL7129A/MAX7129 digital section will connect the C_{REF}^- terminal to Common during the De-integrate phase. Since the C_{REF}^- terminal was also connected to Common during the Integrate phase, the C_{REF} terminals do not change voltage during the transition from Integrate phase to De-integrate phase. If, however, the input voltage during the Integrate phase is positive, the ICL7129A/MAX7129 digital section will connect the Ref Cap^+ terminal to Common. In

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

this case the two terminals of the reference capacitor both move 1V more negative. Any stray capacitance on the reference capacitor terminals must also be charged during the 1V movement, thereby reducing the voltage on the reference capacitor and changing the scale factor for positive input voltages. This error, called "rollover error" can be reduced to less than 1 count by using a reference capacitor value of 1μF or greater.

Crystal Oscillator Components

The ICL7129A/MAX7129 crystal oscillator is designed to work with tuning fork type crystals such as the Statek CX-1V series. The two capacitors are not critical components and can be the low cost disc ceramic type. The crystal frequency should be 120kHz to reject 60Hz normal mode signals and 100kHz to reject 50Hz normal mode signals. With these crystal frequencies the integration will be 10 cycles of the 60/50Hz signal on the 200mV range and 1 cycle on the 2V range. There is no single oscillator frequency that results in good normal mode rejection of both 50Hz and 60Hz on the 2V range, but a 100kHz oscillator frequency will reject both 50Hz and 60Hz on the 200mV scale.

Component Manufacturers

The following list of component suppliers is intended to be of assistance in identifying suitable external components for use with the ICL7129A/MAX7129. The list is not intended to be comprehensive, nor does it constitute an endorsement by Maxim of the companies listed.

Triplexed Liquid Crystal Displays

Epson America, Inc., Torrance, CA.
(213) 534-4500
Part #: LD-H7960A

Crystaloid, Inc., Hudson, OH
(216) 655-2429

Hamlin, Inc., Lake Mills, WI
(414) 648-2361

UCE, Inc., Norwalk, CT
(203) 838-7509

LXD INC, Cleveland, OH
(216) 292-3300
Part #: 353E3/8R03H

Varitronix Limited, Los Angeles, CA
(213) 661-8883
Part #: VIM-503-DP

Display Mounting Bezels

Techknits, Inc., Cranford, N.J.
(201) 272-5500

Conductive Rubber Technology, Santa Barbara, CA.
(805) 969-5807

Crystals

Statek, Inc., Orange, CA
(714) 639-7810
Part #: CX-1V 120C

Saronix, Inc., Palo Alto, CA
(415) 856-6900

Polypropylene Capacitors

West Lake Capacitors, West Lake Village, CA
(818) 889-4120

Seacor, Inc., Westwood, N.J.
(201) 666-5600

TRW Capacitors, Ogallala, NE
(308) 284-3611

Sprague Electric Co., North Adams, MA
(413) 664-4411

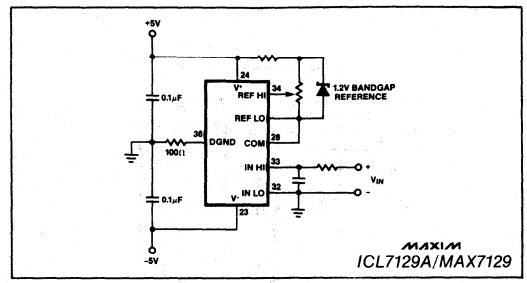


Figure 12. Powering the ICL7129A/MAX7129 from +5V and -5V Power Supplies

Applications

Power Supply

The ICL7129A/MAX7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies.

The standard battery connection using a 9V battery is shown in the Typical Operating Circuit on the front page of this data sheet.

Figure 12 shows the power connection for systems with +5V and -5V supplies. Note that measurements are given with respect to ground. COMMON is not connected to INPUT LO and is used only as a pre-regulator for the external voltage reference. Digital ground of the ICL7129A/MAX7129 (DGND, pin 36) is not directly connected to power supply ground. The ICL7129A/MAX7129's digital inputs have protective diodes to DGND and should not be driven to any voltage below DGND. This problem is handled by placing a 100Ω resistor between the ICL7129A/MAX7129's DGND terminal and the ±5V system's digital ground, which pulls down the ICL7129A/MAX7129's DGND terminal if it reaches a voltage more positive than the ±5V system's digital ground. This prevents the forward biasing of the input protection diodes. If DGND voltage is more negative than the system digital ground the 10Ω resistor will limit the amount of current that DGND sinks.

A power supply with single polarity can be used to power the ICL7129A/MAX7129 in applications where battery operation is not convenient or appropriate. Measurements must be made with respect to COMMON or some other voltage within the ICL7129A/MAX7129's input common mode range.

Voltage References

The Common output has a typical temperature coefficient of ±80ppm/°C. Since the ICL7129A/MAX7129 has a resolution of 1 count in 20,000 or 50ppm, a precision external reference is needed unless the ambient temperature is held constant. The diagram of the Typical Operating Circuit on the front page of this data sheet shows a 1.2V bandgap voltage source used as the reference for the ICL7129A/MAX7129, with Common used only as a pre-regulator for the bandgap

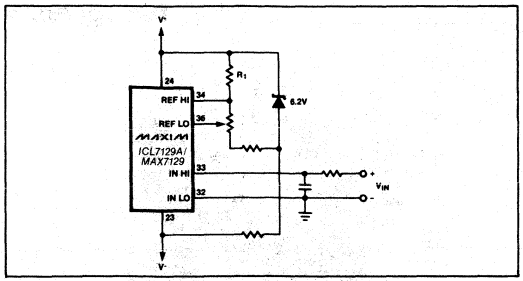


Figure 13. Using a 6.2V Reference Diode with the ICL7129A/MAX7129.

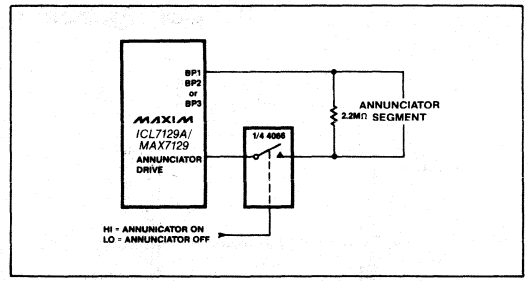


Figure 14. Externally Controlled Annunicators

reference. The ICL7129A/MAX7129 reference voltage is approximately 1.000V for both 2V and 200mV full-scale operation. To trim the reference voltage, first apply a precision 1000.05mV input voltage, then adjust the reference voltage until the display reading alternates equally between 10000 and 10001.

Figure 13 shows the ICL7129A/MAX7129 with an external 6.8V zener reference voltage.

Annunciator Drivers

The Annunciator Drive output is a square wave at the backplane frequency, swinging from V^+ to V_{DISP}. Any segment connected to Annunciator Drive will be turned on, regardless of which backplane drives that segment. Figure 14 shows how to control annunciator segments with external logic levels.

Display Voltage Compensation

An adequate display can be obtained in most applications by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is expected, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers usually specify the temperature variation of the LCD threshold voltage, which is approximately 1/3 of the optimum peak display voltage. The peak display voltage is equal to (V^+ - V_{DISP}), so a typical -4mV/°C temperature coefficient of an LCD threshold corresponds to a +12mV/°C temperature coefficient at the V_{DISP} pin. Two circuits that can be adjusted to give a temperature compensation of approximately +12mV/°C at V_{DISP} are shown in Figure 15. The diode between DGND and V_{DISP} should have a low turn-on voltage to ensure that V_{DISP} is never driven more than 300mV negative with respect to DGND.

Input Protection

The input pins of the ICL7129A/MAX7129 have protection diodes built in to protect it from electrostatic discharges (ESD) of up to 2000V (Mil Standard 883, Method 3015.1 test circuit). These diodes also protect the ICL7129A/MAX7129 from excessive input voltage overload in multimeter circuits, provided that the current into these diodes is limited to less than 1mA. The ICL7129A/MAX7129 will therefore be fully protected for input voltages up to 1000V if the input current limiting resistor is 1MΩ.

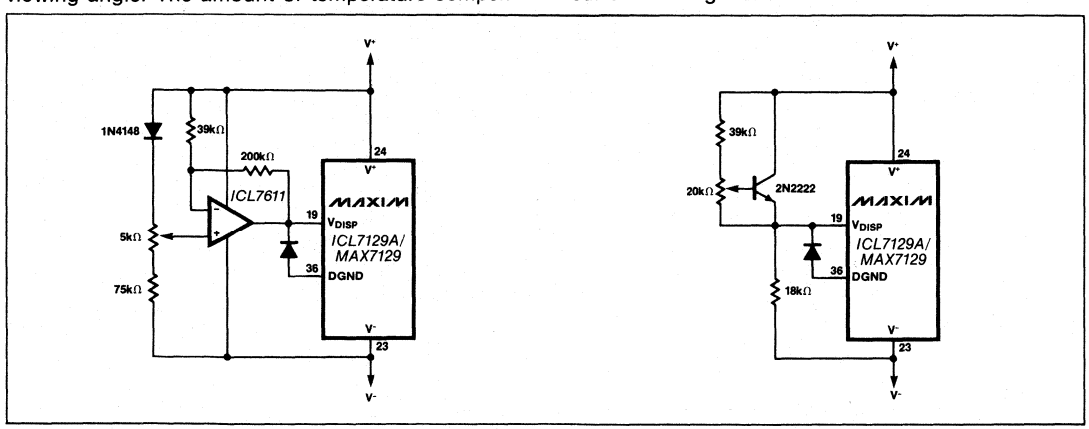
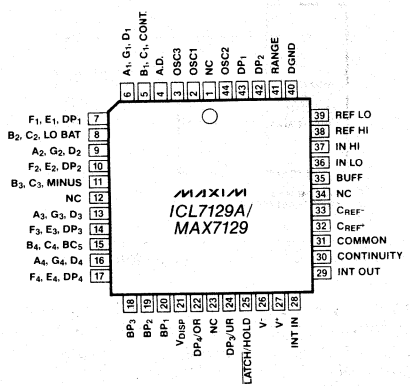


Figure 15. V_{DISP} Temperature Compensation

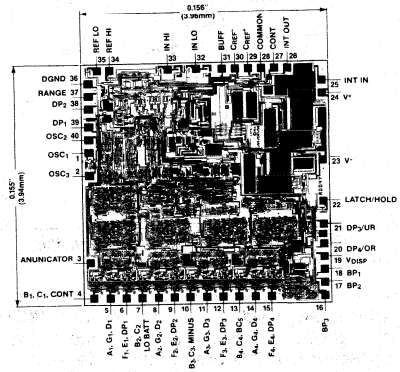
4-1/2 Digit Single-Chip A/D Converter with LCD Driver

Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pak)

Chip Topography



Substrate is Connected to V+.

MAXIM

4½ Digit A/D Converter with Multiplexed BCD Outputs

General Description

The Maxim ICL7135 is a high precision monolithic 4½ digit A/D converter. Dual slope conversion reliability is combined with ±1 in 20,000 count accuracy and a 2.0000V full scale capability. It features high impedance differential inputs, nearly ideal differential linearity, true ratiometric operation, auto zero and auto-polarity. The multiplexed BCD outputs and digit drivers provide easy interface to external display drivers like the Maxim ICM7211A. The only other external components needed to make precision DVM/DPMs are a reference and a clock. For more complex systems the BCD outputs are enhanced by $\overline{\text{STROBE}}$, OVERRANGE, UNDERRANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines providing easy interface to microprocessors and UARTs. This interfacing capability makes the ICL7135 an ideal device for use in microprocessor based data acquisition and control systems.

The ICL7135 has auto-zero accuracy better than 10μV, zero drift of 0.5μV/°C, input bias current of 10pA max. and rollover error of less than 1 count.

Features

- **Improved 2nd Source (See our "Maxim Advantage™" Page 3)**
- **±20,000 Count Resolution**
- **Guaranteed ±1 Count accuracy**
- **Over-range, under-range signals for auto-range capability**
- **Easy interface to UARTs and μPs**
- **TTL compatible, Multiplexed BCD outputs**
- **True differential input. Zero reading guaranteed for 0 volt input**
- **True polarity at zero for precise null detection**
- **Monolithic CMOS design**

Applications

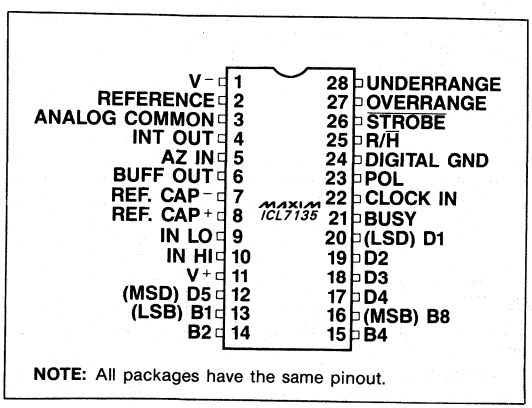
This device is used in a wide range of measurement applications involving the manipulation and display of analog data:

Pressure	Weight
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Ordering Information

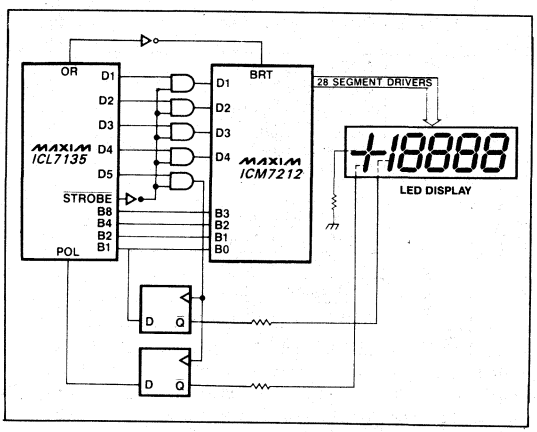
PART	TEMP. RANGE	PACKAGE
ICL7135CJI	0°C to 70°C	28 Lead CERDIP
ICL7135CPI	0°C to 70°C	28 Lead Plastic DIP
ICL7135CQI	0°C to 70°C	28 Lead Plastic chip carrier
ICL7135C/D	0°C to 70°C	Dice

Pin Configuration



NOTE: All packages have the same pinout.

Typical Operating Circuit



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

4½ Digit A/D Converter with Multiplexed BCD Outputs

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
- CERDIP Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Gnd to V^+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

(V^+ = +5V, V^- = −5V, T_A = 25°C, Clock Frequency Set for 3 Reading/Sec

		CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG (Note 1) (Note 2)		Zero Input Reading		V_{IN} = 0.0V Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
		Ratiometric Reading (2)		V_{IN} = V_{REF} Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
		Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
		Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
		Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
		Noise (P-P value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 2.000V		15		μV
		Leakage Current at Input	I_{ILK}	V_{IN} = 0V		1	10	pA
		Zero Reading Drift		V_{IN} = 0V $0° \le T_A \le 70°C$		0.5	2	μV/°C
		Scale Factor Temperature Coefficient (3)	TC	V_{IN} = +2V $0° \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL	INPUTS	Clock In, Run/$\overline{\text{Hold}}$	V_{INH} V_{INL} I_{INL} I_{INH}	 V_{IN} = 0 V_{IN} = +5V	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V mA μA
	OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OL} V_{OH}	I_{OL} = 1.6mA I_{OH} = −1mA	 2.4	0.25 4.2	0.40	V V
		BUSY, $\overline{\text{STROBE}}$ OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	I_{OH} = −10μA	4.9	4.99		V
	SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
		−5V Supply Range	V^-		−3	−5	−8	V
		+5V Supply Current	I^+	f_c = 0		1.1	3.0	mA
		−5V Supply Current	I^-	f_c = 0		0.8	3.0	
		Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
	Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

4½ Digit A/D Converter with Multiplexed BCD Outputs

- **Guaranteed 2mA Max Supply Current**
- **Key Parameters Guaranteed Over Temperature**
- **Significantly Improved ESD Protection (Note 6)**
- **Low Noise**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS Specifications below satisfy or exceed all "tested" parameters on adjacent page.

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

	Characteristics	Symbol	Conditions	Min	Typ	Max	Units
ANALOG	**Zero Input Reading**		**V_{IN} = 0.0V, Full Scale = 2.000V $0° \le T_A \le +70°C$**	**−0.0000**	**±0.0000**	**+0.0000**	**Digital Reading**
ANALOG	**Ratiometric Reading (Note 2)**		$V_{IN} = V_{REF}$, Full Scale = 2.000V $T_A = 25°C$ **$0° \le T_A \le +70°C$**	+0.9998 **+0.9995**	+0.9999 **+0.9999**	+1.0000 **+1.0005**	**Digital Reading**
ANALOG	Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
ANALOG	Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
ANALOG	Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} = +V_{IN} \approx 2V$		0.5	1	Digital Count Error
ANALOG (Note 1) (Note 2)	Noise (P-P value not exceeded 95% of time)	e_n	V_{IN} = 0V, Full Scale = 2.000V		15		μV
ANALOG (Note 1) (Note 2)	**Leakage Current at Input**	**I_{ILK}**	V_{IN} = 0V $T_A = 25°C$ **$0° \le T_A \le +70°C$**		1	10 **250**	pA **pA**
ANALOG (Note 1) (Note 2)	Zero Reading Drift		V_{IN} = 0V $0° \le T_A \le +70°C$		0.5	2	μV/°C
ANALOG (Note 1) (Note 2)	Scale Factor Temperature Coefficient (Note 3)	TC	$V_{IN} = +2V$ $0° \le T_A \le +70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
INPUTS	Clock In, Run/$\overline{Hold}$	V_{INH} V_{INL} I_{INL} I_{INH}	$0° \le T_A \le +70°C$ $0° \le T_A \le +70°C$ V_{IN} = 0 $0° \le T_A \le +70°C$ $V_{IN} = +5V$ $0° \le T_A \le +70°C$	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V V mA μA
DIGITAL OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OL} V_{OH}	I_{OL} = 1.6mA I_{OH} = −1mA	 2.4	0.25 4.2	0.40	V V
DIGITAL OUTPUTS	BUSY, $\overline{STROBE}$ OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	I_{OH} = −10μA	4.9	4.99		V
DIGITAL SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
DIGITAL SUPPLY	−5V Supply Range	V^-		−3	−5	−8	V
DIGITAL SUPPLY	**+5V Supply Current**	**I^+**	**f_C = 0 $T_A = 25°C$ $0° \le T_A \le +70°C$**		**1.1**	**2.0 3.0**	**mA mA**
DIGITAL SUPPLY	**−5V Supply Current**	**I^-**	**f_C = 0 $T_A = 25°C$ $0° \le T_A \le +70°C$**		**0.8**	**2.0 3.0**	**mA mA**
DIGITAL SUPPLY	Power Dissipation Capacitance	C_{PD}	(Note 5)		40		pF
CLOCK	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The Temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Clock Frequency" below for limitations on the clock frequency range in a system.

Note 5: +5V Supply current for $f_C \neq 0$ is $I^+ = I^+_{(f_C = 0)} + C_{PD} \times 5V \times f_C$.

Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

4½ Digit A/D Converter with Multiplexed BCD Outputs

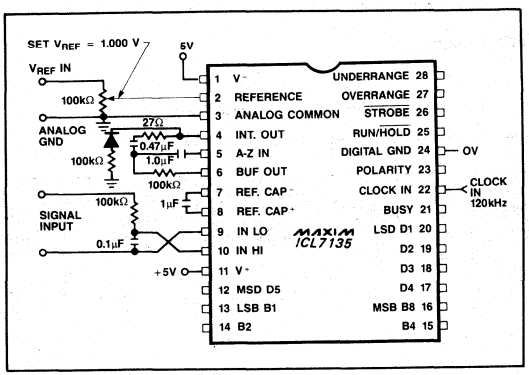


Figure 1. ICL7135 Test Circuit

Detailed Description

General Operation

The ICL7135 is divided into an Analog section and a Digital section. The digital section includes the counters, input and output interfaces, and control logic which controls the timing of each measurement cycle. Each measurement is divided into four phases: 1) auto-zero (AZ), 2) signal integrate (INT), 3) reference deintegrate (DE), and 4) zero integrator (ZI). The digital section controls the operation of the analog section during each of these phases, using counters and the state of the comparator to determine when to start each of the four phases.

Auto-Zero Phase

During auto-zero Input HI and Input LO are disconnected from the input pins and are internally shorted to Analog COMMON. The output of the comparator is connected to the inverting input of the Integrator, and at the same time the non-inverting input of the integrator is connected to the input of the buffer. This feedback loop charges the autozero capacitor, C_{AZ}, to compensate for the offset voltages of the buffer amplifier, integrator, and comparator. Also during auto-zero, the reference capacitor is connected to the voltage reference and is charged to the reference voltage. The auto-zero cycle is a minimum of 9800 clock cycles, except after an over-range reading. After an over-range, the extended zero integrate phase reduces the auto-zero phase to 3800 clock cycles.

Signal Integrate Phase

At the end of the auto-zero phase the auto-zero loop is opened, and the Input High and Input Low are switched to the external pins IN-HI and IN-LO. The analog section integrates the differential voltage between Input High and Input Low. The differential voltage must be within the ICL7135's common mode range. The voltage on the integrator capacitor at the end of signal integrate is directly proportional to the differential voltage between Input High and Input Low, and is also directly proportional to the length of the signal integrate phase. The signal integrate phase lasts precisely 10,000 clock cycles. At the end of this phase the input signal polarity is determined.

De-Integrate Phase

At the end of signal integrate, Input High and Input Low are disconnected from the external pins. The integrator non-inverting input pin is then internally connected to Analog Common and the buffer input is connected to one side of the reference capacitor. The other side of the reference capacitor is connected to Analog Common. The polarity at the output of the integrator (as detected by the comparator at the end of signal integrate phase) determines which terminal of the reference capacitor is connected to the buffer input. The reference capacitor polarity is chosen so that the integrator output will always return towards Analog Common. Since the reference capacitor was charged to the reference voltage during the auto-zero phase, the integrator input voltage is now the reference voltage. The De-Integrate phase lasts for 20,001 counts, or until the comparator detects that the integrator output has crossed zero, whichever occurs first. The time required to return to zero is proportional to the input signal and is inversely proportional to the reference voltage. The number of clock cycles required to return to zero is counted by the digital section and is latched as the measurement result.

$$\text{Displayed reading} = 10{,}000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

The last of the four phases is the zero integrator phase. The non-inverting input of the integrator is internally shorted to Analog Common and the buffer input is internally connected to the output of the comparator. This closes a loop that forces the integrator output to zero. Normally this phase lasts only 100 to 200 counts, sufficient time to remove the small residual charge on the integrator capacitor caused by the comparator delay and the one count delay created by sampling the comparator output only once per clock cycle. However, an overrange condition will exist when the integrator output does not return to zero by the end of the De-Integrate phase, and can leave a residual voltage on the integrator capacitor. In this case, the Zero Integrator phase is increased to 6200 counts to ensure that the integrator capacitor is fully discharged before the next measurement cycle is started.

Analog Section

Analog COMMON

Analog COMMON is the Analog ground reference for the ICL7135. If Input Low is at a voltage other than Analog

4½ Digit A/D Converter with Multiplexed BCD Outputs

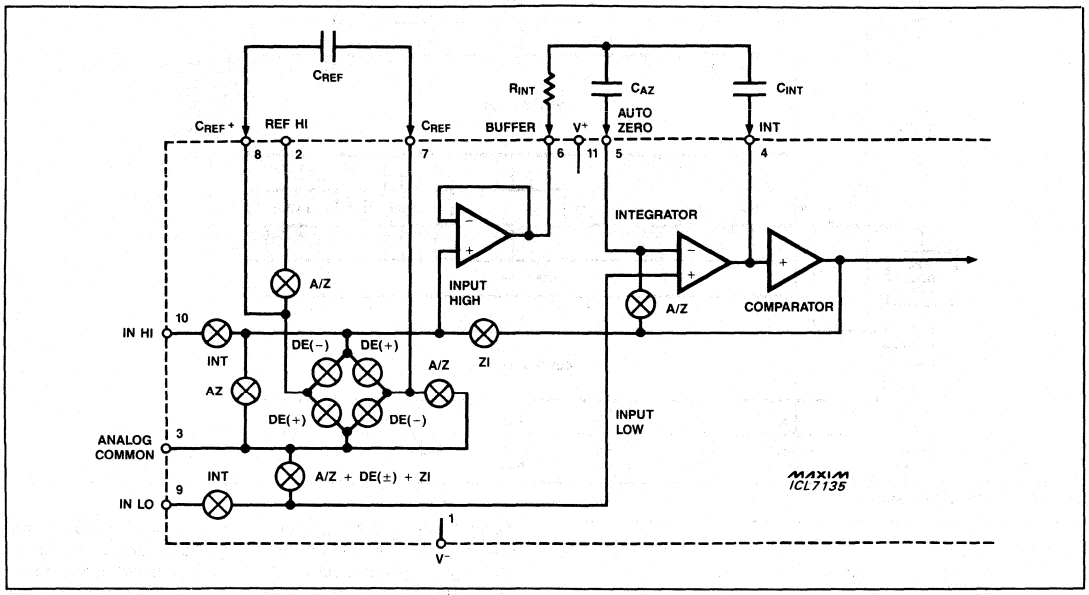


Figure 2. Analog Section of ICL7135

COMMON a common mode voltage will be introduced and, although the ICL7135 has an excellent CMRR, Input Low and Analog COMMON should be connected together whenever possible. Analog COMMON is also the reference point for the reference voltage. The Analog Common voltage is normally connected to the system ground when using ±5V supplies. When the ICL7135 is operated from a single supply voltage the Analog Common should be connected to a voltage source approximately halfway between V^+ and ground.

Input Buffer

The ICL7135 input buffer is a CMOS buffer with a common mode input voltage range of approximately V^+–1.0V to V^-+1.5V. The quiescent current is approximately 100μA and the buffer can deliver up to 40μ of output current with excellent linearity.

Integrator

The integrator amplifier, similar to the buffer amplifier, can deliver 20μA of output current with high linearity while swinging to within 0.3V of either supply rail. The integrator's non-inverting terminal is connected to IN LO during the signal integrate phase, so the voltage on the IN LO terminal sets the starting point for the integrator output during signal integrate. If IN LO is at a voltage other than ground, this will limit the maximum allowable swing at the integrator output, and the value of the integrating capacitor should be increased. (Refer to Component Selection)

Comparator

The comparator monitors the voltage on the integrator capacitor during deintegrate. The digital section samples the comparator output once per clock cycle and terminates the deintegrate cycle when the comparator changes its state as the integrator voltage passes through zero. The offset voltage of the comparator is not critical since the auto-zero phase compensates for the offset. The output of the comparator is the only output from the analog section to the digital section.

Digital Section

As shown in Figure 3, the digital section consists of counters, latches, output multiplexer, and control logic. The control logic monitors the counters and the comparator to determine the start of each phase, and sends control signals to the analog section to drive the analog switches to the proper state for each measurement phase. The control section also responds to the external input, RUN/$\overline{\text{HOLD}}$, and creates the control outputs; OVERRANGE, UNDERRANGE, BUSY, and $\overline{\text{STROBE}}$.

RUN/$\overline{\text{HOLD}}$

When RUN/$\overline{\text{HOLD}}$ is high or open the ICL7135 will continuously perform conversions with each measurement being 40,002 clock cycles long. When RUN/$\overline{\text{HOLD}}$ goes low, the ICL7135 will complete the measurement in progress then remain in the auto-zero cycle, holding the last reading. If RUN/$\overline{\text{HOLD}}$ goes high after the maximum period assigned to deintegrate, a new conversion will start, with a delay of 1 to 10,001 clock cycles between the

4½ Digit A/D Converter with Multiplexed BCD Outputs

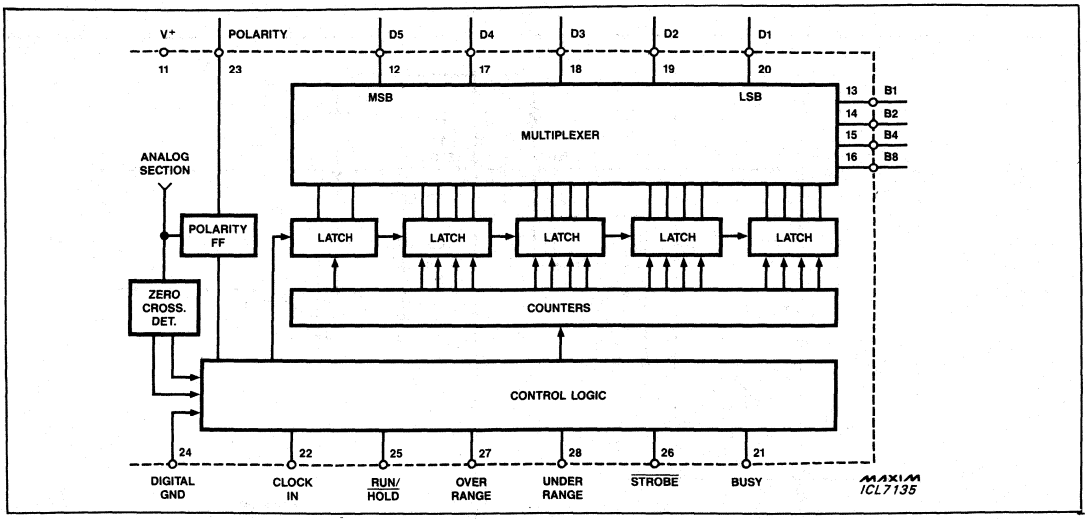


Figure 3. ICL7135 Digital Section

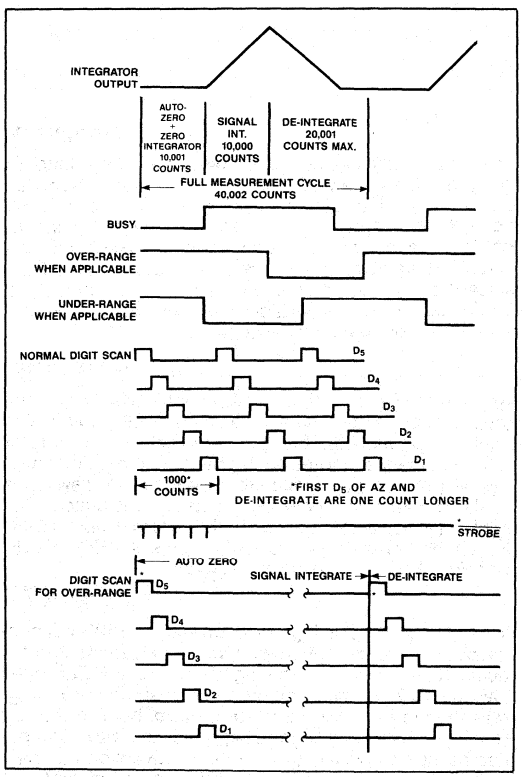


Figure 4. Timing Diagram

rising edge of the RUN/$\overline{\text{HOLD}}$ input and the BUSY output. A RUN/$\overline{\text{HOLD}}$ pulse during the unused portion of deintegrate phase will be ignored, but when in the auto-zero phase a positive pulse of only 300ns (typical) will start the conversion. Figure 5 shows a simple method of obtaining one, and only one, conversion for each measurement request.

BUSY

BUSY is a status output that goes high at the beginning of signal integrate and stays high until the first clock pulse after zero crossing during De-integrate (or end of De-Integrate if overranged). The internal data latches are loaded during the next clock cycle after the falling edge of BUSY. Since BUSY is high for the 10,000 counts of signal integrate + number of counts during De-Integrate + 1 clock cycle, a simple way of sending conversion data down a single pair of wires is to logically 'AND' BUSY with the clock and to subtract 10,001 counts from the number received. Figure 6 shows a system using this method to remotely display data.

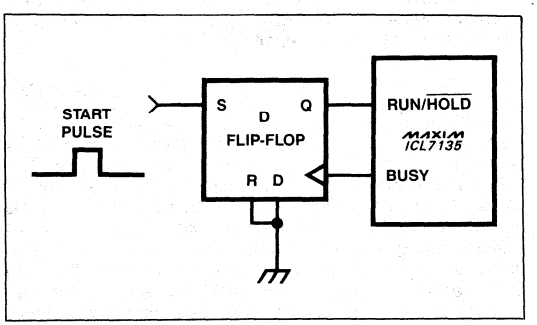


Figure 5. External RUN/$\overline{\text{HOLD}}$ Latch

4½ Digit A/D Converter with Multiplexed BCD Outputs

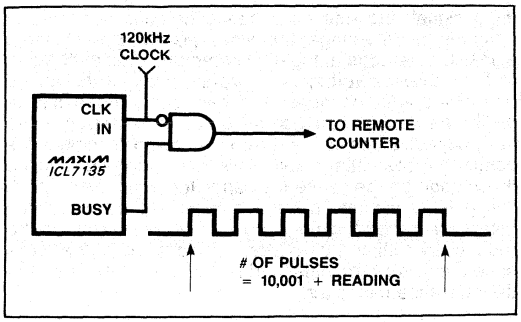


Figure 6. Serial Pulse Stream for Remote Reading

Digit Outputs

The digit outputs go high sequentially, D5 to D1, for a period of 200 clock cycles per digit. The 5 digits are continuously scanned except after an over-range measurement. After an over-range reading the digit scan stops after the strobe sequence, and remains stopped until the start of De-Integrate. For a continuous series of over-range readings, the digits will be scanned for 21,000 counts out of 40,002, resulting in a flashing display as an over-range indicator. D5 is the most significant digit.

BCD Outputs

The 4 BCD output pins are positive logic signals whose BCD data corresponds to the currently active digit strobe. The ICL7135 does not have inter-digit blanking and the BCD data changes simultaneously with the edges of the digit outputs.

$\overline{\text{STROBE}}$

The $\overline{\text{STROBE}}$ output is a negative going pulse that is useful for latching the multiplexed BCD outputs into external BCD latches. Five negative going $\overline{\text{STROBE}}$ pulses occur in the center of the data corresponding to each of the 5 digits of measurement results, once and only once after the end of each conversion (immediately after the falling edge of BUSY). The BCD data is valid at both edges of $\overline{\text{STROBE}}$, and data can be latched in either a level sensitive latch, or an edge triggered latch. Figures 11, 12 and 14 show the use of $\overline{\text{STROBE}}$ to latch the BCD data. $\overline{\text{STROBE}}$ pulse width is 1μs less than ½ clock period.

Over-range and Under-range Outputs

These active high status outputs are set to a high level at the end of BUSY if the measurement result is 1800 or less (Under-range), or greater than 19,999 (Over-range). Under-range is reset at the beginning of the signal integrate phase; over-range is reset at the beginning of the de-integrate phase.

Polarity

The Polarity output is updated at the beginning of each de-integrate phase, and is high for a positive input signal. The Polarity output is valid for all inputs, including ±0 and overrange signals.

Component Selection

The analog component values must be selected with care to achieve optimum performance in each application. Factors that affect the proper values include the reading rate, input common mode voltage, the full scale and reference voltages, and the power supply voltages.

Integrating Resistor

Good linearity is obtained when the integrating resistor value is chosen such that the buffer's maximum output current is between 5 and 40μA. The quiescent current of the buffer is 100μA, and it can supply 20μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the integrating resistor value may be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as:

$$Vswing = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

Where $I_{INT} = 20\mu A$ if R_{INT} is chosen as described above and $T_{INT} = 10{,}000$ clock periods (83.3ms for 120kHz clock frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. Normally the integrator will not saturate until its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. For ±5V supply and Analog Common and IN LO connected to ground, a ±3.5V to ±4V swing range is optimum. Rearranging the above formula and inserting values as described above, C_{INT} may be calculated as:

$$C_{INT} = \frac{20\mu A \times 83.3ms}{3.5V} = 0.47\mu F$$

The integrator swing must be reduced if either Analog Common or IN LO is not grounded, or if the supply voltage is less than ±5V.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the IN HI is a good indication of the

4½ Digit A/D Converter with Multiplexed BCD Outputs

amount of dielectric absorption in the integrating capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon capacitors. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero Capacitor

The size of the auto-zero capacitor will have a significant effect on the overall system noise, with larger auto-zero capacitors resulting in a quieter system. The dielectric absorption of the auto-zero capacitor affects only the speed of settling at power-up or recovery from overload and nearly any capacitor type can be used. The zero integrator phase of the ICL7135 allows the use of large auto-zero capacitors while avoiding the "over-range hangover" and hysteresis effects that occur in A/D converters without the zero integrator phase.

Reference Capacitor

Like the auto-zero capacitor, the reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are only required where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in multimeters.

The reference capacitor DOES need to be a low leakage capacitor since it must store the reference voltage while floating during both the signal integrate and the reference deintegrate phases. Any leakage or charge loss during these two phases results in an effective change in the scale factor of the ICL7135. Low cost film capacitors such as polyester or polystyrene have been found to be suitable in most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. For a negative polarity input signal, the reference capacitor does not shift its common mode voltage, but with a positive polarity input signal it undergoes a negative common mode shift equal to the reference voltage. If there are stray capacitances on the reference capacitor terminals, some of the charge on the reference capacitor will be used to charge these stray capacitances as the reference capacitor makes this common mode voltage shift. This loss of charge reduces the voltage on the reference capacitor, and causes positive polarity signals to have a higher measured result than a corresponding negative voltage. This error can be reduced by minimizing the stray capacitance on the reference capacitor terminals, and by increasing the value of the reference capacitor.

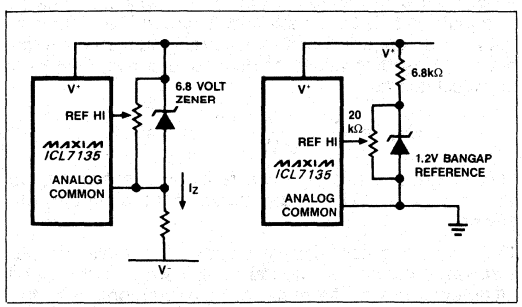


Figure 7. External Reference Voltage

Reference Voltage

The full scale reading of 20,000 will occur when $V_{IN} = 2 \times V_{REF}$. Since the 20,000 count resolution of the ICL7135 is equivalent to a 50ppm resolution, a high stability reference is recommended for high accuracy absolute measurements. Figure 7 shows two suitable methods of generating the reference voltage.

Rollover Resistor and Diode

The ICL7135 is tested for rollover using the circuit of Figure 1, with the 100kΩ resistor and diode in the circuit. The diode is noncritical, and is typically a low cost 1N4148. The resistor value is dependent on many factors including integrator swing, clock frequency, and the amount of rollover error due to "charge suckout" on the reference capacitor. 100kΩ is the optimum value for most circuits and is the value used in testing the ICL7135.

Speedup Resistor

The 27Ω speedup resistor in series with the integrating capacitor adds a pedestal voltage on top of the integrating capacitor voltage. This pedestal voltage causes zero crossing to occur earlier than would occur without the resistor. The effect of the earlier zero crossing is to give the comparator an overdrive voltage, speeding its response and reducing the conversion error due to comparator delay. If the integrator current is changed, the speedup resistor value should be changed so that the $I_{INT} \times R_{SPEEDUP} = 500\mu V$.

Clock Frequency

The clock source should be free of short-term phase and frequency jitter during the conversion period, but long term stability is not critical. The clock frequency is chosen to obtain the desired conversion rate, and to maximize the normal mode rejection of power line frequency interference. The conversion rate is directly proportional to the clock frequency, with each conversion taking 40,002 clock cycles. For maximum normal mode rejec-

4½ Digit A/D Converter with Multiplexed BCD Outputs

tion, the signal integration period should be an integral multiple of the power line cycles.

$$\text{Reading Rate (in readings per second)} = \frac{f_{CLK}}{40{,}002}$$

$$f_{CLK} \text{ for maximum normal mode rejection} = \frac{f_{LINE} \times 10{,}000}{N}$$

Where f_{LINE} is the line frequency, normally 50Hz or 60Hz and N is the number of line cycles that occur during a signal integration period. For maximum normal mode rejection, N should be an integer.

For 60Hz rejection, suitable clock frequencies include 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, and 75kHz. Suitable frequencies for use with 50Hz power include 250kHz, 166⅔kHz, 125kHz, and 100kHz. The two most common clock frequencies are 120kHz (3 readings per second) and 100kHz (2½ readings per second). Note that a 100kHz clock frequency rejects both 50Hz and 60Hz normal mode signals.

The maximum clock rate is limited by the maximum rate at which the digital logic will correctly function (typically 2MHz), and by the speed of response of the comparator. The comparator delay, about 3μs, has the same effect on the measurement result as does an offset voltage with the same polarity of the input signal. At the recommended clock frequency of 120kHz, this small offset is slightly less than ½ count. At higher clock frequencies the value of the speedup resistor in series with the integration capacitor (normally 27Ω) should be increased. At frequencies above 120kHz, ringing on the integrator output may cause nonlinearities in the first few counts.

The minimum clock frequency is limited by the leakage of the auto-zero and reference capacitors. While seldom desired, measurement cycles as long as 10 seconds can be performed with negligible error at room temperature. Figures 8A and 8B show two methods of generating a suitable clock signal for the ICL7135.

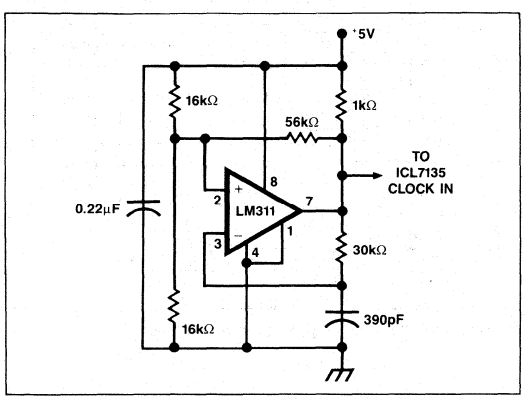


Figure 8A. LM311 Clock Source

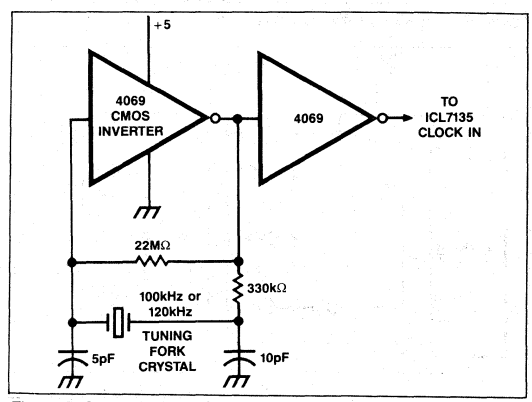


Figure 8B. Crystal Oscillator Clock Source

Application Hints

Grounds

As with all sensitive analog circuitry, it is important to keep the Digital Ground separate from the analog ground (called Analog Common on the ICL7135) to minimize errors caused by the coupling of noise from the digital circuitry into the sensitive analog section. Analog Common should be connected to Digital Ground at only one point, and return currents from digital loads must not flow through the analog ground lines. Avoid any unnecessary current flow in the analog ground path.

Single 5V Supply Operation

The ICL7135 normally uses ±5V supplies, however, in some applications the negative supply is not needed. Specifically, the negative 5V supply is not required if the input signal can be referenced to the center of the ICL7135's common mode voltage range AND the signal voltage is less than ±1.5V. The integrator swing must be reduced, and there will be a slight increase in system noise and nonlinearity. See Figure 9 for recommended component values.

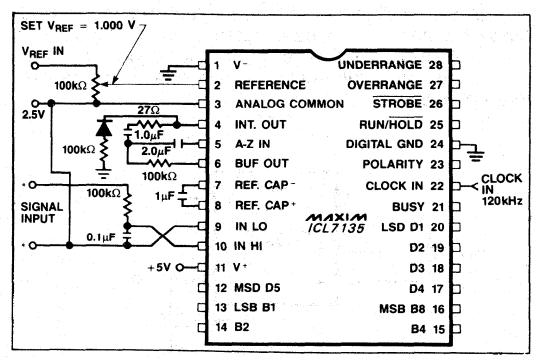


Figure 9. Single +5V Supply Operation

4½ Digit A/D Converter with Multiplexed BCD Outputs

Generating a Negative Supply from +5V

Figures 10A and 10B show two methods of generating a negative supply for the ICL7135. The Maxim ICL7660 will supply 2mA (the maximum supply current of the ICL7135) at 4.85V drop, while the circuit using the CMOS inverter will deliver approximately −3.5V. If the CMOS inverter is used to generate a minus supply, the integrator swing should be reduced to 2.5 to 3V.

Noise

The normal system noise around zero is about 15μV peak-to-peak (not exceeded 95% of the time). Near full scale, the noise increases to about 30μV. The main noise source is the auto-zero loop, and increasing the value of the auto-zero capacitor will reduce the noise. Other noise sources include the buffer and integrator noise; comparator noise; and stray pickup in the input circuitry, the integrator, and the reference capacitor. The noise caused by stray pickup of interfering signals can be reduced by a tight layout and shielding. If the interfering signal frequency is constant, the effects of stray pickup in the input and integrator can be reduced by choosing a clock frequency such that the signal integration period is an integral multiple of the interfering signal's period. Since the length of the de-integration period depends on the input signal level, no single clock frequency can be chosen to reject interfering signals during the de-integrate phase.

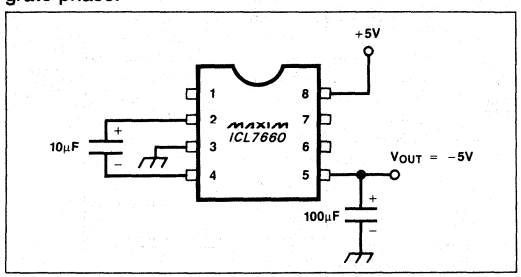


Figure 10A. Generating a Negative Supply

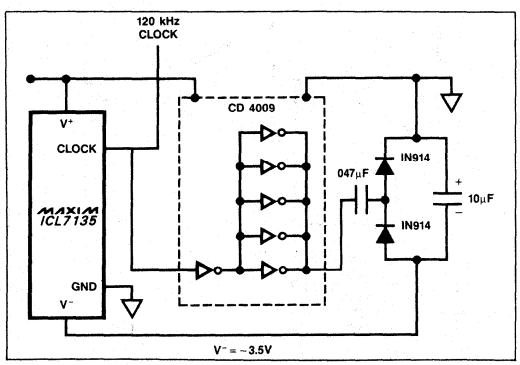


Figure 10B. Generating a Negative Supply

Typical Applications

Figure 11 uses Maxim's ICL7211 LCD display driver to drive 4 digits of LCD display. The backplane signal of the ICL7211 and the CMOS exclusive OR gates are used to drive the ½ digit and the polarity sign. The four AND gates combine the digit outputs with the STROBE output to generate the digit select signals that latch data into the ICL7211. Since the Strobe occurs in the middle of each digit's data there is ample data setup and hold time to ensure that valid data is latched. The OR gates will force the BCD data to all ones when over-range goes high. The ICL7211A will blank the display when all ones (hex F) is loaded.

The typical operating circuit on the first page of this data sheet shows a 4½ digit A/D with LED drive using the Maxim ICL7212 display driver. In this case the polarity and ½ digit segments are driven by D flip-flops that latch polarity and ½ digit data at the end of each measurement. The ICL7135 Overrange output drives the ICM7212 Brightness input, blanking the four least significant digits when the input voltage is greater than full-scale.

Some applications require non-multiplexed, latched BCD outputs. The circuit shown in Figure 12 will demultiplex and latch the ICL7135 output. If only the first rank of latches is used, the data should not be used during the 800 clock cycle update period that takes place at the end of each conversion since during this update period the

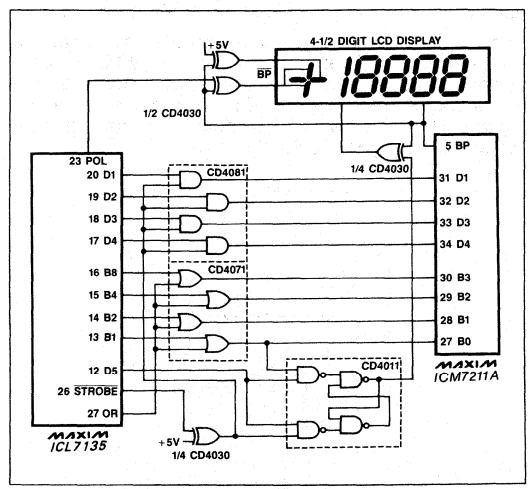


Figure 11. LCD Display with Digit Blanking on Overrange

4½ Digit A/D Converter with Multiplexed BCD Outputs

most significant digit (MSD) data will correspond to the new reading and the least significant digit (LSD) data will be old data from the previous converison. The second rank of latches shown in dotted lines will eliminate this problem by updating all digits simultaneously with the rising edge of D5.

There are many different possible ways of interfacing the ICL7135 to a microprocessor. Figure 13 shows a method that uses only 8 I/O lines. The digit outputs drive a priority encoder, which converts the 1-of-5 format of the digit outputs to a 3 bit binary code. When no digit is active (as in over-range), the binary output code is 0, otherwise the output corresponds to the digit number of the active digit. By sensing BUSY as either an input or as an interrupt, the microprocessor can detect when new data is available.

Another possible interface scheme is to sense only digit D5, then use time delays to choose when to read the other digits' data.

Interfacing With UARTs and Microprocessors

Figure 14 shows a simple interface between a UART and a free running ICL7135. The transmission of the five data words is started by the five STROBE pulses. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. The polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). A parity flag at the receiver can be decoded as a positive signal, no flag as negative, if EPE of the receiver is held low. Figure 15 shows a more complex arrangement. DR goes high when the UART receives a byte via the send input, RRI. Since DR is connected to the ICL7135's RUN/HOLD input this starts a new conversion. At the end of the conversion the falling edge of BUSY resets DR via the UART's DRR input. The transmit sequence is again started by STROBE. A quad 2-input multiplexer is used to superimpose polarity, over-range, and under-range onto the D5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

To insure proper operation, it is necessary that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives.

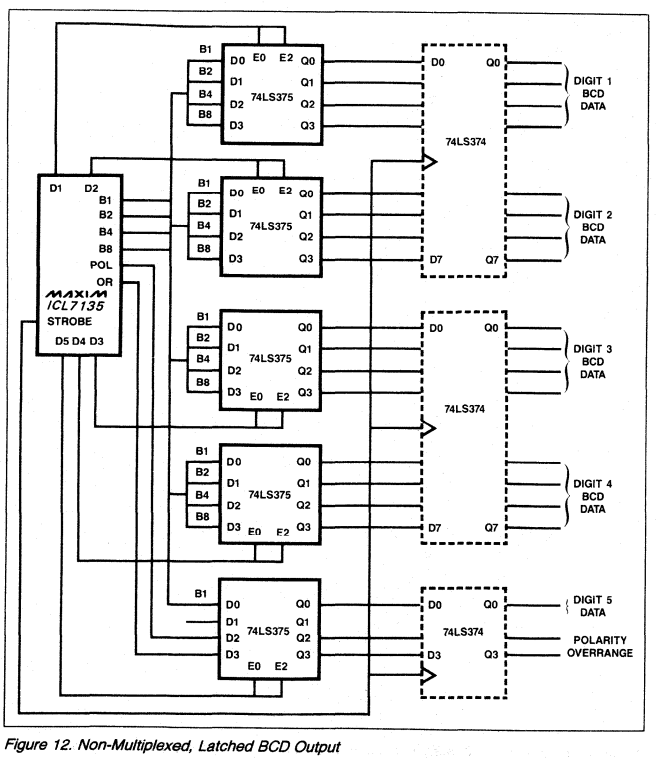


Figure 12. Non-Multiplexed, Latched BCD Output

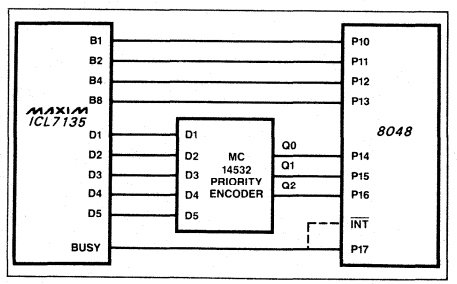


Figure 13. µP Interface

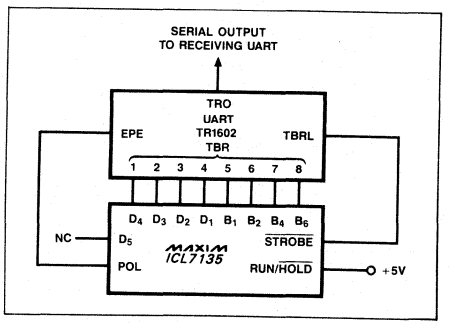


Figure 14. ICL7135 to UART Interface

4½ Digit A/D Converter with Multiplexed BCD Outputs

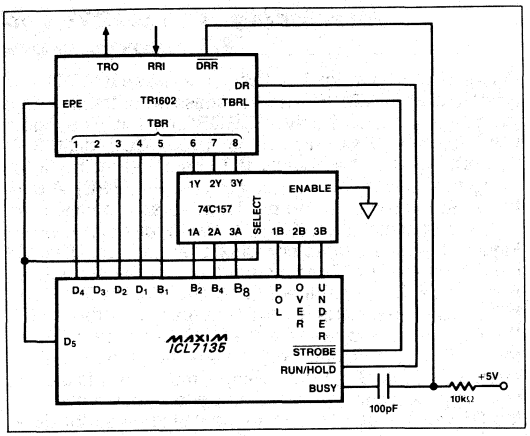
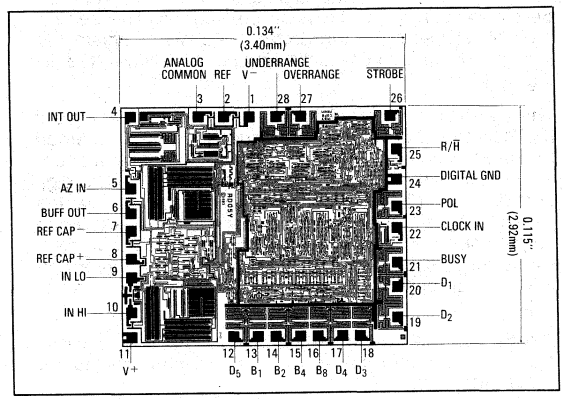


Figure 15. Complex ICL7135 to UART Interface

Chip Topography



MAXIM

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7136 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7136 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7136 a superior device, especially for portable systems.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7136 eliminates overrange hangover and hysteresis effects. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

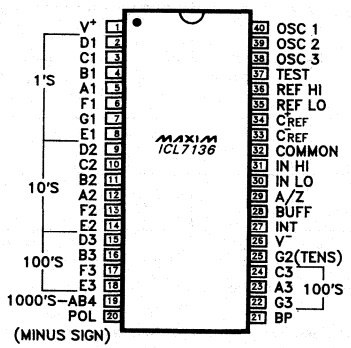
Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Pin Configuration

Top View



See ICL7106 Data Sheet for 44 Lead Chip Carrier Pin Configuration

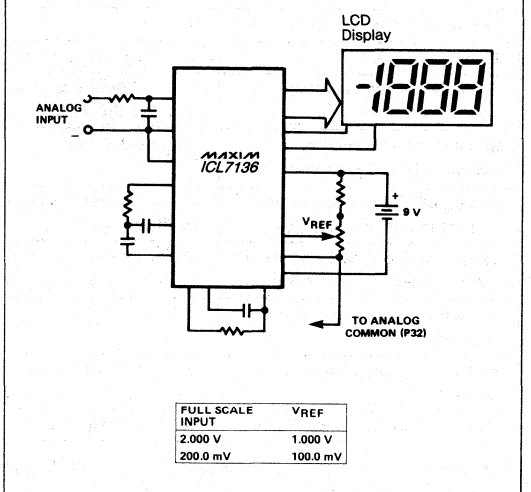
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Power dissipation guarateed less than 1mW-9V battery life 3000 hours typical**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LCD Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS Design**

Ordering Information

Part	Temp. Range	Package
ICL7136CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7136CJL	0°C to +70°C	40 Lead CERDIP
ICL7136CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7136C/D	0°C to +70°C	Dice

Typical Operating Circuit



FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

(Detailed Circuit Diagram—Figures 1 & 2)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 1000mW
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{CLOCK} = 16kHz and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 9)**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 10)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 8)	−000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**−000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 8)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0mV				
	T_A = 25°C (Note 8)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ +70°C (Note 12)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		5		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 8)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0				
	T_A = 25°C		60	100	µA
	0° ≤ T_A ≤ +70°C			**120**	
Analog Common Voltage (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	**With respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	V_{IN} changing from ±10V to 0V		0	1	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO through a 1MΩ series resistor as shown in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.

Low Power, 3½ Digit A/D Converter

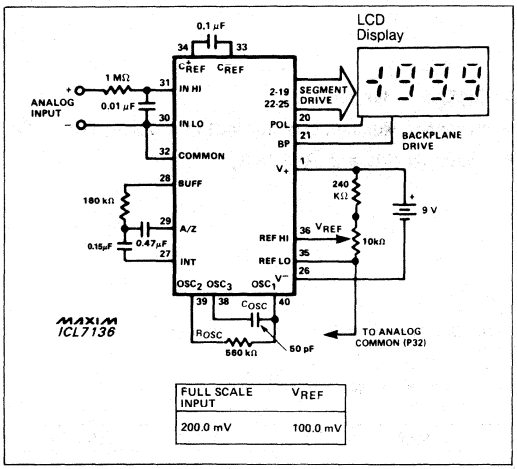


Figure 1. Maxim ICL7136 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)

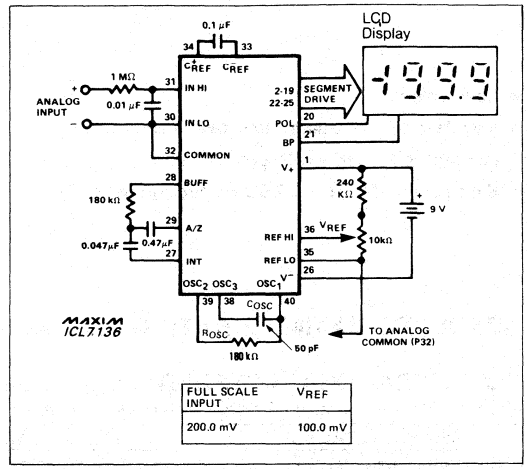


Figure 2. Maxim ICL7136 Typical Operating Circuit Clock Frequency 48kHz (3 readings/sec)

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

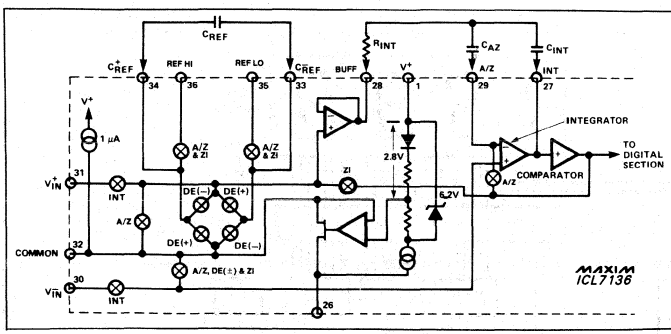


Figure 3. Analog Section of 7136

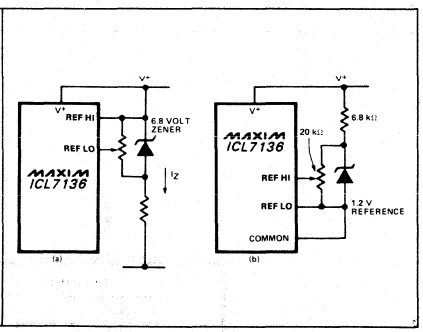


Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 µA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 µA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7136. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.

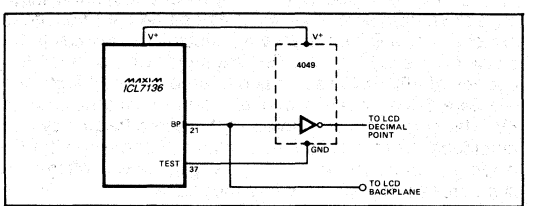


Figure 5. Simple Inverter for Fixed Decimal Point

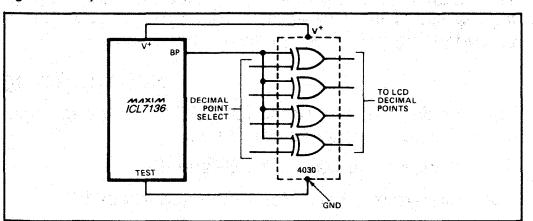


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Low Power, 3½ Digit A/D Converter

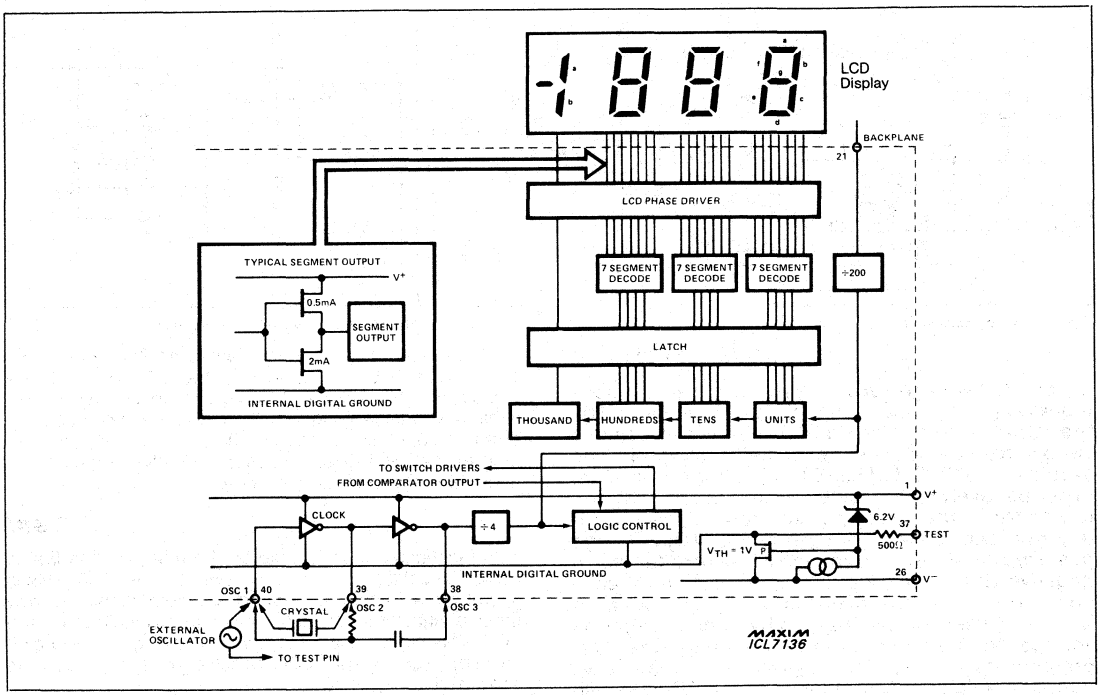


Figure 7. ICL7136 Digital Section

Digital Section

The digital section for the ICL7136 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currrents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7136. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7136 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

Low Power, 3½ Digit A/D Converter

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a 0.1μF capacitor is adequate. A 0.47μF capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is 0.15μF at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 6μA of quiescent current and can supply 1μA of drive current with negligible non-linearity.

The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 180kΩ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. A suitable value of the integrating resistor would be 330kΩ. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for V_{IN} ≠ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation f ≈ 0.45/RC. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Typical Applications

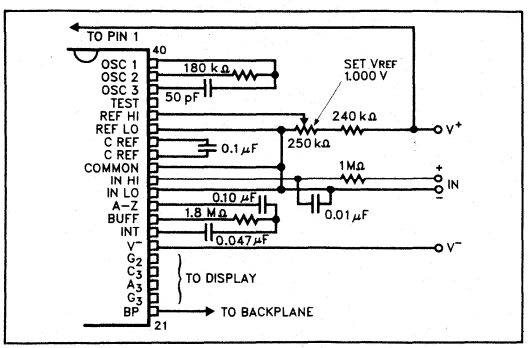


Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.

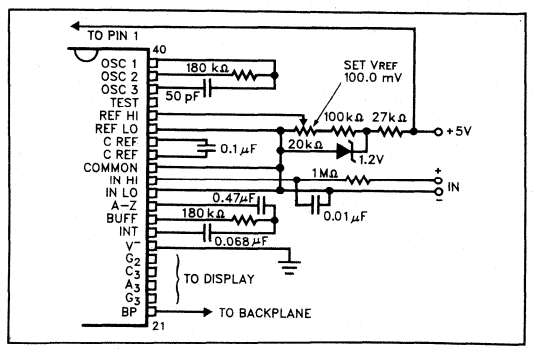


Figure 9. 7136 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.

Low Power, 3½ Digit A/D Converter

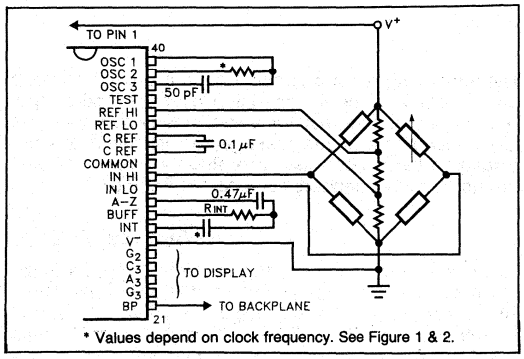


Figure 10. 7136 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

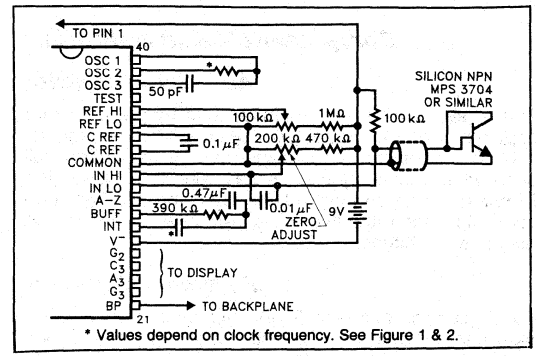
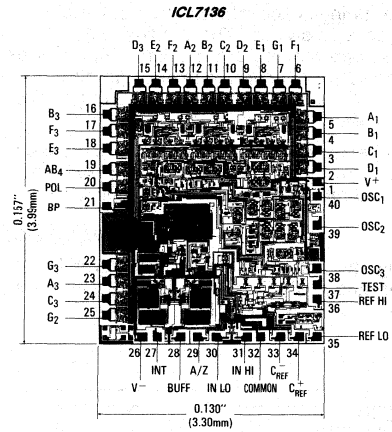


Figure 11. 7136 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

Chip Topography



MAXIM
Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7137 is a monolithic analog to digital converter with all the necessary active devices to directly interface with a light emitting diode (LED) display. Excluding the LED display current, the ICL7137 supply current is under 200μA, making it suitable for battery operation.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7137 eliminates overrange hangover and hysteresis effects. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Features

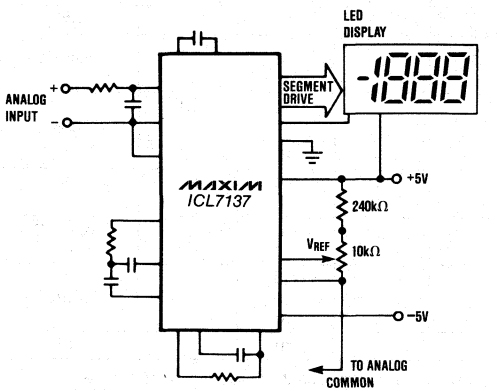
- **Improved 2nd Source! (see 3rd page for "Maxim Advantage™")**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LED Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7137CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7137CJL	0°C to +70°C	40 Lead CERDIP
ICL7137CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7137C/D	0°C to +70°C	Dice

1

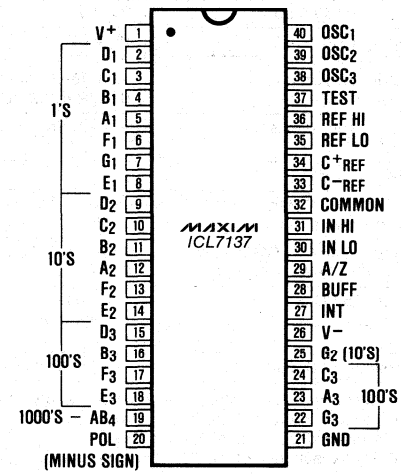
Typical Operating Circuit



(Detailed Circuit Diagram—See last page)

Pin Configuration

Top View



See last page for Plastic Chip Carrier Pin Configuration

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... -9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Cerdip Package 1000mW
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near full scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0° < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply Current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (with respect to Positive Supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A=25°C, f_{CLOCK}=16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion in the ICL7136 data sheet.
Note 5: 48kHz oscillator, Figure 2, increases current by 35μA (typ).
Note 6: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed Over Temperature**
- **Guaranteed Overload Recovery Time**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 8)**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 7)**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1 unless noted.)

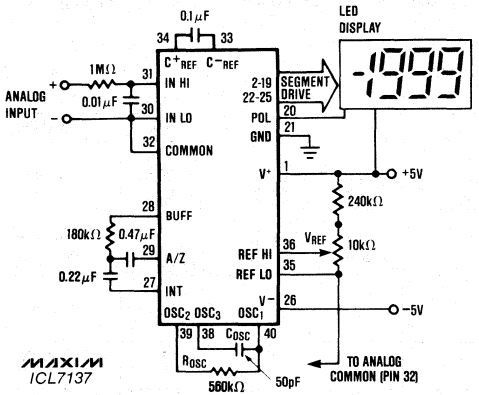
PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 9)	-000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**-000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 9)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200mV				
	T_A = 25°C (Note 9)	-1	±0.2	+1	Counts
	0° ≤ T_A ≤ +70°C (Note 10)		±0.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio	**V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV**	**-100**	**±5**	**+100**	μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		μV
Input Leakage Current	V_{IN} = 0,				
	T_A = 25°C (Note 9)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0V, 0° ≤ T_A ≤ 70°C (Note 9)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C)(Note 9)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0V				
	T_A = 25°C		60	200	μA
	0° ≤ T_A ≤ 70°C			**240**	
V^- Supply Current	**V_{IN} = 0V,**		**60**	**200**	μA
Analog Common Voltage (with respect to Pos. supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment Voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA
Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	V_{IN} changing from ± 10V to 0V		0	1	Measurement Cycles

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883C, Method 3015.2)
Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).
Note 9: Test condition is V_{IN} applied between the "Analog Input" pins (Figure 1).
Note 10: 1MΩ resistor is removed in Figures 1 and 2.
Note 11: Number of measurement cycles for display to give accurate reading.

Low Power, 3½ Digit A/D Converter

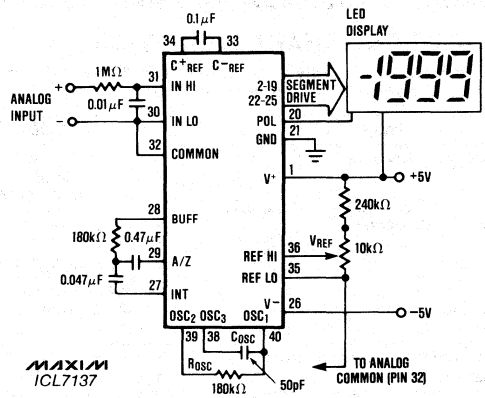
Detailed Description

The Maxim ICL7137 3½ digit A/D converter is similar to the Maxim ICL7136 except for the LED segment driver outputs, and is similar to the ICL7107 except for much reduced power supply currents (exclusive of the LED currents.) For a detailed product description, component value selection, and package dimensions, refer to Maxim's ICL7136 data sheets; for applications information refer to Maxim's ICL7107 data sheets.



FULL SCALE INPUT	V_{REF}
200.0 mV	100.0mV

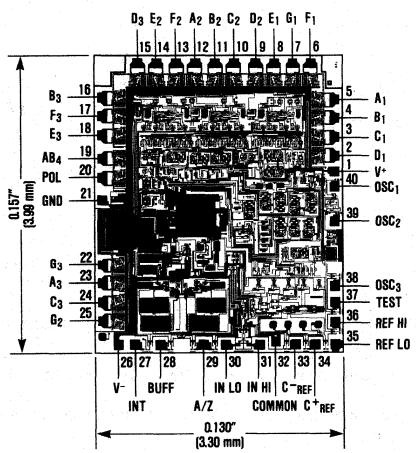
Figure 1. Maxim ICL7137 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)



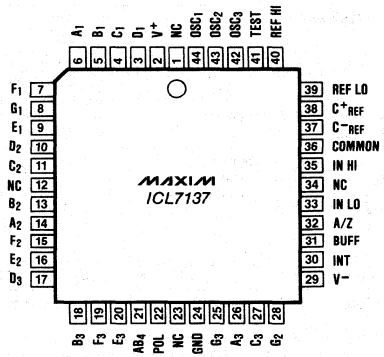
FULL SCALE INPUT	V_{REF}
200.0 mV	100.0mV

Figure 2. Maxim ICL7137 Typical Operating Circuit Clock Frequency 48kHz (3 reading/sec)

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

D/A Converters

D/A Converters

Part Number	Type	Resolution	Relative Accuracy % F.S.	Gain Tempco ppm/°C (max)	Settling Time	Output	Power Dissipation (mW)	Page No.
AD565A	Bipolar, w/Ref.	12-bit	0.012 to 0.006	20	250ns max	Current	345	2-1
AD566A	Bipolar	12-bit	0.012 to 0.006	20	350ns max	Current	300	2-1
AD7224	Multiplying	8-bit	0.2	20	5µs max	Voltage	75	2-9
AD7225	Quad, Multiplying	8-bit	0.2	20	4µs max	Voltage	150	2-19
AD7226	Quad, Multiplying	8-bit	0.2	20	4µs max	Voltage	195	2-19
AD7520	Multiplying	10-bit	0.2 to 0.05	10	500ns typ	Current	30	2-31
AD7521	Multiplying	12-bit	0.2 to 0.05	10	500ns typ	Current	30	2-31
AD7523	Multiplying, Low Cost	8-bit	0.2 to 0.05	67	150ns typ	Current	1.6	2-37
AD7524/ MAX7624	Multiplying	8-bit	0.5 to 0.2	40	250ns max	Current	30	2-41
AD7528/ AD7628	Dual, Multiplying	8-bit	0.5 to 0.2	35	180ns max	Current	15	2-49
AD7530	Multiplying	10-bit	0.2 to 0.05	10	500ns typ	Current	30	2-61
AD7531	Multiplying	12-bit	0.2 to 0.05	10	500ns typ	Current	30	2-61
AD7533	Multiplying	10-bit	0.2 to 0.05	10	600ns max	Current	30	2-65
AD7541	Multiplying	12-bit	0.025 to 0.012	10	1µs max	Current	30	2-71
AD7541A	Multiplying	12-bit	0.025 to 0.012	5	600ns typ	Current	30	2-75
AD7542	Multiplying	12-bit	0.012	5	2µs max	Current	12.5	2-81
AD7543	Serial Input	12-bit	0.012	5	2µs max	Current	12.5	2-89
AD7545	Multiplying	12-bit	0.05 to 0.012	5	2µs max	Current	30	2-97

Digital/Analog Converter Terminology

Absolute Accuracy: The difference between the ideal expected DAC output voltage or current and the actual observed output. See Total Unadjusted Error.

Channel-To-Channel Isolation: In multiple DAC devices, the amount of signal which couples from one DAC reference input to a different DAC output. Specified in dB.

Differential Nonlinearity: The difference between the measured and the ideal output step change for a 1 LSB digital input change. Specified in LSB. A specification of ±1 LSB or less guarantees monotonicity.

Digital Crosstalk: In multiple DAC devices, the Glitch Impulse coupled from the digital inputs of one DAC to the analog output of a different DAC channel. Specified in nV-s.

Digital To Analog Converter: Also DAC, D/A, and D-to-A. A device which converts a digital input code to a variable analog output current or voltage.

Feedthrough Error: Signal caused by coupling from reference input to output when the DAC logic inputs are all LOW. Expressed in mV or dB relative to V_{REF} and measured with an AC reference input.

Four-Quadrant: Refers to the ability of the DAC to operate with reference inputs and analog outputs of both positive and negative polarity.

Full-Scale Error: Also Gain Error. The difference between the actual and ideal DAC output at Full-Scale. Expressed in mV, % of FSR, or LSBs.

Gain: Ratio of output voltage to input voltage. For DMOS multiplying DACs, when used with an output amplifier, it is the ratio of output voltage to reference voltage.

Glitch Impulse: The amount of charge injected from the digital inputs to the analog output when the inputs change state. Specified as the area under the impulse, in pA-s or nV-s.

Least Significant Bit (LSB): The digital input bit that has the smallest weight. Also the smallest analog step that a DAC can take. As an analog quantity, 1 LSB = $V_{REF} \times 2^{-N}$, where N is the number of DAC input bits.

Linearity: Also Nonlinearity and Integral Nonlinearity. See Relative Accuracy.

Monotonic: A DAC is said to be monotonic if its analog output either increases or stays the same for an increasing digital input. Monotonicity is either guaranteed by direct statement or by a maximum Differential Nonlinearity Specification of ±1 LSB.

Most Significant Bit: The digital input bit that has the largest weight.

Multiplying DAC: A type of DAC in which the reference input can be varied. The output signal is then the "product" of the reference input and the digital input code.

Output Amplifier: Typically an op-amp, connected to a DAC output, which converts an output current to a voltage. Also used to buffer a high impedance voltage output or provide additional gain. Some DACs include on-chip output amplifiers.

Output Capacitance: Capacitance from DAC output terminals to ground.

Output Leakage Current: DAC output current when the ideal value is zero. OUT1 current when all digital inputs are low and OUT2 current when all digital inputs are high.

Propagation Delay: Time required, after an input code change, for a DAC output to reach 90% of its final value. Usually specified for a Full Scale output step.

R-2R Ladder: A resistor network used to generate binarily weighted currents or voltages in Digital-to-Analog and Analog-to-Digital Converters.

Relative Accuracy: (or End-Point Nonlinearity) The maximum deviation from a straight line which passes through the endpoints of the DAC transfer function (Zero and Full Scale). It is expressed in % or ppm of the Full Scale Range (FSR) or in LSBs.

Resolution: The number of steps that a DAC can take expressed in number of bits. A DAC with N-bit resolution can take 2^N steps.

Settling Time: The time required for a DAC to settle (and remain) within ½ LSB of its final value. Usually specified for a Full Scale step change.

Temperature Coefficient: The variation of a parameter (such as Zero Error, Full Scale Gain, or Linearity) with ambient temperature. Specified in %/°C or ppm/°C.

Total Unadjusted Error: Includes Full Scale, Relative Accuracy, and Zero Code Error specifications. The maximum output deviation from the ideal expected values. Specified in LSBs or % of FSR at a fixed reference voltage, usually +10V.

Unipolar: Refering to DAC output, either 0 to +V or 0 to -V output.

Bipolar: Refering to DAC output, -V to +V output.

Zero Code Error: Also Offset Error. The DAC output voltage for an all zero digital input code (Unipolar configuration). Specified in mV or LSBs.

MAXIM

High Speed 12-Bit Monolithic D/A Converters

General Description

The AD565A and AD566A are 12-bit monolithic digital to analog converters (DACs) built in bipolar technology that offer an excellent combination of high speed settling and ±¼LSB linearity. The AD565A also features an on-chip precision 10V reference, whereas the AD566A requires an external reference.

Laser trimming of the on chip thin film resistor networks achieve ±⅛LSB typical linearity (±¼LSB max.) at +25°C. Full scale settling time to ±½ LSB is specifed at 250ns max. for the AD565A and 350ns max. for the AD566A. This high speed and accuracy makes the AD565A and AD566A DACs ideal choices for fast analog to digital converters and CRT display drivers.

The AD565A and AD566A contain onboard application resistors that can be used as feedback and offset resistors with an external output amplifier to generate unipolar and bipolar outputs or as the input resistors in analog to digital converter applications. The excellent matching and tracking of the DAC's current setting resistor and application resistors assure good gain stability over both time and temperature.

Applications

High Speed Display Drivers
High Speed Control Systems
High Speed A/D Converters
Data Acquisition Systems
Test Equipment

Features

- **250ns Settling to ±½LSB**
- **Montonicity Guaranteed Over Temperature**
- **TTL and CMOS Logic Compatibility**
- **High Stability Buried Zener 10V Reference (AD565A Only)**
- **±½LSB Linearity Guaranteed Over Temperature (AD565AK,AT and AD566AK,AT Only)**
- **Low Power Consumption: 225mW**
- **Widely Second Sourced**

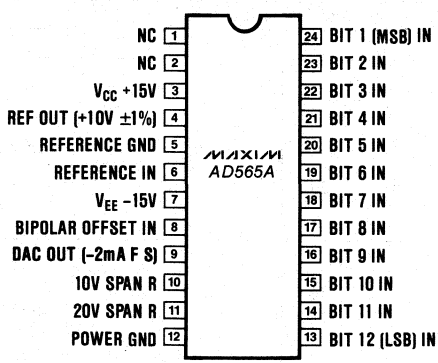
Ordering Information

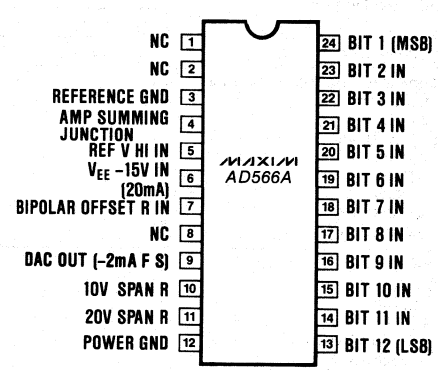
PART	TEMP. RANGE	PACKAGE*	ERROR
AD565AJN	0°C to +70°C	Plastic DIP	±½LSB
AD565AJD	0°C to +70°C	Ceramic	±½LSB
AD565AJQ	0°C to +70°C	CERDIP**	±½LSB
AD565AJCWG	0°C to +70°C	Small Outline	±½LSB
AD565AJC/D	0°C to +70°C	Dice	±½LSB
AD565AKN	0°C to +70°C	Plastic DIP	±¼LSB
AD565AKD	0°C to +70°C	Ceramic	±¼LSB
AD565AKQ	0°C to +70°C	CERDIP**	±¼LSB
AD565AKCWG	0°C to +70°C	Small Outline	±¼LSB
AD565ASD	-55°C to +125°C	Ceramic	±½LSB
AD565ASQ	-55°C to +125°C	CERDIP**	±½LSB
AD565ATD	-55°C to +125°C	Ceramic	±¼LSB
AD565ATQ	-55°C to +125°C	CERDIP**	±¼LSB

* *All devices — 24 lead packages*
** *MAXIM reserves the right to ship Ceramic packages in lieu of CERDIP packages.*
Ordering information for AD566A continued on back page

Pin Configurations

Top View





High Speed 12-Bit Monolithic D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground (AD565A only) ..... 0V to +18V
V_{EE} to Power Ground ..... 0V to -18V
Voltage on DAC Output ..... -3V to +12V
Digital Inputs (pins 13 to 24) to Power Ground ..... -1V to +7V
REF IN to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span R to Reference Ground ..... ±12V
20V Span R to Reference Ground ..... ±24V
REF OUT (AD565A only)
Short Circuit to Power Ground ..... Continuous
Short to V_{CC} ..... Momentary
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering, 10 sec) ..... +300° C
Package Dissipation 1000mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25° C, V_{CC} = +15V (AD565A only), V_{EE} = -15V , unless noted)

PARAMETER	CONDITIONS	AD565AJ, AS AD566AJ, AS			AD565AK, AT AD566AK, AT			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data Inputs (Pins 13 to 24)								
Input Voltage								
Bit ON Logic "1"	TTL or 5V CMOS	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	T_{MIN} to T_{MAX} (Note 1)	0		+0.8	0		+0.8	V
Logic Current (each bit)								
Bit ON Logic "1"			+120	+300		+120	+300	μA
Bit OFF Logic "0"			+35	+100		+35	+100	μA
Resolution				12			12	Bits
Output								
Output Current								
Unipolar (all bits on)		-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Output Resistance (exclusive of span resistors)		6	8	10	6	8	10	kΩ
Output Offset								
Unipolar (adjustable to zero per Fig. 1)			0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Fig. 2, R_1 and R_2 = 50Ω fixed)			0.05	0.15		0.05	0.1	
Output Capacitance			25			25		pF
Output Compliance Voltage	T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
Accuracy (error relative to full scale)	+25° C		±¼ (0.006)	±½ (0.012)		±⅛ (0.003)	±¼ (0.006)	LSB
	T_{MIN} to T_{MAX}		±½ (0.012)	±¾ (0.018)		±¼ (0.006)	±½ (0.012)	(% of F.S.)
Differential Nonlinearity	+25° C		±½	±¾		±¼	±½	LSB
	T_{MIN} to T_{MAX}	Monotonicity Guaranteed						
Temperature Coefficients								
AD565A with Internal Reference								
Unipolar Zero			1	2		1	2	
Bipolar Zero			5	10		5	10	
Gain (Full Scale)								
AD565AJ			15	50				ppm/° C
AD565AK						10	20	
AD565AS			15	30				
AD565AT						10	15	
Differential Nonlinearity			2			2		
AD566A								
Unipolar Zero			1	2		1	2	
Bipolar Zero			5	10		5	10	
Gain (Full Scale)								ppm/° C
AD566AJ, AS			7	10				
AD566AK, AT						2	3	
Differential Nonlinearity			2			2		

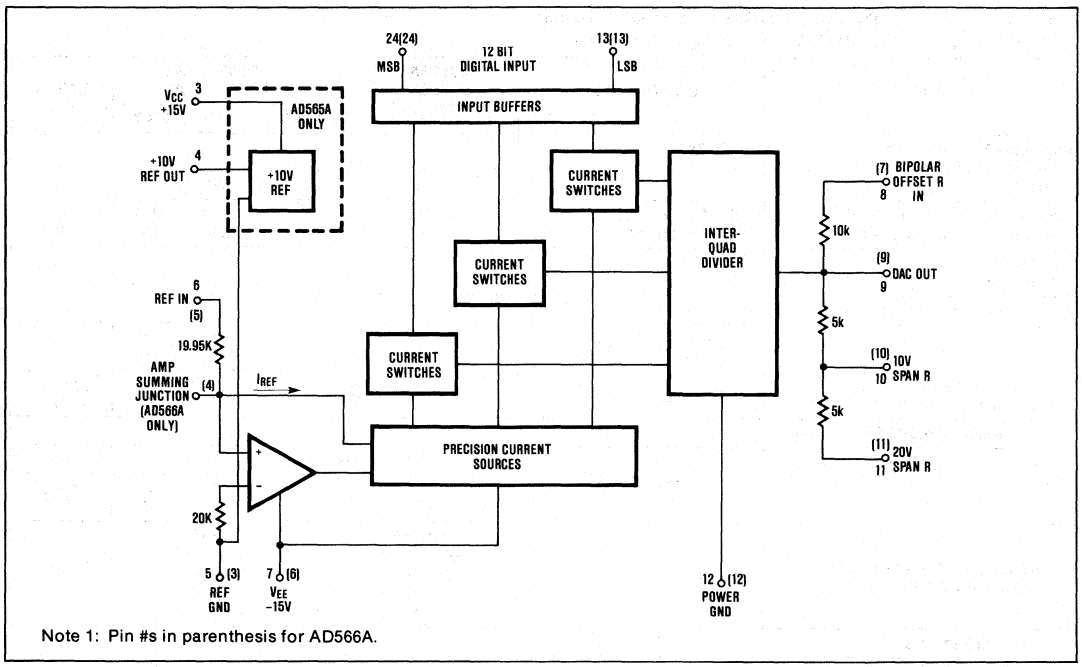
ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25° C, V_{CC} = +15V (AD565A only), V_{EE} = -15V , unless noted)

PARAMETER	CONDITIONS	AD565AJ, AS AD566AJ, AS			AD565AK, AT AD566AK, AT			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Full Scale Transition (Note 3)								
70% to 90% Delay plus Rise Time			15	30		15	30	ns
90% to 10% Delay plus Full Time			30	50		30	50	
Settling Time to within ±½ LSB	AD565A (Note 3)		150	250		150	250	ns
All Bits on-to-off or off-to-on	AD566A (Note 3)		250	350		250	350	
Temperature Range	AJ, AK	0		+70	0		+70	°C
(Operating)	AS, AT	-55		+125	-55		+125	
Power Requirements (AD565A Only)								
$+I_{PS}$	11.4V > $\lvert V_{CC} \rvert$ > 16.5V		3	5		3	5	mA
$-I_{PS}$			-12	-18		-12	-18	
$+V_{CC}$ Gain Sensitivity	11.4V > $\lvert V_{CC} \rvert$ > 16.5V		3	10		3	10	ppm of F.S./%
$-V_{EE}$ Gain Sensitivity (Note 2)	11.4V > $\lvert V_{EE} \rvert$ > 16.5V		15	25		15	25	
Power Requirements (AD566A Only)								
$-I_{PS}$	11.4V > $\lvert V_{EE} \rvert$ > 16.5V		-12	-20		-12	-20	mA
$-V_{EE}$ Gain Sensitivity			15	25		15	25	ppm of F.S./%
Programmable Output Ranges (AD565A and AD566A)	See Figs. 4,5		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V
External Adjustments								
Gain Error with Fixed 50Ω Resistor	See Figs. 4,5		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor			±0.05	±0.15		±0.05	±0.1	
Gain Adjustment Range			±0.25			±0.25		
Bipolar Zero Adjustment Range			±0.15			±0.15		
Reference Input Impedance		15	20	25	15	20	25	kΩ
Reference Output Voltage (AD565A Only)		9.90	10.00	10.10	9.90	10.00	10.10	V
Reference Output Current (available for external loads) (AD565A Only)		1.5	2.5		1.5	2.5		mA
Power Dissipation (AD565A)			225	345		225	345	mW
AD566A			180	300		180	300	
Multiplying Mode Performance (AD566A Only)								
Quadrants		Two (2): Bipolar Operation at Digital Input Only						
Reference Voltage		+1V to +10V, Unipolar						
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1V DC Reference Voltage						
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p] sinewave frequency for ½ LSB [p-p] feedthrough)		40kHz typ						
Output Slew Rate 10%-90%		5mA/μs						
90%-10%		1mA/μs						
Output Settling Time (all bits on and a 0-10V step change in reference voltage)		1.5μs to 0.01% F.S.						
Control Amplifier (AD566A)								
Full Power Bandwidth		300kHz						
Small-Signal Closed-Loop Bandwidth		1.8MHz						

Note 1: The digital input levels are guaranteed but not tested over the temperature range.
Note 2: The power supply gain sensitivity is tested in reference to a V_{CC} of +15V and V_{EE} of -15V d.c.
Note 3: Sample tested at +25°C to ensure compliance.

High Speed 12-Bit Monolithic D/A Converters



Note 1: Pin #s in parenthesis for AD566A.

Figure 1. Functional Block Diagram

Circuit Description

The AD565A and AD566A are 12-bit precision DACs that consist of three binary weighted quad current sources with 16:1 interquad current dividers (see figure 1). Each quad has four current switches with 8-4-2-1 current weighting ratios. The current switches are optimized for fast switching and low transient glitches at the output of the DAC during input code changes.

Full scale accuracy of the DACs are maintained over temperature and time by the DAC control amplifier that includes a current switch reference device that implements first order correction for resistor, transistor V_{BE} and beta changes with temperature so that the only remaining errors are those that are induced by component mismatch.

The AD565A has a buried zener diode that is used for the on chip 10V voltage reference. In the feedback of the reference amplifier is a temperature compensation circuit that allows reference temperature coefficients as low as 10ppm/°C to be achieved. The 10V output of the voltage reference is laser trimmed to within ±10mV.

Application Hints

To realize the true performance of the AD565A and AD566A special attention must be taken in the application of the device.

The settling time of the DAC is specified in the current output mode. However, most DAC applications require a current to voltage conversion. The simplest, and fastest voltage conversion technique is achieved by connecting a low value resistor directly between the output and ground (see figure 2). The settling time is a function of the cell switching and the RC time constant of the AD565A and AD566A output capacitance (typically 25pF) plus any stray capacitance, and the value of the output resistor. Settling to 0.01% (½LSB) of full scale for a full scale change requires 9.1 time constants. The effect of the external resistor becomes important when the equivalent resistance at the output of the DAC is over 1kΩ.

The wide compliance voltages of the AD565A and AD566A allow direct current to voltage conversion with just an output resistor. Connecting the internal gain (span) resistors (pins 10 and 11) to ground and the bipolar offset resistor to the internal 10V reference on the AD565A and an external 10V reference for the AD566A, a bipolar output voltage swing of ±1.60V

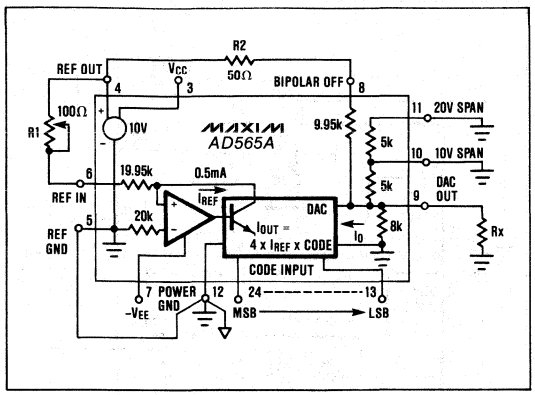


Figure 2. Unbuffered Bipolar Voltage Output

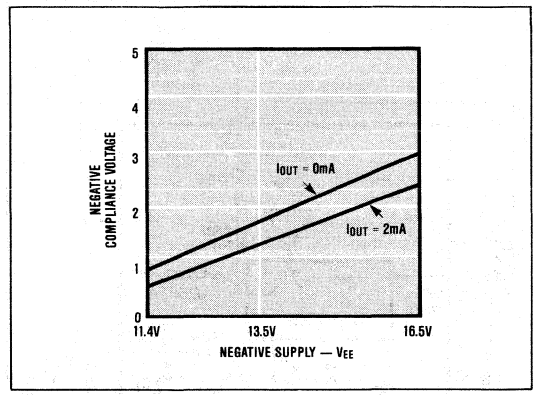


Figure 3. Typical Negative Compliance Range vs. Negative Supply

can be generated. Other combinations of external and the internal resistors can scale the full scale output current of 0 to -2mA to any voltage as long as this voltage stays within the compliance voltage of the AD565A and AD566A, which is typically -2V to +10V. For example, setting the Rx = 2.67kΩ produces an equivalent impedance of 1kΩ giving a ±1V output voltage swing.

The output voltage compliance of typically -2V to +10V allows the performance of the DAC to be unaffected by changes in the output terminal voltage. There is however, an equivalent output resistance of 8kΩ in parallel with 25pF which produces an equivalent current error when the output voltage deviates from ground. This effect is linear and is independent of the digital input code. Output swings outside the compliance range can cause either output stage saturation or breakdown which may result in non-linear performance. The compliance limits are affected only by the output current and the negative supply voltage. The positive supply voltage has no effect. Figure 3 shows the typical negative compliance versus the negative supply voltage.

The current output of the DAC can directly drive 50Ω and 75Ω coaxial cable. Terminating the cable in it's characteristic impedance would produce a ±50mV full scale swing for the 50Ω and ±75mV for the 75Ω cable. The settling times are dominated by the internal settling of the AD565A and AD566A.

The high speed current steering switching cell and internally compensated reference amplifier of the AD565A and AD566A have been specifically designed for fast settling. The typical settling time to ±0.01% (½LSB) for the major carry or full scale change (worst case transition) is about 200ns; the lower order bits all settle in less than 200ns. The maximum guaranteed settling time to 0.01% (±½LSB) for the AD565A is 250ns and 350ns for the AD566A.

Buffered Voltage Output

If an external op-amp is used to provide low impedance output drive and high voltage swing, some loss in settling time will occur due to the op-amp's own settling characteristics. In these applications the DAC's output capacitance should be compensated by a feedback capacitor connected across the amplifier's output and inverting input as shown in figures 4 and 5.

If a low offset amplifier such as the MAX400M (10μV max.) or MAX400C (15μV max.) is used, excellent performance can be obtained without any trimming. Figures 4(a), 4(b), and 4(c) show how to connect the AD565A for both unipolar and bipolar voltage outputs. The connections for the AD566A are shown in figures 5(a), 5(b), and 5(c). The preferred trimming techniques are shown for both offset and gain adjustments if required. Substituting a fixed 50Ω resistor in place of the 100Ω potentiometers, the unipolar zero offset error will be within ±½LSB (plus op-amp offset), and full scale accuracy will be within 0.1% (0.25% max.). Similarly, the bipolar zero offset error will be typically within ±2LSB (0.05%).

Unipolar configuration zero and gain adjustment

Figures 4(a) and 5(a) show the configurations for a unipolar 0 to +10V output. The bipolar offset resistor is tied to ground if zero offset adjustment is not required.

Turn all bits OFF and adjust potentiometer R1 until DAC output reads 0.000V (1LSB = 2.44mV). If offset adjust is not required tie pin 8 to ground.

Next, turn all bits ON and adjust gain potentiometer R2 until DAC output reads 9.9976V (full scale -1 LSB). If full scale of 10.2400V is required (2.5mV/bit) then insert a 120Ω resistor between op-amp output and pin 10 (10V span resistor).

High Speed 12-Bit Monolithic D/A Converters

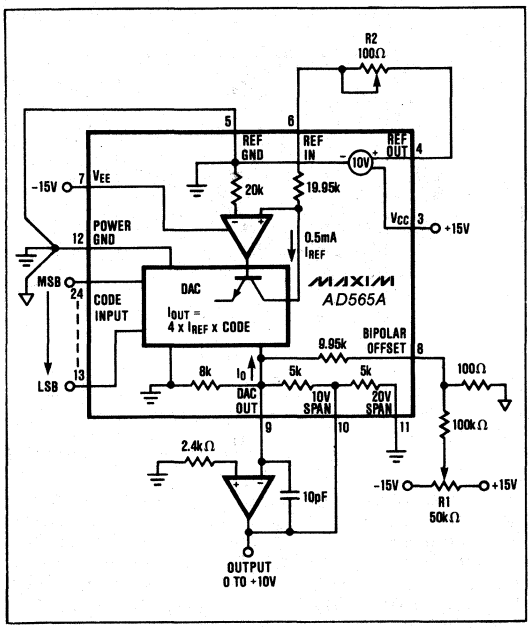


Figure 4(a). AD565A 0 to +10V Unipolar Voltage Output

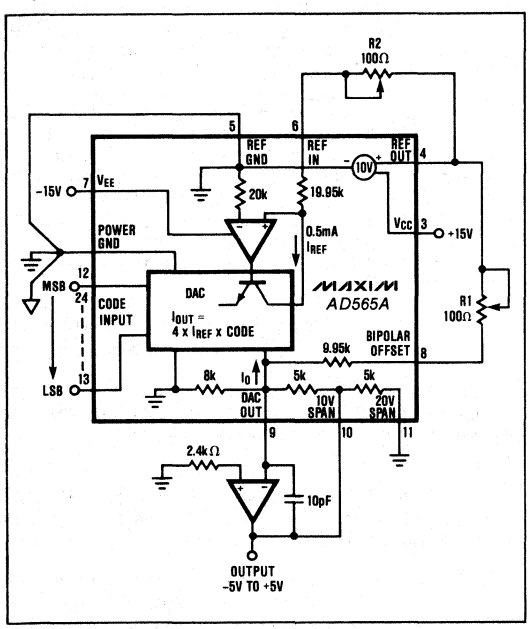


Figure 4(b). AD565A ±5V Bipolar Voltage Output

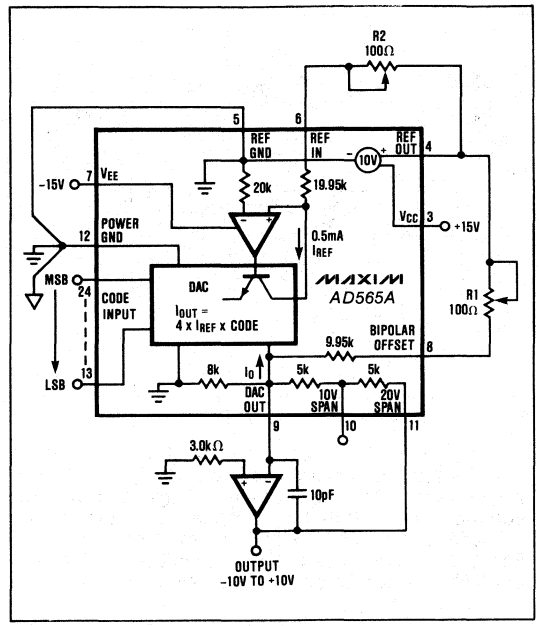


Figure 4(c). AD565A ±10V Bipolar Voltage Output

Bipolar configuration offset and gain adjustment

Figures 4(b) and 5(b) show how to configure the DAC to produce an output from -5.000V (all 0's) to +4.9976V (all 1's).

First turn OFF all bits, adjust potentiometer R1 to give -5.000V output.

Then turn all bits ON. Adjust potentiometer R2 to give a DAC output of +4.9976V.

Other voltage ranges

The AD565A and AD566A can easily be configured for unipolar 0 to +5V range or ±2.5V and ±10V bipolar ranges by using the 20V span resistor (pin 11). Connecting pin 9 and 11 together a 5V span can be developed by connecting pin 10 to the output of the op-amp and the bipolar offset resistor to either ground for the unipolar 0 to +5V range or to REF OUT for the bipolar ±2.5V range. For the ±10V (20V span) connect pin 11 to the op-amp output and the bipolar offset resistor to potentiometer R1 as shown in figures 4(c) and 5(c).

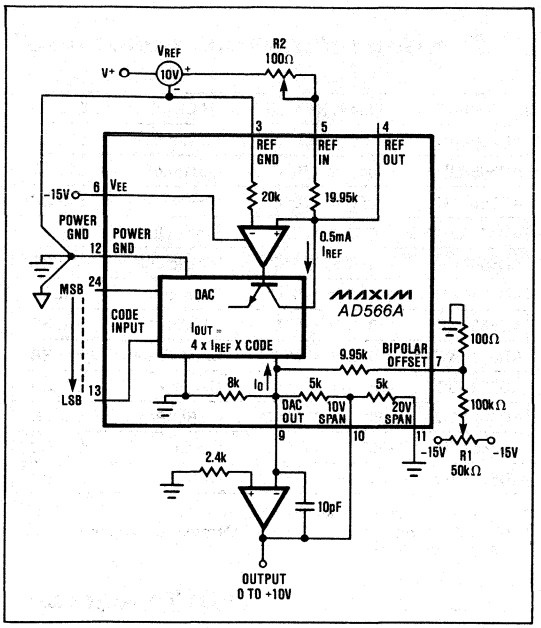


Figure 5(a). AD566A 0 to +10V Unipolar Voltage Output

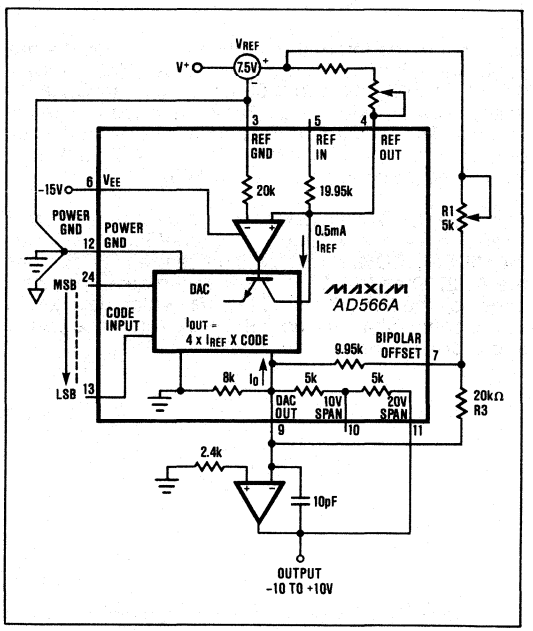


Figure 5(c). AD566A ±10V Bipolar Voltage Output

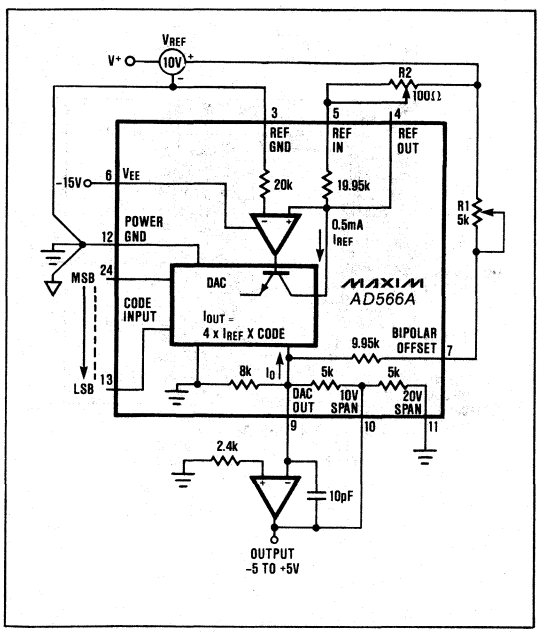


Figure 5(b). AD565A ±5V Bipolar Voltage Output

Grounding

The AD565A and AD566A have two ground pins, Reference GND and Power GND. The current in the power ground varies with the digital input code and should be connected to the local ground, digital ground or power ground. The reference ground is the ground point for the internal reference amplifier and should be connected to the system's "high quality" ground, usually called signal or analog ground.

Internal/External Reference Use

The AD565A has an internal reference whereas the AD566A requires an external reference. The AD565A can be used with either the internal reference or an external reference. With an external 10V reference there may not be enough adjustment range to accommodate a reference that does not match the internal reference voltage. The AD566A is recommended for applications that need to be driven with an external reference.

The internal reference of the AD565A is a low noise buried zener diode that is buffered by an internal amplifier whose gain is trimmed for absolute accuracy and temperature stability. The performance of the AD565A DAC is tested and specified using the internal reference.

High Speed 12-Bit Monolithic D/A Converters

In addition, the internal reference of the AD565A has sufficient buffering to drive the internal DAC (typically 0.5mA to REF IN and 1.0mA to Bipolar Offset, if used) plus an additional 1.5mA for driving external circuits. The temperature coefficient of the reference output voltage is comparable to the DAC's full scale TC for the particular grade of AD565A.

For the AD566A an external reference is required that should have a low temperature coefficient, such as the AD581, AD584, or precision references such as the AD2700 and AD2710. For the ultimate in performance use the MAX670 and MAX671, which have kelvin sense connections for both the +10V reference output and ground return.

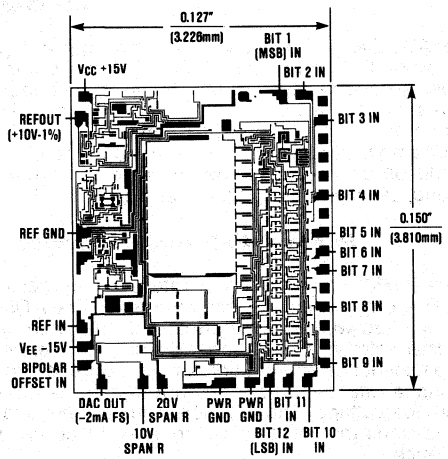
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD566AJN	0°C to +70°C	Plastic DIP	±½LSB
AD566AJD	0°C to +70°C	Ceramic	±½LSB
AD566AJQ	0°C to +70°C	CERDIP**	±½LSB
AD566AJCWG	0°C to +70°C	Small Outline	±½LSB
AD566AKN	0°C to +70°C	Plastic DIP	±¼LSB
AD566AKD	0°C to +70°C	Ceramic	±¼LSB
AD566AKQ	0°C to +70°C	CERDIP**	±¼LSB
AD566AKCWG	0°C to +70°C	Small Outline	±¼LSB
AD566ASD	-55°C to +125°C	Ceramic	±½LSB
AD566ASQ	-55°C to +125°C	CERDIP**	±½LSB
AD566ATD	-55°C to +125°C	Ceramic	±¼LSB
AD566ATQ	-55°C to +125°C	CERDIP**	±¼LSB

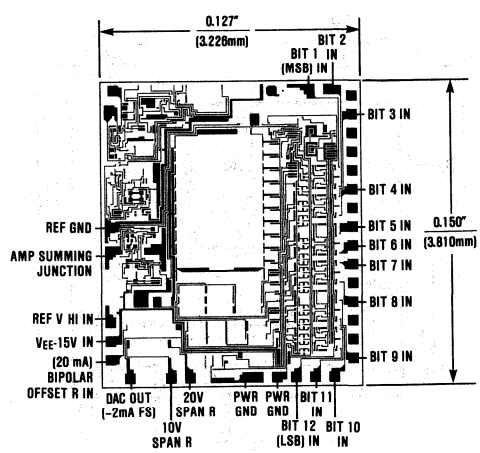
* *All devices — 24 lead packages*
** *MAXIM reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Chip Topography

AD565A



AD566A



CMOS 8-Bit DAC with Output Amplifier

General Description

The AD7224 is a precision voltage-output CMOS digital-to-analog converter (DAC) which includes an output amplifier on chip. Only an external reference source is required for operation and the fully specified accuracy is achieved with no external trims.

Double buffered interface logic is included to allow simultaneous updating in systems which have several DAC channels in operation. Control is provided by CS, WR, and LDAC (Load DAC) inputs. A RESET input is provided which acts as a zero override. All logic inputs are compatible with TTL and 5V CMOS logic levels.

Specified Performance is guaranteed for reference inputs ranging from +2V to +12.5V when using dual supplies. With a +10V reference the performance is also specified for single supply operation. The DAC output can drive +10V into a 2kΩ load.

Applications

Automatic Calibration

Motion Control

Digital Attenuators

Function Generators

Features

- Voltage Output
- Complete DAC with Output Amplifier
- Single or Dual Supply Operation
- 1 LSB Unadjusted Error
- Double Buffered Logic Inputs

Ordering Information

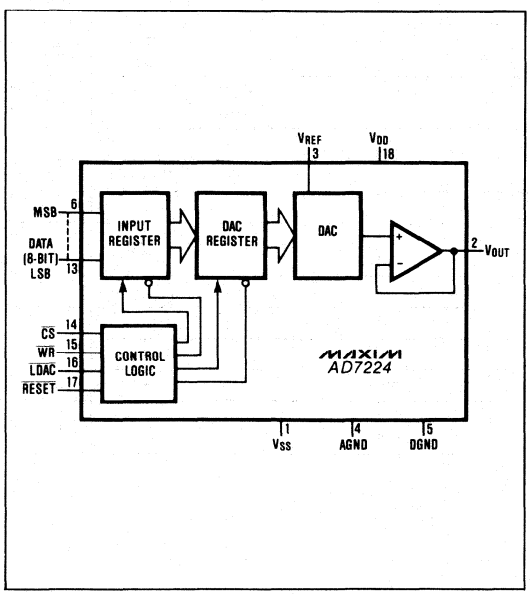
PART	TEMP. RANGE	PACKAGE*	ERROR
AD7224KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7224LN	0°C to +70°C	Plastic DIP	±1 LSB
AD7224C/D	0°C to +70°C	Dice	±2 LSB
AD7224KCWN	0°C to +70°C	Wide S.O.	±2 LSB
AD7224LCWN	0°C to +70°C	Wide S.O.	±1 LSB
AD7224BQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7224CQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7224TD	-55°C to +125°C	Ceramic	±2 LSB
AD7224UD	-55°C to +125°C	Ceramic	±1 LSB
AD7224TQ	-55°C to +125°C	CERDIP**	±2 LSB
AD7224UQ	-55°C to +125°C	CERDIP**	±1 LSB

* *All devices—18 lead packages*

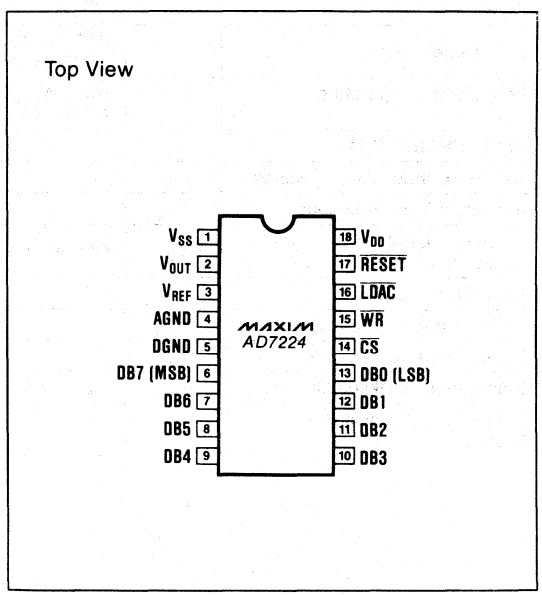
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

2

Functional Diagram



Pin Configuration



CMOS 8-Bit DAC with Output Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
AGND to DGND ..... -0.3V, V_{DD}
V_{SS} to DGND ..... -7V, V_{DD} + 0.3V
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{REF} to AGND ..... -0.3V, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}

Power Dissipation (Any Package) to +75°C 450mW
Derating above +75°C ..... 6mW/°C
Operating Temperature
AD7224K/L ..... 0°C to +70°C
AD7224A/B ..... -25°C to +85°C
AD7224T/U ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 secs) ..... +300°C

The output may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7224, Dual Supply Operation

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V) (Note 1), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{REF} = +10V V_{DD} = +15V ± 5%	AD7224L/C/U AD7224K/B/T			±1 ±2	LSB
Relative Accuracy		AD7224L/C/U AD7224K/B/T				±½ ±1	LSB
Differential Nonlinearity		Guaranteed Monotonic				±1	LSB
Full Scale Error		AD7224L/C/U AD7224K/B/T				±1 ±1½	LSB
Full Scale Temperature Coefficient		V_{REF} = +10V			±5		ppm/°C
Zero Code Error		AD7224L/C/U AD7224K/B/T				±20 ±30	mV
Zero Code Temperature Coefficient		AD7224L/C/U AD7224K/B/T			±30 ±50		μV/°C
REFERENCE INPUT							
Reference Input Voltage Range	V_{REF}			2		V_{DD} - 4	V
Reference Input Resistance	V_{REF}			8			kΩ
Reference Input Capacitance (Code Dependent, Note 2)	C_{REF}	DAC at full scale code.				100	pF
DIGITAL INPUTS							
Digital Input High Voltage	V_{INH}			2.4			V
Digital Input Low Voltage	V_{INL}					0.8	V
Digital Input Leakage Current		V_{IN} = 0V or V_{DD}				±1	μA
Digital Input Capacitance (Note 2)						8	pF

ELECTRICAL CHARACTERISTICS—AD7224, Dual Supply Operation (Continued)

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V) (Note 1), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate (Note 2)			2.5	10		V/µs
Voltage Output Settling Time (Note 5)		To 1/2 LSB, V_{REF} = +10V		2	5	µs
Digital Feedthrough (Notes 3, 4)		All 0's to all 1's code change, V_{REF} = 0V		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+11.4		+16.5	V
V_{SS} Range		For Specified Performance	-4.5		-5.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, at V_{INL}/V_{INH} T_A = 25°C Over Temp			4 6	mA
Negative Supply Current	I_{SS}	Outputs unloaded, at V_{INL}/V_{INH} T_A = 25°C Over Temp			3 5	mA
SWITCHING CHARACTERISTICS (Note 2)						
Chip Select to Write Setup Time	t_{CS}		0			ns
Load DAC to Write Setup Time	t_{LS}		0			ns
Chip select to Write Hold Time	t_{CH}		0			ns
Load DAC to Write Setup Time	t_{LH}		0			ns
Data Valid to Write Setup Time	t_{DS}	T_A = 25°C Over Temp	90 100			ns
Data Valid to Write Hold Time	t_{DH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C Over Temp	150 200			ns
Chip Select Pulse Width	t_{CW}	T_A = 25°C Over Temp	150 200			ns
Reset Pulse Width	t_{RS}	T_A = 25°C Over Temp	150 200			ns
Load DAC ($\overline{LDAC}$) Pulse Width	t_{LD}	T_A = 25°C Over Temp	150 200			ns

Note 1: Maximum possible reference voltage.
Note 2: Sample tested at 25°C to ensure compliance.
Note 3: Guaranteed, but not 100% production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.
Note 5: Positive or negative full scale change.

CMOS 8-Bit DAC with Output Amplifier

ELECTRICAL CHARACTERISTICS—AD7224, Single Supply Operation

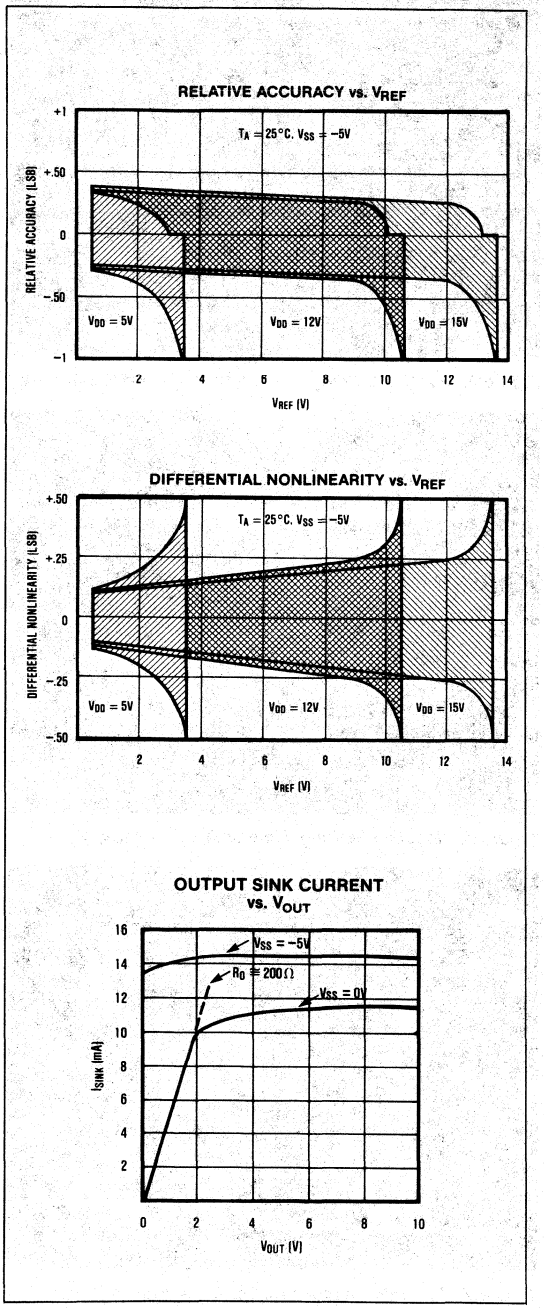
(V_{DD} = +15V ± 5%, V_{SS} = AGND = DGND = 0V, V_{REF} = +10V (Note 1), Over Temperature unless otherwise stated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error					±2	LSB
Differential Nonlinearity		Guaranteed Monotonic			±1	LSB
REFERENCE INPUT						
Reference Input Resistance	R_{REF}		8			kΩ
Reference Input Capacitance (Code Dependent)(Note 2)	C_{REF}	DAC at full scale code			100	pF
DIGITAL INPUTS						
Digital Input High Voltage	V_{INH}		2.4			V
Digital Input Low Voltage	V_{INL}				0.8	V
Digital Input Leakage Current		V_{IN} = 0V to V_{DD}			±1	μA
Digital Input Capacitance (Note 2)					8	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate (Note 2)			2.5	10		V/μs
Output Settling Time (Note 2)		To 1/2 LSB, Positive FS Chg		2	5	μs
		To 1/2 LSB, Negative FS Chg		3	8	μs
Digital Feedthrough (Notes 3, 4)		All 0's to all 1's code change, V_{REF} = 0V		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+14.25		+15.75	V
Positive Supply Current	I_{DD}	Outputs unloaded, at V_{INL}/V_{INH}, T_A = 25°C			4	mA
		Outputs unloaded, at V_{INL}/V_{INH}, Over Temp			6	mA
SWITCHING CHARACTERISTICS (Note 2)						
Chip Select to Write Setup Time	t_{CS}		0			ns
Load DAC to Write Setup Time	t_{LS}		0			ns
Chip select to Write Hold Time	t_{CH}		0			ns
Load DAC to Write Setup Time	t_{LH}		0			ns
Data Valid to Write Setup Time	t_{DS}	T_A = 25°C	90			ns
		Over Temp	100			ns
Data Valid to Write Hold Time	t_{DH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C	150			ns
		Over Temp	200			ns
Chip Select Pulse Width	t_{CW}	T_A = 25°C	150			ns
		Over Temp	200			ns
Reset Pulse Width	t_{RS}	T_A = 25°C	150			ns
		Over Temp	200			ns
Load DAC ($\overline{LDAC}$) Pulse Width	t_{LD}	T_A = 25°C	150			ns
		Over Temp	200			ns

Note 1: Maximum possible reference voltage.
Note 2: Sample tested at 25°C to ensure compliance.
Note 3: Guaranteed, but not 100% production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

CMOS 8-Bit DAC with Output Amplifier

Typical Operating Characteristics



Detailed Description

D/A Section

The AD7224 contains an 8-bit digital-to-analog converter that operates in the voltage output mode. The output voltage is of the same polarity as the external reference voltage thus allowing single supply operation. A DAC switch pair arrangement on the AD7224 allows a reference voltage range from +2V to +12.5V.

The DAC consists of a stable thin-film resistor R-2R ladder and eight NMOS single pole, double-throw switches. A simplified circuit diagram is shown in Figure 1.

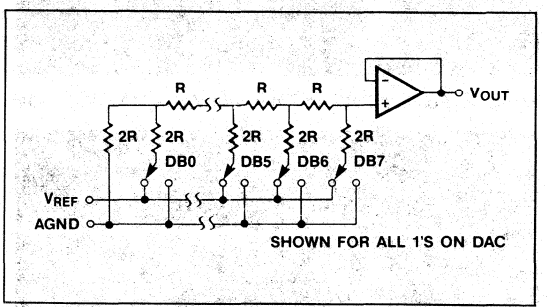


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin is code dependent and varies from 8kΩ minimum to infinity. The lowest input impedance occurs when the DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low impedance under changing load conditions. Capacitance at the reference terminal is also code dependent and typically varies from 25pF to 50pF.

The V_{OUT} pin can be considered as a digitally-programmable voltage source with the output defined by:

$$V_{OUT} = D \cdot V_{REF}$$

where D is a fractional representation of the digital input code and can vary from 0 to 255/256.

Output Buffer Amplifier

The DAC's voltage output is buffered by a unity-gain CMOS voltage follower that slews at greater than 2.5V/μs. This amplifier is capable of driving a 2kΩ load to +10V. When driving a 2kΩ load in parallel with 100pF with full-scale transitions (0V to +10V or +10V to 0V), the output settles to 1/2LSB in less than 5μs. Typical dynamic response and settling performance of the AD7224 is shown in Figures 2 through 7.

The AD7224 can be operated single or dual supply. In single supply operation, Maxim's AD7224 can sink and source up to 5mA.

CMOS 8-Bit DAC with Output Amplifier

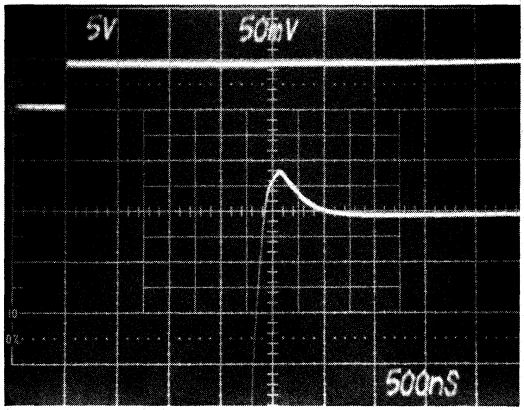


Figure 2. Positive Settling Time with V_{DD} = +15V, V_{SS} = -5V.

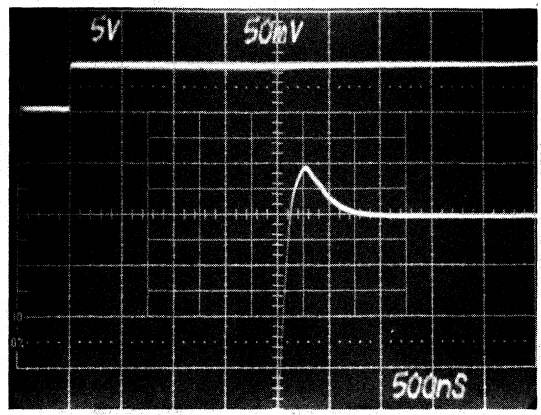


Figure 3. Positive Settling Time with V_{DD} = +15V, V_{SS} = 0V.

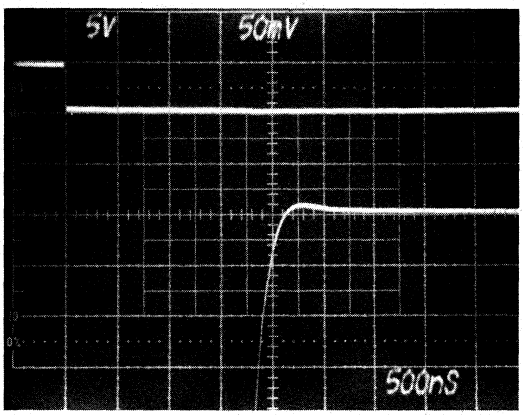


Figure 4. Negative Settling Time with V_{DD} = +15V, V_{SS} = -5V.

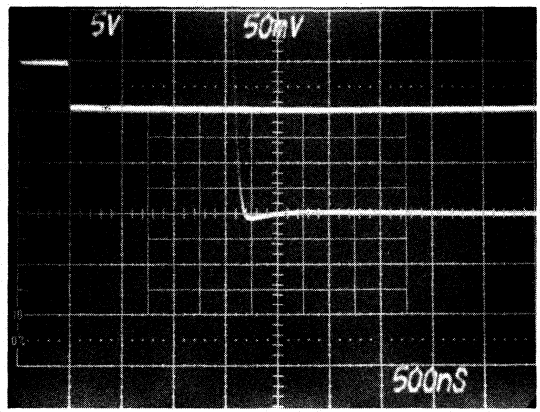


Figure 5. Negative Settling Time with V_{DD} = +15V, V_{SS} = 0V.

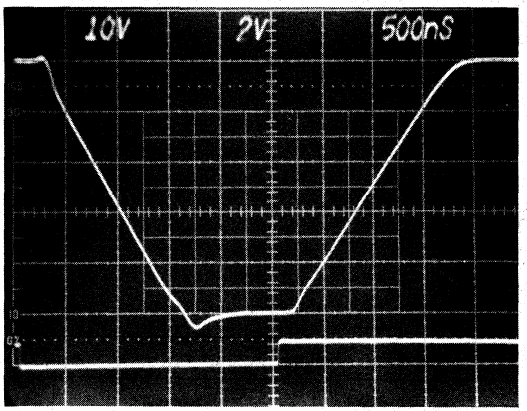


Figure 6. Dynamic Response with V_{DD} = +15V, V_{SS} = -5V.

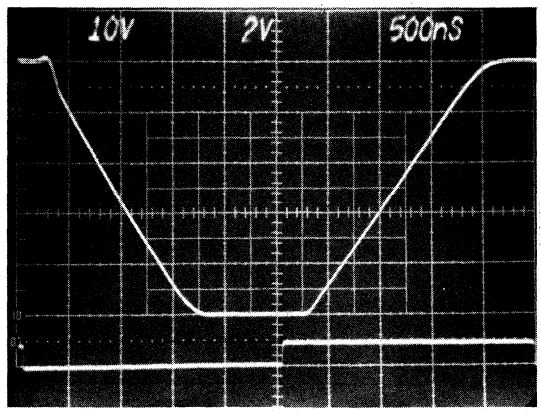


Figure 7. Dynamic Response with V_{DD} = +15V, V_{SS} = 0V.

A simplified circuit diagram of the output buffer is shown is Figure 8. Input common-mode range to V_{SS} is provided by a PMOS input structure. The improved output circuitry incorporates a Maxim proprietary pull-down circuit to actively drive V_{OUT} to within typically +15mV of the negative supply (V_{SS}). Maxim's improved buffer circuitry allows the output to sink and source up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to GND, so that zero error is kept at or under 1/2LSB (V_{REF} = +10V). A plot of output sink current versus output voltage is shown in the Typical Operating Characteristics section.

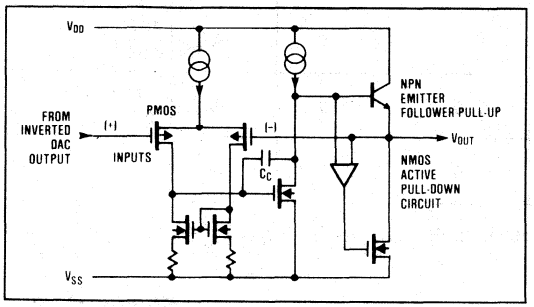


Figure 8. Simplified Output Buffer Circuit

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic. Power supply current, I_{DD} and I_{SS}, are specified for TTL input levels. The supply currents are somewhat dependent on input logic level and are highest when the AD7224 is driven from TTL, however, they can be significantly reduced if the inputs are driven as close to +5V as possible.

Table 1 shows the truth table for AD7224 operation. The part contains two registers, an input register and a DAC register. $\overline{CS}$ and $\overline{WR}$ control the loading of the input register while $\overline{LDAC}$ and $\overline{WR}$ control the transfer of information from the input to the DAC register. Only the data held in the DAC register will determine the converter's analog output.

All control signals are level-triggered and therefore either or both registers may be made transparent; the input register by keeping $\overline{CS}$ and $\overline{WR}$ "LOW," the DAC register by keeping $\overline{LDAC}$ and $\overline{WR}$ "LOW." The rising edge of the $\overline{WR}$ input latches input data.

The contents of both registers are reset by a low level on the $\overline{RESET}$ line. With both registers transparent, the $\overline{RESET}$ line overrides input data for the duration of the $\overline{RESET}$ pulse. If both registers are latched, a "LOW" pulse on the $\overline{RESET}$ will latch all 0's into the registers, with the output remaining at 0V after the reset pulse has been removed. The $\overline{RESET}$ line can be used to force 0V on the output at power-up, and is also useful as a zero override in system calibration cycles. Figure 9 shows the input control logic for the AD7224.

Table 1. AD7224 Truth Table

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	⌐	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	⌐	H	DAC Register Latched
L	X	X	X	Both Registers Loaded with all Zeros
⌐	H	H	H	Both Registers Latched with all Zeros and Output Remains at Zero
⌐	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care

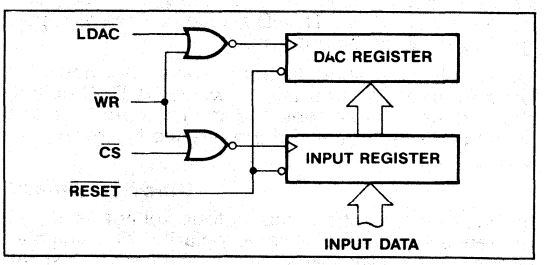


Figure 9. Input Control Logic

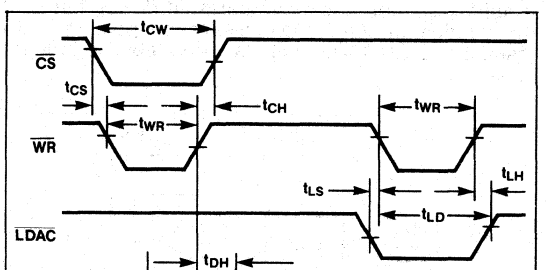


Figure 10. Write Cycle Timing Diagram

CMOS 8-Bit DAC with Output Amplifier

Applications Information

Power Supply and Reference Operating Ranges

The AD7224 is fully specified to operate with V_{DD} between +12V ± 5% and +15V ± 10% (+11.4V to +16.5V), and with V_{SS} from 0V to -5.5V. Eight bit performance is also guaranteed for single supply operation (V_{SS} = 0V), however zero code error is reduced when V_{SS} is -5V (see Output Buffer Amplifier section).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least 4V below V_{DD}. The AD7224 is specified to operate with a reference input range of +2V to V_{DD} - 4V.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (1N914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between the DAC output, the reference input, and the digital inputs. This is particularly important if the reference is driven from an AC source.

Unipolar Output

In unipolar operation, the output voltage and the reference input are the same polarity. The unipolar circuit configuration is shown in Figure 11. A slight increase in zero error occurs when the AD7224 is operated from a single supply (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to DGND. The unipolar code table is given in Table 2.

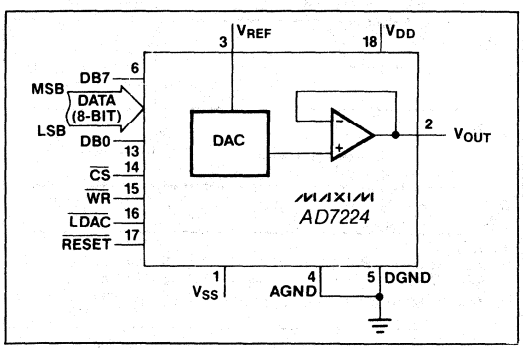


Figure 11. Unipolar Output Circuit

Table 2. Unipolar Code Table

DAC CONTENTS MSB	DAC CONTENTS LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Bipolar Output

The DAC output may be configured for bipolar operation using the circuit in Figure 12. Only one op-amp and two resistors are required. With R1 = R2:

$$V_{OUT} = V_{REF} \cdot (2D - 1)$$

where D is a fractional representation of the digital word in the DAC regiser.

Table 3 shows the digital code versus output voltage for the circuit in Figure 12.

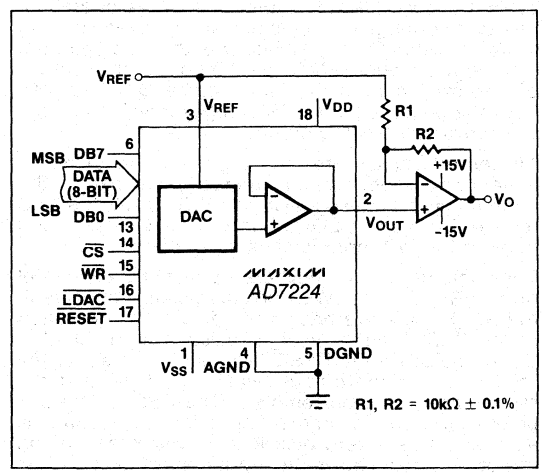


Figure 12. Bipolar Output Circuit

Table 3. Bipolar (Offset Binary) Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary non-zero output voltage for a "zero" input code. This is shown in Figure 13. The output voltage at V_{OUT} is:

$$V_{OUT} = V_{BIAS} + (D \cdot V_{IN})$$

where D is a fractional representation of the digital input word and can vary from 0 to 255/256. For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}-V_{REF} which must be at least 4V to ensure specified operation. Note that V_{DD} and V_{SS} for the AD7224 must be referenced to DGND.

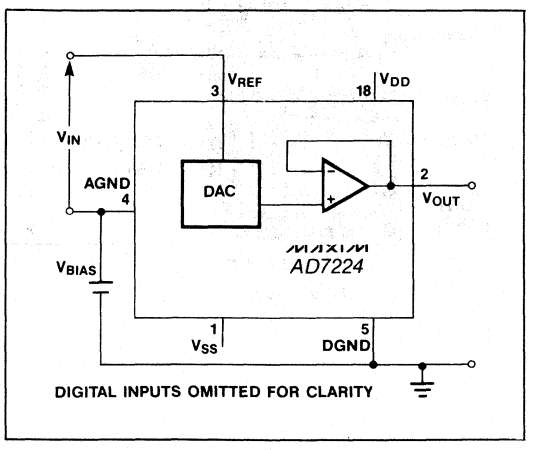


Figure 13. AGND Bias Circuit

Using an AC Reference

In applications where V_{REF} has AC signal components, the AD7224 has multiplying capability within the limits of the V_{REF} input range specifications. Figure 14 shows a technique for applying a sinewave signal to the reference input where the AC signal is biased up before being applied to V_{REF}. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

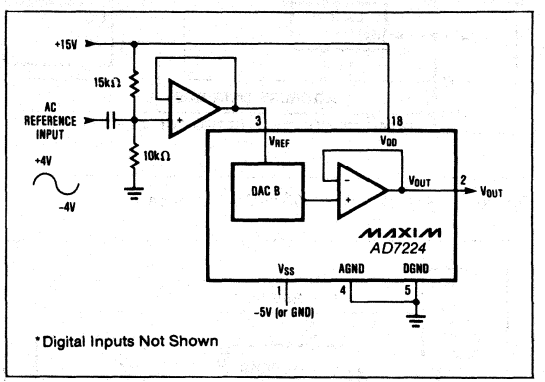


Figure 14. AC Reference Input Circuit

Generating V_{SS}

The performance of the AD7224 is specified for both dual and single supply (V_{SS} = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V V_{SS} supply can be generated using an ICL7660 in one of the circuits of Figure 15.

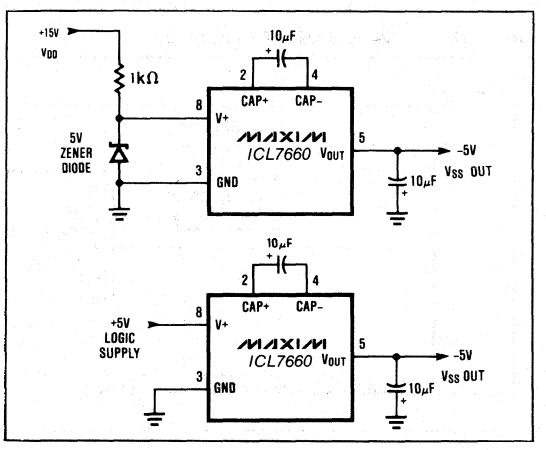


Figure 15. Generating -5V for V_{SS}

CMOS 8-Bit DAC with Output Amplifier

Microprocessor Interfacing

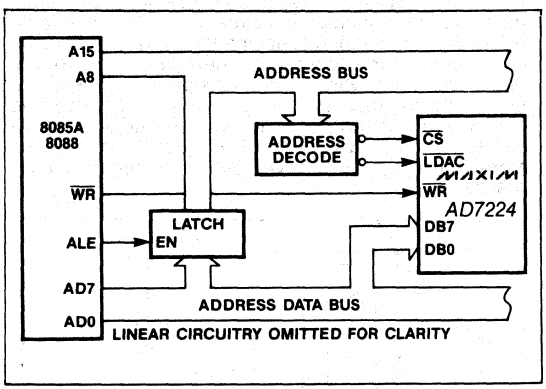


Figure 16. AD7224 to 8085A/8088 Interface

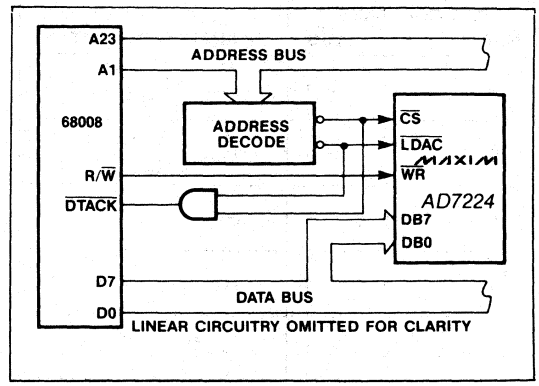


Figure 19. AD7224 to 68008 Interface

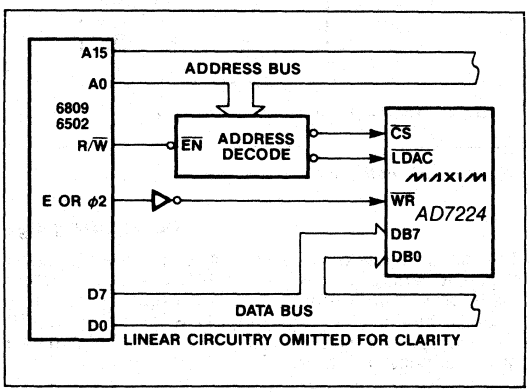


Figure 17. AD7224 to 6809/6502 Interface

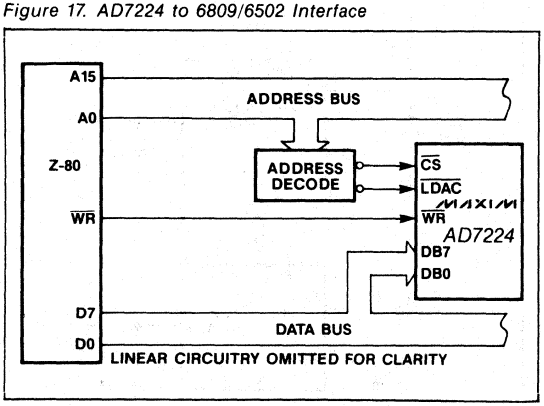
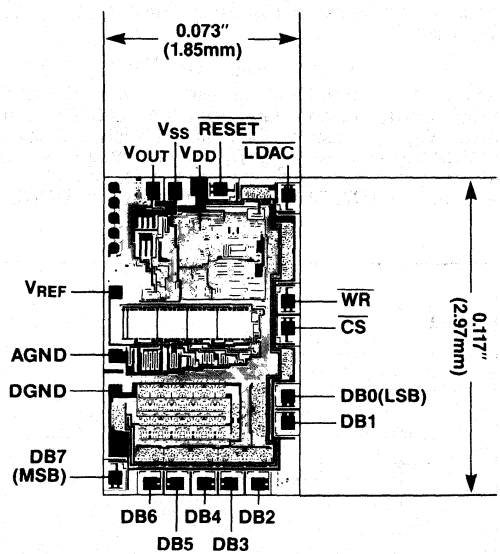


Figure 18. AD7224 to Z-80 Interface

Chip Topography



CMOS Quad 8-Bit D/A Converters

General Description

Maxim's AD7225 and AD7226 each contain four 8-bit voltage output digital-to-analog converters (DACs). They include output buffer amplifiers and input logic for simple microprocessor and TTL/CMOS interfaces. 8-bit performance is achieved over the full operating temperature range without external trimming.

The AD7225 contains double-buffered logic inputs which allow all analog outputs to be simultaneously updated using one control signal. There are also four separate reference inputs so that the range of each DAC can be independently set.

The AD7226 has separate input registers for each of its four DACs. Data is transferred into an input register from a common 8-bit TTL/CMOS compatible input port. Address inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. All DACs share a common reference input.

Applications

Minimum Component Count Analog Systems

Digital Offset/Gain Adjustment

Industrial Process Control

Arbitrary Function Generators

Automatic Test Equipment

Microprocessor Controlled Calibration

Features

- **Buffered Voltage Output**
- **Double-Buffered Inputs (AD7225)**
- **Microprocessor and TTL/CMOS Compatible**
- **Operates from Single or Dual Supplies**
- **Requires No External Adjustments**

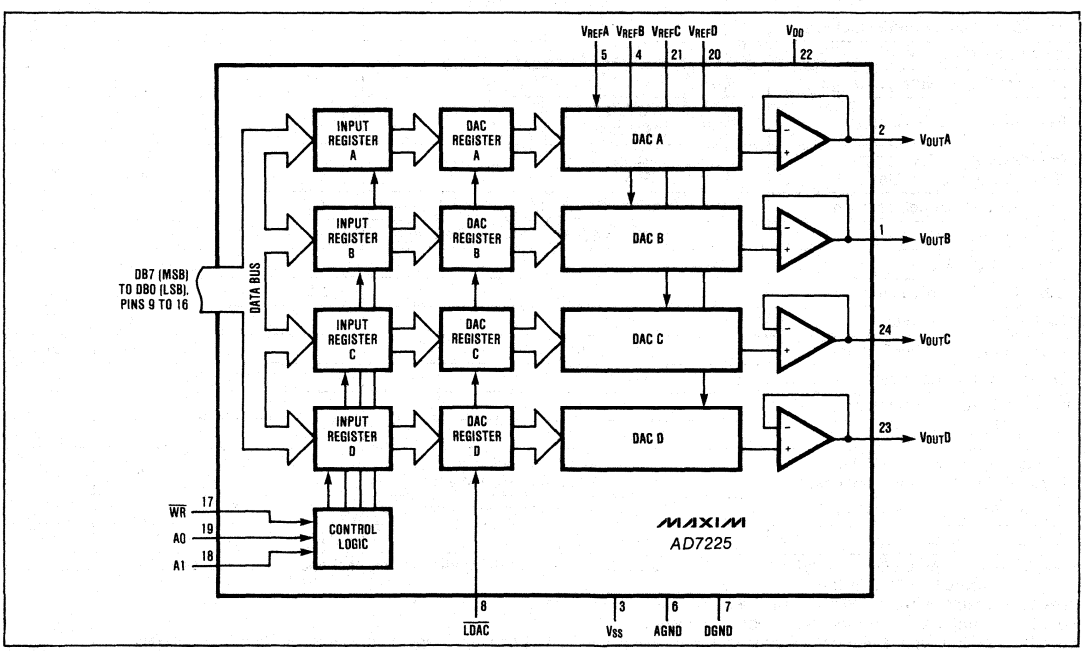
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7225KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7225KCWG	0°C to +70°C	Small Outline	±2 LSB
AD7225LN	0°C to +70°C	Plastic DIP	±1 LSB
AD7225LCWG	0°C to +70°C	Small Outline	±1 LSB
AD7225KC/D	0°C to +70°C	Dice	±2 LSB
AD7225BQ	-25°C to +85°C	CERDIP	±2 LSB
AD7225CQ	-25°C to +85°C	CERDIP	±1 LSB
AD7225TQ	-55°C to +125°C	CERDIP	±2 LSB
AD7225UQ	-55°C to +125°C	CERDIP	±1 LSB
AD7226KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7226KCWP	0°C to +70°C	Small Outline	±2 LSB
AD7226KC/D	0°C to +70°C	Dice	±2 LSB
AD7226BQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7226TD	-55°C to +125°C	Ceramic	±2 LSB
AD7226TQ	-55°C to +125°C	CERDIP**	±2 LSB

* *AD7225 — 24 lead, 300 mil package, AD7226 — 20 lead package.*

** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Functional Block Diagram (AD7225)



CMOS Quad 8-Bit D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to AGND ..... -7V, V_{DD}
V_{SS} to DGND ..... -7V, V_{DD}
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{REF} to AGND ..... -0.3V, V_{DD}
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}

Power Dissipation (Any Package) to +75°C 500mW
Derating above +75°C ..... 2mW/°C
Operating Temperature
Commercial (AD722XK/L) ..... 0°C to +70°C
Industrial (AD722XB/C) ..... -25°C to +85°C
Military (AD722XT/U) ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Dual Supply Specifications

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error		V_{DD} = +15V±5%, V_{REF} = +10V: AD7225LN/CQ/UQ			±1	LSB
		V_{DD} = +15V±5%, V_{REF} = +10V: All other devices			±2	LSB
Relative Accuracy		AD7225LN/CQ/UQ			±½	LSB
		All Other Devices			±1	LSB
Differential Nonlinearity		Guaranteed Monotonic			±1	LSB
Full Scale Error		AD7225LN/CQ/UQ			±½	LSB
		AD7225KN/BQ/TQ			±1	LSB
		All other devices			±1½	LSB
Full Scale Temperature Coefficient		V_{REF} = +10V		±5		ppm/°C
Zero Code Error		AD7225LN/CQ/UQ, T_A = +25°C			±15	mV
		AD7225LN/CQ/UQ, Over Temp.			±20	mV
		AD7225KN/BQ/TQ, T_A = +25°C			±20	mV
		All other devices, Over Temp.			±30	mV
Zero Code Temperature Coefficient				±30		µV/°C
REFERENCE INPUT						
Reference Input Voltage Range	V_{REF}		2		V_{DD} - 4	V
Reference Input Resistance	R_{REF}	AD7225	11			kΩ
		AD7226	2			kΩ
Reference Input Capacitance (Code Dependent, Note 3)	C_{REF}	AD7225			100	pF
		AD7226	65		300	pF
Channel-to-Channel Isolation		V_{REF} = 10kHz, $10V_{P-P}$ (Note 2)	-60			dB
AC Feedthrough		V_{REF} = 10kHz, $10V_{p-p}$ (Note 2, 4)	-70			dB
DIGITAL INPUTS						
Digital Input High Voltage	V_{INH}		2.4			V
Digital Input Low Voltage	V_{INL}				0.8	V
Digital Input Leakage Current		V_{IN} = 0V or V_{DD}			±1	µA
Digital Input Capacitance		(Note 2)			8	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate		(Note 2)	3			V/µs
Voltage Output Settling Time (Pos. or Neg. Full Scale Change)		to ½LSB, V_{REF} = +10V, 2kΩ and 100pF Load (Note 2)			4	µs
Digital Feedthrough and Crosstalk		All 0's to 1's code change (Note 4)		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ

Note 1: The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.
Note 2: Sample tested at +25°C to ensure compliance.
Note 3: Guaranteed by design. Not production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND. (AD7226 only)

ELECTRICAL CHARACTERISTICS Dual Supply Specifications (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+11.4		+16.5	V
Positive Supply Current (Outputs Unloaded)	I_{DD}	AD7225KN/BQ/LN/CQ AD7225TQ/UQ AD7226			10 12 13	mA
Negative Supply Current (Outputs Unloaded)	I_{SS}	AD7225KN/BQ/LN/CQ AD7225TQ/UQ AD7226			-9 -10 -11	mA
SWITCHING CHARACTERISTICS (Note 2)						
Address to Write Setup Time	t_{AS}	Over Temp.	0			ns
Address to Write Hold Time	t_{AH}	Over Temp. AD7225 AD7226	0 10			ns
Data Valid to Write Setup Time	t_{DS}	AD7225, T_A = +25°C Over Temp. AD7226, T_A = +25°C Over Temp.	70 90 90 100			ns
Data Valid to Write Hold Time	t_{DH}	Over Temp.	10			ns
Write Pulse Width	t_{WR}	AD7225, T_A = +25°C AD7225KN/BQ/LN/CQ, Over Temp. AD7225TQ/UQ, Over Temp. AD7226, T_A = +25°C Over Temp.	95 120 150 150 200			ns
Load DAC ($\overline{LDAC}$) Pulse Width (AD7225 Only)	t_{LC}	AD7225, T_A = +25°C AD7225KN/BQ/LN/CQ, Over Temp. AD7225TQ/UQ, Over Temp.	95 120 150			ns

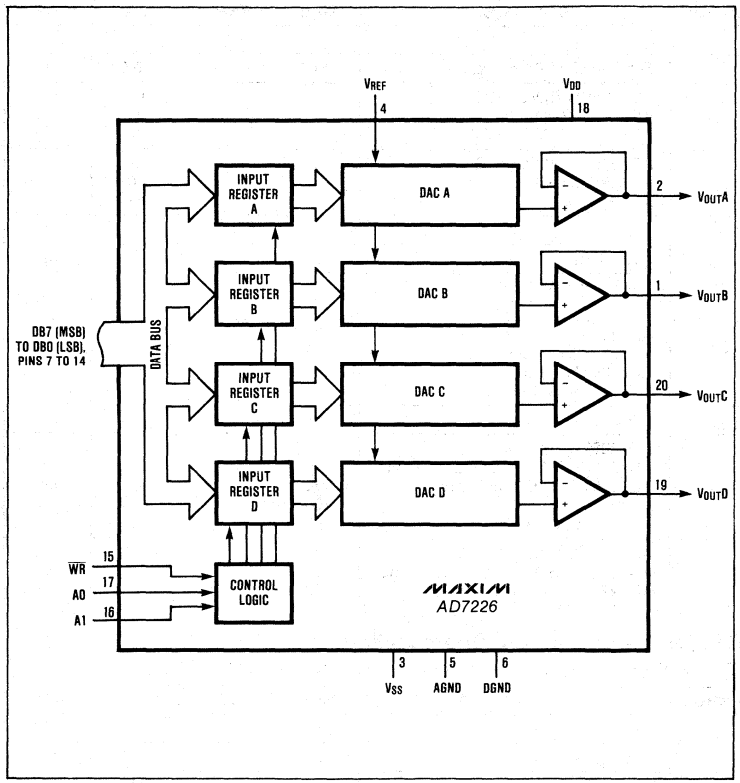
ELECTRICAL CHARACTERISTICS Single Supply Specifications

(V_{DD} = +15V ± 5%, V_{SS} = AGND = DGND = 0V, V_{REF} = +10V, Over Temperature unless otherwise stated.)

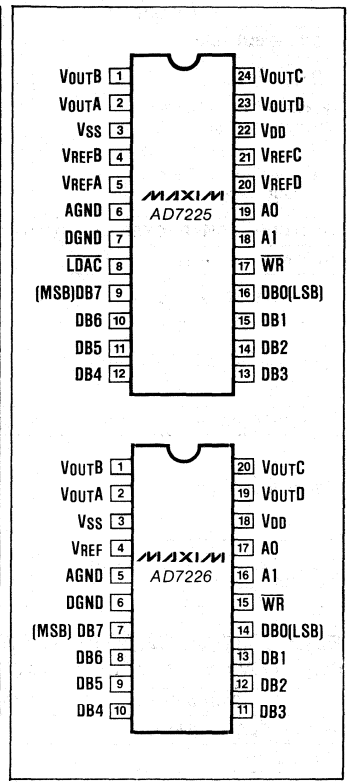
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error		AD7225LN/CQ/UQ All other devices			±1 ±2	LSB
Differential Nonlinearity		Guaranteed Monotonic			±1	LSB
REFERENCE INPUT						
Reference Input Voltage Range	V_{REF}		2		V_{DD}-4	V
Reference Input Resistance	R_{REF}	AD7225 AD7226	11 2			kΩ
Reference Input Capacitance (Code Dependent, Note 3)	C_{REF}	AD7225 AD7226	 65		100 300	pF
Channel-to-Channel Isolation		V_{REF} = 10kHz, 10V_{P-P} (Note 2)	-60			dB
AC Feedthrough		V_{REF} = 10kHz, 10V_{P-P} **(Note 2, 4)**	-70			dB
DIGITAL INPUTS — All Specifications Are The Same as For Dual Supply Operation						
DYNAMIC PERFORMANCE — All Specifications Are The Same as For Dual Supply Operation						
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+14.25		+15.75	V
Positive Supply Current Output Unloaded	I_{DD}	AD7225KN/BQ/LN/CQ AD7225TQ/UQ AD7226			10 12 13	mA
SWITCHING CHARACTERISTICS — All Specifications Are The Same as For Dual Supply Operation						

CMOS Quad 8-Bit D/A Converters

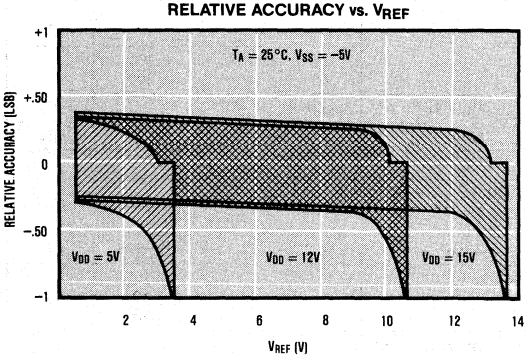
Functional Block Diagram (AD7226)

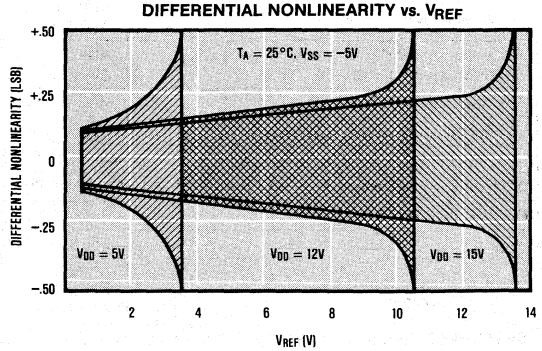


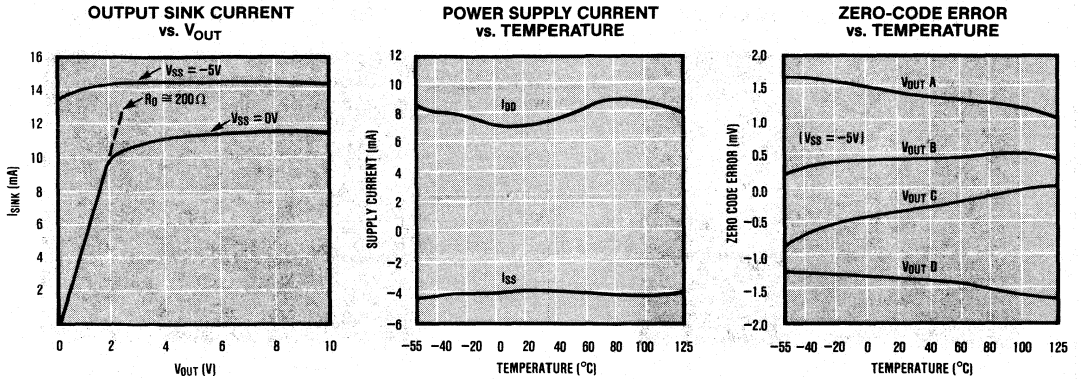
Pin Configurations



Typical Operating Characteristics







Detailed Description

The AD7225 and AD7226 have four matched voltage output digital-to-analog converters (DACs). The DAC's are "inverted" R-2R ladder networks which convert 8 bit digital words into equivalent analog output voltages in proportion to the applied reference voltage(s). Each DAC in the AD7225 has a separate reference input whereas in the AD7226, all reference inputs are tied together. A simplified circuit diagram of one of the four DACs is provided in Figure 1.

V_{REF} Input

The voltage at V_{REF} sets the full-scale output of the DAC. The input impedance of the V_{REF} input(s) is code dependent. The lowest value, approximately 11kΩ for the AD7225 and 2kΩ for the AD7226, occurs when the input code is 01010101. The maximum value is infinity, which occurs when the input code is 00000000. Because the input resistance at V_{REF} is code dependent, the DAC's reference sources must have an output impedance of no more than 20Ω for the AD7225 and 4Ω for the AD7226, to maintain output linearity. The input capacitance at V_{REF} is also code dependent and typically varies from 15pF to 35pF for the AD7225 and 100pF to 250pF for the AD7226.

V_{OUT}A, B, C, or D can be represented by a digitally programmable voltage source as:

$$V_{OUT} = N_B \times V_{REF}/256,$$

where N_B is the numeric value of the DAC's binary input code.

Output Buffer Amplifiers

All AD7225/26 voltage outputs are internally buffered by precision unity gain followers which slew at greater than 3V/μs. When driving 2kΩ in parallel with 100pF with full scale transitions (0V to +10V or +10V to 0V), the output settles to ±1/2LSB in less than 4μs. Typical dynamic response and settling performance of the AD7225 and AD7226 is shown in Figure 2 and 3.

A simplified circuit diagram of an output buffer is shown in Figure 4. Input common mode range to AGND is provided by a PMOS input structure. The improved

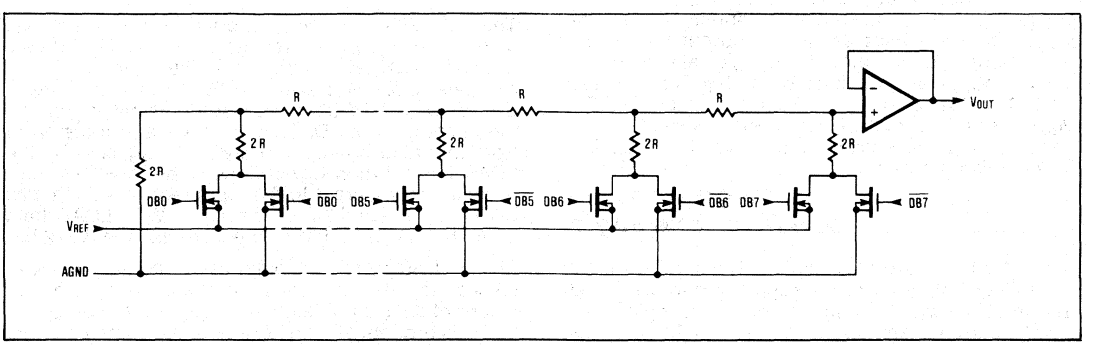


Figure 1. Simplified DAC Circuit Diagram

CMOS Quad 8-Bit D/A Converters

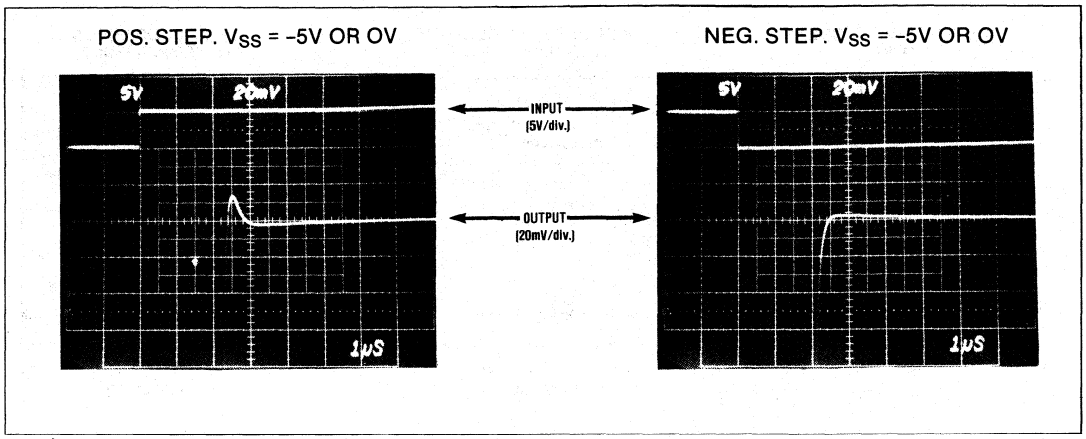


Figure 2. Positive and Negative Settling Times, V_{SS} = 0V or -5V

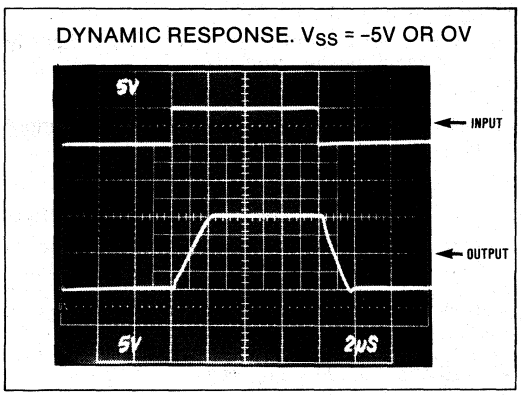


Figure 3. Dynamic Response, V_{SS} = 0V or -5V

output circuitry incorporates a Maxim proprietary pull-down circuit to actively drive V_{OUT} to within typically +15mV of the negative supply (V_{SS}). The buffer circuitry allows each DAC output to sink, as well as source, up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to GND, so that zero error is kept at or under 1/2LSB (V_{REF} = +10V). A plot of output sink current versus output voltage is shown in the Typical Operating Characteristics section.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic, however power supply currents, I_{DD} and I_{SS}, are somewhat dependent on input logic level. Supply currents are specified for TTL input levels (worst case) but are significantly reduced when the logic inputs are driven as close to DGND as possible, or above 4 volts.

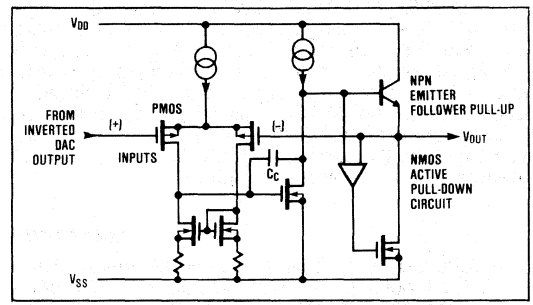


Figure 4. Simplified Output Buffer Circuit

Address lines A0 and A1 select which DAC receives data from the input port. When $\overline{WR}$ is low, the input register of the addressed DAC is transparent. The data is then latched when $\overline{WR}$ goes high. Figure 5 shows the input control logic for the AD7225 and AD7226. Table 1 lists the channel addresses.

The AD7226's four DAC outputs represent the data held in four 8 bit input registers. The AD7225 differs from the AD7226 in that in addition to the input registers, there is a separate DAC register for each DAC as well. A DAC's analog output is based only on the contents of its DAC register. Data is transferred from the input registers to the DAC registers by the $\overline{LDAC}$ input. When $\overline{LDAC}$ is LOW, all four DAC registers are transparent to the input registers so that all DACs are updated simultaneously. With $\overline{LDAC}$ held LOW, the AD7225 interface behaves like the AD7226.

Since $\overline{LDAC}$ (AD7225 only) is asynchronous with respect to $\overline{WR}$, care must be taken to assure that incorrect data is not latched through to the output. If $\overline{LDAC}$ is brought LOW before or at the same time that $\overline{WR}$ goes HIGH, then $\overline{LDAC}$ must remain LOW for at least t_{LD} to ensure that the correct data is latched. Data is latched into all four DAC registers on the

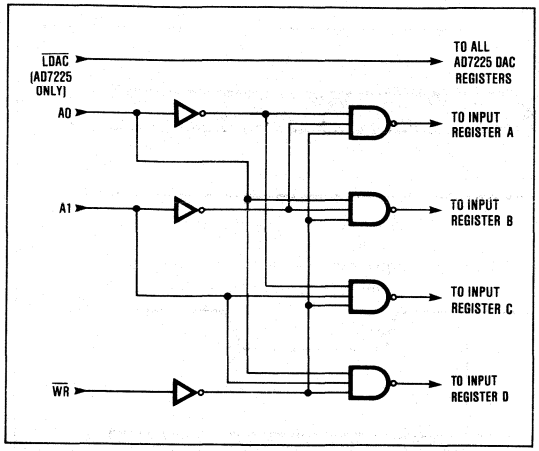


Figure 5. AD7225, AD7226 Input Control Logic

Table 1. DAC Addressing

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Table 2. AD7225, AD7226 Write Cycle Truth Table

$\overline{WR}$	$\overline{LDAC}$ (AD7225 ONLY)	FUNCTION
H	H	No operation. Device deselected.
L	H	Input register of selected DAC transparent.
⌐¯_	H	Latch the input register of selected DAC.
H	L	(AD7225 only) All four DAC registers transparent i.e. DAC outputs reflect the data held in their respective input registers. Input registers are latched.
H	⌐¯_	(AD7225 only) Latch the four DAC registers. Input registers are latched.
L	L	(AD7225 only) DAC Registers and the selected input register transparent. DAC output follows input data for selected channel.

rising edge of $\overline{LDAC}$. Table 2 shows the truth table for $\overline{WR}$ and $\overline{LDAC}$ operation. Figure 6 shows the write cycle timing for both the AD7225 and AD7226.

Applications Information

Power Supply and Reference Operating Ranges

The AD7225 and AD7226 are fully specified to operate with V_{DD} between +12V ± 5% and +15V ± 10% (+11.4V to +16.5V), and with V_{SS} from 0V to -5.5V. 8 bit performance is also guaranteed for single supply operation (V_{SS} = 0V), however zero code error is reduced when V_{SS} is -5V (see Output Buffer Amplifier).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least 4V below V_{DD}. Both the AD7225 and AD7226 are specified to operate with a reference input range of +2V to V_{DD} - 4V.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (IN914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between DAC outputs, the reference input(s), and the digital inputs. This is particularly important if the reference is driven from an AC source. Figure 7 and 8 show suggested circuit board layouts for minimizing crosstalk.

Unipolar Output

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Unipolar circuit configurations are shown in Figure 9 and 10 for the AD7225 and AD7226. Both devices can be operated from a single supply with a slight increase in zero error (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to DGND. The unipolar code table is given in Table 3.

Bipolar Output

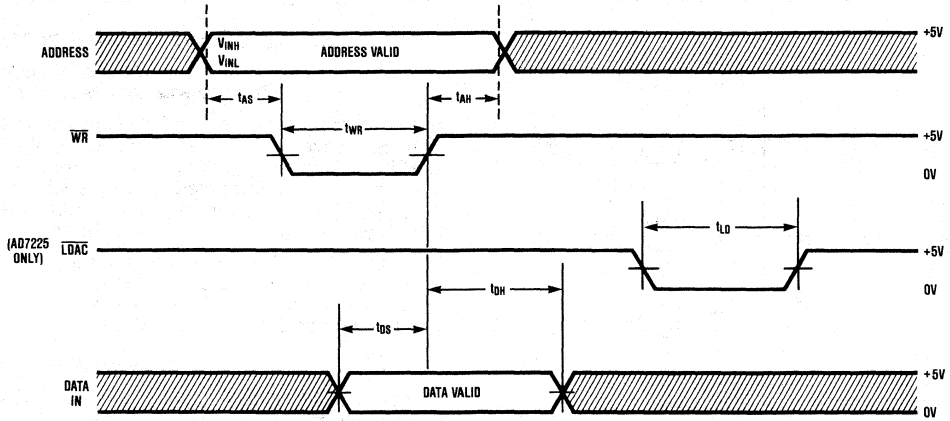
Each DAC output may be configured for bipolar operation using the circuit in Figure 11. One op-amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = V_{REF}(2D_A - 1),$$

where D_A is a fractional representation of the digital word in register A.

Table 4 shows the digital code versus output voltage for the circuit in Figure 11.

CMOS Quad 8-Bit D/A Converters



Notes:

1. All input signal rise and fall times measured from 10% to 90% of +5V $t_r = t_f = 20ns$ over V_{DD} range.
2. Timing measurement reference level is,
$$\frac{V_{INH} + V_{INL}}{2}$$
3. If $\overline{LDAC}$ (AD7225 only) is activated prior to the rising edge of $\overline{WR}$, then it must stay low for t_{LD} (or longer) after $\overline{WR}$ goes high.

Figure 6. Write Cycle Timing Diagram

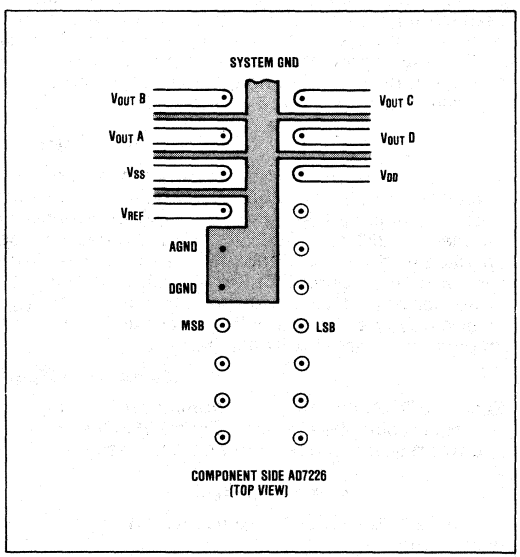


Figure 7. Suggested AD7226 PCB Layout for Minimizing Crosstalk

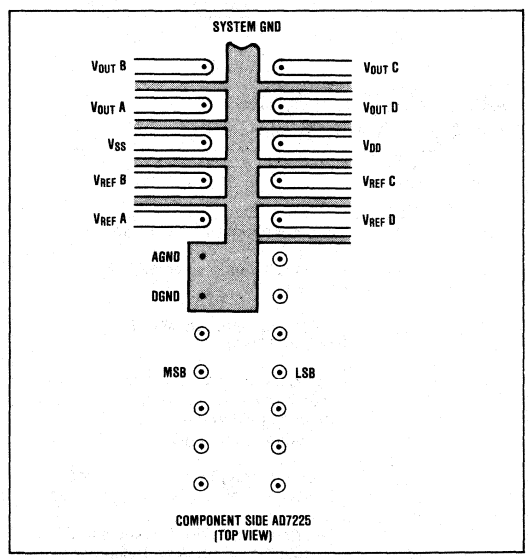


Figure 8. Suggested AD7225 PCB Layout for Minimizing Crosstalk

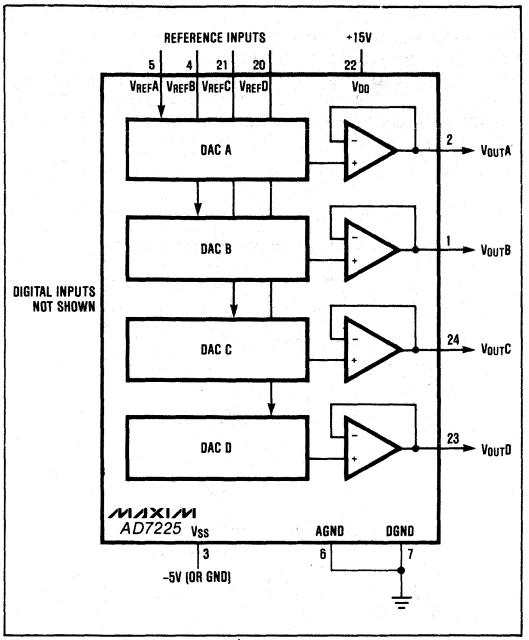


Figure 9. AD7225 Unipolar Output Circuit

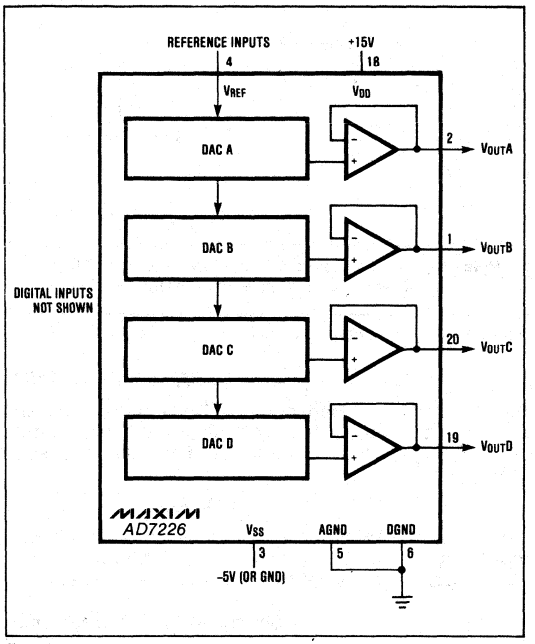


Figure 10. AD7226 Unipolar Output Circuit

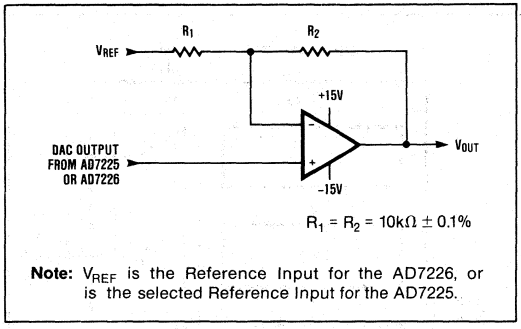
Table 3. Unipolar Code Table

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Table 4. Bipolar Code Table

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	0V
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$



Note: V_{REF} is the Reference Input for the AD7226, or is the selected Reference Input for the AD7225.

Figure 11. Bipolar Output Circuit

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "zero" input code. This is shown in Figure 12. The output voltage at $V_{OUT}A$ is:

$$V_{OUT}A = V_{BIAS} + D_A V_{IN},$$

where D_A is a fractional representation of the digital input word. Since AGND is common to all four DAC's, all outputs will be offset by V_{BIAS} in the same manner.

Using an AC Reference

In applications where V_{REF} has AC signal components, the AD7225 and AD7226 have multiplying capability within the limits of the V_{REF} input range specifications. Figure 13 shows a technique for applying a sine wave signal to the reference input where the AC signal is biased up before being applied to V_{REF}. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

Generating V_{SS}

The performance of the AD7225/7226 is specified for both dual and single supply (V_{SS} = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V V_{SS} supply can be generated using an ICL7660 in one of the circuits of figure 14.

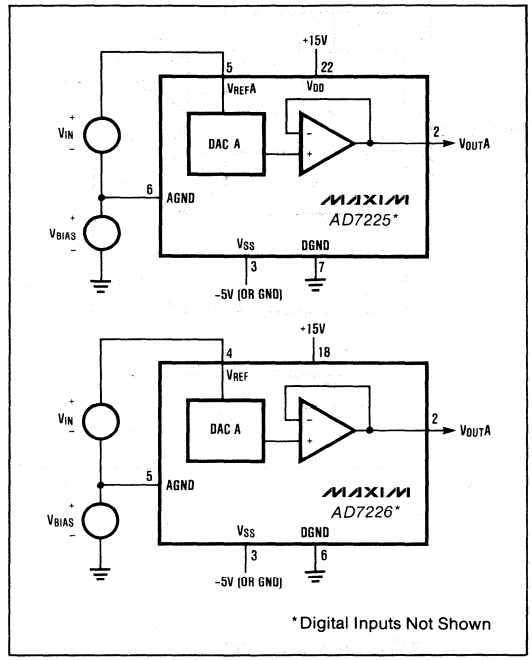


Figure 12. AGND Bias Circuits

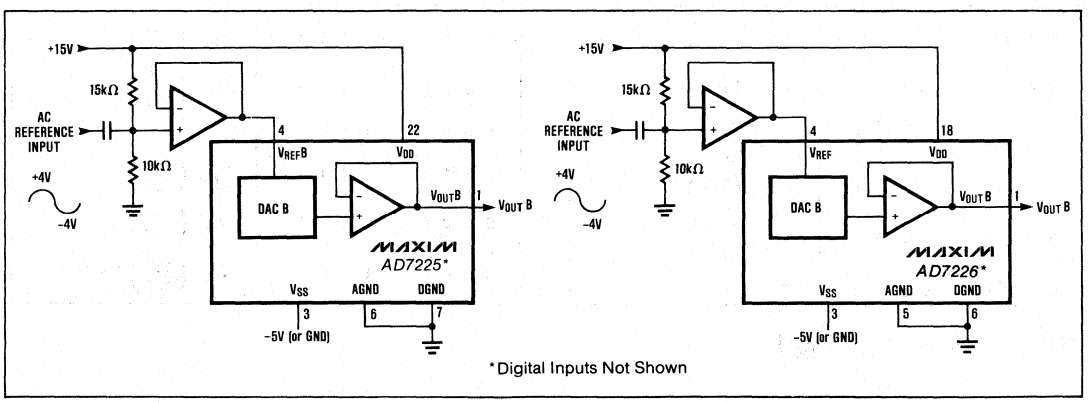


Figure 13. AC Reference Input Circuit

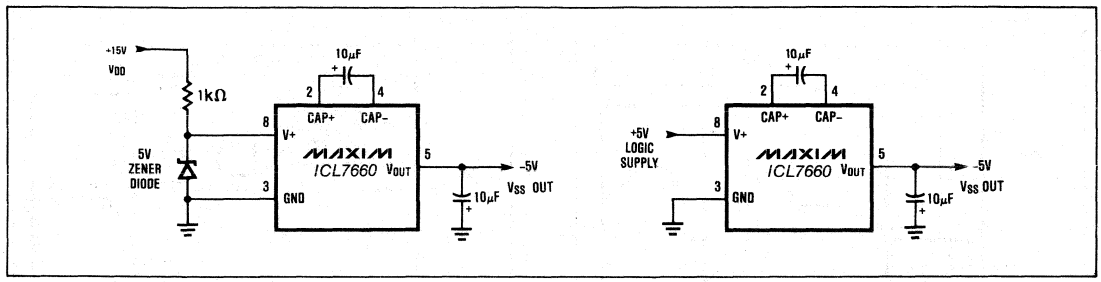


Figure 14. Generating -5V for V_{SS}

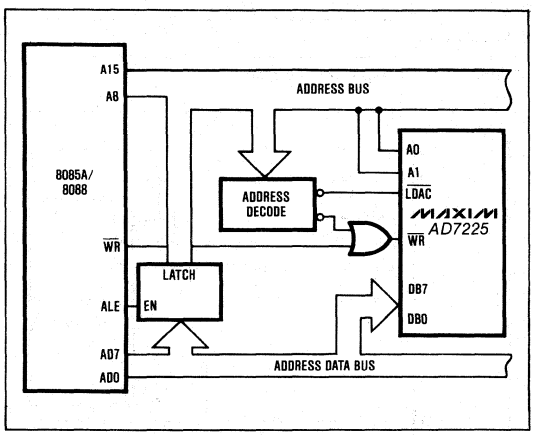


Figure 15. AD7225 to 8085A/8088 Interface, Double-Buffered Mode

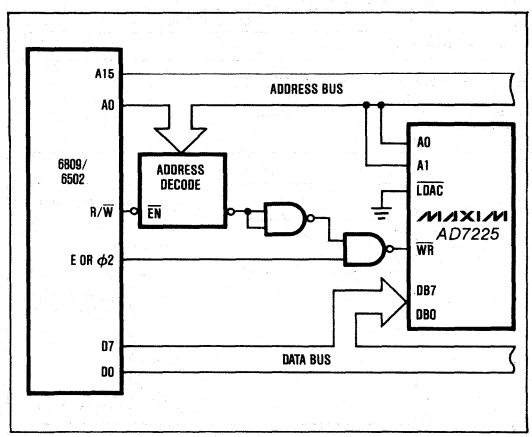


Figure 16. AD7225 to 6089/6502 Interface, Single-Buffered Mode

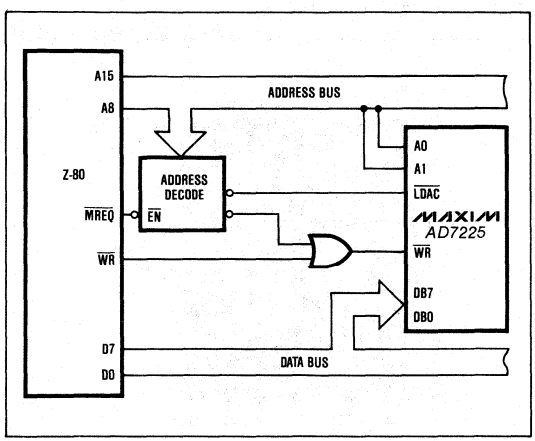


Figure 17. AD7225 to Z-80 Interface Double-Buffered Mode

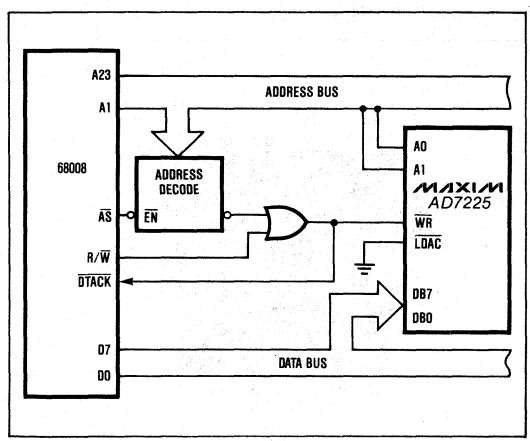


Figure 18. AD7225 to 68008 Interface, Single-Buffered Mode

CMOS Quad 8-Bit D/A Converters

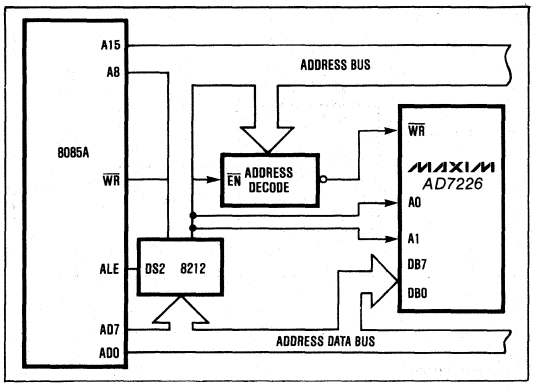


Figure 19. AD7226 to 8085A Interface

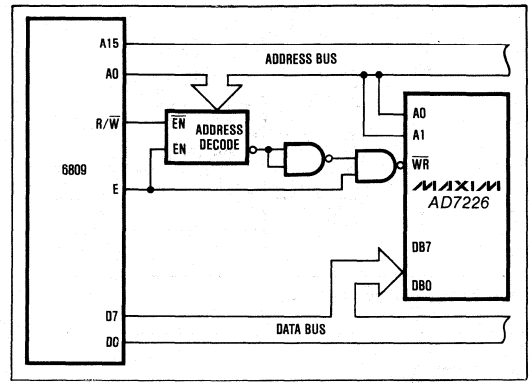


Figure 20. AD7226 to 6809 Interface

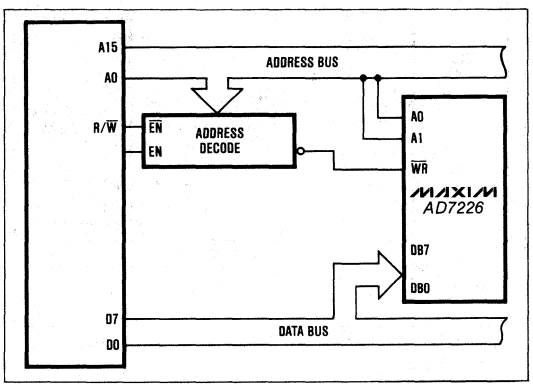


Figure 21. AD7226 to 6502 Interface

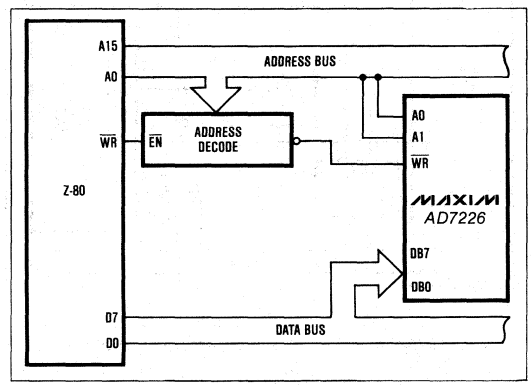
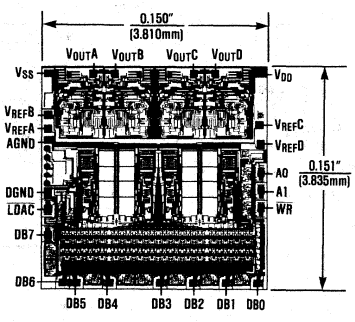
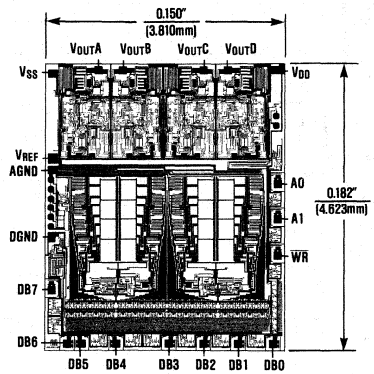


Figure 22. AD7226 to Z-80 Interface

Chip Topography



AD7225



AD7226

MAXIM

CMOS 10 and 12 Bit Multiplying D/A Converters

General Description

The AD7520 and AD7521 are low cost CMOS multiplying digital-to-analog converters (DACs) with 10 and 12 bit resolution respectively. Both DACs operate from a +5V to +15V supply and dissipate only 20mW.

Thin-film resistors provide typically 0.3% untrimmed gain error and 10ppm/°C gain temperature coefficient. All digital inputs are compatible with both CMOS and TTL logic levels.

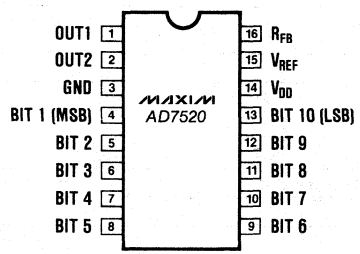
Maxim's AD7520 and AD7521 are electrically and pin compatible with Analog Devices' AD7520 and AD7521. The AD7520 is packaged in a 16-lead DIP while the AD7521 is packaged in an 18-lead DIP. Both devices are also available in small outline (SO) packages.

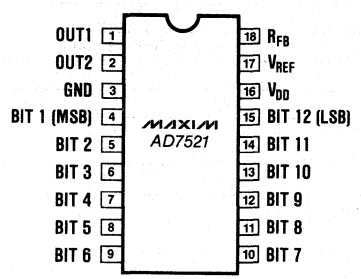
Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Pin Configuration

Top View





Features

- 10 or 12 Bit Resolution
- 8, 9, and 10 Bit End Point Linearity
- Low Power Consumption — 20mW
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

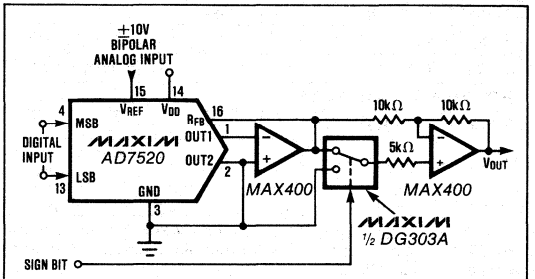
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7520JN	0°C to +70°C	Plastic DIP	0.2%
AD7520KN	0°C to +70°C	Plastic DIP	0.1%
AD7520LN	0°C to +70°C	Plastic DIP	0.05%
AD7520JCWE	0°C to +70°C	Small Outline	0.2%
AD7520KCWE	0°C to +70°C	Small Outline	0.1%
AD7520LCWE	0°C to +70°C	Small Outline	0.05%
AD7520JC/D	0°C to +70°C	Dice	0.2%
AD7520JQ	-25°C to +85°C	CERDIP**	0.2%
AD7520KQ	-25°C to +85°C	CERDIP**	0.1%
AD7520LQ	-25°C to +85°C	CERDIP**	0.05%
AD7520JD	-25°C to +85°C	Ceramic	0.2%
AD7520KD	-25°C to +85°C	Ceramic	0.1%
AD7520LD	-25°C to +85°C	Ceramic	0.05%
AD7520SQ	-55°C to +125°C	CERDIP**	0.2%
AD7520TQ	-55°C to +125°C	CERDIP**	0.1%
AD7520UQ	-55°C to +125°C	CERDIP**	0.05%
AD7520SD	-55°C to +125°C	Ceramic	0.2%
AD7520TD	-55°C to +125°C	Ceramic	0.1%
AD7520UD	-55°C to +125°C	Ceramic	0.05%

** AD7520 — 16 lead package, AD7521 — 18 lead package.*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Ordering Information continued on last page.

Typical Operating Circuit



10 Bit Plus Sign Multiplying DAC

CMOS 10 and 12 Bit Multiplying D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature
Commercial (JN/KN/LN/JC/KC/LC) ..... 0°C to +70°C
Industrial (JD/KD/LD/JQ/KQ/LQ) ..... -25°C to +85°C
Military (S/T/U) ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

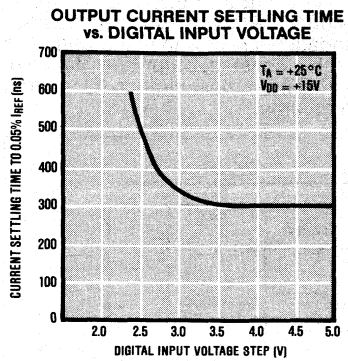
(T_A=+25°C, V_{DD} =+ 15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

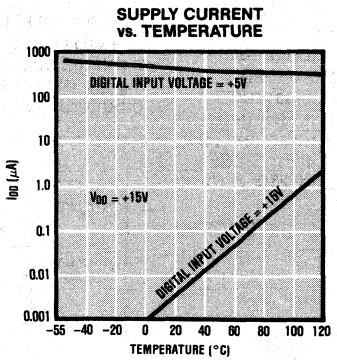
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 2)						
Resolution		AD7520 AD7521	10 12			Bits
Relative Accuracy (Note 3)		-10V ≤ V_{REF} ≤ +10V, T_A = T_{MIN} to T_{MAX} 0.2% FSR = 8 Bits J/S 0.1% FSR = 9 Bits K/T 0.05% FSR = 10 Bits L/U			±0.2 ±0.1 ±0.05	% FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V (Note 4)			2	ppm/°C
Gain Error		-10V ≤ V_{REF} ≤ +10V (Note 5)		0.3		% FSR
Gain Error Tempco		-10V ≤ V_{REF} ≤ +10V (Note 4,5)			10	ppm/°C
Output Leakage Current		OUT1 or OUT2, T_A = T_{MIN} to T_{MAX}		200		nA
Power Supply Rejection	PSRR	(Note 3)		50		ppm/ %V_{DD}
V_{REF} Input Resistance	R_{REF}	R_{REF} tempco = -150ppm/°C typ.	5	10	20	kΩ
AC ACCURACY						
Output Current Settling Time (Note 3)		To 0.05% of FSR, all digital inputs high to low and low to high.		500		ns
Feedthrough Error (Note 3,4,6)		All digital inputs low, V_{REF} = 20V_{P-P}, 100kHz sinewave.		10		mV_{P-P}
ANALOG OUTPUTS						
Output Capacitance (Note 3)	C_{OUT}	All digital inputs high, OUT1 All digital inputs high, OUT2 All digital inputs low, OUT1 All digital inputs low, OUT2		120 37 37 120		pF
Output Noise (Note 3)	e_N	Both outputs, equivalent Johnson noise resistance			10	kΩ
DIGITAL INPUTS (T_A = T_{MIN} to T_{MAX})						
Low State Threshold	V_{INL}				0.8	V
High State Threshold	V_{INH}		2.4			V
Input Current		Low to high state		±1		µA
Input Coding		Unipolar (Table 1), Bipolar (Table 2)	Binary, Offset Binary			
POWER REQUIREMENTS						
Power Supply Range	V_{DD}		+5		+15	V
Power Supply Current	I_{DD}	Digital inputs at GND Digital inputs high or low		5	 2	nA mA
Total Power Dissipation		Including V_{REF}		20		mW

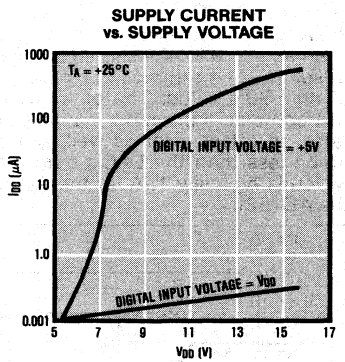
Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage if the current is limited to 30mA or less.
Note 2: Full Scale Range is 10V for unipolar mode and ±10V for bipolar mode.
Note 3: See Test Circuits.
Note 4: Guaranteed by design but not 100% tested.
Note 5: Using internal feedback resistor, R_{FB}.
Note 6: To minimize feedthrough with the ceramic package, the metal lid must be grounded. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.

CMOS 10 and 12 Bit Multiplying D/A Converters

Typical Operating Characteristics







Detailed Description

The basic AD7520/21 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. The V_{REF} input accepts a wide range of reference signals including fixed and time-varying voltage or current inputs.

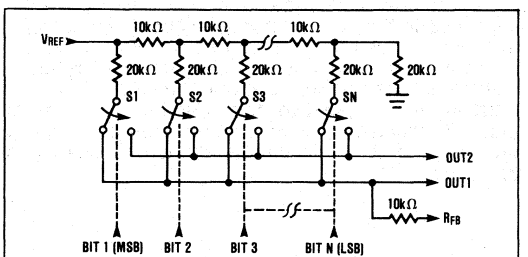


Figure 1. AD7520/AD7521 Functional Diagram

Application Information

Unipolar Operation

The most common configuration for the AD7520/21 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 is used for gain adjustment. If no adjustment is desired, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The correct compensation value depends on the type of op-amp used but typically ranges from 10 to 50pF.

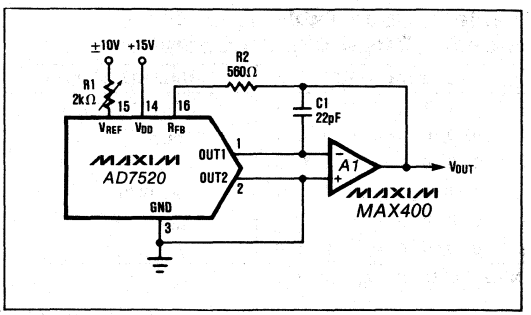


Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)

Table 1: Code Table (AD7520) — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(\frac{1}{2} + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(\frac{1}{2} - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Note: 1 LSB = 2^{-10} V_{REF} (AD7520)

CMOS 10 and 12 Bit Multiplying D/A Converters

The output op-amp's offset voltage can degrade DAC linearity by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1μA for the AD7520 and 250nA for the AD7521.

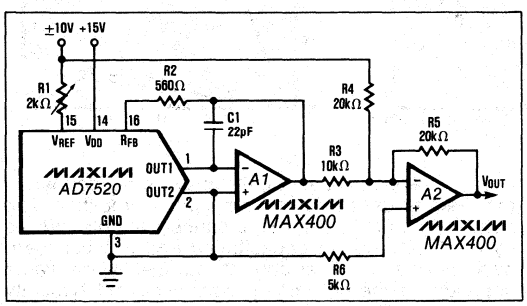


Figure 3. Bipolar Operation (4-Quadrant Multiplication)

Table 2: Code Table (AD7520) — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

Note: 1 LSB = 2^{-9} V_{REF} (AD7520)

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 3. A second amplifier and three matched resistors are required. The output vs. code table is listed in Table 2. In multiplying applications, the MSB determines polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

Voltage Mode (Single Supply)

The AD7520 is connected as a voltage output DAC in Figure 4. OUT1 is connected to the external reference and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). In most circuits this output is buffered with an op-amp.

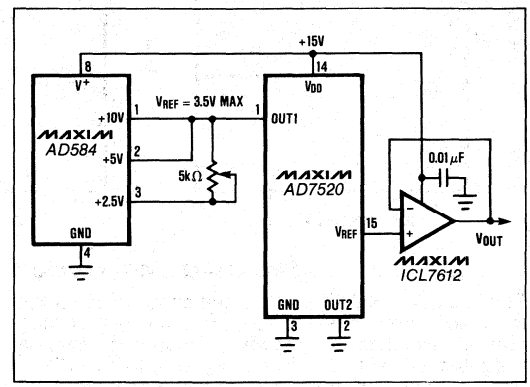


Figure 4. Single Supply Voltage Mode Operation

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must always be positive and is limited to no more than 3.5V when V_{DD} is 15V. If the reference voltage is greater than 3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

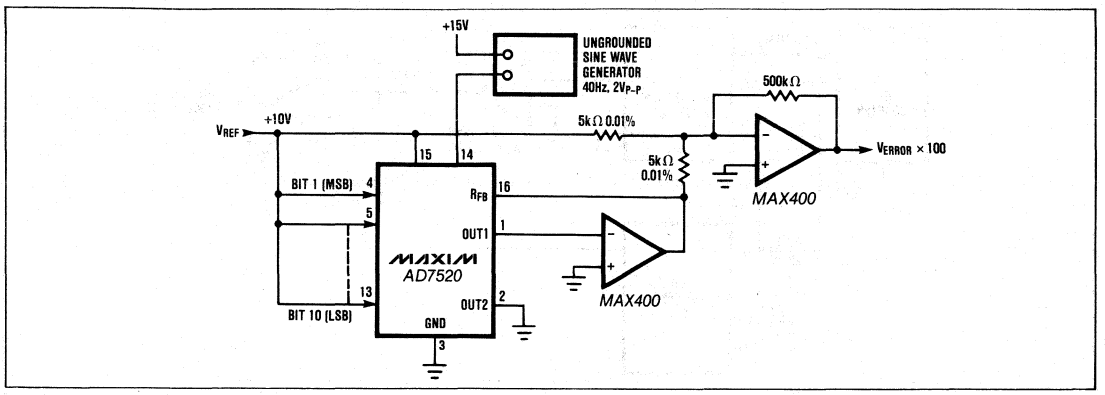


Figure 5. Power Supply Rejection

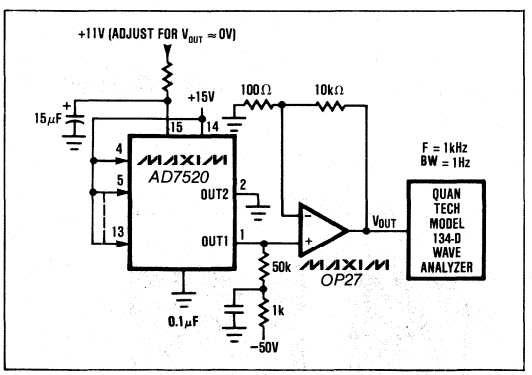


Figure 6. Noise

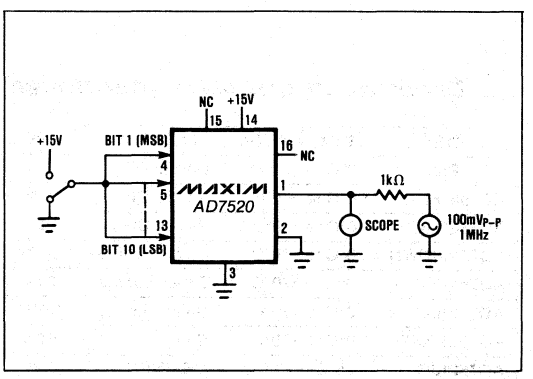


Figure 7. Output Capacitance

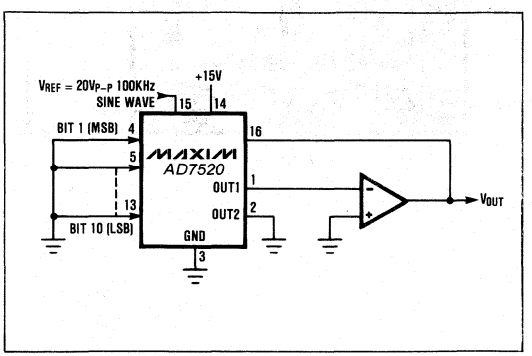


Figure 8. Feedthrough Error

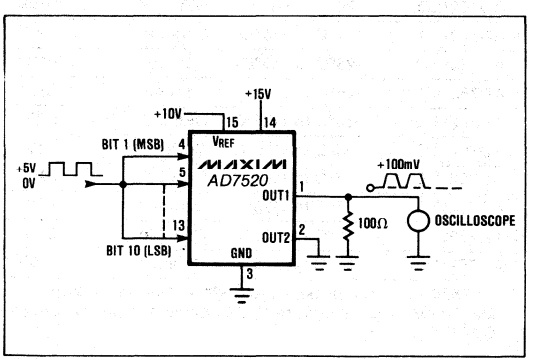


Figure 9. Output Current Settling Time

CMOS 10 and 12 Bit Multiplying D/A Converters

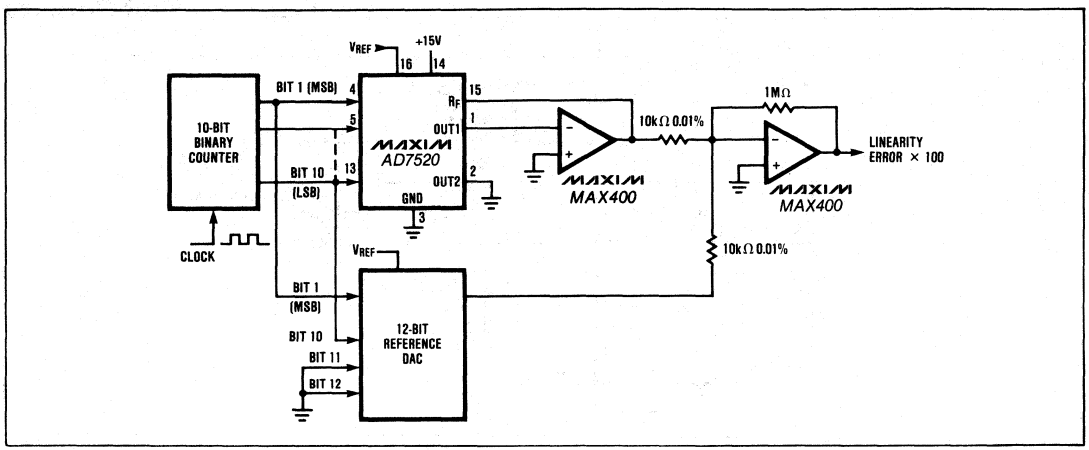


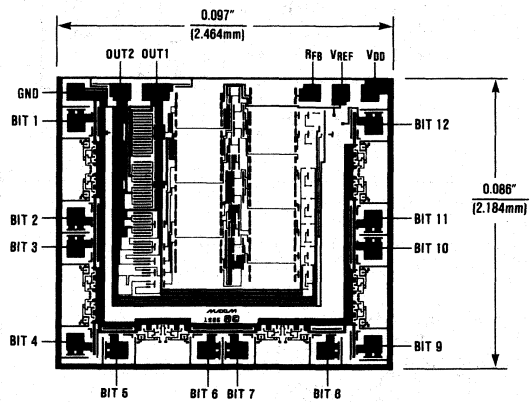
Figure 10. Relative Accuracy

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7521JN	0°C to +70°C	Plastic DIP	0.2%
AD7521KN	0°C to +70°C	Plastic DIP	0.1%
AD7521LN	0°C to +70°C	Plastic DIP	0.05%
AD7521JCWN	0°C to +70°C	Small Outline	0.2%
AD7521KCWN	0°C to +70°C	Small Outline	0.1%
AD7521LCWN	0°C to +70°C	Small Outline	0.05%
AD7521JC/D	0°C to +70°C	Dice	0.2%
AD7521JQ	-25°C to +85°C	CERDIP**	0.2%
AD7521KQ	-25°C to +85°C	CERDIP**	0.1%
AD7521LQ	-25°C to +85°C	CERDIP**	0.05%
AD7521JD	-25°C to +85°C	Ceramic	0.2%
AD7521KD	-25°C to +85°C	Ceramic	0.1%
AD7521LD	-25°C to +85°C	Ceramic	0.05%
AD7521SQ	-55°C to +125°C	CERDIP**	0.2%
AD7521TQ	-55°C to +125°C	CERDIP**	0.1%
AD7521UQ	-55°C to +125°C	CERDIP**	0.05%
AD7521SD	-55°C to +125°C	Ceramic	0.2%
AD7521TD	-55°C to +125°C	Ceramic	0.1%
AD7521UD	-55°C to +125°C	Ceramic	0.05%

** AD7520 — 16 lead package, AD7521 — 18 lead package.*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Chip Topography



CMOS 8 Bit Multiplying D/A Converter

General Description

The AD7523 is high performance multiplying 8 bit digital-to-analog converter (DAC). Low power CMOS technology and low cost make it suitable for a wide range of analog data acquisition and control applications.

Thin-film resistors assure 8 bit resolution with up to 10 bit linearity (L grade) over the full operating temperature range. In addition, all digital inputs are compatible with CMOS logic levels.

Maxim's AD7523 is electrically and pin compatible with the Analog Devices AD7523 and is available in a standard width 16-lead DIP as well as small outline package.

Features

- **8, 9 and 10 Bit Linearity**
- **±1.5% Untrimmed Gain Accuracy**
- **Guaranteed Monotonic**
- **Low Feedthrough 1/2LSB at 200kHz**
- **Low Power Consumption**
- **CMOS Compatible Logic Inputs**
- **Widely Second Sourced**

Applications

Automatic Test Equipment
Digital Calibration Systems
Battery Powered Instruments
Audio Gain Control
Digitally Controlled Filters
Programmable Power Supplies
Motion Control Systems

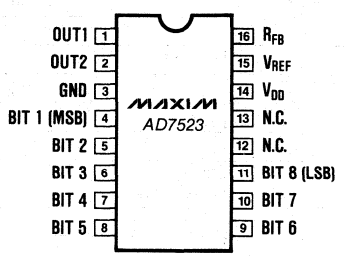
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7523JN	0°C to +70°C	Plastic DIP	½LSB
AD7523KN	0°C to +70°C	Plastic DIP	¼LSB
AD7523LN	0°C to +70°C	Plastic DIP	⅛LSB
AD7523JCWE	0°C to +70°C	Small Outline	½LSB
AD7523KCWE	0°C to +70°C	Small Outline	¼LSB
AD7523LCWE	0°C to +70°C	Small Outline	⅛LSB

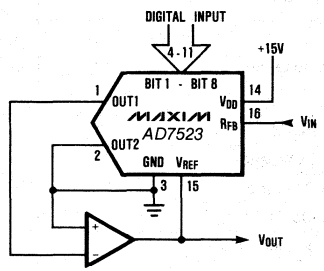
** All devices — 16 lead packages*

Pin Configuration

Top View



Typical Operating Circuit



$$V_{OUT} = \frac{256}{D}$$

D = Digital Input Code

Digitally Controlled Gain

CMOS 8 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C
Power Dissipation to +70°C
Plastic DIP 670mW
Small Outline 450mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY							
Resolution				8			Bits
Nonlinearity (Note 2)		0.2% FSR = ½LSB 0.1% FSR = ¼LSB 0.05% FSR = ⅛LSB	J K L			±½ ±¼ ±⅛	LSB
Monotonicity				Guaranteed			
Gain Error (Note 2, 3)		Digital Inputs = V_{INH}	T_A = +25°C T_{MIN} to T_{MAX}			±1.5 ±1.8	% FSR
Power Supply Rejection (Note 2)	PSRR	V_{DD} = +14V to +15V	T_A = +25°C T_{MIN} to T_{MAX}			0.02 0.03	%/%V_{DD}
Output Leakage Current		OUT1, Digital Inputs = V_{INL}	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
		OUT2, Digital Inputs = V_{INH}	T_A = 25° C T_{MIN} to T_{MAX}			±50 ±200	
V_{REF} Input Resistance	R_{REF}	T_A = +25°C		5	10	**20**	kΩ
V_{REF} Resistance Tempco		(Note 4)				-500	ppm/° C
AC PERFORMANCE (Note 4)							
Output Current Settling Time to 0.2% of FSR		R_L = 100Ω, Digital Inputs = V_{INH} to V_{INL} and V_{INL} to V_{INH}	T_A = +25°C T_{MIN} to T_{MAX}			150 200	ns
Feedthrough Error		Digital Inputs = V_{INL}, V_{REF} = 20V_{P-P}, 200 KHz	T_A = +25°C T_{MIN} to T_{MAX}			±½ ±1	LSB
Output Capacitance	C_{OUT}	Digital Inputs = V_{INH}	OUT1 OUT2			100 30	pF
		Digital Inputs = V_{INL}	OUT1 OUT2			30 100	
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+14.5			V
Logic LOW Threshold	V_{INL}					+0.5	V
Input Leakage Current		Digital inputs = 0V or +15V				±1	μA
Input Capacitance, (Note 4)						4	pF
Input Coding		Unipolar Operation (Table 1) Bipolar Operation (Table 2)		Binary Offset Binary			
POWER REQUIREMENTS							
Power Supply Range	V_{DD}	Accuracy not guaranteed over this range.		+5		**+16**	V
Power Supply Current	I_{DD}	Digital inputs = V_{INH} or V_{INL}				100	μA

Note 1: $V_{OUT1, 2}$ may exceed the Absolute Maximum voltage rating if the current is limited to 30mA or less.
Note 2: Using internal feedback resistor (R_{FB}). Full scale range (FSR) = -(V_{REF} - 1LSB) in unipolar mode.
Note 3: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±0.3% FSR.
Note 4: Guaranteed by design but not 100% tested.

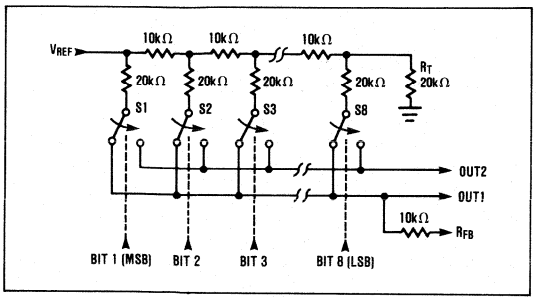
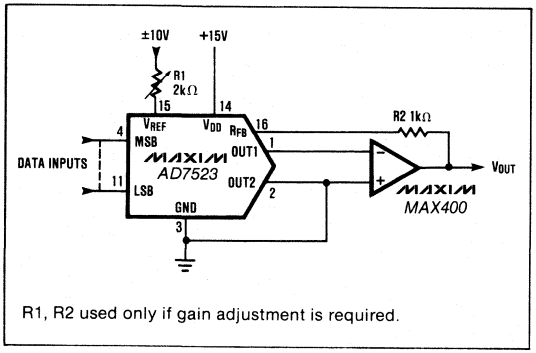
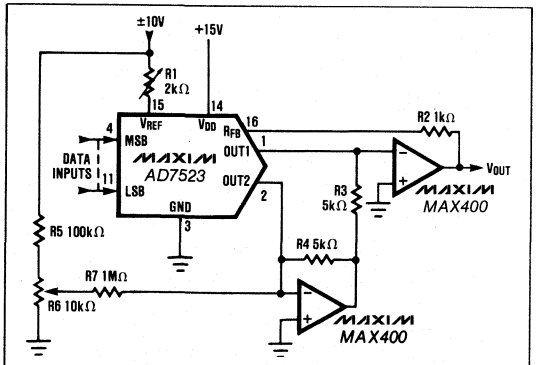


Figure 1. AD7523 Functional Diagram



R1, R2 used only if gain adjustment is required.

Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)



Notes:
1. R3/R4 match 0.1% or better.
2. R1, R2 used only if gain adjustment is required.
3. R5–R7 used to adjust V_{OUT} = 0V at input code 10000000.

Figure 3. Bipolar (4-Quadrant) Operation

Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{225}{256}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

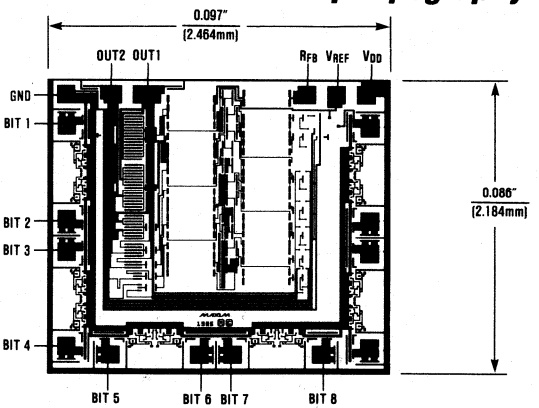
Note: $1LSB = (2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$+V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Chip Topography



CMOS 8-Bit Buffered Multiplying DACs

General Description

The AD7524 and MAX7624 are CMOS 8-bit digital-to-analog converters (DAC) which will interface directly with most microprocessors. On-chip input latches make the DAC interface similar to a RAM write cycle where CS and WR are the only control inputs required.

Linearity up to ±⅛ LSB is available (AD7524L/C/U grades) and power consumption is less than 10mW. Monotonicity is guaranteed over the full temperature range.

For the AD7524, +5V TTL and CMOS logic compatibility is guaranteed when using +5V power. Over the supply range of +5V to +15V, all logic inputs are high voltage CMOS compatible.

The MAX7624 has +5V TTL/CMOS compatible inputs for a +12V to +15V supply range.

Applications

μP Controlled Gain

Function Generators

Bus Structured Instruments

Automatic Test Equipment

Digital Control Systems

Features

- **Microprocessor Compatible**
- **On-Chip Data Latches**
- **Guaranteed Monotonic Over Temp.**
- **Low Power Consumption**
- **8, 9, and 10-Bit Linearity**
- **AD7524 TTL/CMOS Compatible at +5V**
- **MAX7624 TTL/CMOS Compatible at +12V to +15V**

Ordering Information

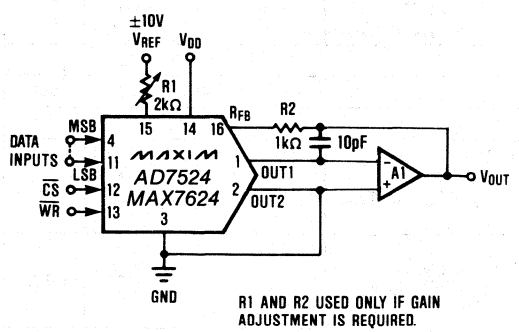
PART	TEMP. RANGE	PACKAGE*	ERROR
AD7524JN	0°C to +70°C	Plastic DIP	±½ LSB
AD7524KN	0°C to +70°C	Plastic DIP	±¼ LSB
AD7524LN	0°C to +70°C	Plastic DIP	±⅛ LSB
AD7524JCSE	0°C to +70°C	Small Outline	±½ LSB
AD7524KCSE	0°C to +70°C	Small Outline	±¼ LSB
AD7524LCSE	0°C to +70°C	Small Outline	±⅛ LSB
AD7524JC/D	0°C to +70°C	Dice	±½ LSB
AD7524AD	-25°C to +85°C	Ceramic	±½ LSB
AD7524BD	-25°C to +85°C	Ceramic	±¼ LSB
AD7524CD	-25°C to +85°C	Ceramic	±⅛ LSB

* *All devices — 16 lead packages*

** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

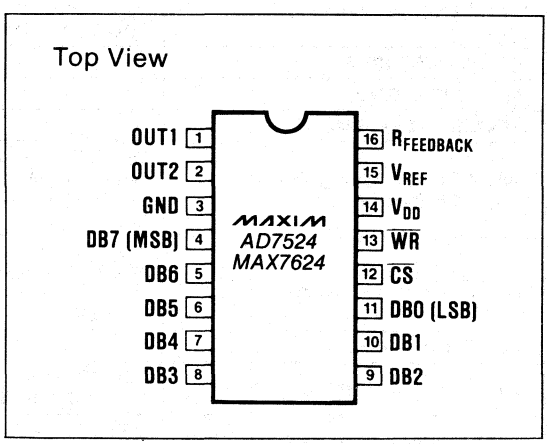
(Ordering Information continued on last page)

Typical Operating Circuit



Unipolar Binary Operation
(2-Quadrant Multiplication)

Pin Configuration



CMOS 8-Bit Buffered Multiplying DACs

ABSOLUTE MAXIMUM RATINGS—AD7524, MAX7624

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V to V_{DD} + 0.3V
OUT1, OUT2 to GND ..... -0.3V, V_{DD}
Operating Temperature Ranges
AD7524JN, KN, LN, JCSE, KCSE, LCSE
MAX7624CPE, CSE ..... 0°C to +70°C
Operating Temperature Ranges (continued)
AD7524AD, AQ, BD, BQ, CD, CQ .... -25°C to +85°C
MAX7624EPE ..... -40°C to +85°C
AD7524SD, SQ, TD, TQ, UD, UQ
MAX7624MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 450mW
Derate Above +75°C by ..... 6 mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7524, +5V Operation

(V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1/2 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 1)		T_A = 25°C T_A = T_{MIN} to T_{MAX}				±2½ ±3½	LSB
Gain Temp. Coefficient (Note 2, 3)					±2	±40	ppm/°C
Supply Rejection (Note 2)	PSR	ΔV_{DD} = ±10%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.002 0.01	0.08 0.16	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V DAC is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V DAC is 11111111	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
REFERENCE INPUT							
R_{IN} (pin 15 to GND)				5	10	20	kΩ
DYNAMIC PERFORMANCE							
Output Current Settling-Time to 1/2 LSB (Note 2)		DB0-DB7 = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUT1 Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			400 500	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V 100kHz Sinewave DB0-DB7 = $\overline{WR}$ = $\overline{CS}$ = 0V	T_A = 25°C T_A = T_{MIN} to T_{MAX}			0.25 0.5	%FSR
ANALOG OUTPUTS							
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V				120 30	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V				30 120	pF

Note 1: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 2: Guaranteed, but not tested.
Note 3: Gain error measured from 25°C to T_{MAX} or from 25°C to T_{MIN}.
Note 4: Sample tested at 25°C to ensure compliance.

ELECTRICAL CHARACTERISTICS—AD7524, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$			8 20	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 2	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	170 220 240			ns
Chip Select to Write Hold Time	t_{CH}		0			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	170 220 240			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	135 170 170			ns
Data Hold Time	t_{DH}		10			ns

ELECTRICAL CHARACTERISTICS—AD7524, +15V Operation

(V_{DD} = +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U			±1/2 ±1/4 ±1/8	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.			±1	LSB
Gain Error (Note 1)		T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1¼ ±1½	LSB
Gain Temp. Coefficient (Note 2, 3)				±1	±10	ppm/°C
Supply Rejection (Note 2)	PSR	ΔV_{DD} = ±10% T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.005	0.02 0.04	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V T_A = 25°C DAC is 00000000 T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V T_A = 25°C DAC is 11111111 T_A = T_{MIN} to T_{MAX}			±50 ±200	nA

CMOS 8-Bit Buffered Multiplying DACs

ELECTRICAL CHARACTERISTICS—AD7524, +15V Operation (Continued)

(V_{DD} = +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT						
R_{IN} (pin 15 to GND)			5	10	20	kΩ
DYNAMIC PERFORMANCE						
Output Current Settling-Time to 1/2 LSB (Note 2)		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V T_A = 25°C OUT1 Load = 100Ω, T_A = T_{MIN} to T_{MAX} C_{EXT} = 13pF;			250 350	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V 100kHz Sinewave T_A = 25°C $\overline{DB0}$-$\overline{DB7}$ = $\overline{WR}$ = T_A = T_{MIN} to T_{MAX} $\overline{CS}$ = 0V			0.25 0.5	%FSR
ANALOG OUTPUTS						
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			120 30	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			30 120	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		13.5			V
Input Low Voltage	V_{IL}				1.5	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	$\overline{DB0}$-$\overline{DB7}$ $\overline{WR}$, $\overline{CS}$			8 20	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}			2	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	100 130 150			ns
Chip Select to Write Hold Time	t_{CH}		0			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	100 130 150			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	60 80 100			ns
Data Hold Time	t_{DH}		10			ns

Note 1: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 2: Guaranteed, but not tested.
Note 3: Gain error measured from 25°C to T_{MAX} or from 25°C to T_{MIN}.
Note 4: Sample tested at 25°C to ensure compliance.

ELECTRICAL CHARACTERISTICS—MAX7624, +12V to +15V Operation

(V_{DD} = +10.8V to +15.75V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy	INL				±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.			±1	LSB
Gain Error (Note 1)					±2	LSB
Gain Temp. Coefficient (Note 2, 3)				±1	±10	ppm/°C
Supply Rejection (Note 2)	PSR	V_{DD} = +10.8V to +15.75V; T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.005	0.02 0.04	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V, DAC is 00000000; T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V, DAC is 11111111; T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT						
R_{IN} (pin 15 to GND)			5	10	20	kΩ
DYNAMIC PERFORMANCE						
Output Current Settling-Time to 1/2 LSB (Note 2)		DB0-DB7 = 0V to +5V to 0V; $\overline{WR}$ = $\overline{CS}$ = 0V; OUT1 Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			250 350	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V, 100kHz Sinewave, DB0-DB7 = $\overline{WR}$ = $\overline{CS}$ = 0V; T_A = 25°C T_A = T_{MIN} to T_{MAX}			0.25 0.5	%FSR
ANALOG OUTPUTS						
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = +5V; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			60 25	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = +5V; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			25 60	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	µA
Input Capacitance (Note 2)	C_{IN}	DB0-DB7, $\overline{WR}$, $\overline{CS}$			8	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}			2.5	mA
		Digital inputs 0V or V_{DD}; T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	µA

CMOS 8-Bit Buffered Multiplying DACs

ELECTRICAL CHARACTERISTICS—MAX7624, +12V to +15V Operation (Continued)

(V_{DD} = +10.8V to +15.75V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	160 160 210			ns
Chip Select to Write Hold Time	t_{CH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	150 170 210			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	160 160 210			ns
Data Hold Time	t_{DH}		10			ns

Detailed Description

The AD7524/MAX7624 is an 8-bit multiplying digital-to-analog converter (DAC) that consists of a thin-film R-2R resistor array with CMOS current steering switches. In applications requiring a voltage output, an output operational amplifier and reference will be needed. Figure 1 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at either OUT terminal depends on the number of switches selected, and therefore the output is an analog representation of the digital input. The two OUT terminals must be held at the same potential so a constant current is maintained in each ladder leg. This makes the V_{REF} input current independent of switch state and also ensures that the AD7524/MAX7624 maintains its excellent linearity performance.

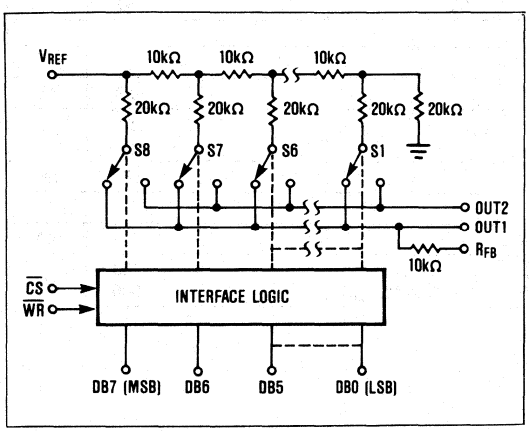


Figure 1. AD7524/MAX7624 Functional Diagram

Equivalent-Circuit Analysis

The equivalent circuit for all digital inputs LOW is shown in figure 2. In this state the reference current is switched to OUT2. The current source, $I_{LEAKAGE}$, is composed of small surface and junction leakages to the substrate which double every 10°C. The R-2R ladder termination resistor generates a constant 1/256 current which represents 1 LSB of the reference current, I_{REF}. The value of output capacitance at the OUT1 and OUT2 terminals is input code dependent and lies in the range 20pF to 30pF.

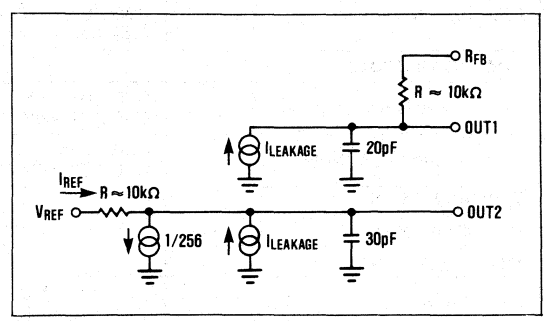


Figure 2. AD7524/MAX7624 DAC Equivalent Circuit—All Digital Inputs LOW

The AD7524's digital inputs are TTL compatible when operated with a V_{DD} of +5V (V_{IH} = 2.4V, V_{IL} = 0.8V). Internal level shifters convert from TTL to CMOS logic levels. When V_{IN} is in the region 1.5 to 3.5 volts, the input buffers operate in their linear region and the quiescent current increases as indicated by the graph in figure 3. Therefore to minimize supply current it is recommended that the digital inputs be as close to the supply rails as possible (V_{DD} and DGND).

The AD7524 may be operated with any supply voltage in the range $5V < V_{DD} < 15V$. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e. 1.5V and 13.5V.

The MAX7624's digital inputs are TTL/CMOS compatible for a +12V to +15V supply range. However, when V_{IN} is in the range of 1.5V to V_{DD} - 1.5V the input buffers operate in their linear region and the quiescent current increases (see figure 3).

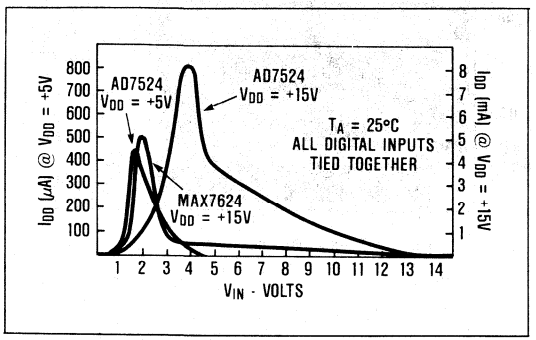


Figure 3. Typical Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V

Interface Logic Information

Mode Selection

The inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the AD7524/MAX7624. See Mode Selection Table.

Mode Selection Table

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB0-DB7) inputs
H X	X H	HOLD HOLD	Data bus (DB0-DB7) is locked out; DAC holds last data present when $\overline{CS}$ or $\overline{WR}$ assumed HIGH state

L = Low State, H = High State, X = Don't Care

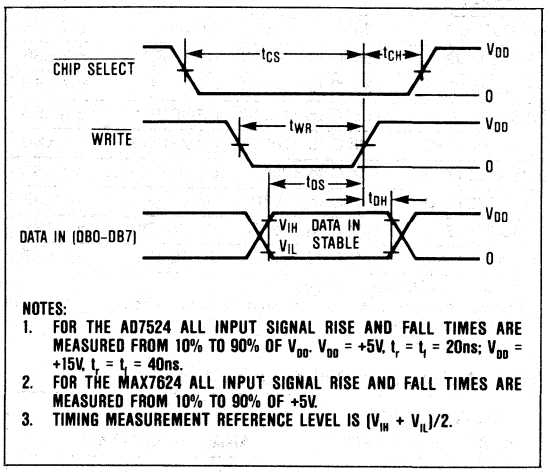
Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524/MAX7624 is in the write mode, and the AD7524/MAX7624 analog output responds to data activity at the DB0-DB7 data bus inputs. In this mode, the data latches are transparent.

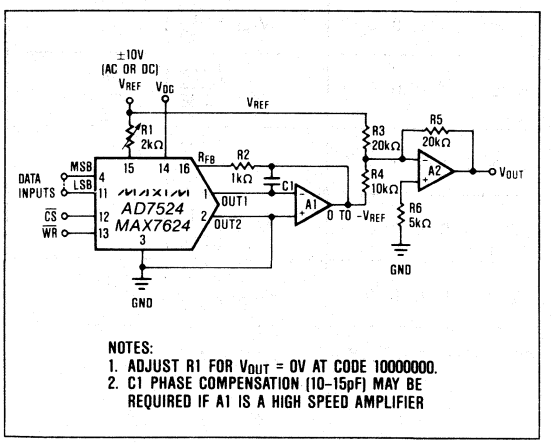
Hold Mode

The AD7524/MAX7624 retains the data that was present on DB0-DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. The analog output remains at the value corresponding to the digital code locked in the data latch.

Write Cycle Timing Diagram



NOTES:
1. FOR THE AD7524 ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. FOR THE MAX7624 ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM 10% TO 90% OF +5V.
3. TIMING MEASUREMENT REFERENCE LEVEL IS $(V_{IH} + V_{IL})/2$.



NOTES:
1. ADJUST R1 FOR V_{OUT} = 0V AT CODE 10000000.
2. C1 PHASE COMPENSATION (10-15pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER

Figure 4. Bipolar (4-Quadrant) Operation

CMOS 8-Bit Buffered Multiplying DACs

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7524AQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7524BQ	-25°C to +85°C	CERDIP**	±¼ LSB
AD7524CQ	-25°C to +85°C	CERDIP**	±⅛ LSB
AD7524SD	-55°C to +125°C	Ceramic	±½ LSB
AD7524TD	-55°C to +125°C	Ceramic	±¼ LSB
AD7524UD	-55°C to +125°C	Ceramic	±⅛ LSB
AD7524SQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7524TQ	-55°C to +125°C	CERDIP**	±¼ LSB
AD7524UQ	-55°C to +125°C	CERDIP**	±⅛ LSB
MAX7624CPE	0°C to +70°C	Plastic DIP	±½ LSB
MAX7624CSE	0°C to +70°C	Small Outline	±½ LSB
MAX7624C/D	0°C to +70°C	Dice	±½ LSB
MAX7624EPE	-40°C to +85°C	Plastic DIP	±½ LSB
MAX7624MJE	-55°C to +125°C	CERDIP	±½ LSB

* *All devices—16 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Chip Topography

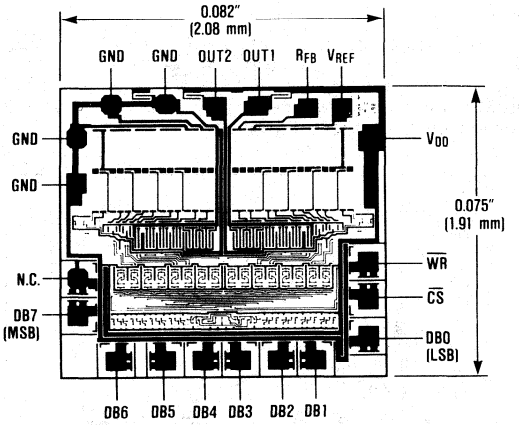


Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{127}{126}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

CMOS Dual 8-Bit Buffered Multiplying DACs

General Description

The AD7528/AD7628 contains two 8-bit multiplying digital-to-analog converters (DACs). Separate on-chip latches hold the input data for each DAC to allow easy interface to microprocessors. The data load operation is similar to a static RAM write cycle. Data is loaded using only CS, WR, and DAC Select (DAC A/DAC B) inputs.

Each DAC has a separate reference input and internal feedback resistor which allow fully independent operation while maintaining excellent DAC-to-DAC matching.

The AD7528 operates from a single +5V to +15V power supply whereas the AD7628 operates from +12V to +15V. The AD7528 has TTL compatible inputs at +5V supply only and the AD7628 has TTL compatible inputs from +12V to +15V supplies.

The AD7528/AD7628 is supplied in 20-lead narrow DIP and Small Outline Packages.

Applications

Programmable Attenuators
Digitally Controlled Filters
X-Y Graphics
Motion Control Systems
Digital-to-Synchro Conversion
Disk Drives

Features

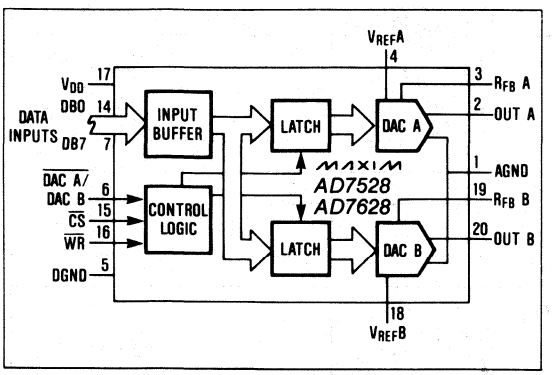
- Data Latches For Both DACs
- AD7528—+5V to +15V Single Supply Operation
- AD7628—+12V to +15V Single Supply Operation With TTL/CMOS Compatible Inputs
- ±½ LSB Linearity
- Microprocessor Compatible
- Four-Quadrant Multiplication
- DACs Matched to 1%

Ordering Information

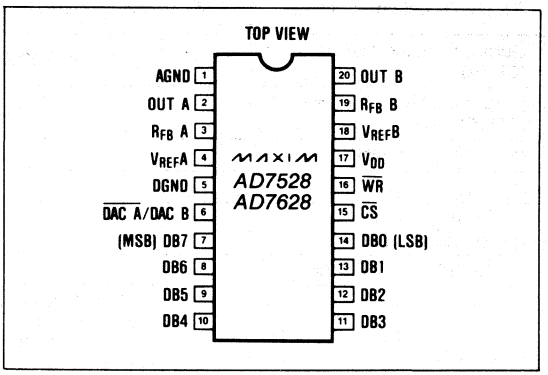
PART	TEMP. RANGE	PACKAGE*	ERROR
AD7528JN	0°C to +70°C	Plastic DIP	±1 LSB
AD7528KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7528LN	0°C to +70°C	Plastic DIP	±½ LSB
AD7528JCWP	0°C to +70°C	Wide SO	±1 LSB
AD7528KCWP	0°C to +70°C	Wide SO	±½ LSB
AD7528LCWP	0°C to +70°C	Wide SO	±½ LSB
AD7528JC/D	0°C to +70°C	Dice	±1 LSB
AD7528AQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7528BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7528CQ	-25°C to +85°C	CERDIP**	±½ LSB

* *All devices — 20 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*
Ordering Information continued on last page.

Functional Diagram



Pin Configuration



CMOS Dual 8-Bit Buffered Multiplying DACs

ABSOLUTE MAXIMUM RATINGS—AD7528, AD7628

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
Pin 2, Pin 20 to AGND ..... -0.3V, V_{DD}
$V_{REF}A$, $V_{REF}B$ to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V

Operating Temperature Ranges
AD7528JN, KN, LN, JCWP,
KCWP, LCWP; AD7628KN, KCWP ..... 0°C to +70°C
AD7528AQ, BQ, CQ; AD7628BQ ..... -25°C to +85°C
AD7528SD, SQ, TD, TQ,
UD, UQ; AD7628TQ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 450mW
Derate Above +75°C by ..... 6 mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation

(V_{DD} = +5V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		J,A,S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±6	LSB
		K,B,T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±4	
		L,C,U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±3	
Gain Temp. Coefficient (Note 2, 3)					±2	±70	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.02 0.04	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
REFERENCE INPUT							
R_{IN} ($V_{REF}A$, $V_{REF}B$)				8	10	15	kΩ
$V_{REF}A$, $V_{REF}B$ Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			350 400	ns

ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
Propagation Delay (from digital input to 90% of final analog output current)		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			220 270	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111		60		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		30		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 4)	C_{IN}	$\overline{DB0}$-$\overline{DB7}$ $\overline{WR}$, $\overline{CS}$, DAC A/DAC B			10 15	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 1	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	200 230			ns
Chip Select to Write Hold Time	t_{CH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	20 30			ns

Note 1: Specifications apply to both DACs in AD7528.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

CMOS Dual 8-Bit Buffered Multiplying DACs

ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram) (Continued)						
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	200 230			ns
DAC Select to Write Hold Time	t_{AH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	20 30			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	180 200			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	110 130			ns
Data Hold Time	t_{DH}		0			ns

ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation

(V_{DD} = +15V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U			±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.			±1	LSB
Gain Error (Note 2)		J,A,S: T_A = 25°C			±4	LSB
		J,A,S: T_A = T_{MIN} to T_{MAX}			±5	
		K,B,T: T_A = 25°C			±2	
		K,B,T: T_A = T_{MIN} to T_{MAX}			±3	
		L,C,U: T_A = 25°C			±1	
		L,C,U: T_A = T_{MIN} to T_{MAX}			±1	
Gain Temp. Coefficient (Note 2, 3)				±2	±35	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%: T_A = 25°C		0.001	0.01	%FSR/%
		ΔV_{DD} = ±5%: T_A = T_{MIN} to T_{MAX}		0.001	0.02	
Output Leakage Current (OUTA)		DAC A is 00000000: T_A = 25°C			±50	nA
		DAC A is 00000000: T_A = T_{MIN} to T_{MAX}			±200	
Output Leakage Current (OUTB)		DAC B is 00000000: T_A = 25°C			±50	nA
		DAC B is 00000000: T_A = T_{MIN} to T_{MAX}			±200	
REFERENCE INPUT						
R_{IN} (V_{REF}A, V_{REF}B)			8	10	15	kΩ
V_{REF}A, V_{REF}B Input Resistance Match					±1	%
DYNAMIC PERFORMANCE (Note 4)						
Output Current Settling-Time to 1/2 LSB		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C			180	ns
		T_A = T_{MIN} to T_{MAX}			200	

ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation (Continued)

(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
Propagation Delay (from digital input to 90% of final analog output current)		$\overline{DB0\text{-}DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			80 100	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111		125		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		60		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		13.5			V
Input Low Voltage	V_{IL}				1.5	V
Input Current	I_{IN}	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 4)	C_{IN}	$\overline{DB0\text{-}DB7}$ $\overline{WR}$, $\overline{CS}$, DAC A/DAC B			10 15	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 1	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
Chip Select to Write Hold Time	t_{CH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	10 15			ns

Note 1: Specifications apply to both DACs in AD7528.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

CMOS Dual 8-Bit Buffered Multiplying DACs

ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation (Continued)

(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram) (Continued)						
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
DAC Select to Write Hold Time	t_{AH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	10 15			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	30 40			ns
Data Hold Time	t_{DH}		0			ns

ELECTRICAL CHARACTERISTICS—AD7628, +12V to +15V Operation

(V_{DD} = +10.8V to +15.75V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL					±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		T_A = 25°C T_A = T_{MIN} to T_{MAX}				±2 ±3	LSB
Gain Temp. Coefficient (Note 2, 3)					±2	±35	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.01 0.02	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT							
R_{IN} (V_{REF}A, V_{REF}B)				8	10	15	kΩ
V_{REF}A, V_{REF}B Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		DB0-DB7 = 0V to +5V to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			350 400	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111			125		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V	T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB

Note 1: Specifications apply to both DACs in AD7628.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

ELECTRICAL CHARACTERISTICS—AD7628, +12V to +15V Operation (Continued)

(V_{DD} = +10.8V to +15.75V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V, 100kHz Sinewave, V_{REF}A = 0V; T_A = 25°C			-70	dB
		T_A = T_{MIN} to T_{MAX}			-65	
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave, V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave, V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		60		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000			25	pF
		DAC latches loaded with 11111111			60	pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000			25	pF
		DAC latches loaded with 11111111			60	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C			±1	μA
		T_A = T_{MIN} to T_{MAX}			±10	
Input Capacitance (Note 4)	C_{IN}	DB0-DB7, $\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A/DAC\ B}$			10	pF
					15	
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}; T_A = 25°C			2	mA
		T_A = T_{MIN} to T_{MAX} K			2	
		T_A = T_{MIN} to T_{MAX} B,T			2.5	
		Digital inputs 0V or V_{DD}; T_A = 25°C			100	μA
		T_A = T_{MIN} to T_{MAX}			500	
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C	160			ns
		T_A = T_{MIN} to T_{MAX} K,B	160			
		T_A = T_{MIN} to T_{MAX} T	210			
Chip Select to Write Hold Time	t_{CH}		10			ns
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C	160			ns
		T_A = T_{MIN} to T_{MAX} K,B	160			
		T_A = T_{MIN} to T_{MAX} T	210			
DAC Select to Write Hold Time	t_{AH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C	150			ns
		T_A = T_{MIN} to T_{MAX} K,B	170			
		T_A = T_{MIN} to T_{MAX} T	210			
Data Setup Time	t_{DS}	T_A = 25°C	160			ns
		T_A = T_{MIN} to T_{MAX} K,B	160			
		T_A = T_{MIN} to T_{MAX} T	210			
Data Hold Time	t_{DH}		10			ns

CMOS Dual 8-Bit Buffered Multiplying DACs

Interface Logic Information

DAC Selection

Both DAC latches share a common 8-Bit input port. The control input DAC A/DAC B selects which DAC will accept data from the input port.

Mode Selection

The inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table.

Mode Selection Table

$\overline{DAC\ A}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low state, H = High state, X = Don't care

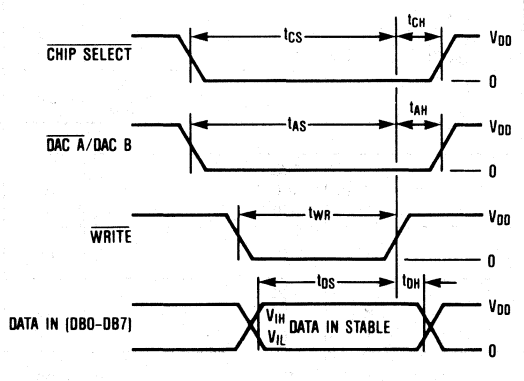
Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both low, the selected DAC is in the write mode. The input latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0–DB7.

Hold Mode

The selected DAC latch retains the data that was present on DB0–DB7 just prior to CS or WR assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Write Cycle Timing Diagram



Note 1: For the AD7528, all input signal rise and fall times are measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.

Note 2: For the AD7628, all input signal rise and fall times are measured from 10% to 90% of +5V. $t_r = t_f$ = 20ns; V_{DD} = +10.8V to +15.75V.

Note 3: Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Detailed Description

The AD7528/AD7628 contains two identical 8-Bit multiplying digital-to-analog converters (DAC). Each DAC circuit consists of a thin-film R-2R resistor array with CMOS current steering switches. Figure 1 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at the OUT terminal depends on the number of switches selected, and therefore the output is an analog representation of the digital input. The DAC OUT and analog ground terminals must be maintained at the same potential for proper operation.

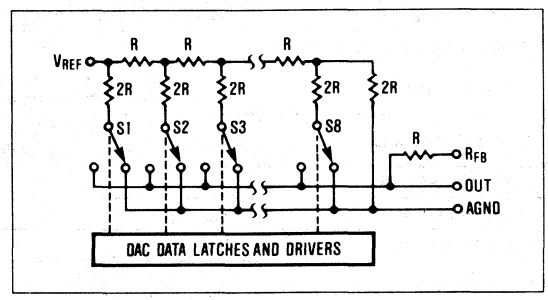


Figure 1. Simplified DAC Schematic

Equivalent-Circuit Analysis

The DAC equivalent-circuit, typical of both DACs, is shown in figure 2. Each DAC shares the analog ground pin 1. When all the digital inputs are high, 255/256 of the reference current flows to OUT A. A small junction leakage current ($I_{LEAKAGE}$), which doubles every 10°C, also flows to the output. The R-2R ladder termination resistor generates a constant 1/256 current which represents 1 LSB of the reference current, I_{REF}. C_{OUT} is the parallel combination of the capacitance associated with the individual NMOS current steering switches. The value of output capacitance is input code dependent and lies in the range 20pF to 30pF. The equivalent output resistance, R_O, also varies with input code in the range 0.8R to 3R, where R is the nominal ladder resistance.

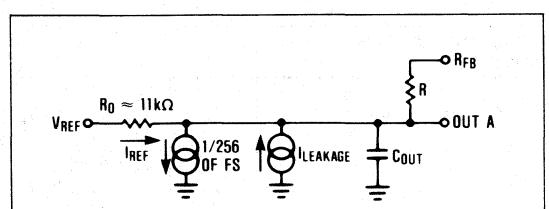


Figure 2. DAC Equivalent Circuit. All Digital Inputs High

CMOS Dual 8-Bit Buffered Multiplying DACs

Circuit Information—Digital Section

The AD7528's digital inputs are TTL compatible when operated with a V_{DD} of +5V (V_{IH} = 2.4V, V_{IL} = 0.8V). Internal level shifters convert from TTL to CMOS logic levels. When V_{IN} is in the region of 1.0 to 3.5 volts, the input buffers operate in their linear region and the quiescent current increases as indicated by the graph in figure 3. Therefore to minimize supply current it is recommended that the digital inputs be as close to the supply rails as possible (V_{DD} and DGND).

The AD7528 may be operated with any supply voltage in the range 5V < V_{DD} < 15V. With V_{DD} = +15V, the input logic levels are CMOS compatible only, i.e. 1.5V and 13.5V.

The AD7628's digital inputs are TTL and CMOS compatible with any supply voltage in the range of +12V to +15V.

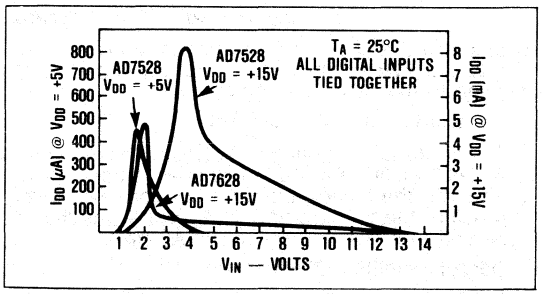
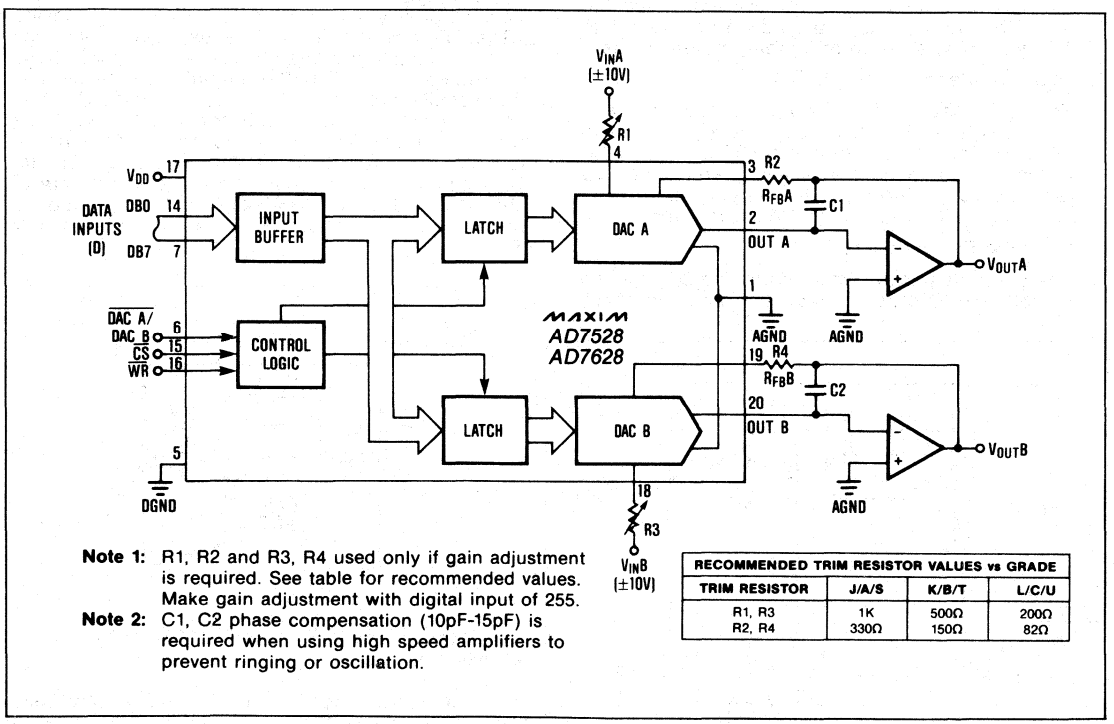


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V



Note 1: R1, R2 and R3, R4 used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.

Note 2: C1, C2 phase compensation (10pF-15pF) is required when using high speed amplifiers to prevent ringing or oscillation.

RECOMMENDED TRIM RESISTOR VALUES vs GRADE			
TRIM RESISTOR	J/A/S	K/B/T	L/C/U
R1, R3	1K	500Ω	200Ω
R2, R4	330Ω	150Ω	82Ω

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication)

CMOS Dual 8-Bit Buffered Multiplying DACs

Applications Information

To ensure system performance consistent with the AD7528/AD7628 specifications, careful attention must be given to the following points:

1. General Ground Management:

   AC or transient voltages between the AD7528/AD7628 AGND and DGND can cause noise injection into the analog output. Therefore, whenever possible, the analog and digital ground pins should be tied together at the AD7528/AD7628.

2. Output Amplifier Offset:

   CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The result is a code-dependent differential nonlinearity term at the amplifier output which depends on the amplifier's offset voltage, V_{OS}. The offset dependent nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier offset voltage should be no more than 1/10 LSB over the operating temperature range.

3. High Frequency Considerations:

   The combination of DAC output capacitance and the amplifier's feedback resistance adds a pole to the open-loop response which can cause ringing or oscillation in severe cases. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

4. Dynamic Performance:

   The dynamic performance of the two DACs in the AD7528/AD7628 depends on the gain and phase characteristics of the output amplifiers, together with the stray capacitance contributed by the PC layout, and the power supply decoupling components. A 0.1μF decoupling capacitor is recommended between V_{DD} and DGND.

5. Circuit Layout Suggestions:

   Analog and digital ground traces should be routed between the package pins to reduce coupling between the digital inputs and the analog output. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, and 4-5 to minimize reference feedthrough to the output in multiplying applications.

Single Supply Operation

The AD7528/AD7628 R-2R ladder termination resistors are internally connected to AGND. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between V_{DD} and DGND. Figure 5 shows a circuit which provides dual +5V to +8V analog outputs by biasing AGND 5V above DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the stable matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1, and R1 is adjusted until $V_{REF}A$ and $V_{REF}B$ inputs are at +2V. DAC codes from 00000000 to 11111111 adjust the analog output voltages from +5V to +8V in 11.7mV steps.

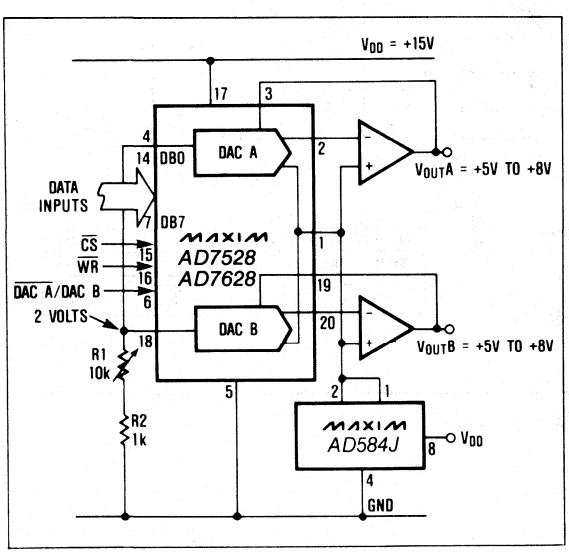


Figure 5. AD7528/AD7628 Single Supply Operation

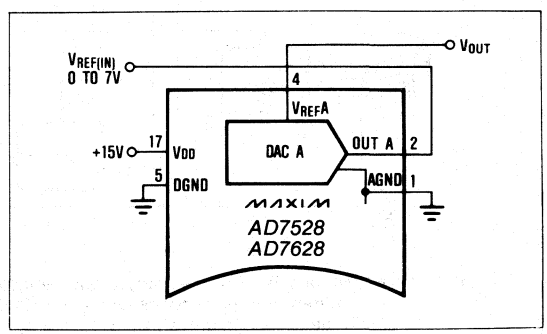


Figure 6. AD7528/AD7628 in Single Supply, Voltage Switching Mode

Figure 6 shows one DAC of the AD7528/AD7628 connected in the voltage switching mode which uses a positive reference voltage. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to maintain linearity, V_{IN} must be limited to approximately +7V (V_{DD} = +15V), and the output must be buffered or loaded with a high impedance. In the voltage switching mode, the output resistance is independent of the digital input code and is typically 10kΩ.

CMOS Dual 8-Bit Buffered Multiplying DACs

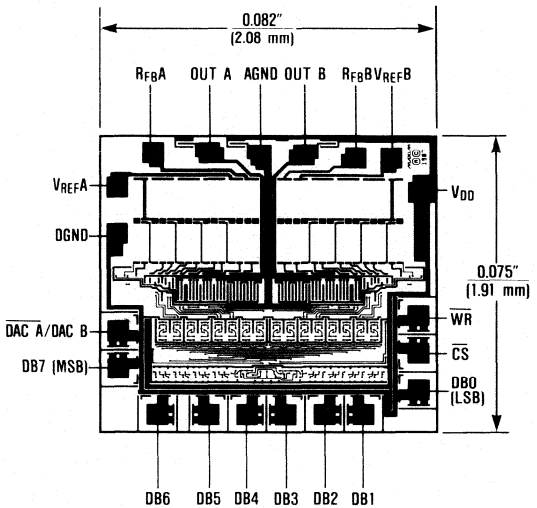
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7528SD	-55°C to +125°C	Ceramic	±1 LSB
AD7528TD	-55°C to +125°C	Ceramic	±½ LSB
AD7528UD	-55°C to +125°C	Ceramic	±½ LSB
AD7528SQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7528TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7528UQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7628KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7628KCWP	0°C to +70°C	Wide SO	±½ LSB
AD7628KC/D	0°C to +70°C	Dice	±½ LSB
AD7628BQ	-25°C to +85°C	CERDIP	±½ LSB
AD7628TQ	-55°C to +125°C	CERDIP	±½ LSB

* *All devices — 20 lead packages*

** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Chip Topography



2

MAXIM

CMOS 10 and 12 Bit Multiplying D/A Converters

General Description

The AD7530 and AD7531 are low cost CMOS multiplying digital-to-analog converters (DAC) with 10 and 12 bit resolution respectively. Both DACs operate from a single +5V to +15V supply and dissipate only 20mW.

Thin-film resistors provide typically 0.3% untrimmed gain error and 10ppm/°C maximum gain tempco. All digital inputs are compatible with both CMOS and TTL logic levels.

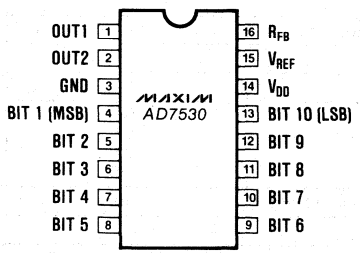
Maxim's AD7530 and AD7531 are electrically and pin compatible with Analog Devices' AD7530 and AD7531. The AD7530 is packaged in a 16-lead DIP and the AD7531 is packaged in an 18-lead DIP. Both parts are available in Small Outline packages as well.

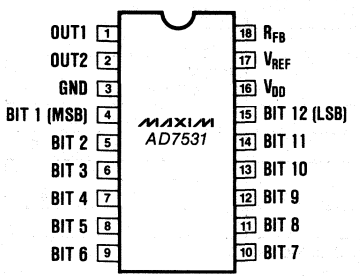
Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Pin Configurations

Top View





Features

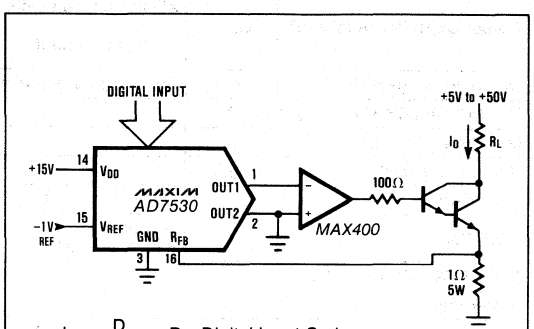
- 10 or 12 Bit Resolution
- 8, 9, and 10 Bit End Point Linearity
- Low Power Consumption - 20mW
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7530JN	0°C to +70°C	Plastic DIP	0.2%
AD7530KN	0°C to +70°C	Plastic DIP	0.1%
AD7530LN	0°C to +70°C	Plastic DIP	0.05%
AD7530JCWE	0°C to +70°C	Small Outline	0.2%
AD7530KCWE	0°C to +70°C	Small Outline	0.1%
AD7530LCWE	0°C to +70°C	Small Outline	0.05%
AD7530JC/D	0°C to +70°C	Dice	0.2%
AD7530JD	-25°C to +85°C	Ceramic	0.2%
AD7530KD	-25°C to +85°C	Ceramic	0.1%
AD7530LD	-25°C to +85°C	Ceramic	0.05%
AD7530JQ	-25°C to +85°C	CERDIP**	0.2%
AD7530KQ	-25°C to +85°C	CERDIP**	0.1%
AD7530LQ	-25°C to +85°C	CERDIP**	0.05%

** AD7530 — 16 lead package, AD7531 — 18 lead package*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*
Ordering information continued on last page.

Typical Operating Circuit



$I_O = \frac{D}{1024}$. D = Digital Input Code.

Digital Current Controller

CMOS 10 and 12 Bit Multiplying D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature
Commercial (JN/KN/LN/JC/KC/LC) ..... 0°C to +70°C
Industrial (JD/KD/LD/JQ/KQ/LQ) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 2)						
Resolution		AD7530 AD7531	10 12			Bits
Relative Accuracy		-10V ≤ V_{REF} ≤ +10V, T_A = T_{MIN} to T_{MAX} — 0.2% FSR = 8 Bits J; 0.1% FSR = 9 Bits K; 0.05% FSR = 10 Bits L			±0.2 ±0.1 ±0.05	% FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V, (Note 3)			2	ppm/°C
Gain Error		-10V ≤ V_{REF} ≤ +10V		0.3		% FSR
Gain Error Tempco		-10V ≤ V_{REF} ≤ +10V, (Note 3)			10	ppm/°C
Output Leakage Current		OUT1 or OUT2, T_A = T_{MIN} to T_{MAX}		300		nA
Power Supply Rejection	PSRR			50		ppm/%
V_{REF} Input Resistance	R_{REF}			10		kΩ
Reference Input Range		±10V typical input		±1		mA
AC ACCURACY						
Output Current Settling Time		To 0.05% of FSR, all digital inputs high to low and low to high.		500		ns
Feedthrough Error (Note 3,4)		All digital inputs low, V_{REF} = $20V_{P-P}$, 50kHz sine			10	mV_{P-P}
ANALOG OUTPUTS						
Output Current Range		Both Outputs		±1		mA
Output Capacitance (Note 3)	C_{OUT}	All digital inputs high, OUT1 All digital inputs high, OUT2 All digital inputs low, OUT1 All digital inputs low, OUT2		120 37 37 120		pF
Output Noise (Note 3)	e_N	Both outputs, equivalent Johnson noise resistance		10		kΩ
DIGITAL INPUTS (T_A = T_{MIN} to T_{MAX})						
Low State Threshold	V_{INL}				0.8	V
High State Threshold	V_{INH}		2.4			V
Input Current		Low to high state		1		μA
Input Coding		Unipolar (Table 1) Bipolar (Table 2)	Binary Offset Binary			
POWER REQUIREMENTS						
Power Supply Range	V_{DD}		+5		+15	V
Power Supply Current	I_{DD}	Digital inputs at GND Digital inputs high or low		5	 2	nA mA
Total Power Dissipation		Including ladder		20		mW

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage if the current is limited to 30mA or less.
Note 2: Full Scale Range is 10V for unipolar mode and ±10V for bipolar mode.
Note 3: Guaranteed by design, but not 100% tested.
Note 4: To minimize feedthrough with the ceramic package, the metal lid must be grounded. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.

CMOS 10 and 12 Bit Multiplying D/A Converters

Detailed Description

The basic AD7530/31 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and reference source. The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs.

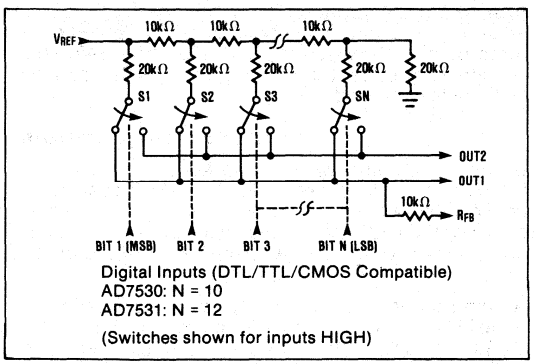


Figure 1. AD7530/AD7531 Functional Diagram

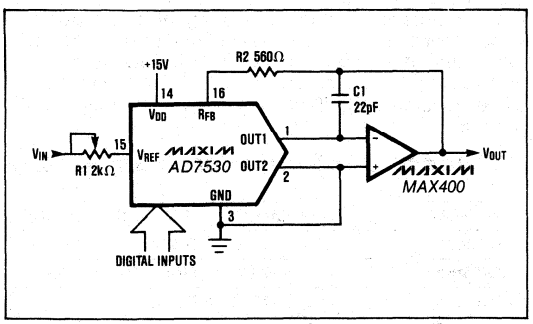


Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)

Application Information

Unipolar Operation

The most common configuration for the AD7530/31 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 can be used for gain adjustment if desired, if not, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The value depends on the type of op-amp used but typically ranges from 10 to 50pF.

The output op-amp's offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1 μA for the AD7530 and 250nA for the AD7531.

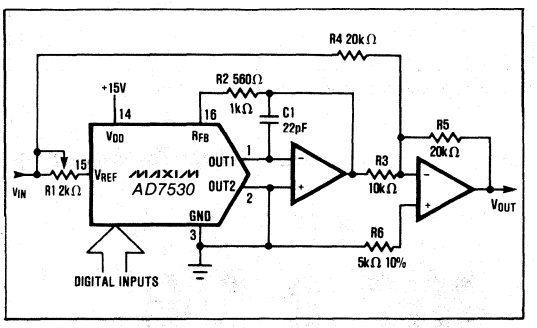


Figure 3. Bipolar Operation (4-Quadrant Multiplicaiton)

Table 1: Code Table (AD7530) — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(½ + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(½ - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Note: 1 LSB = 2^{-10} V_{REF} (AD7530)

Table 2: Code Table (AD7530) — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

Note: 1 LSB = 2^{-9} V_{REF} (AD7530)

CMOS 10 and 12 Bit Multiplying D/A Converters

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in figure 3. A second amplifier and three matched resistors are required. The output vs. code table is listed in Table 2. In multiplying applications, the MSB sets polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

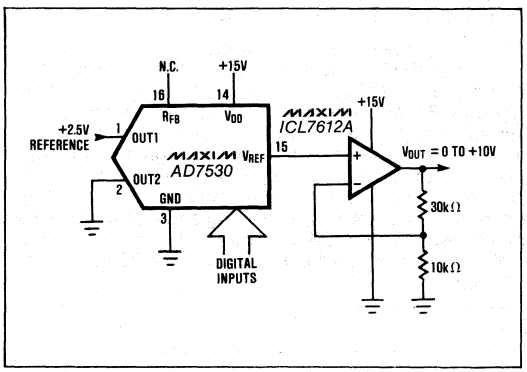
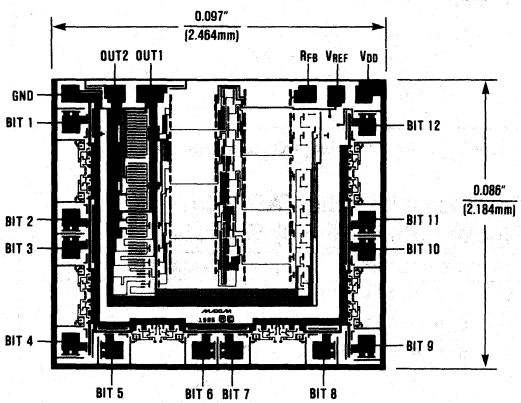


Figure 4. Single Operation Using Voltage Mode

Chip Topography



Voltage Mode (Single Supply)

The AD7530 is connected as a voltage output DAC in Figure 4. OUT1 is connected to the reference input and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). This outptut is usually buffered with an op-amp.

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted in voltage mode. The reference input (voltage at OUT1) must always be positive and is limited to no more than +3.5V when V_{DD} is +15V. If the reference voltage is greater than +3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

A common error source in dymamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough from V_{REF} and the digital inputs can be minimized with guard traces to isolate the digital inputs, V_{REF}, and the DAC outputs.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7531JN	0°C to +70°C	Plastic DIP	0.2%
AD7531KN	0°C to +70°C	Plastic DIP	0.1%
AD7531LN	0°C to +70°C	Plastic DIP	0.05%
AD7531JCWN	0°C to +70°C	Small Outline	0.2%
AD7531KCWN	0°C to +70°C	Small Outline	0.1%
AD7531LCWN	0°C to +70°C	Small Outline	0.05%
AD7531KJC/D	0°C to +70°C	Dice	0.2%
AD7531JD	-25°C to +85°C	Ceramic	0.2%
AD7531KD	-25°C to +85°C	Ceramic	0.1%
AD7531LD	-25°C to +85°C	Ceramic	0.05%
AD7531JQ	-25°C to +85°C	CERDIP**	0.2%
AD7531KQ	-25°C to +85°C	CERDIP**	0.1%
AD7531LQ	-25°C to +85°C	CERDIP**	0.05%

** AD7530 — 16 lead package, AD7531 — 18 lead package*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

MAXIM

CMOS Low Cost 10 Bit Multiplying D/A Converter

General Description

The AD7533 is a low cost CMOS 4-quadrant multiplying digital-to-analog converter (DAC). An advanced silicon gate CMOS process combines 10 bit linearity, low power consumption, and excellent long term stability. Thin-film resistors provide 1.4% untrimmed gain error and less than 0.1% gain change with temperature over all operating ranges.

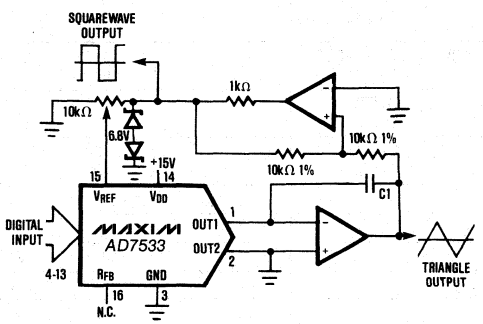
The device operates from a single +5V to +15V supply. All digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's AD7533 is pin and functionally compatible with Analog Devices' AD7533 as well as the AD7520. It is packaged in 16-lead DIP and small outline packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Programmable Function Generator

Features

- 10 Bit Resolution
- 8, 9, and 10 Bit End Point Linearity
- Low Power Consumption - 20mW
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

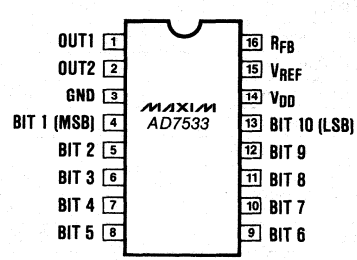
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7533JN	0°C to +70°C	Plastic DIP	0.2%
AD7533KN	0°C to +70°C	Plastic DIP	0.1%
AD7533LN	0°C to +70°C	Plastic DIP	0.05%
AD7533JCWE	0°C to +70°C	Small Outline	0.2%
AD7533KCWE	0°C to +70°C	Small Outline	0.1%
AD7533LCWE	0°C to +70°C	Small Outline	0.05%
AD7533JC/D	0°C to +70°C	Dice	0.2%
AD7533AQ	-25°C to +85°C	CERDIP**	0.2%
AD7533BQ	-25°C to +85°C	CERDIP**	0.1%
AD7533CQ	-25°C to +85°C	CERDIP**	0.05%
AD7533AD	-25°C to +85°C	Ceramic	0.2%
AD7533BD	-25°C to +85°C	Ceramic	0.1%
AD7533CD	-25°C to +85°C	Ceramic	0.05%
AD7533SQ	-55°C to +125°C	CERDIP**	0.2%
AD7533TQ	-55°C to +125°C	CERDIP**	0.1%
AD7533UQ	-55°C to +125°C	CERDIP**	0.05%
AD7533SD	-55°C to +125°C	Ceramic	0.2%
AD7533TD	-55°C to +125°C	Ceramic	0.1%
AD7533UD	-55°C to +125°C	Ceramic	0.05%

* *All devices — 16 lead packages.*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration

Top View



CMOS Low Cost 10 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation
  Plastic DIP (Derate 8.3mW/° C above +70° C) 670mW
  Ceramic, CERDIP, Small Outline
    (Derate 6mW/° C above +75° C) 450mW

Operating Temperature Range
  Commercial J/K/L ..... 0° C to +70° C
  Industrial A/B/C ..... -25° C to +85° C
  Military S/T/U ..... -55° C to +125° C
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering 10 secs) ..... +300° C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

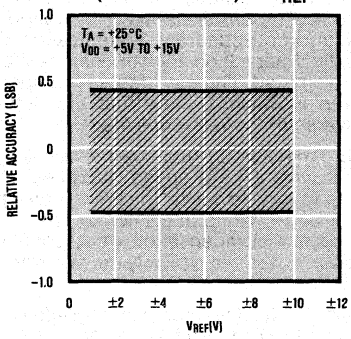
PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY							
Resolution				10			Bits
Relative Accuracy (Note 2)		AD7533J/A/S AD7533K/B/T AD7533L/C/U				±0.2 ±0.1 ±0.05	% FSR
Gain Error (Note 2,3)		Digital Inputs = V_{INH}	T_A = +25°C T_{MIN} to T_{MAX}			±1.4 ±1.5	% FSR
Power Supply Rejection (Note 4) $\Delta Gain/\Delta V_{DD}$	PSRR	V_{DD} = +14V to +17V	T_A = +25°C T_{MIN} to T_{MAX}			0.005 0.008	%/%V_{DD}
Output Leakage Current		OUT1, Digital Inputs = V_{INL}, V_{REF} = ±10V	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
		OUT2, Digital Inputs = V_{INH}, V_{REF} = ±10V	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	
V_{REF} Input Resistance	R_{REF}	T_A = +25°C		5	10	20	kΩ
V_{REF} Resistance Tempco					-300		ppm/° C
DYNAMIC PERFORMANCE							
Output Current Settling Time (Note 5)		To 0.05% of FSR, R_L = 100Ω, Digital Inputs = V_{INH} to V_{INL} and V_{INL} to V_{INH}.	T_A = +25° C T_{MIN} to T_{MAX}			600 800	ns
Feedthrough Error (Note 4)		Digital Inputs = V_{INL}, V_{REF} = ±10V, 100KHz Sinewave	T_A = +25° C T_{MIN} to T_{MAX}			±0.05 ±0.1	% FSR
Output Capacitance (Note 4)	C_{OUT}	Digital Inputs = V_{INH}	OUT1 OUT2			100 35	pF
		Digital Inputs = V_{INL}	OUT1 OUT2			35 100	
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	V
Input Leakage Current		Digital Inputs = 0V or V_{DD}				±1	μA
Input Capacitance (Note 4)						5	pF
POWER REQUIREMENTS							
Operating Supply Range	V_{DD}	+15V ±10% for Rated Accuracy		+13.5		+16.5	V
		Accuracy Not Guaranteed (Note 4)		+5		+16.5	
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				2	mA

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage rating if the current is limited to 30mA or less.
Note 2: Using internal feedback resistor (R_{FB}). Full scale range (FSR) = -(V_{REF} - 1LSB) in unipolar mode.
Note 3: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
Note 4: Guaranteed by design but not 100% tested.
Note 5: Guaranteed by design and sample tested at +25°C to ensure compliance.

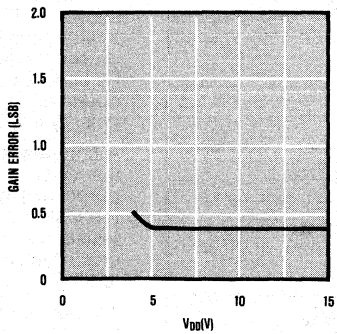
CMOS Low Cost 10 Bit Multiplying D/A Converter

Typical Operating Characteristics

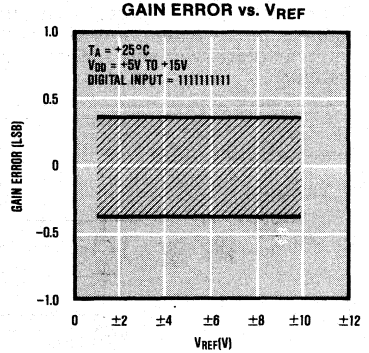
RELATIVE ACCURACY (NONLINEARITY) vs. V_{REF}



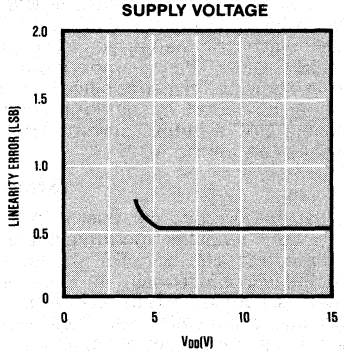
GAIN ERROR vs. SUPPLY VOLTAGE



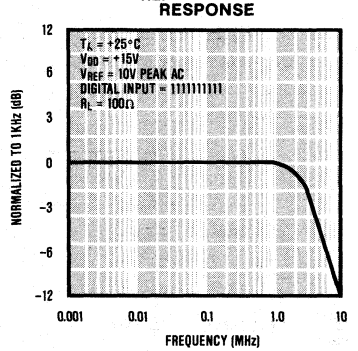
GAIN ERROR vs. V_{REF}



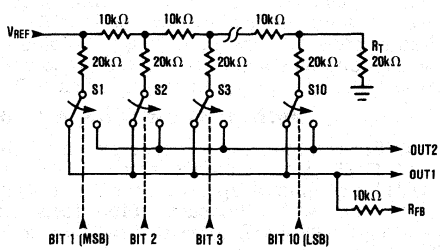
LINEARITY ERROR vs. SUPPLY VOLTAGE



V_{REF} FREQUENCY RESPONSE



Detailed Description



Digital Inputs (DTL/TTL/CMOS Compatible)
(Switches Shown for Inputs HIGH)

Figure 1. AD7533 Functional Diagram

The basic AD7533 DAC circuit consists of a thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and an external reference. The V_{REF} input accepts a wide range of reference signals including fixed and time-varying voltage or current inputs.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 10kΩ and does not change with digital input code. The $I_{REF}/1024$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

CMOS Low Cost 10 Bit Multiplying D/A Converter

Capacitors COUT1 and COUT2 represent the switches' ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from 35pF to 100pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

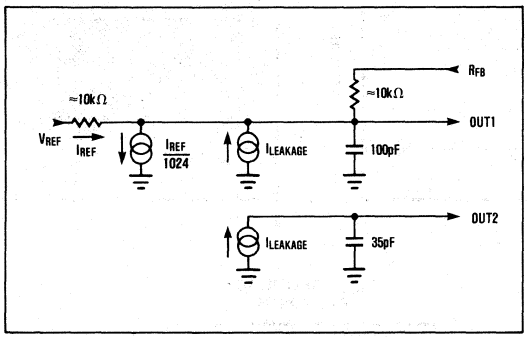


Figure 2. Equivalent DAC Circuit (All digital inputs HIGH)

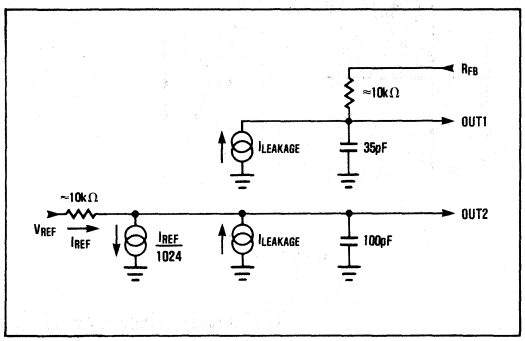


Figure 3. Equivalent DAC Circuit (All digital inputs LOW)

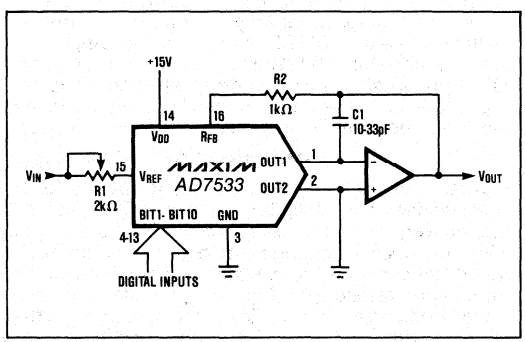


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

Application Information

Unipolar Operation

The most common configuration for the AD7533 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 is used for gain adjustment. If no adjustment is desired, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The correct compensation value depends on the type of op-amp used but typically ranges from 10 to 33pF.

The output op-amp's offset voltage can degrade DAC linearity by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1μA for the AD7533.

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 5. A second amplifier and three matched resistors are required. R3, R4, and R5 should be matched or trimmed to 0.05% to maintain 10 bit performance. The output vs. code table is listed in Table 2. In multiplying applications, the MSB determines output polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 10000 00000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

Voltage Mode (Single Supply)

The AD7533 is connected as a voltage output DAC in Figure 6. OUT1 is connected to the external reference and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). In most circuits this output is buffered with an op-amp.

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must

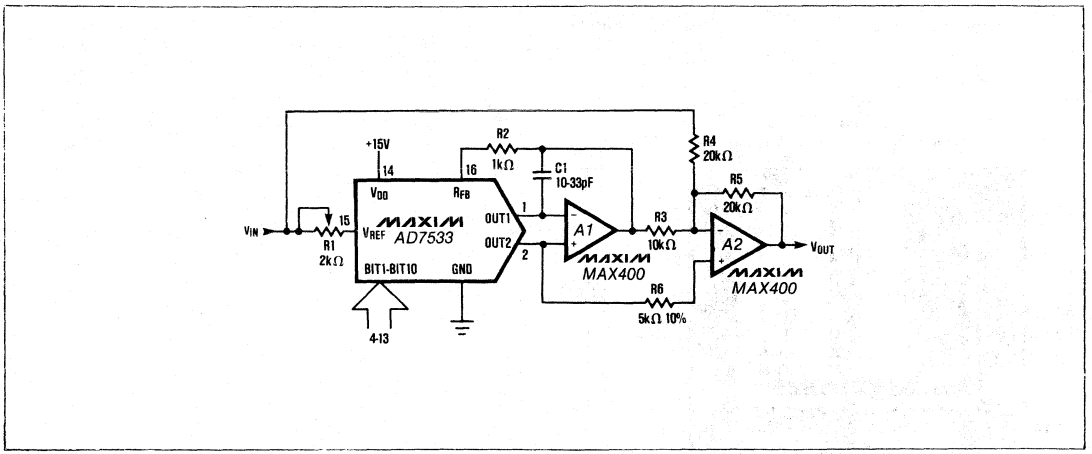


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

always be positive and is limited to no more than 3.5V when V_{DD} is 15V. If the reference voltage is greater than 3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dymamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

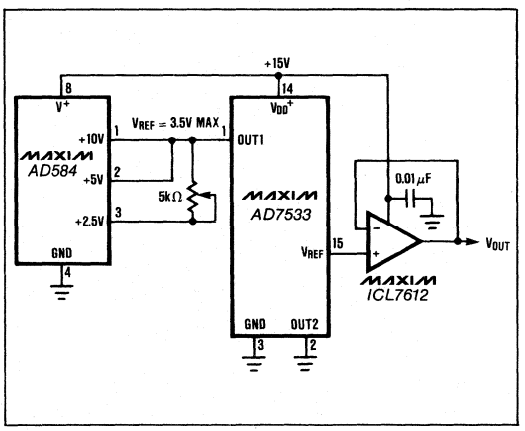


Figure 6. Voltage Mode Operation

Table 1: Code Table — Unipolar Binary Operation

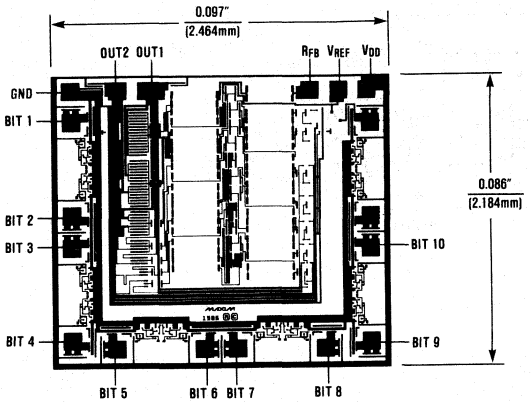
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(\frac{1}{2} + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(\frac{1}{2} - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Table 2: Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

CMOS Low Cost 10 Bit Multiplying D/A Converter

Chip Topography



MAXIM

CMOS 12 Bit Multiplying D/A Converter

General Description

The AD7541 is a high performance CMOS multiplying 12 bit digital-to-analog converter (DAC). Low power operation and 12-bit linearity (0.012%) make it suitable for a wide range of precision data acquisition and control applications.

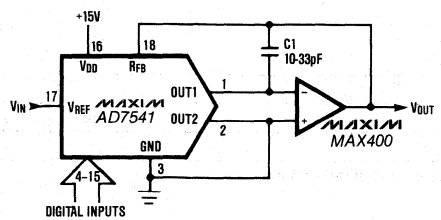
Wafer level laser trimmed thin-film resistors and temperature compensated NMOS switches assure true 12-bit performance over the full operating temperature range. In addition, all digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's AD7541 is electrically and pin compatible with the Analog Devices AD7541. It is available in standard width 18-lead DIP and Small Outline (SO) packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Unipolar Operation

Features

- 12 Bit Linearity (1/2 LSB)
- 1 LSB Gain Accuracy
- Guaranteed Monotonic
- Low Power Consumption
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

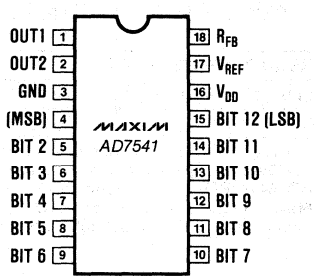
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7541JN	0°C to +70°C	Plastic DIP	1 LSB
AD7541KN	0°C to +70°C	Plastic DIP	½ LSB
AD7541JCWN	0°C to +70°C	Small Outline	1 LSB
AD7541KCWN	0°C to +70°C	Small Outline	½ LSB
AD7541JC/D	0°C to +70°C	Dice	1 LSB
AD7541AQ	-25°C to +85°C	CERDIP**	1 LSB
AD7541BQ	-25°C to +85°C	CERDIP**	½ LSB
AD7541AD	-25°C to +85°C	Ceramic	1 LSB
AD7541BD	-25°C to +85°C	Ceramic	½ LSB
AD7541SQ	-55°C to +125°C	CERDIP**	1 LSB
AD7541TQ	-55°C to +125°C	CERDIP**	½ LSB
AD7541SD	-55°C to +125°C	Ceramic	1 LSB
AD7541TD	-55°C to +125°C	Ceramic	½ LSB

* *All devices — 18 lead package.*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration

Top View



CMOS 12 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature Range
Commercial AD7541J/K ..... 0°C to +70°C
Industrial AD7541A/B ..... -25°C to +85°C
Military AD7541S/T ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC ACCURACY						
Resolution			12			Bits
Nonlinearity		AD7541J/A/S (Note 2) AD7541K/B/T (Note 3)			±1 ±0.5	LSB
Gain Error (Note 4)		Using R_{FB}; T_A = +25°C T_{MIN} to T_{MAX}			±12.5 ±16.7	LSB
Power Supply Rejection	PSRR	V_{DD} = +14.5V to +15.5V; T_A = 25°C T_{MIN} to T_{MAX}			0.01 0.02	%/%V_{DD}
Output Leakage Current		V_{REF} = ±10V; T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
Reference Input Resistance	R_{REF}	T_A = 25°C	5		20	kΩ
DYNAMIC PERFORMANCE (Note 5)						
Output Current Settling Time		To 1/2LSB			1	µs
Feedthrough Error		V_{REF} = 20V_{P-P} at 10kHz			1	mV_{P-P}
DIGITAL INPUTS						
Logic HIGH Threshold	V_{INH}		+2.4			V
Logic LOW Threshold	V_{INL}				+0.8	V
Input Leakage Current		Digital Inputs = 0V or V_{DD}			±1	µA
Input Capacitance	C_{IN}	(Note 5)			8	pF
Input Coding		Binary, Offset Binary				
ANALOG OUTPUTS						
Output Capacitance (Note 5)	C_{OUT}	Digital Inputs = V_{INH} OUT1 OUT2 Digital Inputs = V_{INL} OUT1 OUT2			200 60 60 200	pF
POWER REQUIREMENTS						
Operating Supply Range	V_{DD}	Accuracy Not Guaranteed	+5		+16	V
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}			2	mA

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum Voltage rating if the current is limited to 30mA or less.
Note 2: AD7541J/A/S are monotonic to 11 bits.
Note 3: AD7541K/B/T are monotonic to 12 bits.
Note 4: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±4.2 LSBs using internal feedback resistor.
Note 5: Guaranteed by design but not 100% tested.

CMOS 12 Bit Multiplying D/A Converter

Detailed Description

The basic AD7541 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and reference source. The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs.

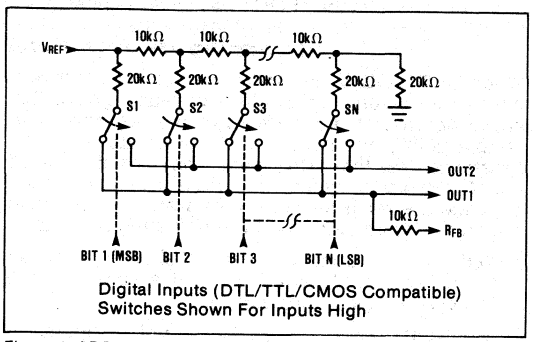
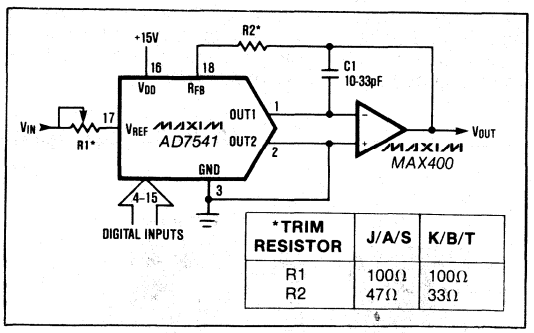


Figure 1. AD7541 Functional Diagram



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 2. Unipolar Binary Operation

Table 1. Code Table — Unipolar Binary

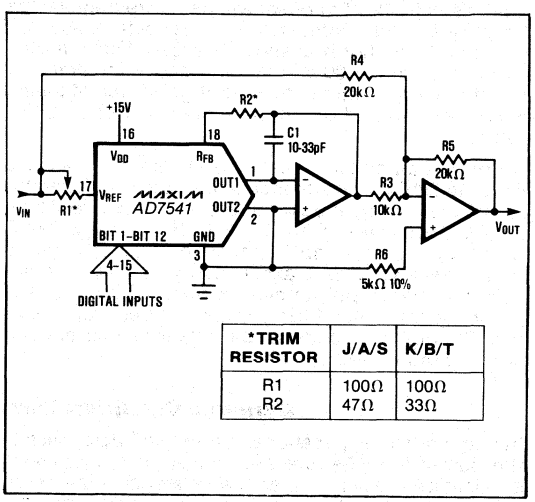
DIGITAL INPUT MSB												LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1		$-V_{REF}\left(\frac{4095}{4096}\right)$
1	0	0	0	0	0	0	0	0	0	0	0		$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2V_{REF}$
0	0	0	0	0	0	0	0	0	0	0	1		$-V_{REF}\left(\frac{1}{4096}\right)$
0	0	0	0	0	0	0	0	0	0	0	0		0V

Application Information

Unipolar Operation

The most common configuration for the AD7541 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7541 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 2 can be omitted. However, if the trims are required and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 3. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB												LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1		$+V_{REF}\left(\frac{2047}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	1		$+V_{REF}\left(\frac{1}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	0		0V
0	1	1	1	1	1	1	1	1	1	1	1		$-V_{REF}\left(\frac{1}{2048}\right)$
0	0	0	0	0	0	0	0	0	0	0	0		$-V_{REF}\left(\frac{2048}{2048}\right)$

CMOS 12 Bit Multiplying D/A Converter

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 3. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated at exactly 0V. In most applications, OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

An output amplifier's input bias current (I_B) can also limit the DAC's performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor." This resistor adds to the offset at this pin and should not be used.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

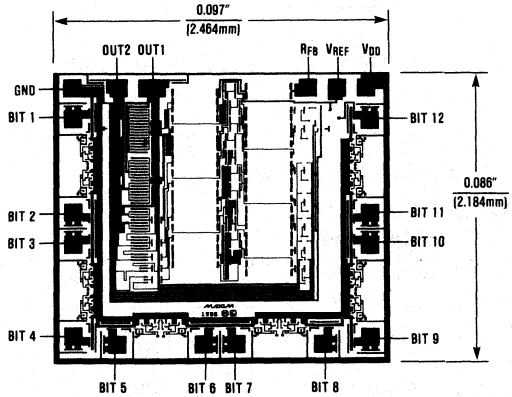
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting input are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The AD7541 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either VDD or GND when not used. It is also good practice to connect active inputs to VDD or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



CMOS 12 Bit Multiplying D/A Converter

General Description

The AD7541A is high performance CMOS multiplying 12-bit digital-to-analog converter (DAC). Low power operation and 12 bit (0.012%) linearity make it suitable for a wide range of precision data acquisition and control applications.

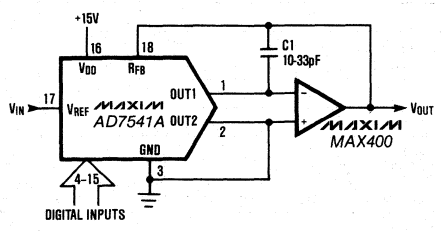
Wafer level laser trimmed thin-film resistors and temperature compensated NMOS switches assure true 12-bit performance over the full operating temperature range. In addition, all digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's AD7541A is electrically and pin compatible with the Analog Devices AD7541A and AD7541. Package types include 18-lead standard width DIP and Small Outline packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Unipolar Operation

Features

- 12 Bit Linearity (1/2 LSB)
- 1 LSB Gain Accuracy
- Guaranteed Monotonic
- Low Power Consumption
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

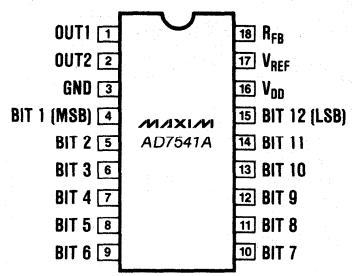
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7541AJN	0° C to +70° C	Plastic DIP	1 LSB
AD7541AKN	0° C to +70° C	Plastic DIP	½ LSB
AD7541AJCWN	0° C to +70° C	Small Outline	1 LSB
AD7541AKCWN	0° C to +70° C	Small Outline	½ LSB
AD7541AJC/D	0° C to +70° C	Dice	1 LSB
AD7541AAQ	-25° C to +85° C	CERDIP**	1 LSB
AD7541ABQ	-25° C to +85° C	CERDIP**	½ LSB
AD7541AAD	-25° C to +85° C	Ceramic	1 LSB
AD7541ABD	-25° C to +85° C	Ceramic	½ LSB
AD7541ASQ	-55° C to +125° C	CERDIP**	1 LSB
AD7541ATQ	-55° C to +125° C	CERDIP**	½ LSB
AD7541ASD	-55° C to +125° C	Ceramic	1 LSB
AD7541ATD	-55° C to +125° C	Ceramic	½ LSB

* *All devices — 18 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Pin Configuration

Top View



CMOS 12 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature Range
Commercial 7541AJ/AK ..... 0° C to +70° C
Industrial 7541AA/AB ..... -25° C to +85° C
Military 7541AS/AT ..... -55° C to +125° C
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering 10 secs) ..... +300° C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 3)							
Resolution				12			Bits
Relative Accuracy		1 LSB = 0.024% FSR 1/2 LSB = 0.012% FSR	AD7541AJ/AA/AS AD7541AK/AB/AT			±1 ±1/2	LSB
Differential Nonlinearity		12 Bit Monotonicity Guaranteed	AD7541AJ/AA/AS AD7541AK/AB/AT			±1 ±1/2	LSB
Gain Error (Note 3)		AD7541AJ/AA/AS AD7541AK/AB/AT	T_A = +25° C T_{MIN} to T_{MAX} T_A = +25° C T_{MIN} to T_{MAX}			±6 ±8 ±1 ±3	LSB
Gain Temperature Coefficient					2	5	ppm/° C
Output Leakage Current (OUT1 with Digital Inputs = 0V, and OUT2 with Digital Inputs = V_{DD})		AD7541AJ/AK/AA/AB AD7541AS/AT	T_A = +25° C T_{MIN} to T_{MAX} T_A = +25° C T_{MIN} to T_{MAX}			±5 ±10 ±5 ±200	nA
Power Supply Rejection	PSRR	V_{DD} = 15V ±5%	T_A = +25° C T_{MIN} to T_{MAX}			±0.01 ±0.02	%/%V_{DD}
V_{REF} Input Resistance	R_{REF}			7	11	18	kΩ
V_{REF} Resistance Tempco					-300		ppm/° C
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	
Input Leakage Current	I_{IN}	Digital Inputs = 0V or V_{DD}	T_A = +25° C T_{MIN} to T_{MAX}		±0.001	±1	μA
Input Capacitance	C_{IN}	(Note 2)				8	pF
DYNAMIC PERFORMANCE (Note 2)							
Propagation Delay to 90% of Final Analog Output		Digital Input Change 0V to V_{DD} and V_{DD} to 0V, OUT1 Load = 100Ω, C_{EXT} = 13pF, T_A = +25° C			100		ns
Digital to Analog Glitch Impulse		V_{REF} = 0V, Dig. Inputs = 0V to V_{DD} or V_{DD} to 0V			1000		nV-sec
Multiplying Feedthrough Error		V_{REF} = ±10V, 10kHz Sinewave, T_A = +25° C			1		mVp-p
Output Current Settling Time to 0.01% of FSR		Digital Input Change 0V to V_{DD} and V_{DD} to 0V, OUT1 Load = 100Ω, C_{EXT} = 13pF, T_A = +25° C			600		ns
Output Capacitance	C_{OUT}	Digital Inputs = V_{INH} Digital Inputs = V_{INL}	OUT1 OUT2 OUT1 OUT2			200 70 70 200	pF

ELECTRICAL CHARACTERISTICS (continued)

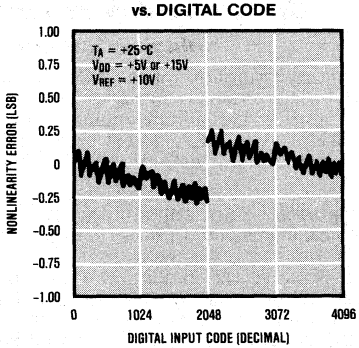
(T_A = T_{MIN} to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
POWER REQUIREMENTS							
Operating Supply Range	V_{DD}	Accuracy Not Guaranteed		+5		+16	V
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				2	mA
		Digital Inputs = 0V or V_{DD}	T_A = +25°C			100	μA
			T_{MIN} to T_{MAX}			500	

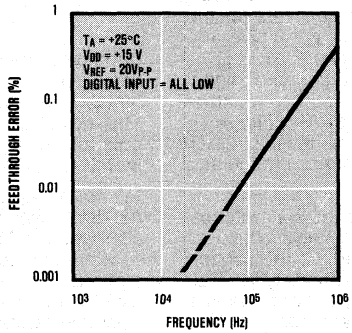
Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum Voltage rating if the current is limited to 30mA or less.
Note 2: Guaranteed by design but not 100% tested.
Note 3: Measured using internal R_{FB} and includes effect of Leakage Current and Gain Tempco. Gain Error can be trimmed to zero.

Typical Operating Characteristics

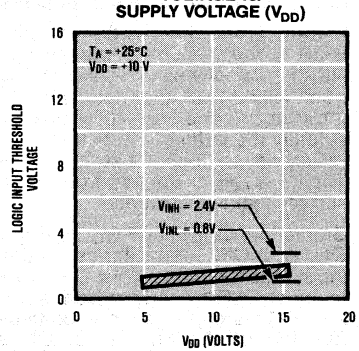
NONLINEARITY ERROR vs. DIGITAL CODE



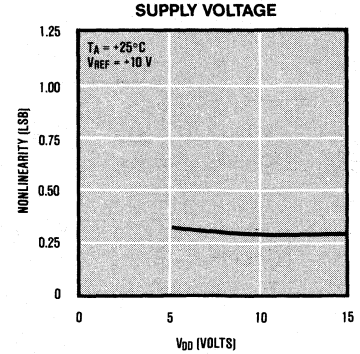
FEEDTHROUGH ERROR vs. FREQUENCY



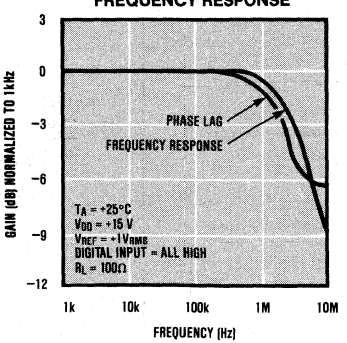
LOGIC INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE (V_{DD})



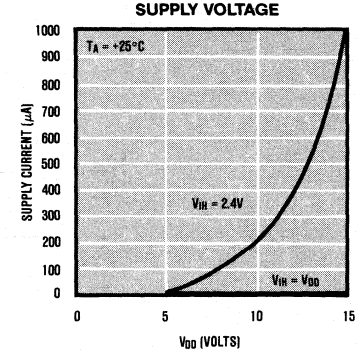
NONLINEARITY vs. SUPPLY VOLTAGE



V_{REF} PHASE LAG AND FREQUENCY RESPONSE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



CMOS 12 Bit Multiplying D/A Converter

Detailed Description

The basic AD7541A DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

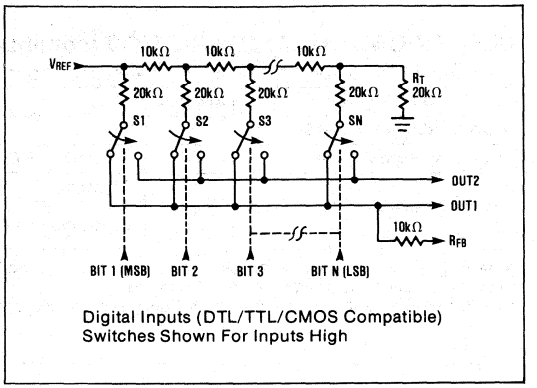


Figure 1. AD7541A Functional Diagram

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 11kΩ and does not change with digital input code. The $I_{REF}/4096$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches' ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 70pF to 200pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7541A is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7541A will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

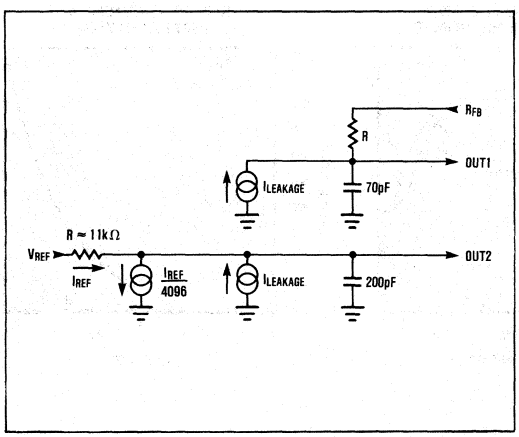


Figure 2. AD7541A DAC Equivalent Circuit, All Digital Inputs LOW

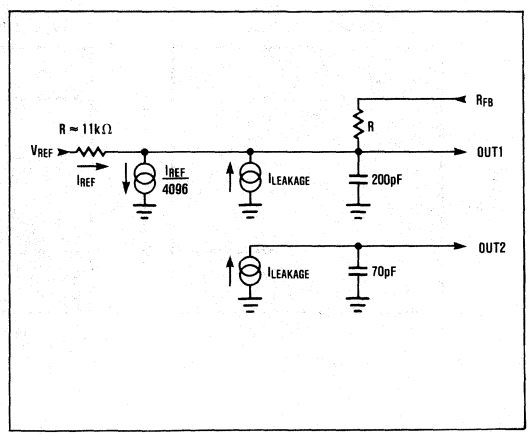
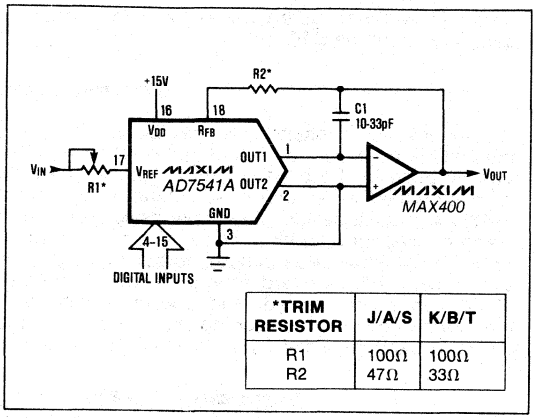
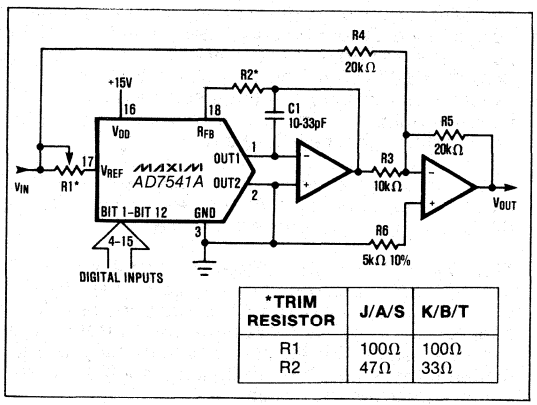


Figure 3. AD7541A DAC Equivalent Circuit, All Digital Inputs HIGH



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 4. Unipolar Binary Operation



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

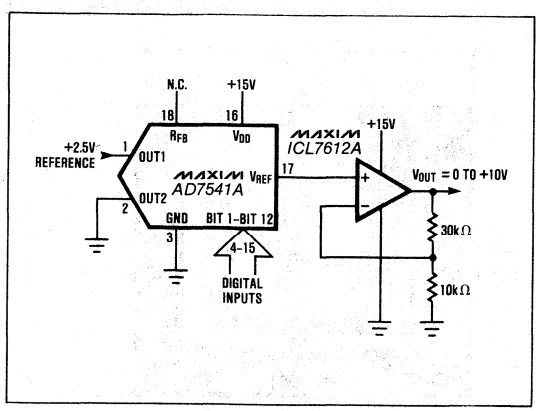


Figure 6. Single Supply Operation Using Voltage Mode

Table 1. Code Table — Unipolar Binary

DIGITAL INPUT MSB												LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1		$-V_{REF}\left(\frac{4095}{4096}\right)$
1	0	0	0	0	0	0	0	0	0	0	0		$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2V_{REF}$
0	0	0	0	0	0	0	0	0	0	0	1		$-V_{REF}\left(\frac{1}{4096}\right)$
0	0	0	0	0	0	0	0	0	0	0	0		0V

Table 2. Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB												LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1		$+V_{REF}\left(\frac{2047}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	1		$+V_{REF}\left(\frac{1}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	0		0V
0	1	1	1	1	1	1	1	1	1	1	1		$-V_{REF}\left(\frac{1}{2048}\right)$
0	0	0	0	0	0	0	0	0	0	0	0		$-V_{REF}\left(\frac{2048}{2048}\right)$

Bipolar Operation

With the circuit configuration in Figure 5, the AD7541A operates in the bipolar, or four-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

Voltage Mode (Single Supply)

The AD7541A is connected as a voltage output DAC in Figure 6. OUT1 is connected to the reference input and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). This output is usually buffered with an op-amp.

CMOS 12 Bit Multiplying D/A Converter

Two advantages of voltage mode operation are single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (voltage at OUT1) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal switches degrade linearity.

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 10kΩ to 30kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF}=10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

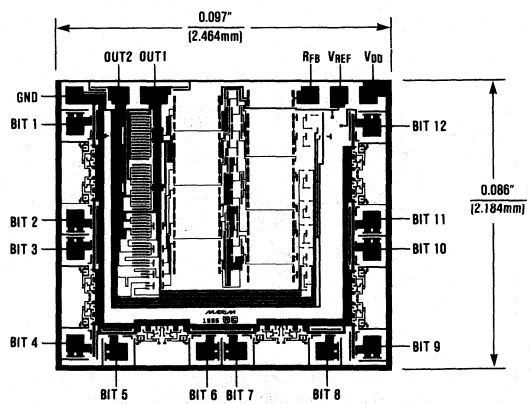
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting input are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The 7541A has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either VDD or GND when not used. It is also good practice to connect active inputs to VDD or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



CMOS µP-Compatible 12-Bit DAC

General Description

The AD7542 is a CMOS 12-Bit digital-to-analog converter (DAC) which directly interfaces to both 8-bit and 4-bit microprocessors. Input data is loaded as three 4-bit bytes, and is then transferred to an internal 12-bit DAC register. Data load and transfer interface timing is similar to that of a static RAM write cycle.

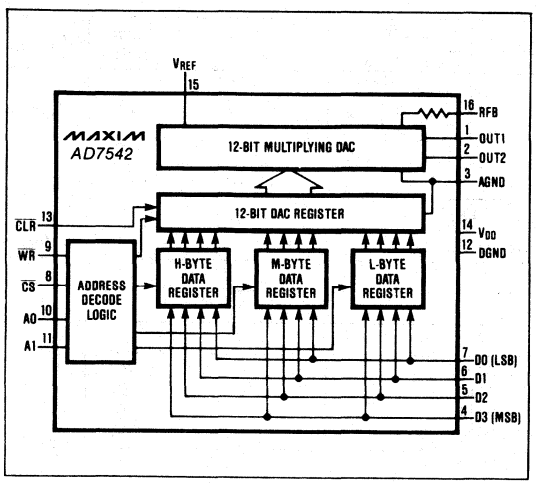
A clear input is also provided which resets the DAC register to all zeros. This can be used to initialize the device on power up or during software calibration routines.

Low power consumption, +5V operation, and multiplying capability make the AD7542 suitable for numerous high precision processor controlled DAC applications. The AD7542 is supplied in 16-lead DIP and Small Outline packages.

Applications

Programmable Power Sources
Portable Test Equipment
Digitally Controlled Filters
Auto-Calibration Circuitry
Motion Control Systems

Functional Diagram



Features

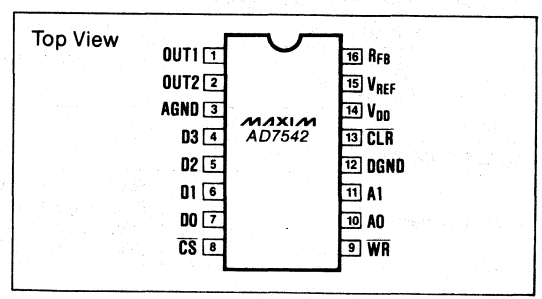
- 12-Bit Resolution
- ±1/2 LSB Linearity Over Temperature
- ±1 LSB Gain Accuracy (AD7542G)
- 5ppm/°C Max. Gain Drift
- Microprocessor Compatible
- 40mW Max. Power Dissipation
- +5V Operation

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7542JN	0°C to +70°C	Plastic DIP	±1 LSB
AD7542KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7542GKN	0°C to +70°C	Plastic DIP	±½ LSB
AD7542JCWE	0°C to +70°C	Small Outline	±1 LSB
AD7542KCWE	0°C to +70°C	Small Outline	±½ LSB
AD7542GKCWE	0°C to +70°C	Small Outline	±½ LSB
AD7542JC/D	0°C to +70°C	Dice	±1 LSB
AD7542AD	-25°C to +85°C	Ceramic	±1 LSB
AD7542BD	-25°C to +85°C	Ceramic	±½ LSB
AD7542GBD	-25°C to +85°C	Ceramic	±½ LSB
AD7542AQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7542BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7542GBQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7542SD	-55°C to +125°C	Ceramic	±1 LSB
AD7542TD	-55°C to +125°C	Ceramic	±½ LSB
AD7542GTD	-55°C to +125°C	Ceramic	±½ LSB
AD7542SQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7542TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7542GTQ	-55°C to +125°C	CERDIP**	±½ LSB

* *All devices — 16 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Pin Configuration



CMOS µP-Compatible 12-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +7V
V_{DD} to DGND ..... -0.3V, +7V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 4-11, 13)
V_{PIN1}, V_{PIN2} to AGND ..... -0.3V, V_{DD} + 0.3V
V_{REF} to AGND ..... ±25V
V_{RFB} to AGND ..... ±25V

Power Dissipation 450mW
(derate 6mW/°C above +70°C)
Operating Temperature Range
Commercial AD7542J, K, GK ..... 0°C to +70°C
Industrial AD7542A, B, GB ..... -25°C to +85°C
Military AD7542S, T, GT ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				12			Bits
Non-Linearity		AD7542J/A/S AD7542K/B/T AD7542GK/GB/GT				±1 ±0.5 ±0.5	LSB
Differential Non-Linearity		AD7542J/A/S (Note 1) AD7542K/B/T (Note 2) AD7542GK/GB/GT (Note 2)				±2 ±1 ±1	LSB
Gain Error		AD7542J/K/A/B/S/T AD7542J/K/A/B AD7542S/T	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±12.3 ±13.5 ±14.5	LSB
		AD7542GK/GB/GT AD7542GK/GB AD7542GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±1 ±1 ±2	
Gain Temperature Coefficient ΔGain/ΔTemperature (Note 4)					2	5	ppm/°C
Power Supply Rejection	PSRR	V_{DD} = +4.75V to +5.25V	T_A = 25°C T_{MIN} to T_{MAX}			0.005 0.01	%/%V_{DD}
Output Leakage Current I_{OUT1}, I_{OUT2} (Note 3)		AD7542J/K/GK AD7542A/B/GB AD7542S/T/GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			1 10 10 200	nA
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling Time		To 1/2 LSB, Out1 Load = 100Ω				2	µs
Feedthrough Error		V_{REF} = ±10V 10kHz sine wave				2.5	mVpp
REFERENCE INPUT							
Input Resistance (pin 15)	R_{REF}			8	15	25	kΩ
ANALOG OUTPUT (Note 4)							
Output Capacitance	C_{OUT1} C_{OUT1} C_{OUT2} C_{OUT2}	DAC Register 0000 0000 0000 DAC Register 1111 1111 1111 DAC Register 1111 1111 1111 DAC Register 0000 0000 0000				75 260 75 260	pF

ELECTRICAL CHARACTERISTICS (Continued)

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Logic HIGH Voltage	V_{INH}		+3.0			V
Logic LOW Voltage	V_{INL}				+0.8	V
Logic Input Current	I_{IN}	0V or V_{DD}			1	µA
Input Capacitance (Note 4)	C_{IN}				8	pF
SWITCHING CHARACTERISTICS (see Figure 6) (Note 5)						
Write Pulse Width	t_{WR}	T_A = 25°C T_{MIN} to T_{MAX}	120 220			ns
Address-to-Write Hold Time	t_{AWH}	T_A = 25°C T_{MIN} to T_{MAX}	50 65			ns
Chip Select-to-Write Hold	t_{CWH}	T_A = 25°C T_{MIN} to T_{MAX}	50 100			ns
Minimum CLEAR Pulse Width	t_{CLR}	T_A = 25°C T_{MIN} to T_{MAX}	200 300			ns
BYTE LOADING						
Chip Select-to-WRITE Setup	t_{CWS}	T_A = 25°C T_{MIN} to T_{MAX}	60 130			ns
Address Valid-to-Write Setup	t_{AWS}	T_A = 25°C T_{MIN} to T_{MAX}	80 180			ns
Data Setup Time	t_{DS}	T_A = 25°C T_{MIN} to T_{MAX}	50 65			ns
Data Hold Time	t_{DH}	T_A = 25°C T_{MIN} to T_{MAX}	50 65			ns
DAC LOADING						
Chip Select-to-WRITE Setup	t_{CWS}	T_A = 25°C T_{MIN} to T_{MAX}	60 150			ns
Address valid-to-Write Setup	t_{AWS}	T_A = 25°C T_{MIN} to T_{MAX}	120 240			ns
POWER SUPPLY						
Supply Voltage	V_{DD}	5V ± 5%	4.75		5.25	V
Supply Current	I_{DD}				2.5	mA

Note 1: Monotonic to 11 bits from T_{MIN} to T_{MAX}
Note 2: Monotonic to 12 bits from T_{MIN} to T_{MAX}
Note 3: I_{OUT1} tested with DAC register loaded to all 0's.
I_{OUT2} tested with DAC register loaded to all 1's.
Note 4: Guaranteed by design but not tested.
Note 5: Sample tested at +25°C to ensure compliance.

CMOS µP-Compatible 12-Bit DAC

Detailed Description

The basic AD7542 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 15kΩ and does not change with digital input code. The $I_{REF}/4096$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 75pF to 260pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

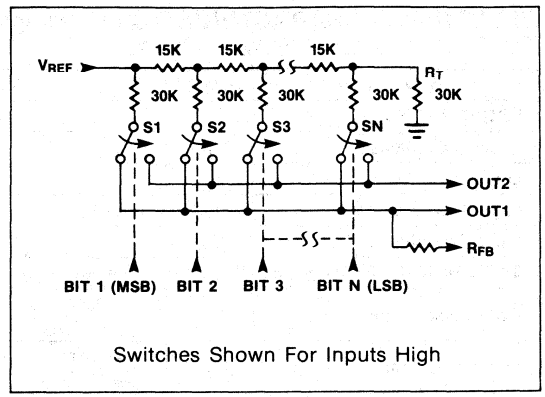


Figure 1. AD7542 Functional Diagram

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7542 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7542 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

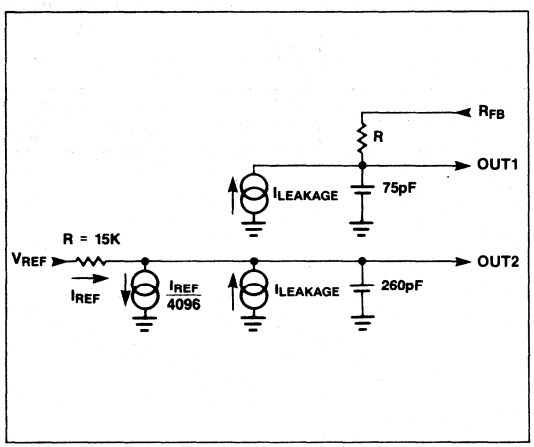


Figure 2. AD7542 DAC Equivalent Circuit, All Digital Inputs LOW

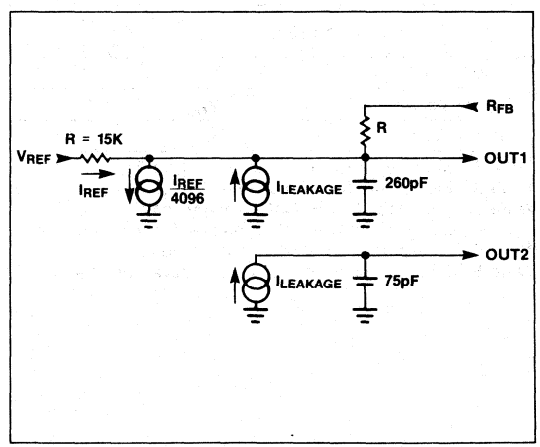


Figure 3. AD7542 DAC Equivalent Circuit, All Digital Inputs HIGH

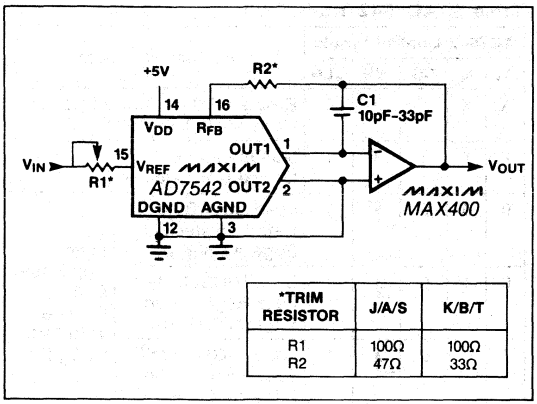


Figure 4. Unipolar Binary Operation

Table 1. Code Table—Unipolar Binary

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0V

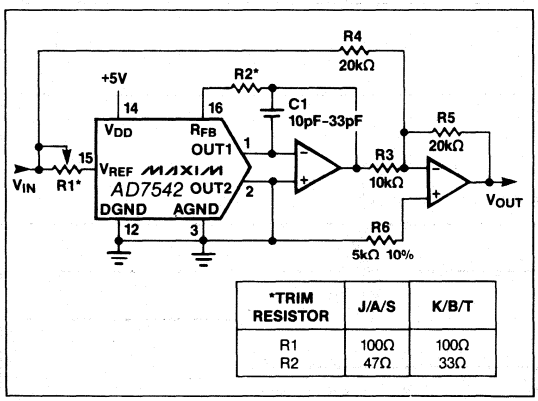


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table—Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

Bipolar Operation

With the circuit configuration in Figure 5, the AD7542 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

CMOS μP-Compatible 12-Bit DAC

Interface Logic

Interface Logic Information

The AD7542 Truth Table is shown in Table 3. The high, middle and low byte, 4 bit data registers are loaded separately. The 12-bit DAC register is then loaded with the contents of the 3 data registers. The interface timing (Figure 6) is the same as writing to static RAM.

The CLR input asynchronously resets the 12-Bit DAC Register to Code 0000 0000 0000. In a unipolar mode the DAC output will be set to 0 volts. In the bipolar mode a CLR input resets the DAC output to $-V_{REF}$.

Notes:
1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. ⌐ indicates LOW to HIGH transition
5. MSB → XXXX (high byte) XXXX (middle byte) XXXX (low byte) ← LSB
6. These control signals are level triggered.

Table 3. AD7542 Truth Table

AD7542 Control Inputs					AD7542 Operation	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0	⌐	1	Load LOW Byte[5] Data Register On Edge As Shown	Load Applicable Data Register With Data At D_0-D_3
0	1	0	⌐	1	Load MIDDLE Byte[5] Data Register On Edge As Shown	
1	0	0	⌐	1	Load HIGH Byte[5] Data Register On Edge As Shown	
1	1	0	⌐¬	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers[6]	

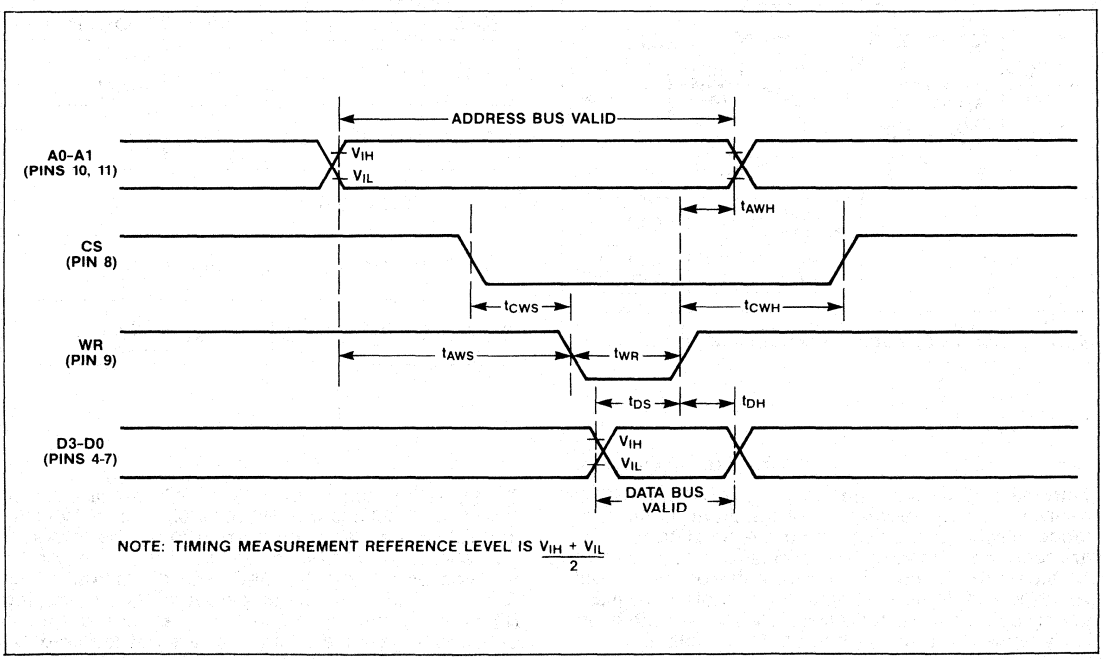


Figure 6. AD7542 Timing Diagram

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 15kΩ to 45kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error, I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensations

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

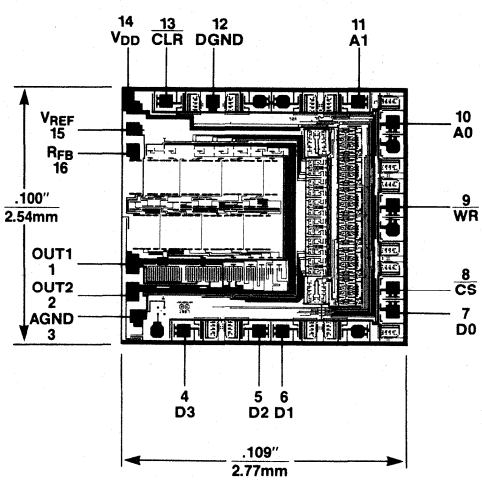
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting inputs are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1µF bypass capacitor, in parallel with a 0.01µF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The AD7542 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is also good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



MAXIM

CMOS Serial Input 12-Bit DAC

General Description

The AD7543 is a high precision 12-bit digital-to-analog converter (DAC) which uses a serial rather than parallel input scheme for loading data. Included are a serial-to-parallel shift register, a separate DAC register, and a multiplying DAC.

Serial data is clocked in at the SRI pin on the rising or falling edge (user selected) of the strobe input. When the input register is full, the contents are transferred to the DAC register using the load input. A clear input is provided to initialize the part asynchronously.

The AD7543 features excellent gain stability (5ppm/°C max.) and operates from a single +5V power supply while dissipating about 10mW.

Applications

Remote Analog Systems

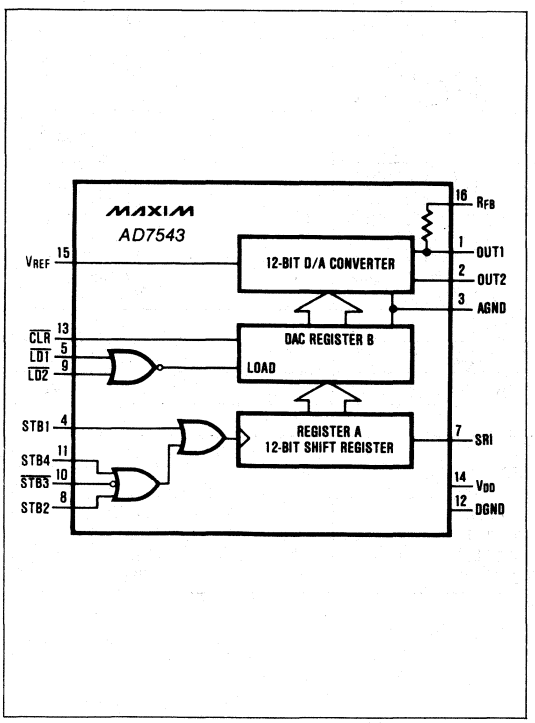
Robotics

Programmable Attenuators

Automatic Test Equipment

Auto-Calibration Systems

Functional Diagram



Features

- Serial Interface
- ±½ and ±1 LSB Linearity
- CLEAR Input For Initialization
- Single +5V Supply Operation
- 5ppm/°C Gain Stability
- 1 LSB Max. Feedthrough At 10kHz
- Small Size: 16-Lead DIP

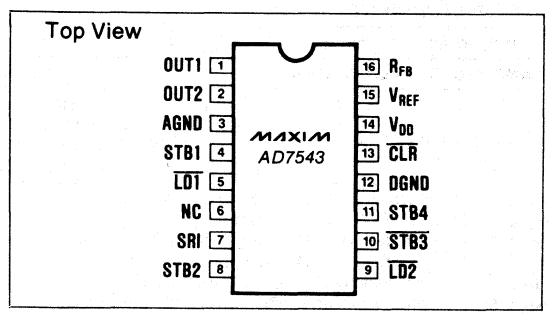
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7543JN	0°C to +70°C	Plastic DIP	±1 LSB
AD7543KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7543GKN	0°C to +70°C	Plastic DIP	±½ LSB
AD7543JCWE	0°C to +70°C	Small Outline	±1 LSB
AD7543KCWE	0°C to +70°C	Small Outline	±½ LSB
AD7543GKCWE	0°C to +70°C	Small Outline	±½ LSB
AD7543JC/D	0°C to +70°C	Dice	±1 LSB
AD7543AD	-25°C to +85°C	Ceramic	±1 LSB
AD7543BD	-25°C to +85°C	Ceramic	±½ LSB
AD7543GBD	-25°C to +85°C	Ceramic	±½ LSB
AD7543AQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7543BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7543GBQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7543SD	-55°C to +125°C	Ceramic	±1 LSB
AD7543TD	-55°C to +125°C	Ceramic	±½ LSB
AD7543GTD	-55°C to +125°C	Ceramic	±½ LSB
AD7543SQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7543TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7543GTQ	-55°C to +125°C	CERDIP**	±½ LSB

** All devices—16-pin packages*

*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration



CMOS Serial Input 12-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +7V
V_{DD} to DGND ..... -0.3V, +7V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 4-11, 13)
V_{PIN1}, V_{PIN2} to AGND ..... -0.3V, V_{DD} + 0.3V
V_{REF} to AGND ..... ±25V
V_{RFB} to AGND ..... ±25V

Power Dissipation 450mW
(derate 6mW/°C above +70°C)
Operating Temperature Range
Commercial AD7543J, K, GK ..... 0°C to +70°C
Industrial AD7543A, B, GB ..... -25°C to +85°C
Military AD7543S, T, GT ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				12			Bits
Non-Linearity		AD7543J/A/S AD7543K/B/T AD7543GK/GB/GT				±1 ±0.5 ±0.5	LSB
Differential Non-Linearity		AD7543J/A/S (Note 1) AD7543K/B/T (Note 2) AD7543GK/GB/GT (Note 2)				±2 ±1 ±1	LSB
Gain Error		AD7543J/K/A/B/S/T AD7543J/K/A/B AD7543S/T	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±12.3 ±13.5 ±14.5	LSB
		AD7543GK/GB/GT AD7543GK/GB AD7543GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±1 ±1 ±2	
Gain Temperature Coefficient ΔGain/ΔTemperature (Note 4)					2	5	ppm/°C
Power Supply Rejection	PSRR	V_{DD} = +4.75V to +5.25V	T_A = 25°C T_{MIN} to T_{MAX}			0.005 0.01	%/%V_{DD}
Output Leakage Current I_{OUT1}, I_{OUT2} (Note 3)		AD7543J/K/GK AD7543A/B/GB AD7543S/T/GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			1 10 10 200	nA
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling Time		To 1/2 LSB, Out1 Load = 100Ω				2	μs
Feedthrough Error		V_{REF} = ±10V 10kHz sine wave				2.5	mVpp
REFERENCE INPUT							
Input Resistance (pin 15)	R_{REF}			8	15	25	kΩ
ANALOG OUTPUT (Note 4)							
Output Capacitance	C_{OUT1} C_{OUT1} C_{OUT2} C_{OUT2}	DAC Register 0000 0000 0000 DAC Register 1111 1111 1111 DAC Register 1111 1111 1111 DAC Register 0000 0000 0000				75 260 75 260	pF

Note 1: Monotonic to 11 bits from T_{MIN} to T_{MAX}
Note 2: Monotonic to 12 bits from T_{MIN} to T_{MAX}
Note 3: I_{OUT1} tested with DAC register loaded to all 0's.
I_{OUT2} tested with DAC register loaded to all 1's.
Note 4: Guaranteed by design but not tested.
Note 5: Sample tested at +25°C to ensure compliance.

ELECTRICAL CHARACTERISTICS (Continued)

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Logic HIGH Voltage	V_{INH}		+3.0			V
Logic LOW Voltage	V_{INL}				+0.8	V
Logic Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			1	μA
Input Capacitance (Note 4)	C_{IN}				8	pF
SWITCHING CHARACTERISTICS (see Figure 6) (Note 5)						
Serial Input to Strobe Setup Time	t_{DS1}	T_A = 25°C T_{MIN} to T_{MAX}	50 100			ns
	t_{DS2}	T_A = 25°C T_{MIN} to T_{MAX}	20 40			ns
	t_{DS3}	T_A = 25°C T_{MIN} to T_{MAX}	0 0			ns
	t_{DS4}	T_A = 25°C T_{MIN} to T_{MAX}	0 0			ns
Serial Input to Strobe Hold Time	t_{DH1}	T_A = 25°C T_{MIN} to T_{MAX}	30 60			ns
	t_{DH2}	T_A = 25°C T_{MIN} to T_{MAX}	60 120			ns
	t_{DH3}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
	t_{DH4}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
SRI data pulse width	t_{SRI}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
STB1 pulse width	t_{STB1}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
STB2 pulse width	t_{STB2}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
$\overline{STB3}$ pulse width	t_{STB3}	T_A = 25°C T_{MIN} to T_{MAX}	100 200			ns
STB4 pulse width	t_{STB4}	T_A = 25°C T_{MIN} to T_{MAX}	100 200			ns
Load 1 pulse width	t_{LD1}	T_A = 25°C T_{MIN} to T_{MAX}	150 300			ns
Load 2 pulse width	t_{LD2}	T_A = 25°C T_{MIN} to T_{MAX}	150 300			ns
Time between strobing LSB into Register A and loading Register B	t_{ASB}	T_A = 25°C T_{MIN} to T_{MAX}	0 0			ns
Clear pulse width	t_{CLR}	T_A = 25°C T_{MIN} to T_{MAX}	200 400			ns
POWER SUPPLY						
Supply Voltage	V_{DD}	5V ± 5%	4.75		5.25	V
Supply Current	I_{DD}				2.5	mA

CMOS Serial Input 12-Bit DAC

Detailed Description

The basic AD7543 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 15kΩ and does not change with digital input code. The I_{REF}/4096 current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 75pF to 260pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

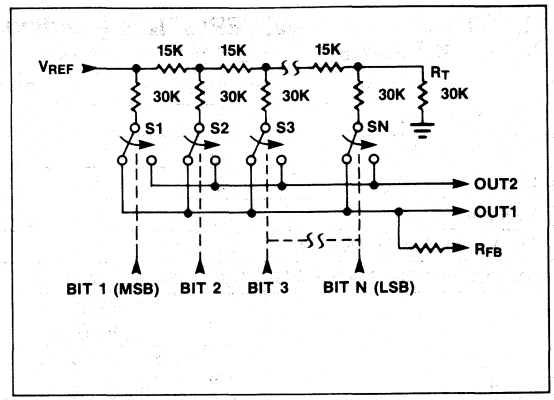


Figure 1. AD7543 Functional Diagram

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7543 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7543 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

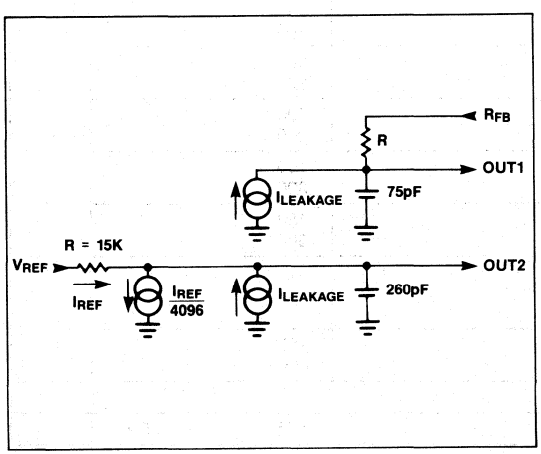


Figure 2. AD7543 DAC Equivalent Circuit, All Digital Inputs LOW

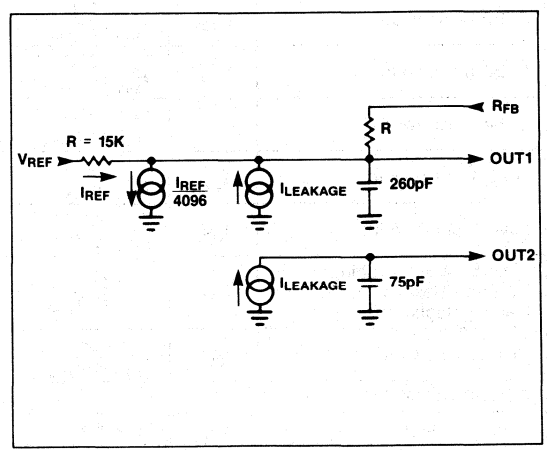


Figure 3. AD7543 DAC Equivalent Circuit, All Digital Inputs HIGH

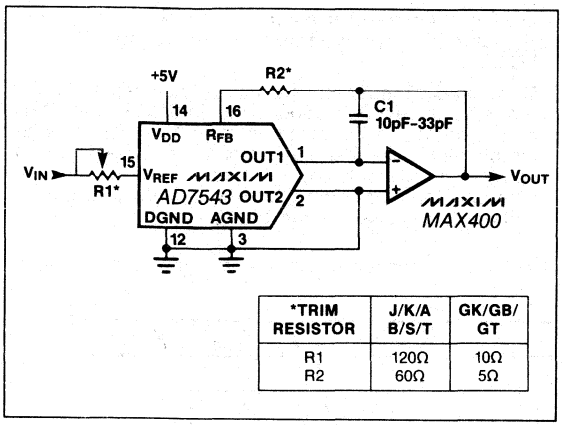


Figure 4. Unipolar Binary Operation

Table 1. Code Table—Unipolar Binary

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0V

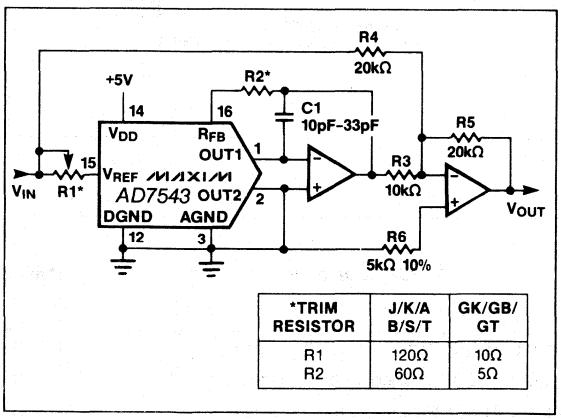


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table—Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

Bipolar Operation

With the circuit configuration in Figure 5, the AD7543 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

CMOS Serial Input 12-Bit DAC

Interface Logic

Serial data is first loaded into the 12-bit Shift Register A, shown in the AD7543 functional diagram. Each bit of serial data appearing at pin SRI is clocked into Register A MSB first, by any one of the four strobe inputs. STB1, STB2, and STB4 all clock data into Shift Register A on the rising edge of the strobe pulse. $\overline{STB3}$ clocks data into Register A on its falling edge. Table 3 illustrates the logic states for the control inputs. Figure 6 shows the timing diagram for the loading sequence.

Data is then transferred from Shift Register A into Register B by momentarily moving both $\overline{LD1}$ and $\overline{LD2}$, low.

Bringing $\overline{CLR}$ input low asynchronously resets Register B to 0000 0000 0000. This initializes the DAC output voltage to a known condition. With the unipolar circuit of Figure 4, a $\overline{CLR}$ results in a DAC output voltage of 0 volts. Using the bipolar circuit of Figure 5, momentarily bringing $\overline{CLR}$ low sets the DAC output voltage to its lowest value of $-V_{REF}$.

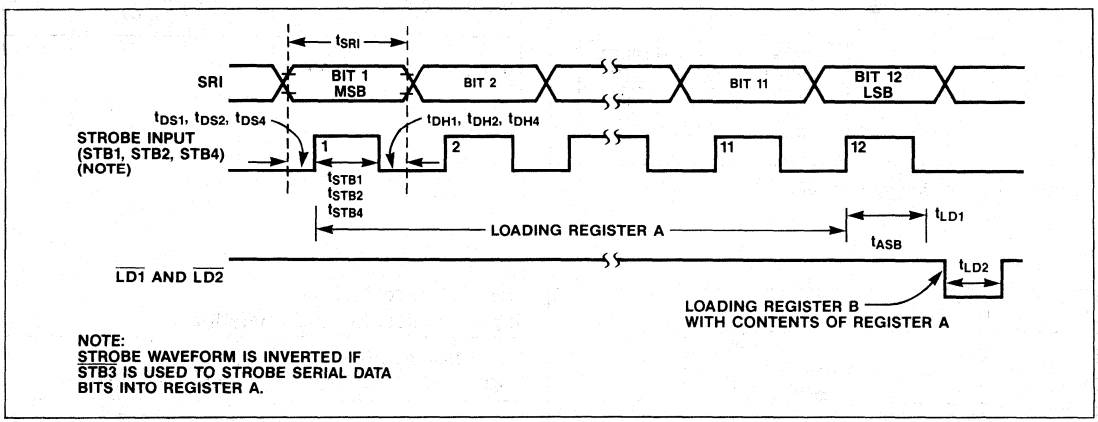


Figure 6. Timing Diagram

Table 3. AD7543 Truth Table

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↓	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
0	1	↓	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
0	↓	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
↓	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1, 3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

Notes:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↓ is positive edge ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated exactly at 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 15kΩ to 45kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error, I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

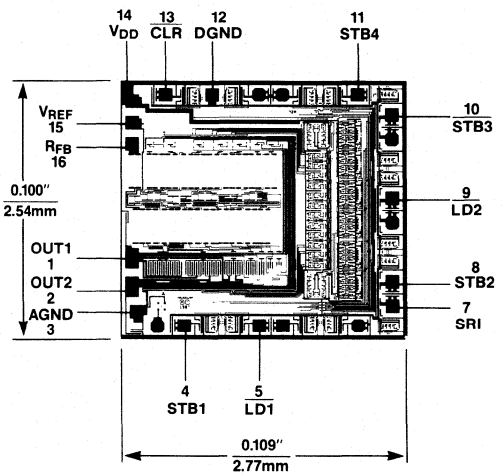
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting inputs are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The AD7543 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is also good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



CMOS 12-Bit Buffered Multiplying DAC

General Description

The AD7545 is a 12-bit CMOS multiplying digital-to-analog converter (DAC) with internal data latches. Input data is loaded as a single 12-bit word and latched under the control of CS and WR inputs. When CS and WR are low, the input data latches are transparent and the DAC output responds to any changes in the digital input.

AD7545 works with a single +5V or +15V power supply. Electrical characteristics are specified at both of these supply voltages. With a +5V supply, the digital inputs are +5V TTL and CMOS compatible while high voltage CMOS compatibility is maintained at +15V supply range.

Maxim AD7545 uses low tempco thin-film resistors which are laser-trimmed to result in linearity errors that are typically ±¼ LSB and gain errors of maximum ±1 LSB (G grade).

The digital inputs are designed with improved protection against electrostatic discharge (ESD) damage and can typically withstand to over 6,000V of ESD voltages.

The AD7545 is supplied in 20-lead narrow DIP and Small Outline packages.

Applications

Motion Control Systems

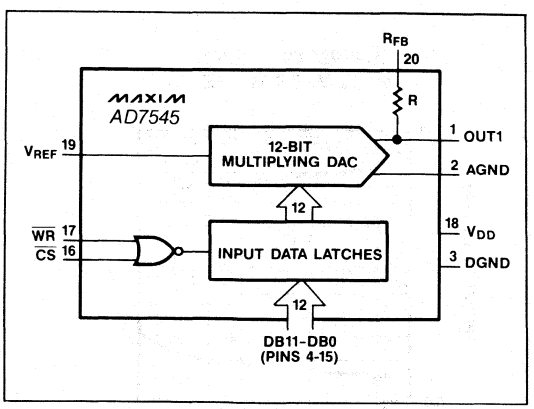
Automatic Test Equipment

μP Controlled Calibration Circuitry

Programmable Gain Amplifiers

Programmable Power Supplies

Functional Diagram



Features

- ◆ 12-Bit Resolution
- ◆ ±1 LSB Gain Accuracy (G Grade)
- ◆ Single Supply Operation
- ◆ Improved ESD Protection
- ◆ CMOS/TTL Compatible for V_{DD} = +5V
- ◆ CMOS Compatible for V_{DD} = +15V

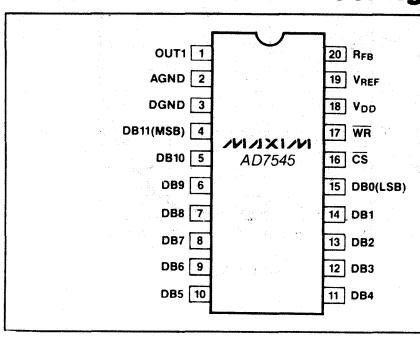
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7545JN	0°C to +70°C	Plastic DIP	±2 LSB
AD7545KN	0°C to +70°C	Plastic DIP	±1 LSB
AD7545LN	0°C to +70°C	Plastic DIP	±½ LSB
AD7545GLN	0°C to +70°C	Plastic DIP	±½ LSB
AD7545JCWP	0°C to +70°C	Small Outline	±2 LSB
AD7545KCWP	0°C to +70°C	Small Outline	±1 LSB
AD7545LCWP	0°C to +70°C	Small Outline	±½ LSB
AD7545GLCWP	0°C to +70°C	Small Outline	±½ LSB
AD7545JC/D	0°C to +70°C	Dice	±2 LSB
AD7545AQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7545BQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7545CQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7545GCQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7545SD	-55°C to +125°C	Ceramic	±2 LSB
AD7545TD	-55°C to +125°C	Ceramic	±1 LSB
AD7545UD	-55°C to +125°C	Ceramic	±½ LSB
AD7545GUD	-55°C to +125°C	Ceramic	±½ LSB
AD7545SQ	-55°C to +125°C	CERDIP**	±2 LSB
AD7545TQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7545UQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7545GUQ	-55°C to +125°C	CERDIP**	±½ LSB

** All devices—20 lead packages*

***Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration



CMOS 12-Bit Buffered Multiplying DAC

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise stated.)

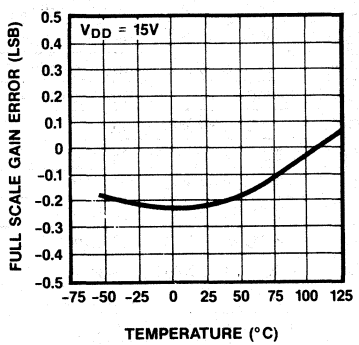
V_{DD} to DGND ..... -0.3 to +17V
Digital Input Voltage to DGND ..... -0.3 to V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
V_{OUT1} to DGND ..... -0.3 to V_{DD}
AGND to DGND ..... -0.3 to V_{DD}
Power dissipation to +75°C (any package) 450mW
Derate above 75°C by ..... 6mW/°C

Operating Temperature Ranges
J, K, L, GL ..... 0°C to +70°C
A, B, C, GC ..... -25°C to +85°C
S, T, U, GU ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

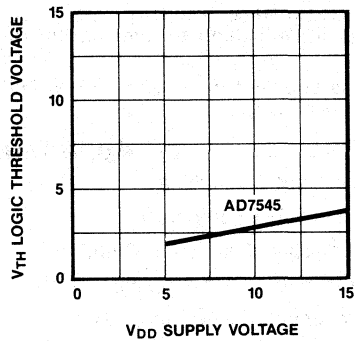
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

Typical Operating Characteristics

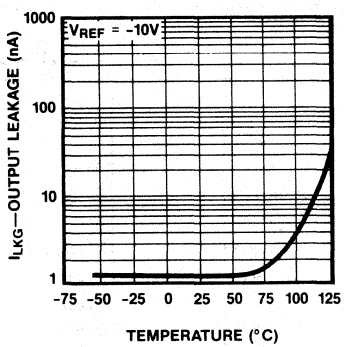
FULL-SCALE GAIN ERROR vs TEMPERATURE



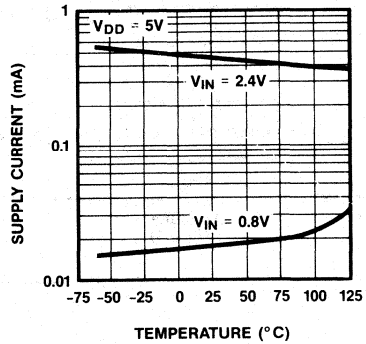
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



OUTPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N					12	Bits
Relative Accuracy	INL		J,A,S K,B,T L,C,U GL,GC,GU			±2 ±1 ±1/2 ±1/2	LSB LSB LSB LSB
Differential Non-Linearity	DNL	10-bit Monotonic 12-bit Monotonic 12-bit Monotonic 12-bit Monotonic	J,A,S K,B,T L,C,U GL,GC,GU			±4 ±1 ±1 ±1	LSB LSB LSB LSB
Gain Error (Note 1)	FSE		J,A,S K,B,T			±20 ±10	LSB LSB
			L,C,U T_A = +25°C Over Temp.			±5 ±6	LSB LSB
			GL,GC,GU T_A = +25°C Over Temp.			±1 ±2	LSB LSB
Gain Tempco ΔGain/ΔTemp. (Note 2)	TCFS				±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 2)	PSR	ΔV_{DD} = ±5%	T_A = +25°C Over Temp.			0.015 0.03	%/% %/%
DYNAMIC PERFORMANCE							
Current Settling Time (Note 2)	t_S	To ±1/2 LSB. OUT1 Load is 100ohms. $\overline{CS}$ = 0V. DAC output measured from falling edge of $\overline{WR}$.				2	μs
Propagation Delay (Note 2)	t_{PD}	From digital inputs, DB11-DB0, change from V_{DD} to 0V or 0V to V_{DD}, to 90% of final analog output. OUT1 load is: R = 100ohms/C = 13pF.	T_A = +25°C			300	ns
Digital to Analog Glitch Impulse	Q	V_{REF} = AGND	T_A = +25°C		400		nV-s
AC Feedthrough at OUT1 (Note 3)	FTE	V_{REF} = ±10V, 10kHz sinewave, DB11-DB0 = 0V.			5		mVp-p
REFERENCE INPUT							
Input Resistance	R_{REF}	V_{REF} pin to AGND		7	11	25	kohms
Input Resistance Tempco	TCR				-300		ppm/°C

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

CMOS 12-Bit Buffered Multiplying DAC

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG OUTPUTS								
OUT1 Capacitance (Note 2)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V					70	pF
		DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V					200	pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V, DB11-DB0 = 0V	J,K,L,GL	T_A = +25°C			10	nA
				Over Temp.			50	nA
			A,B,C,GC	T_A = +25°C			10	nA
				Over Temp.			50	nA
			S,T,U,GU	T_A = +25°C			10	nA
				Over Temp.			200	nA
DIGITAL INPUTS								
Input High Voltage	V_{IH}				2.4			V
Input Low Voltage	V_{IL}						0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}		T_A = +25°C		±0.001	±1	μA
				Over Temp.			±10	μA
Input Capacitance (Note 2)	C_{IN}	V_{IN} = 0V; DB11-DB0					5	pF
		V_{IN} = 0V; $\overline{WR}$, $\overline{CS}$					20	pF
SWITCHING CHARACTERISTICS (Notes 4, 5)								
Chip Select to Write Setup Time	t_{CS}			T_A = +25°C	280	200		ns
				Over Temp.	380	270		ns
Chip Select to Write Hold Time	t_{CH}				0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$		T_A = +25°C	250	175		ns
				Over Temp.	400	280		ns
Data Setup Time	t_{DS}			T_A = +25°C	140	100		ns
				Over Temp.	210	150		ns
Data Hold Time	t_{DH}				10			ns
POWER SUPPLY								
Supply Current	I_{DD}	All digital inputs: V_{IL} or V_{IH}					2	mA
		: 0V or V_{DD},		T_A = +25°C		10	100	μA
		: 0V or V_{DD}		Over Temp.		10	500	μA

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N						12	Bits
Relative Accuracy	INL		J,A,S K,B,T L,C,U GL,GC,GU				±2 ±1 ±1/2 ±1/2	LSB LSB LSB LSB
Differential Non-Linearity	DNL	10-bit Monotonic 12-bit Monotonic 12-bit Monotonic 12-bit Monotonic	J,A,S K,B,T L,C,U GL,GC,GU				±4 ±1 ±1 ±1	LSB LSB LSB LSB
Gain Error (Note 1)	FSE		J,A,S K,B,T L,C,U				±25 ±15 ±10	LSB LSB LSB
			GL,GC,GU	T_A = +25°C Over Temp.			±6 ±7	LSB LSB
Gain Tempco ΔGain/ΔTemp. (Note 2)	TCFS					±2	±10	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 2)	PSR	ΔV_{DD} = ±5%		T_A = +25°C Over Temp.			0.01 0.02	%/% %/%
DYNAMIC PERFORMANCE								
Current Settling Time (Note 2)	t_S	To ±1/2 LSB OUT1 Load is 100ohms. $\overline{CS}$ = 0V. DAC output measured from falling edge of $\overline{WR}$.					2	μs
Propagation Delay (Note 2)	t_{PD}	From digital inputs, DB11-DB0, change from V_{DD} to 0V or 0V to V_{DD}, to 90% of final analog output. OUT1 Load is: R = 100ohms/C = 13pF.		T_A = +25°C			250	ns
Digital to Analog Glitch Impulse	Q	V_{REF} = AGND		T_A = +25°C		250		nV-s
AC Feedthrough at OUT1 (Note 3)	FTE	V_{REF} = ±10V, 10kHz sinewave, DB11-DB0 = 0V.				5		mVp-p
REFERENCE INPUT								
Input Resistance	R_{REF}	V_{REF} pin to AGND			7	11	25	kohms
Input Resistance Tempco	TCR					-300		ppm/°C
ANALOG OUTPUTS								
OUT1 Capacitance (Note 2)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V					70 200	pF pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = 0V	J,K,L,GL	T_A = +25°C Over Temp.			10 50	nA nA
			A,B,C,GC	T_A = +25°C Over Temp.			10 50	nA nA
			S,T,U,GU	T_A = +25°C Over Temp.			10 200	nA nA
DIGITAL INPUTS								
Input High Voltage	V_{IH}				13.5			V
Input Low Voltage	V_{IL}						1.5	V

CMOS 12-Bit Buffered Multiplying DAC

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (Continued)							
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C Over Temp.		±0.001	±1 ±10	µA µA
Input Capacitance (Note 2)	C_{IN}	V_{IN} = 0V; DB11-DB0 V_{IN} = 0V; $\overline{WR}$, $\overline{CS}$				5 20	pF pF
SWITCHING CHARACTERISTICS (Notes 4, 5)							
Chip Select to Write Setup Time	t_{CS}		T_A = +25°C Over Temp.	180 200	120 150		ns ns
Chip Select to Write Hold Time	t_{CH}			0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	T_A = +25°C Over Temp.	160 240	100 170		ns ns
Data Setup Time	t_{DS}		T_A = +25°C Over Temp.	90 120	60 80		ns ns
Data Hold Time	t_{DH}			10			ns
POWER SUPPLY							
Supply Current	I_{DD}	All digital inputs: V_{IL} or V_{IH} : 0V or V_{DD}, : 0V or V_{DD}	T_A = +25°C Over Temp.		10 10	2 100 500	mA µA µA

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

Detailed Description

D/A Converter

The basic AD7545 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or AGND depending on the status of each input bit. Although the current at OUT1 and AGND will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF}.

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 3). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The I_{OUT1} pin output capacitance, C_{OUT1}, is code dependent and is typically 70pF to 200pF, with all switches to AGND and I_{OUT1}, respectively.

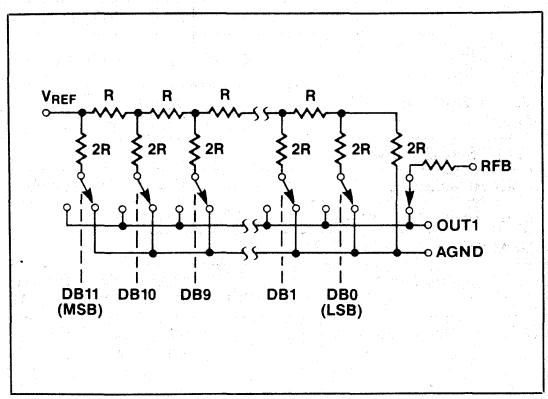


Figure 1. Simplified D/A Circuit of AD7545

Digital Circuit

The digital circuit for one bit is shown in Figure 2. The digital CONTROL signal is HIGH when $\overline{WR}$ and $\overline{CS}$ are both low. When $\overline{WR}$ and $\overline{CS}$ are tied low, the digital input directly controls the D/A switches.

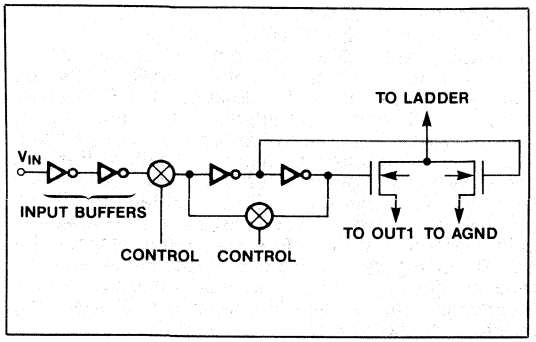
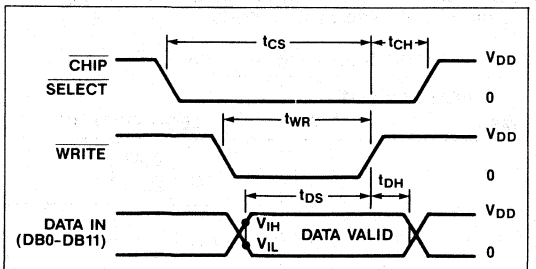


Figure 2. Digital Input Structure

The input buffer inverters act as a level shifter converting TTL levels into CMOS logic levels. These input buffers are CMOS/TTL compatible (0.8V and 2.4V) at V_{DD} = +5V. The AD7545 also works with V_{DD} = +15V where the input buffers are CMOS compatible (1.5V and 13.5V) only. With the digital input voltages at 1V to 6V the input buffers work in their linear regions drawing current from the power supply. Therefore to minimize high supply currents the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and DGND) as possible.

All digital inputs are ruggedized against electrostatic-discharge (ESD) sensitivity and can typically withstand ESD voltages of over 6kV.



MODE SELECTION

WRITE MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.

HOLD MODE:
Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

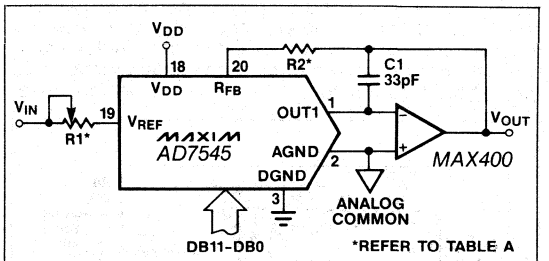
NOTES:

V_{DD} = +5V, $t_r = t_f$ = 20ns
V_{DD} = +15V, $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7545 is shown in Figure 3. This circuit is used for unipolar binary operation or two-quadrant multiplication. The



TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/ GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

TABLE A. RECOMMENDED TRIM RESISTOR VALUES vs. GRADES FOR V_{DD} = +5V

Figure 3. Unipolar Binary Operation

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0

code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, V_{REF}.

In many applications the gain adjustment will not be necessary, especially when using the "G" suffix parts with guaranteed maximum ±1 LSB gain errors. In those cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 3 can be omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

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The capacitor C1 provides phase compensation and helps reduce the overshoot and ringing when using fast amplifiers at the output of the DACs.

Bipolar Operation

With the circuit configuration shown in Figure 4, the AD7545 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors, R3, R4 and R5 are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature characteristics, and they should match to 0.01% for 12-bit performance.

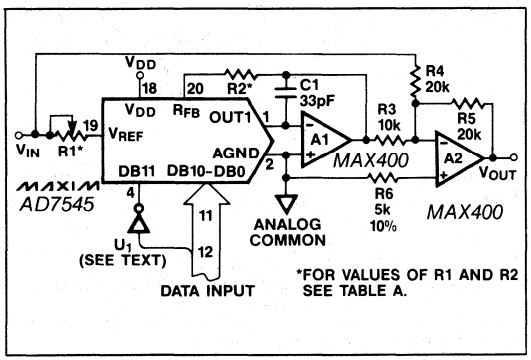


Figure 4. Bipolar Operation (2's Complement Code)

Table 2. 2's Complement Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{2048}\right)$

The code table for the output, which is 2's complement is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude. The U1 inverter on the MSB line converts the 2's complement input code to offset-binary code. If this inversion is done in software using an exclusive-OR instruction or the input code is in offset binary, the U1 inverter can be omitted. Table 3 shows the code relationships to output voltage for the offset binary operation.

To adjust the circuit with offset binary code, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using the "G" suffix parts with guaranteed maximum ±1 LSB gain errors. In those cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However,if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

(Voltage Mode) Single Supply

The AD7545 can be conveniently used in single supply (voltage mode) operation with OUT1 and AGND biased at any voltage between DGND and V_{DD}. This is possible since the ladder termination resistor is connected to AGND. OUT1 and AGND must not be allowed to go 0.3V lower or higher than the DGND or V_{DD}, respectively. Otherwise, internal diodes would turn on and a heavy current flow from the supply, possibly destroying the device.

Figure 5 shows the AD7545 connected as a voltage output DAC. OUT1 is connected to the reference input and AGND is grounded. V_{REF} pin, now the DAC output, is a voltage source with a constant impedance equal to the reference input resistance (typically 11kohms). This output should be buffered with an op-amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

Table 3. Offset Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

The input impedance of the reference input (OUT1) for this mode is code dependent, and the response time of the circuit depends on the behaviour of the reference source with changing load conditions.

Two advantages of the voltage mode operation are

single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (the voltage at OUT1) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded linearity and differential nonlinearity (DNL). Figures 6 and 7 show the typical dependence of DNL on supply voltage, V_{DD}, and the reference voltage, V_{REF}. If the DAC is offset from DGND by biasing OUT1 and AGND at a voltage above DGND, this will effect DNL and its effect will be the same as reducing V_{DD} by the amount of the offset.

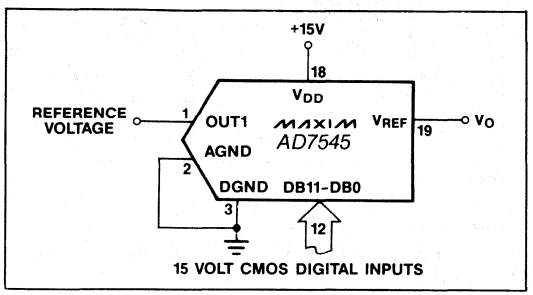


Figure 5. Single Supply Operating Using Voltage Switching Mode

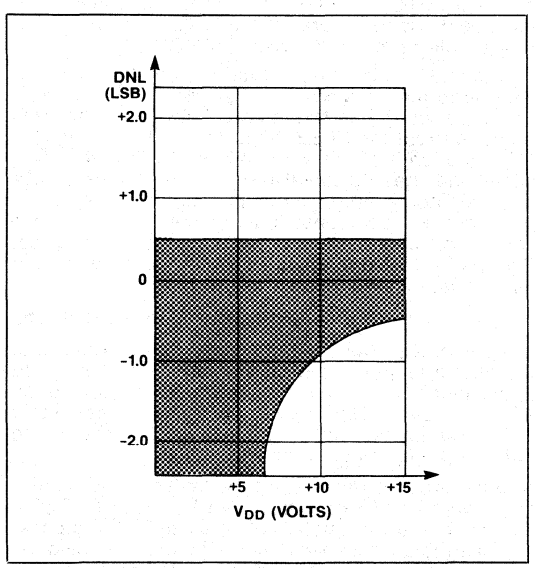


Figure 6. Differential Nonlinearity vs. V_{DD} for Figure 4 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode. For example, Figure 8 shows the 2's complement bipolar circuit of Figure 4 modified to work with an output range of +2V to +8V around an offset ground potential of +5V from a single supply, V_{DD}, of +10V to 15V. The REF02 reference is used to bias the AGND at +5V. The R1 and R2 resistors form a voltage divider together

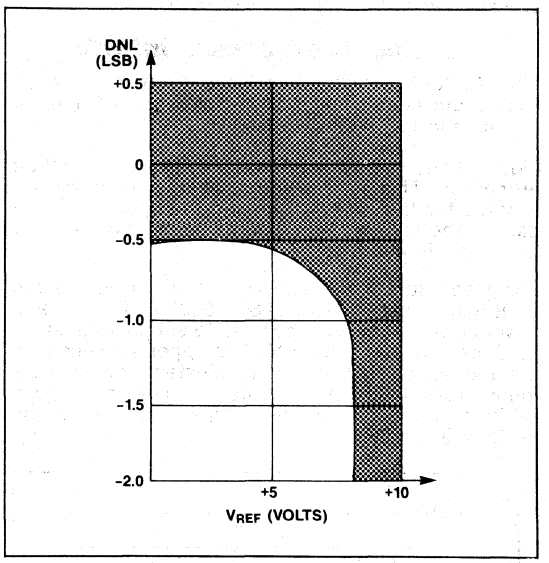


Figure 7. Differential Nonlinearity vs. Reference Voltage for Figure 4 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

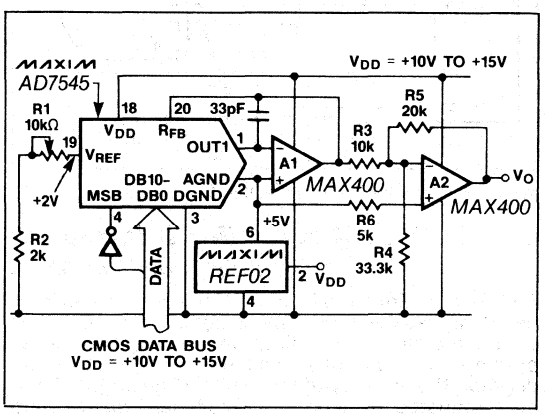


Figure 8. Single Supply "Bipolar" 2's Complement D/A Converter

CMOS 12-Bit Buffered Multiplying DAC

with the DAC reference input resistor, supplying the DAC with +2V input voltage. If the application requires a wide temperature range, the +2V should be generated with an op-amp to avoid drifts due to tempco matching of the DAC resistors to the external resistors. Output voltage ranges can be produced by changing R4 to change the offset, and (R1 + R2) to change the gain (slope) of the DAC transfer function. To ensure good linearity, the supply voltage, V_{DD}, must be kept at least +5V above the OUT1 voltage.

Microprocessor Interfacing

The AD7545 directly interfaces to 8- and 16-bit microprocessors using standard WR and $\overline{CS}$ control signals and its 12-bit data latch.

Figure 9 shows a typical interface circuit for an 8-bit processor. This application uses two memory addresses for the lower 8 bits and the upper 4 bits of data to the DAC. A 4-bit external latch is required to facilitate the interface.

For processors with 16-bit wide address busses and 8-bit data busses, such as 6800, 8080 and Z80, the 12 lower address lines can be used to supply data to the DAC, as shown in Figure 10. The upper 4 bits contain the address of the DAC that is selected. This arrangement takes 4k bytes of address locations for each DAC and the data is written with a single instruction cycle into the DAC.

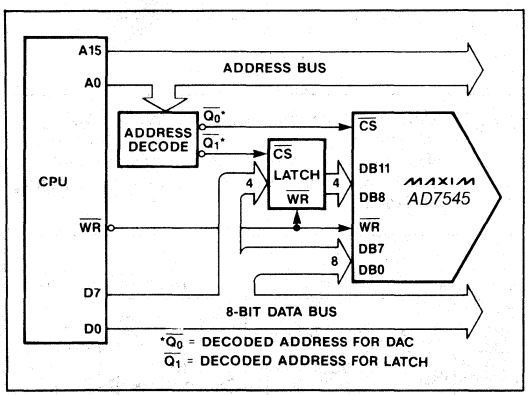


Figure 9. 8-Bit Processor to AD7545 Interface

Application Information

Output Amplifier Offset

For best linearity, OUT1 and AGND should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R_O)$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code and varies from approximately 11kohms to 33kohms. The error voltage range is then typically 4/3 V_{OS} to 2 V_{OS}, a change of 2/3 V_{OS}. An amplifier with 3mV of offset will therefore degrade the

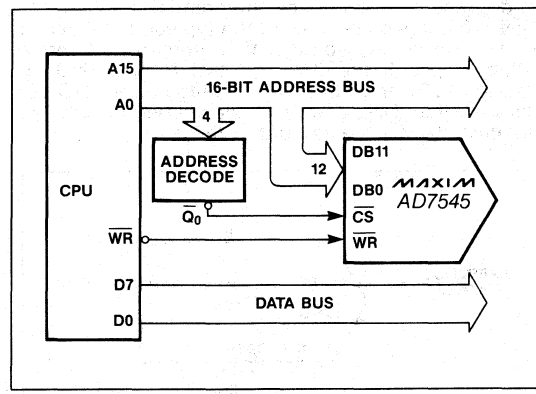


Figure 10. Connecting the AD7545 to 8-Bit Processors via the Address Bus

linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 LSBs.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor". This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to OUT1. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs V_{REF} and OUT1 pins.

CMOS 12-Bit Buffered Multiplying DAC

The DAC output follows the digital inputs when the WR and CS pins are low. In those systems where the data is not valid for the full period where WR is low, invalid outputs and voltage glitches can appear at the DAC output. Adjusting the timing of the WR signal so that it is low only when data is valid eliminates this problem.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance C_{OUT1} and the internal feedback resistor, R_{FB}. Its value depends on the type of op-amp used but typically ranges from 10pF to 3pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at OUT1 as small as possible.

Grounding and Bypassing

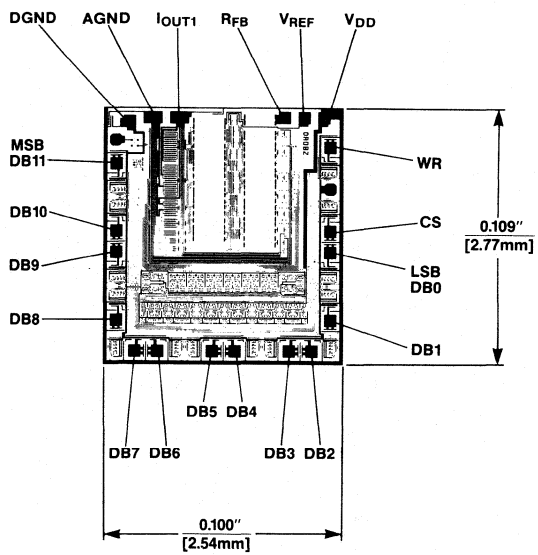
Since OUT1, AGND and noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2ohms) connection. The current at OUT1 and AGND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected as close to the DAC V_{DD} and DGND pins as possible.

The AD7545 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or DGND when not used. It is also a good practice to connect active inputs to V_{DD} or DGND through high valued resistors (1Mohms) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

It is also recommended that two back-to-back diodes be connected between the DGND and AGND pins in those systems where these pins tie on the backplane.

Chip Topology



Voltage References

Voltage References

Part Number	Output Voltage	Temperature Coefficient (ppm/°C)	Initial Output Voltage Accuracy	Supply Voltage	Supply Current (Typ/Max mA)	Features	Page No.
MAX670	10V	3	±2.5mV	+15V	9/14	Kelvin sensing	3-1
MAX671	10V	1	±1.0mV	+15V	9/14	Kelvin sensing	3-1
MAX672	10V	5	±5.0mV	+13V to +40V	1/1.4	Precision/Low Cost	3-7
MAX673	5V	5	±2.5mV	+8V to +40V	1/1.4	Precision/Low Cost	3-7
AD580	2.5V	10	±10mV	+15V	0.75/1.0	+5V power	3-11
AD581	10V	5	±5mV	+15V	0.75/1.0	10mA Output	3-13
AD584	10V,7.5V, 5V,2.5V	5	±5mV	+15V	0.75/1.0	Programmable output voltage	3-19
AD2700	10V	3	±2.5mV	+15V	9/14	Precision	3-25
AD2710	10V	1	±1.0mV	+15V	9/14	Precision	3-25
AD2701	-10V	2	±2.5mV	-15V	9/14	Precision	3-25
ICL8069	1.23V	10 to 100	±25mV	—	50µA to 5mA	2 terminal bandgap	3-29
REF01E	10V	8.5	±30mV	+15V	1/1.4	Trim Input	3-31
REF01HP	10V	25	±50mV	+15V	1/1.4	Trim Input	3-31
REF02E	5V	8.5	±15mV	+15V	1/1.4	Temp Output	3-31
REF02HP	5V	8.5	±25mV	+15V	1/1.4	Temp Output	3-31

Voltage Reference Terminology

Kelvin Sensing: Also Four Terminal Sensing. A voltage sourcing technique where the connections that supply power to a load are separate from those that sense the voltage at the load. A precise voltage can then be supplied at high current since errors caused by wire resistance are eliminated.

Line Regulation: The output voltage change as a function of a specified change in input voltage. Specified in %/ΔV or µV/ΔV.

Load Regulation: The output voltage change as a function of a specified change in load current. Specified in µV/mA or Ω.

Long-Term Stability: The output voltage change with time at a specified temperature. Specified in ppm/1000hrs.

Temperature Coefficient: The average change in output voltage for a specified range of temperature. Specified in ppm/°C or mV/°C.

Turn-On Settling Time: The time required for the output to settle within specified limits from a cold start. Does not include thermal settling time which depends on external conditions.

Voltage Change with Temperature: The total deviation from the actual output at +25°C over the specified temperature range. Specified in mV or %.

Quiescent Current: The power supply current required to operate the reference under no-load conditions. Specified in mA or µA.

MAXIM

+10V Precision Kelvin Sensed References

General Description

The MAX670/671 are precision +10 volt reference sources with Kelvin connections on both output and ground, which offer superior load regulation and line regulation independent of the line impedance between the reference and load. The MAX670 has initial accuracy of 2.5mV with 3ppm/°C temperature coefficient and the MAX671 is specified with initial accuracy of 1.0mV and temperature coefficient of 1ppm/°C. Both devices are designed to upgrade existing sockets which employ the popular AD2700 and AD2710 series by connecting a few of the unused pins together to obtain improved performance. The MAX670/671 have two methods of fine trim adjustment, one which is an improved technique which will not disturb the output voltage temperature coefficient, and the other is compatible with the AD2700/2710. All parts are packaged in 14 lead ceramic side brazed DIP and include burn-in at +150°C.

Applications

Precision D/A and A/D Converters

Digital Voltmeters

Precision Test and Measurement System

Precision Calibrated Voltage Reference Standard

High Accuracy Transducers

Features

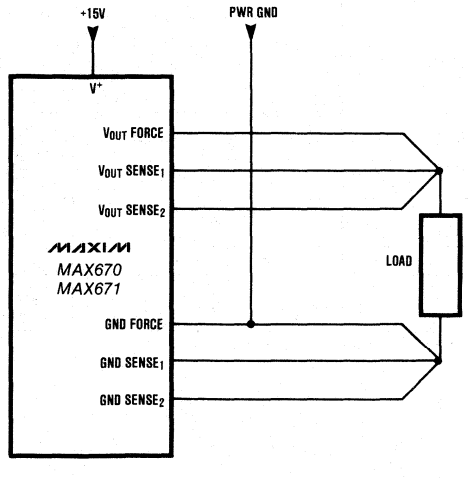
- **Superior Load Regulation: 10μV/mA Max.**
- **Superior Line Regulation: 50μV/V Max.**
- **Excellent Initial Accuracy: +10V ±1mV Max. (MAX671)**
- **Low Temperature Coefficient: 1ppm/°C Max. (MAX671)**
- **10mA Output Current**
- **High Current Capability with External Transistor**
- **Functionally Compatible with AD2700 and AD2710**

Ordering Information

PART	INIT. ACC.	*TEMP. COEFF.	TEMP. RANGE
MAX670CDD	2.5mV	3ppm/°C	0°C to +70°C
MAX670EDD	2.5mV	3ppm/°C	-40°C to +85°C
MAX670MDD	2.5mV	3ppm/°C	-55°C to +125°C
MAX671CDD	1.0mV	1ppm/°C	0°C to +70°C
MAX671EDD	1.0mV	1ppm/°C	-40°C to +85°C
MAX671MDD	1.0mV	1ppm/°C	-55°C to +125°C

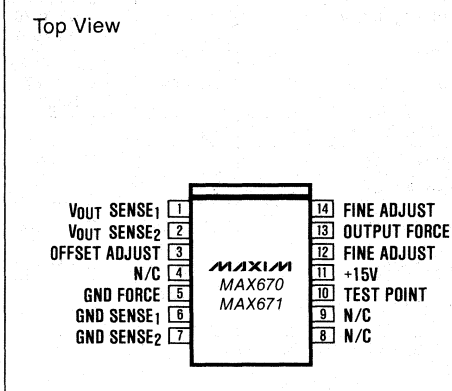
(All devices are packaged in a 14 lead ceramic side brazed DIP.)
**Restricted temperature range (See Electrical Characteristics).*

Typical Operating Circuit



+10V Precision Kelvin Sensed Reference

Pin Configuration



+10V Precision Kelvin Sensed References

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... +20V
Power Dissipation 400mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Short Circuit to GND ..... Continuous

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V, T_A = +25°C, R_L = 2kΩ, unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Initial Output Voltage	V_O	MAX670		9.9975	10.0000	10.0025	V
		MAX671		9.9990	10.0000	10.0010	
Output Voltage Drift (See Figures 12 and 13)	$\Delta V_O/\Delta T$	MAX670C	T_A to +70°C T_A to 0°C	-3 -5		+3 +3	ppm/°C
		MAX670E	T_A to +85°C T_A to -40°C	-3 -5		+3 +3	
		MAX670M	T_A to +85°C T_A to +125°C +85°C to +125°C T_A to -55°C	-3 -5 -10 -5		+3 +3 +3 +3	
		MAX671C	T_A to +70°C T_A to 0°C	-1 -5		+1 +1	
		MAX671E	T_A to +85°C T_A to -40°C	-1 -5		+1 +1	
		MAX671M	T_A to +85°C T_A to +125°C +85°C to +125°C T_A to -55°C	-1 -5 -10 -5		+1 +1 +1 +1	
Load Regulation	$\Delta V_O/\Delta I_O$	0mA to 10mA to GND MAX670 MAX671				 20 10	μV/mA
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 13.5V to 16.5V MAX670 MAX671				 100 50	μV/V
Input Voltage Range	V_{IN}			13.5		16.5	V
Supply Current	I_S	No Load			9	14	mA
Noise (Note 1)	e_N	0.1Hz to 10Hz			12	50	μV_{P-P}
Long Term Stability	$\Delta V_O(T)$	T_A = +55°C			50		ppm/1K hrs
Output Adjust Range	$\Delta V_{ADJ.}$	per Figure 10			20		mV
Output Adjust vs. TC	$\frac{\Delta V_O/\Delta T}{\Delta V_{ADJ.}}$	per Figure 10			0.4		ppm/°C/mV

Note 1: This parameter is sample tested to 10% LTPD, and is not used to calculate outgoing quality level.

+10V Precision Kelvin Sensed References

Theory of Operation

A temperature compensated zener diode is applied to the non-inverting input of an operational amplifier (Figure 1). The zener voltage is amplified and accurately laser trimmed to produce a precise 10.000V. The zener operating current is derived from the regulated output voltage, and actively laser trimmed for the lowest temperature coefficient at the output of the op amp.

The MAX670 and MAX671 each have three Kelvin connections for both output and ground which eliminates errors due to the I-R voltage drops from the resistance of the pins, sockets, and connecting wires. The FORCE pin output current varies as the load changes such that the voltage reflects changes due to I-R drops as well. V_{OUT} SENSE1 and GND SENSE1 are the gain resistors of the op amp that are used to maintain to a precise voltage the points at the load to which they are connected. The V_{OUT} SENSE2 and GND SENSE2 pins when connected in the circuit are constant current points but do not contribute errors from I-R drops as long as they are connected to the same points as V_{OUT} SENSE1 and GND SENSE1.

Applications Information

The Force and Sense lines should be connected together as close as possible to the load or reference input of the converter. The power supply ground must be connected either at the same ground point at the load or along the GND FORCE path.

The additional benefit of separate Force and Sense lines allows the use of an external buffer for increased output current while maintaining the specified output accuracy. There are several methods of buffering, the choice of which depends on the constraints of the application.

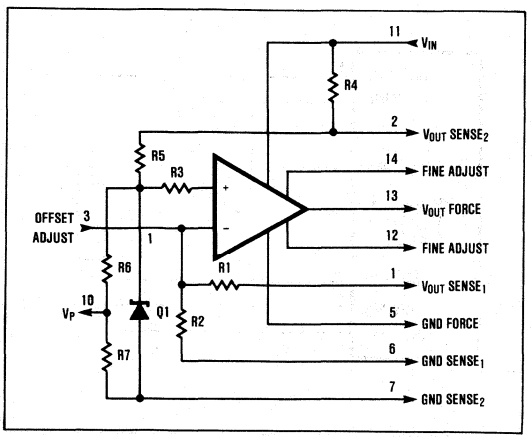


Figure 1. MAX670/671 Schematic Diagram

Emitter Follower

An NPN transistor can be used as a buffer for very low impedance output if only current sourcing (i.e. from Output to GND) is desired (Figure 2). It is advisable to place a small resistor in series with the base of the transistor to prevent oscillation unless the f_T is low. Since the Sense lines will keep the emitter at 10V, the base will rise up to about 10.7V due to the transistor Vbe. This limits the low end of the supply range, especially at cold temperatures where the Vbe of the transistor is the largest and the headroom of the internal op amp is lowest. The output of the internal op amp on the Force pin will change as much as necessary over temperature to maintain the Sense pins on the emitter at a constant voltage.

Similarly, a FET (Figure 3) can be used as a source follower. However, the V_T of a N-channel FET must be low, about 2V, so that the MAX670 output will

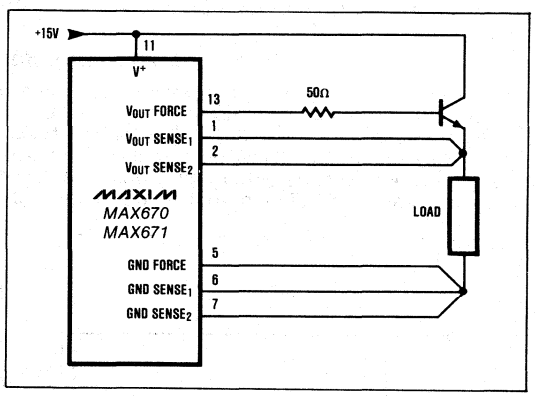


Figure 2. NPN Emitter Follower

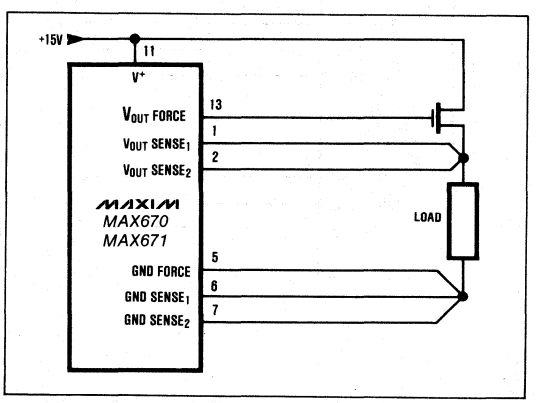


Figure 3. FET Source Follower

+10V Precision Kelvin Sensed References

have sufficient headroom. Alternatively, a P-channel FET, whose gate voltage will be more negative than the source would be more suitable because the op amp output voltage would be driven further into the middle of its output swing range.

If the load only requires the reference to sink current, a PNP transistor can be used as shown in Figure 4.

+12 Volt Operation

A few forward biased diodes in series with the base of the transistor in Figure 5 will drop the MAX670 output by as many Vbe's for more op amp headroom and therefore lower operating voltage. Over temperature, the MAX670 V_{OUT} FORCE will change as much as required due to the temperature coefficient of the Vbe's. One diode will best compensate the Vbe of the transistor so that the Force output will be close to 10V. However, two diodes will place the internal op amp output at about 9.3V to give enough headroom for 12V ±10% operation (i.e. 11.4V minimum).

External Buffer

A more simple, yet more costly method to increase the output current is by the use of an external buffer amplifier, such as a BUF-03, LH0002, or an LH0033 (Figure 6) for up to 100mA of output current. The Force output drives the buffer input, while the Sense lines maintain the buffer output to the initial +10V value, even if the offset drift is high. V_{OUT} SENSE2 can be connected to the input of the buffer if necessary, but there will be a small second order error over temperature as the offset drift slightly changes the reference zener operating current. Therefore it is always better to connect both SENSE lines together at the load.

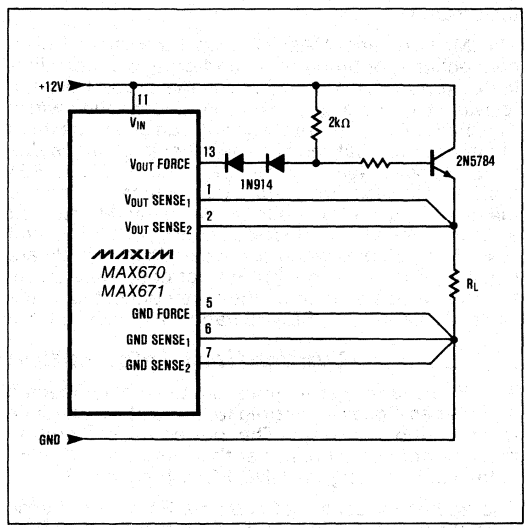


Figure 5. Application Circuit for 12V Operation, 120mA Output Current

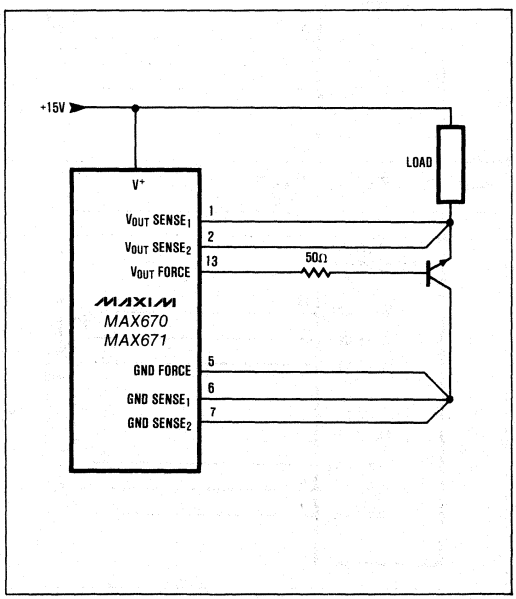


Figure 4. PNP Emitter Follower

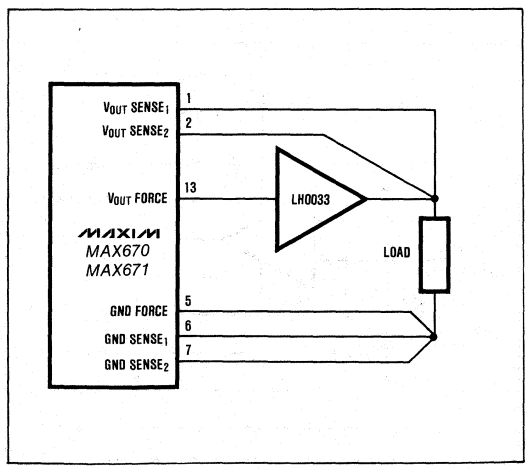


Figure 6. 100mA Output Current with Buffer Amplifier

+10V Precision Kelvin Sensed References

High Power Output

The specified accuracy of the MAX670 can be obtained even at currents of several amps using a Power Amplifier such as the LH0101 as a non-inverting buffer amplifier (Figure 7). By placing the amplifier inside the loop and sensing the output, the reference will have a 2A output capability keeping in mind the heat sink requirements of the LH0101.

High Speed Buffer

In some cases, the reference is required to drive a circuit that contains high speed transients or glitches which must settle back to a steady state value quickly. In this case a fast op amp can be used on the output, such as an HA-2525 or a BB3554 (Figure 7). The high bandwidth of these amplifiers enables them to settle quickly at the expense of higher noise bandwidth that may restrict their applications.

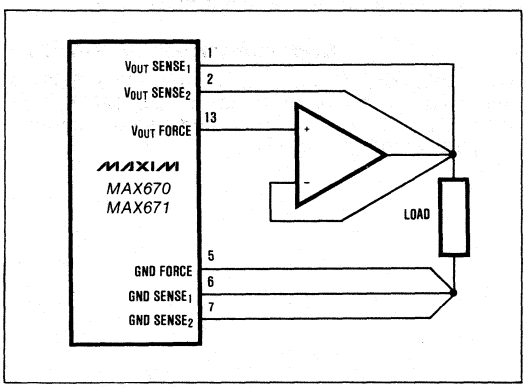


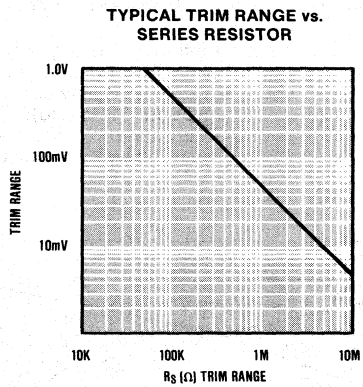
Figure 7. 2A Output Current Using LH0101 Power Amplifier or BB3554 FAST Op-Amp

Load Balancing

If the load current is known, and is constant, such as in the case of driving the reference input of numerous D/A converters, a pull up resistor (Figure 8) can be used to match the load current to ground with the MAX670 regulating the output voltage and supplying the error current up to 10mA. For this special case, the cost of an amplifier is eliminated and the circuit complexity is reduced.

Offset Adjust

The output voltage of the MAX670 and MAX671 can be adjusted in two ways. The Offset Adjust Input on pin 3 (Figure 9) has the unique advantage of changing the output voltage without disturbing the temperature coefficient. Also, a wide variety of trim range and resolution can be obtained by appropriate selection of the resistor in series with pin 3 as shown in graph below.



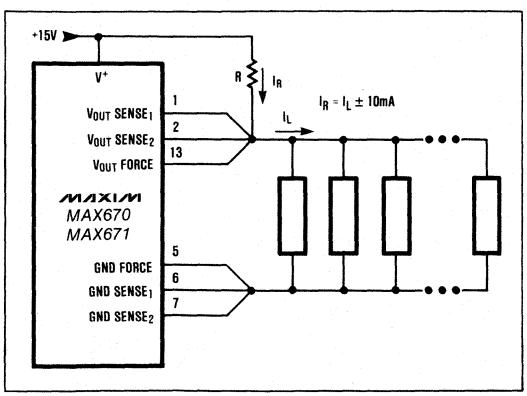


Figure 8. Pull Up Resistor Load Balancing

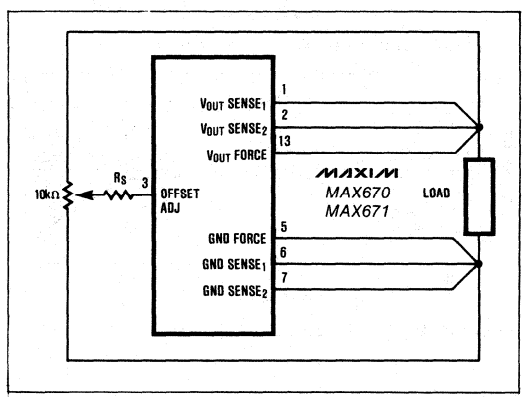


Figure 9. MAX670/671 Improved TC Independent Trim Adjustment

+10V Precision Kelvin Sensed References

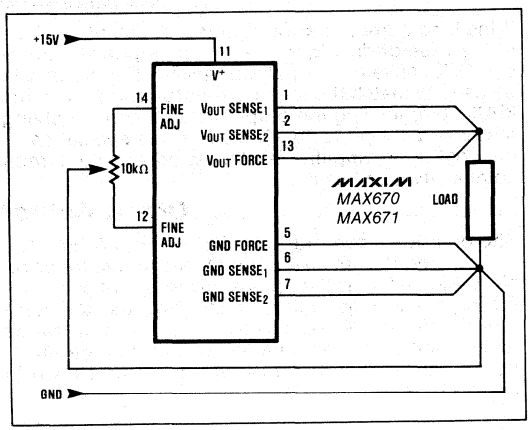


Figure 10. AD2700/2710 Compatible Trim Adjustment

The other adjustment method is designed to be compatible with the AD2700/AD2710 series of references. A potentiometer is connected between pins 12 and 14 with the wiper to ground (Figure 10), but this method affects the output temperature coefficient by approximately 0.4ppm/°C per millivolt of adjustment.

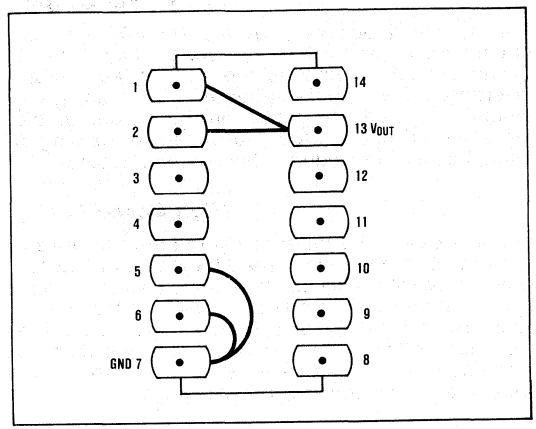


Figure 11. Using MAX670/671 in AD2700/2710 Sockets

Upgrading AD2700/AD2710

Any existing socket containing an AD2700 or AD2710 can be easily adapted to the MAX670 or MAX671 by shorting pin 13 to pins 1 and 2, and also shorting pin 7 to pins 5 and 6 (Figure 11).

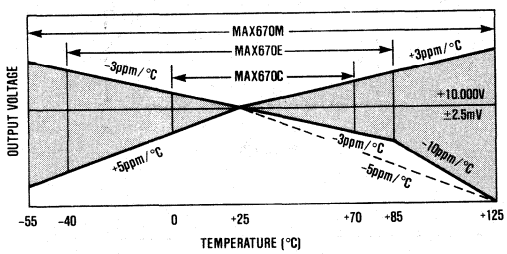


Figure 12. MAX670 Temperature Coefficient

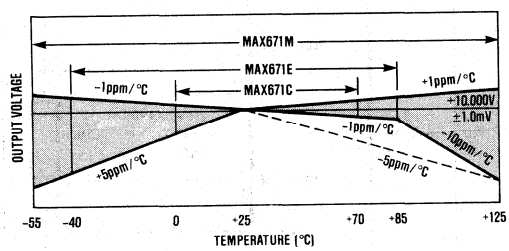


Figure 13. MAX671 Temperature Coefficient

MAXIM

+5V, +10V Precision Voltage References

General Description

The MAX672 and MAX673 are precision voltages references that are pretrimmed to within ±.05% of 10V and 5V respectively. Both references feature excellent temperature stability (as low as 5.0 ppm/°C worst case), low current drain and low noise. The MAX673 also provides a TEMP pin whose output voltage varies linearly with temperature, making this device suitable for a wide variety of temperature sensing and control applications. Both devices are available from Maxim in the space-saving Small Outline package, as well as the standard 8 pin TO-99 and MINI-DIP packages.

Applications

A to D Converters

D to A Converters

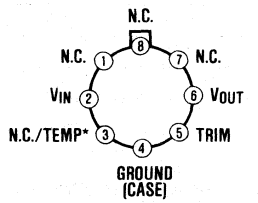
Digital Voltmeters

Voltage Regulators

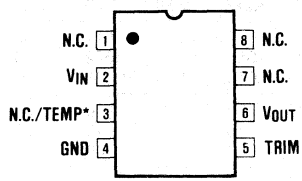
Threshold Detectors

Pin Configuration

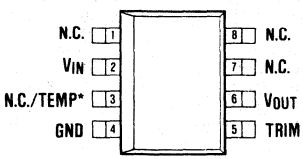
Top View



8 Lead TO-99 Metal Can



8 Lead DIP



8 Lead Small Outline

***NOTE:** Pin 3 is N.C. (No Connection) on MAX672, TEMP Output on MAX673

Features

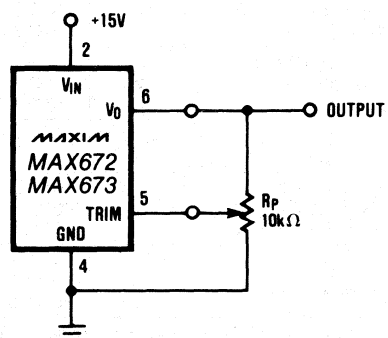
- **Pretrimmed to +5V, +10V ±0.05%**
- **Excellent Temperature Stability 2 ppm/°C**
- **Low Noise: 10μV_{p-p} (MAX673)**
- **Low Supply Current: 1.4mA Max**
- **Short Circuit Proof**
- **Load Regulation 0.001%/mA**
- **Improved REF01 and REF02**

Ordering Information

PART	V_{OUT} @ 25°C	PACKAGE*
TEMP RANGE: 0°C TO +70°C		
MAX672CTV	10V ± 5mV	TO-99
MAX672CPA	10V ± 5mV	Plastic Dip
MAX672CSA	10V ± 5mV	Small Outline
TEMP RANGE: -40°C TO +85°C		
MAX672ETV	10V ± 5mV	TO-99
MAX672EJA	10V ± 5mV	CERDIP
MAX672EPA	10V ± 5mV	Plastic Dip
MAX672ESA	10V ± 5mV	Small Outline
TEMP RANGE: -55°C TO +125°C		
MAX672MTV	10V ± 5mV	TO-99
MAX672MJA	10V ± 5mV	CERDIP

(Ordering information continued on page 4.)

Typical Operating Circuit



Reference with Trimmed Output

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Power Dissipation
TO99 (TV) (Derate at 7.1mW/°C above +80°C) 500mW
CERDIP (J) (Derate at 6.7mW/°C above +75°C) 500mW
Plastic DIP (P) (Derate at 5.6mW/°C above +36°C) 500mW
Small Outline (S) (Derate at 5.0mW/°C above +55°C) ... 300mW
Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
MAX672M/MAX673M ..... -55°C to +125°C
MAX672E/MAX673E ..... -40°C to +85°C
MAX672C/MAX673C ..... 0°C to +70°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
DICE Junction Temperature (T_J) .. -65°C to +150°C
Output Short-Circuit Duration
(to Ground or V_{IN}) ..... Indefinite

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX672			MAX673			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	9.995	10.000	10.005	4.9975	5.000	5.0025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3	±6		±3	±6		%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)		10	15		10	15	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 13V to 33V (MAX672) V_{IN} = 8V to 33V (MAX673)		0.006	0.010		0.006	0.010	%/V
Load Regulation (Note 1)		I_L = 0 to 10mA		0.001	0.002		0.001	0.002	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value		5			5		μs
Quiescent Supply Current	I_{SY}	No Load		1.0	1.4		1.0	1.4	mA
Sink Current	I_S		-0.3	-0.5		-0.3	-0.5		mA
Short-Circuit Current	I_{SC}	V_O = 0		30			30		mA
Temperature Voltage Output	V_T	(Note 2)					630		mV

ELECTRICAL CHARACTERISTICS (V_{IN} = +15V, $T_{MIN} \le T_A \le T_{MAX}$, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX672			MAX673			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 3, 4)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		.014 .022 .036	.035 .055 .090		.014 .022 .036	.035 .055 .090	%
Output Voltage Change with Temperature (Notes 3, 4)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		1.40 2.20 3.60	3.50 5.50 9.00		0.70 1.10 1.80	1.75 2.75 4.50	mV
Output Voltage Temperature Coefficient	TCV_O	(Note 5)		2	5		2	5	ppm/°C
Line Regulation (Note 1) (V_{IN} = 13V to 33V) (MAX672) (V_{IN} = 8V to 33V) (MAX673)		0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		0.007 0.008 0.009	0.012 0.013 0.015		0.007 0.008 0.009	0.012 0.013 0.015	%/V %/V
Load Regulation (I_L = 0 to 8mA) (Note 1)		0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		0.001 0.001 0.001	0.002 0.002 0.002		0.001 0.001 0.001	0.002 0.002 0.002	%/mA

Note 1: Line and Load Regulation specifications include the effect of self heating.
Note 2: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
Note 3: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V (MAX672) or 5V (MAX673).
Note 4: ΔV_{OT} specification applies trimmed to +10.000V/5.000V or untrimmed.
Note 5: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 6: Sample tested.

Output Adjustment

The MAX672(MAX673) trim terminal can be used to adjust the voltage over a 10V(5V) ± 300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V(5V), including 10.240V for binary applications (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7ppm/°C for 100mV of output adjustment.

Temperature Voltage Output

The MAX673 provides a temperature dependent output voltage on the TEMP pin. This voltage is proportional to the absolute temperature, and has a scale factor of approximately 2.1mV/°C (Figure 2).

Output Voltage = 2.1(T + 273)mV
where T = Temperature in °C

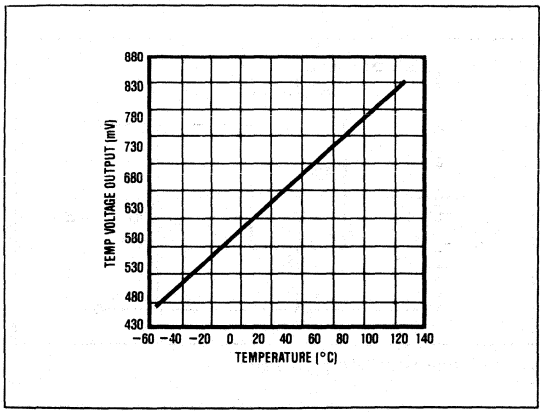
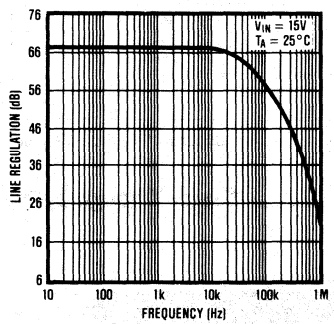


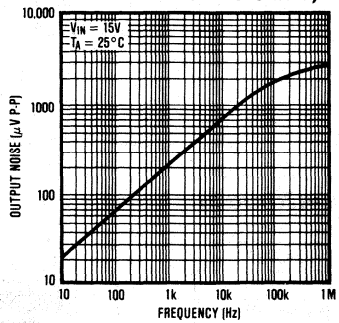
Figure 2. MAX673 Temperature Voltage Output vs. Temperature.

Typical Operating Characteristics

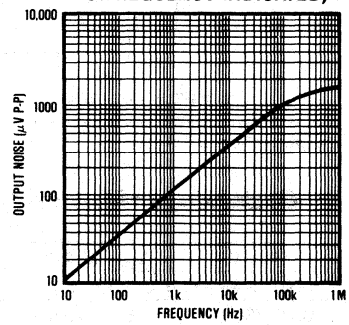
LINE REGULATION vs FREQUENCY



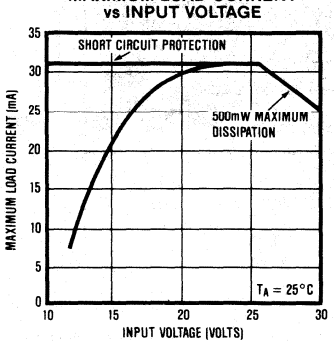
MAX672 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



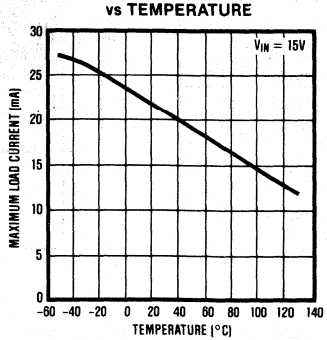
MAX673 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



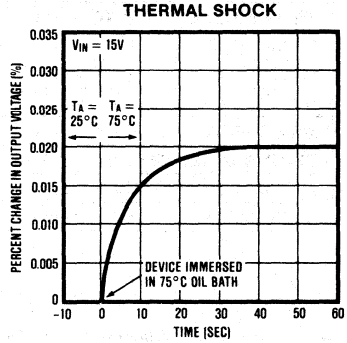
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE



OUTPUT CHANGE DUE TO THERMAL SHOCK



+5V, +10V Precision Voltage References

Typical Applications

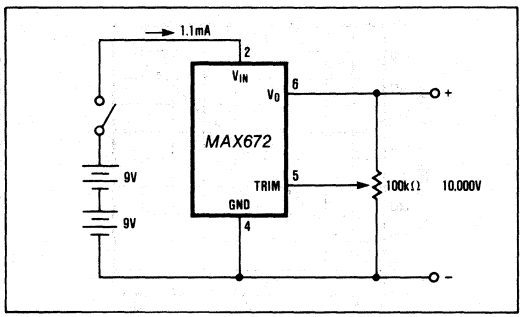


Figure 3. Precision Calibration Standard

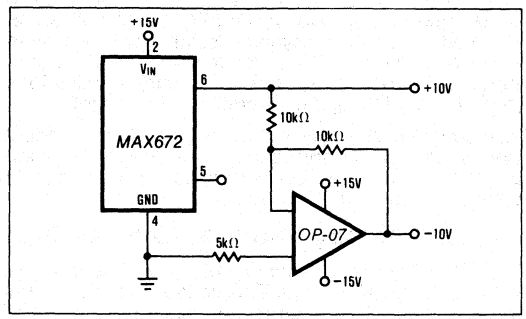


Figure 4. ±10V Reference

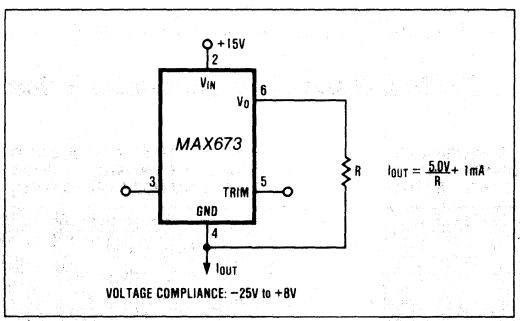


Figure 5. Current Source

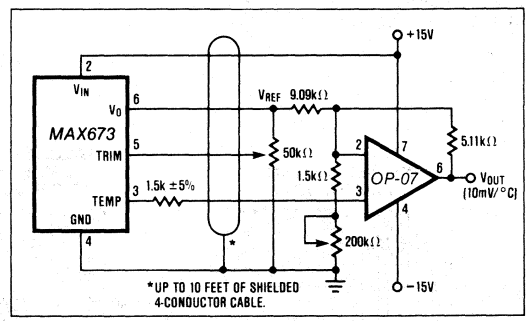
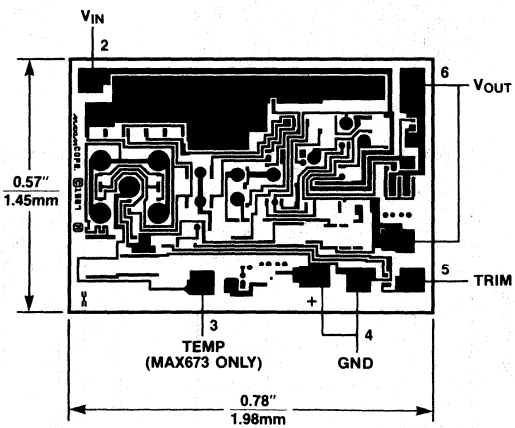


Figure 6. Precision Temperature Transducer with Remote Sensor

Ordering Information (continued)

PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C		
MAX673CTV	5V ± 2.5mV	TO-99
MAX673CPA	5V ± 2.5mV	Plastic Dip
MAX673CSA	5V ± 2.5mV	Small Outline
TEMP RANGE: -40°C TO +85°C		
MAX673ETV	5V ± 2.5mV	TO-99
MAX673EJA	5V ± 2.5mV	Hermetic Dip
MAX673EPA	5V ± 2.5mV	Plastic Dip
MAX673ESA	5V ± 2.5mV	Small Outline
TEMP RANGE: -55°C TO +125°C		
MAX673MTV	5V ± 2.5mV	TO-99
MAX673MJA	5V ± 2.5mV	Hermetic Dip

Chip Topography



High Precision +2.5 Volt Reference

General Description

The AD580 is a high performance three-terminal voltage reference which provides a stable +2.5V source for 8, 10, and 12-bit data converters and analog functions. A temperature compensated internal bandgap operates from +4.5V to +30V and consumes only 1.5mA.

The reference can be connected directly to a number of CMOS A-to-D and D-to-A converters and is especially convenient in +5V powered systems. An inital untrimmed accuracy of 0.4% and temperature stability of 10ppm/°C allow adjustment-free designs in many precision applications.

Available packages include TO-52 metal cans for commercial and military temperature grades, as well as 8 lead small outline for commercial grade devices.

Applications

CMOS Data Conversion
Digital Panel Meters
Portable Instrumentation
Remote Measurement Systems
Logic Powered Analog Systems

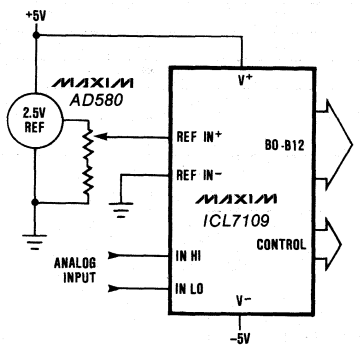
Features

- **2.500V ±0.4% Accuracy (AD580L/M)**
- **10ppm/°C Temperature Stability (AD580M)**
- **No Adjustments**
- **250μV Long Term Stability**
- **1.5mA Quiescent Current**
- **+4.5V to +30V Operation**

Ordering Information

PART	TEMP. RANGE	PACKAGE	TOLERANCE
AD580JH	0°C to +70°C	TO-52 Can	±75mV
AD580KH	0°C to +70°C	TO-52 Can	±25mV
AD580LH	0°C to +70°C	TO-52 Can	±10mV
AD580MH	0°C to +70°C	TO-52 Can	±10mV
AD580JCSA	0°C to +70°C	8 Lead S.O.	±75mV
AD580KCSA	0°C to +70°C	8 Lead S.O.	±25mV
AD580LCSA	0°C to +70°C	8 Lead S.O.	±10mV
AD580MCSA	0°C to +70°C	8 Lead S.O.	±10mV
AD580SH	-55°C to +125°C	TO-52 Can	±25mV
AD580TH	-55°C to +125°C	TO-52 Can	±10mV
AD580UH	-55°C to +125°C	TO-52 Can	±10mV

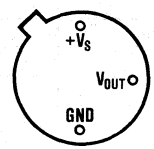
Typical Application



Reference for 12-Bit A/D Converter

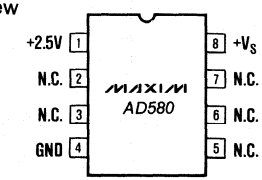
Pin Configurations

Bottom View



TO-52

Top View



8 Lead Small Outline

High Precision +2.5 Volt Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to GND ..... -0.3V, +40V
Power Dissipation
  TO-52 Metal Can (Derate 2.8mW/°C above +25°C) ... 350mW
  Small Outline (Derate 5.3mW/°C above +75°C) 400mW
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
  Commercial (J, K, L, M) ..... 0°C to +70°C
  Military (S, T, U) ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +175°C

Lead Temperature (Soldering 10sec) ..... +300°C
Junction Temperature (T_j) ..... -55°C to +150°C
Thermal Resistance, Junction to Ambient
  TO-52 Metal Can ..... 360°C/W
  Small Outline Package ..... 170°C/W
Junction to Case
  TO-52 Metal Can ..... 100°C/W
  Small Outline Package ..... 55°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Tolerance		I_L = 0mA;	AD580J/S AD580K/T AD580L/M/U			±75 ±25 ±10	mV
Output Voltage Change with Temperature, (Temperature Coefficient)		T_A = 0°C to +70°C;	AD580J AD580K AD580L AD580M			15 (85) 7 (40) 4.3 (25) 1.75 (10)	±mV (ppm/°C)
		T_A = -55°C to +125°C;	AD580S AD580T AD580U			25 (55) 11 (25) 4.5 (10)	
Line Regulation		I_L = 0mA, +4.5V < V_{IN} < +7V;	AD580J/S AD580K AD580L/M/T/U		0.3 0.3	3 2 1	mV
		I_L = 0mA, +7V < V_{IN} < +30V;	AD580J/S AD580K AD580L/M/T/U		1.5 1.5	6 4 2	
Load Regulation		I_L = 0mA to 10mA				10	mV
Quiescent Supply Current	I_Q	I_L = 0mA			1.0	1.5	mA
Noise	e_{NP-P}	0.1Hz to 10Hz			60		μV_{P-P}
Stability Long Term Per Month					 250 25		μV

Note 1: Absolute Maximum power dissipation must not be exceeded.

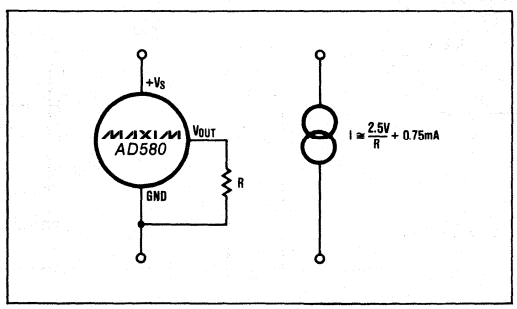


Figure 1. Two-Component Precision Current Limiter

MAXIM
High Precision 10 Volt Reference

General Description

Maxim's AD581 is a three-terminal, temperature compensated, band-gap voltage reference which provides a precise 10.00V output from an unregulated input of 12.5V to 30V. Laser trimming is used to minimize initial error and temperature drift, to as low as 5mV and 5ppm/° C with the AD581L.

No external components are needed to acheive full accuracy over the operating temperature range. Total supply current to the device, including the internal output buffer amplifier, is typically 750μA.

The AD581 is designed for use with 8 to 14 bit A/D and D/A converters as well as data acquisition systems. The reference is available in a 3 pin TO-5 metal can and 8 lead small outline surface mount package.

Applications

CMOS DAC Reference
A/D Converter Reference
Measurement Instrumentation
Threshold Detectors
Precision Analog Systems

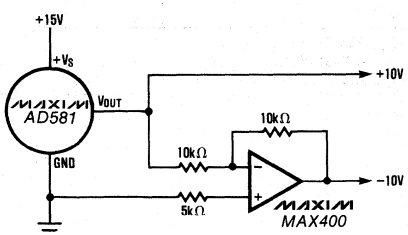
Features

- ±5mV Tolerance (AD581L)
- Low Tempco — 5ppm/° C Max. (AD581L)
- No External Components or Trims
- Short Circuit Proof
- Output Sources and Sinks Current
- 10mA Output Current
- Low Supply Current — 1.0mA Max.
- Three-Terminal Package

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
AD581JH	0°C to +70°C	TO-39 Can	±30mV
AD581KH	0°C to +70°C	TO-39 Can	±10mV
AD581LH	0°C to +70°C	TO-39 Can	±5mV
AD581JCSA	0°C to +70°C	8 Lead S.O.	±30mV
AD581KCSA	0°C to +70°C	8 Lead S.O.	±10mV
AD581LCSA	0°C to +70°C	8 Lead S.O.	±5mV
AD581SH	-55°C to +125°C	TO-39 Can	±30mV
AD581TH	-55°C to +125°C	TO-39 Can	±10mV
AD581UH	-55°C to +125°C	TO-39 Can	±5mV

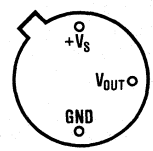
Typical Operating Circuit



±10 Volt Reference

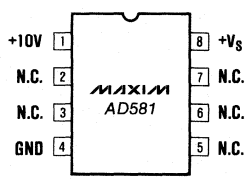
Pin Configurations

Bottom View



TO-39

Top View



8 Lead Small Outline

High Precision 10 Volt Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to GND ..... -0.3V, +40V
Power Dissipation
  Metal Can (Derate 6.7mW/°C above 60°C) 600mW
  Small Outline (Derate 5.3mW/°C above 75°C) 400mW
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
  Commercial (J, K, L) ..... 0°C to +70°C
  Military (S, T, U) ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +175°C
Lead Temperature (Soldering 10sec) ..... +300°C
Dice Junction Temperature (Tj) ..... -55°C to +150°C
Thermal Resistance, Junction to Ambient
  Metal Can ..... 150°C/W
  Small Outline Package ..... 170°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

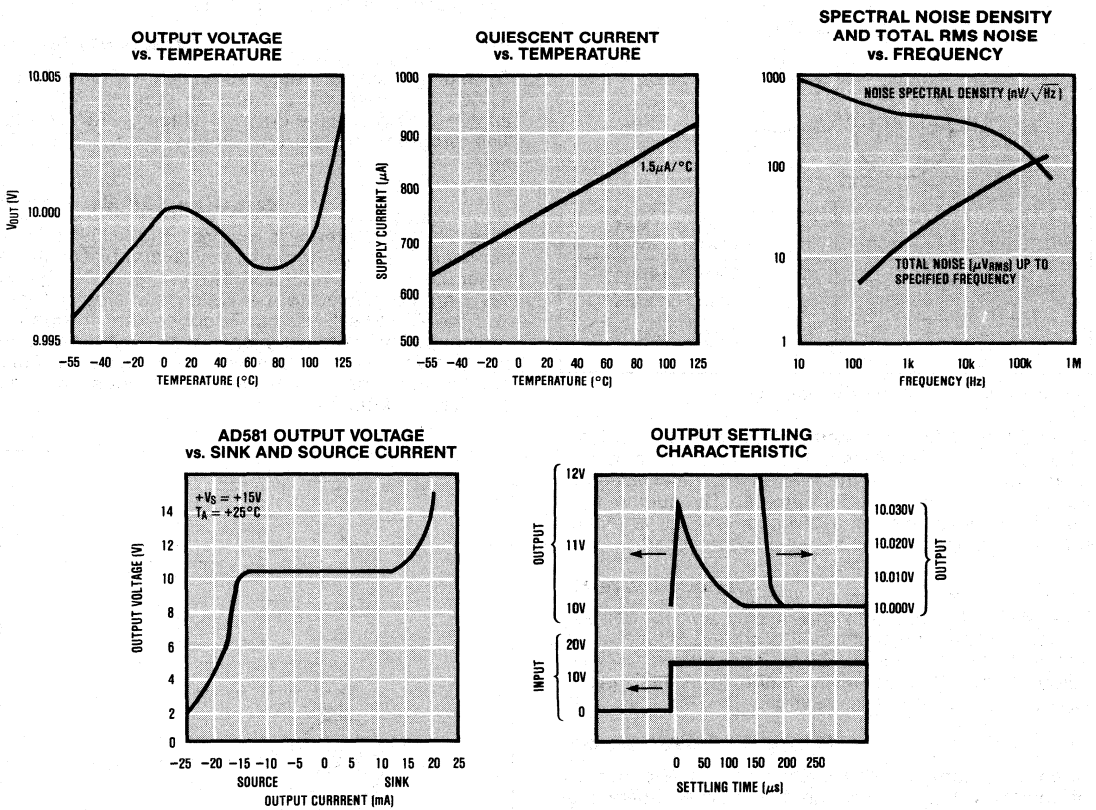
(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Tolerance			I_L = 0mA, AD581J/S AD581K/T AD581L/U				±30 ±10 ±5	mV
Output Voltage Change with Temperature, (Temperature Coefficient)			AD581J AD581K AD581L AD581S AD581T AD581U			13.5 (30) 6.75 (15) 2.25 (5) 30 (30) 15 (15) 10 (10)		±mV (ppm/°C)
Line Regulation			No Load, +12.5V < V_{IN}< +15V +15V < V_{IN} < +30V				0.005 (1.0) 0.002 (3.0)	%/V (mV) %/V (mV)
Load Regulation			I_L = 0mA to 5mA			20 (200)	50 (500)	ppm/mA (μV/mA)
Quiescent Supply Current		I_Q	I_L = 0mA			750	1000	μA
Turn-on Settling Time to 0.1%		t_{ON}				200		μs
Noise		e_{NP-P}	0.1Hz to 10Hz			50		μV_{P-P}
Long-Term Stability			(Non-Cumulative)			25		ppm/kHrs
Short Circuit Current		I_{SC}				30		mA
Output Current	Source	I_L	V_{IN} > V_{OUT} + 2.5V	T_A = +25°C T_{MIN} to T_{MAX}	10 5			mA
	Sink			T_{MIN} to T_{MAX}, AD581J/K/L AD581S/T/U -55°C to +85°C, AD581S/T/U	5 0.2 5			

Note 1: Absolute Maximum power dissipation must not be exceeded.

High Precision 10 Volt Reference

Typical Operating Characteristics



Detailed Description

As shown in Figure 1, most applications of the AD581 require no external components. Connections are $+V_S$, V_{OUT}, and GND (GND is tied to the case in the TO-5 package). Usually the desired accuracy is obtained by selecting the appropriate device grade. However, any part can be adjusted to a tighter tolerance, or to slightly different voltage, using the fine trim circuit in Figure 2. The table in Figure 2 lists the trim range for different values of R in the figure, and also shows the effect on temperature coefficient.

Voltage Temperature Coefficient

The temperature characteristic of the AD581 consistently follows an "S-curve" (see Typical Operating Characteristics). A five-point 100% test guarantees compliance with -55° C to +125° C specifications and a three-point 100% test guarantees 0° C to +70° C specifications.

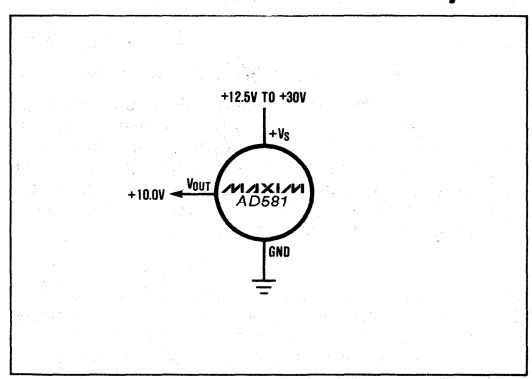
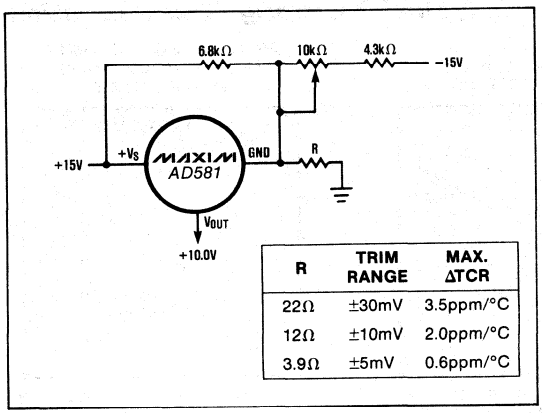


Figure 1. AD581 Basic Connection

High Precision 10 Volt Reference



R	TRIM RANGE	MAX. ΔTCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration

The Voltage Change specifications in the Electrical Characteristics table state the maximum deviation over temperature from the reference's initial value at 25°C, as well as drift in ppm/°C. By adding the maximum deviation for a given device to its initial tolerance, the total error is quickly determined.

Output Current

The AD581 is unique in that it can sink as well as source current. The circuit is also protected for output shorts to either $+V_S$ or GND. The output voltage versus current characteristic is shown in the Typical Operating Characteristics section.

Dynamic Performance

The turn-on characteristics and settling performance of the AD581 are shown in the Typical Operating Characteristics. Both coarse and fine transient response is shown. The reference typically settles to 1mV within 180μs after power is applied.

Applications

Precision High Current Reference

A PNP power transistor, or Darlington, is easily connected to the AD581 to greatly increase its output current. The circuit of Figure 3 provides a +10V output at up to 4 Amps. If the load has a significant capacitive component, compensation capacitor, C1, should be added. If the load is purely resistive, high frequency supply rejection is improved without C1.

Low Input Voltage

Although line regulation is specified from 12.5V to 40V, the AD581 can operate with a +12V ±5% input by adding a resistor as shown in Figure 4. The resistor reduces the current that must be supplied from V_{OUT}. Note that the resistor cannot be used at higher input voltages since, as the supply increases, it sources more current than V_{OUT} can sink.

Current Limiter

By adding a single resistor as shown in Figure 5, the AD581 is turned into a precision current limiter for applications where the driving voltage is 12.5V to 40V. The programmed current ranges from 0.75mA to 5mA.

Negative 10V Reference

Where a -10V reference is required, the AD581 can be connected as a two-terminal device and biased like a zener diode. The circuit is shown in Figure 6. $+V_S$ and V_{OUT} are connected to the system's analog ground, and the AD581's GND pin is connected, through a resistor, to the negative supply. With 1mA flowing in the reference, the output voltage is typically 2mV greater than what is obtained with the conventional, positive, hook-up.

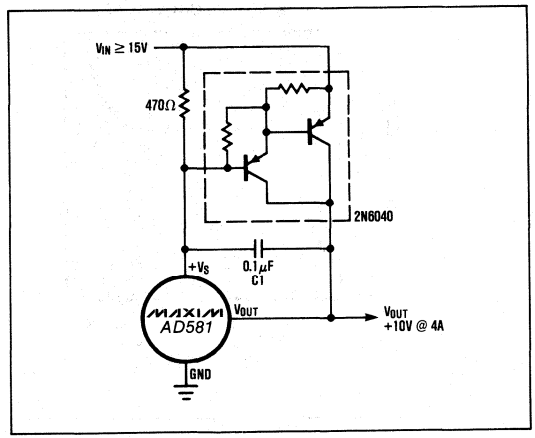


Figure 3. High Current Precision Supply

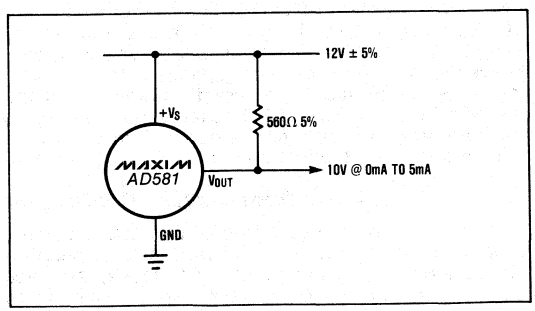


Figure 4. 12-Volt Supply Connection

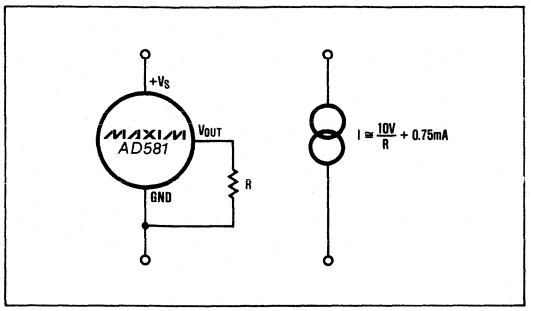


Figure 5. A Two-Component Precision Current Limiter

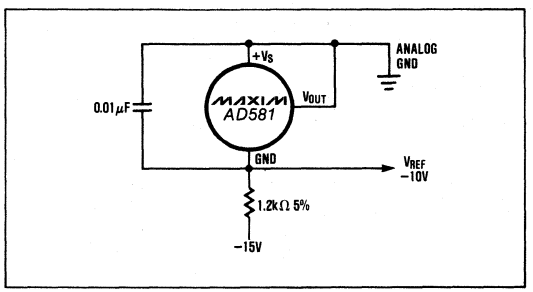


Figure 6. Two-Terminal -10 Volt Reference

When using the 2-terminal connection, the load and the bias resistor must be selected so that the current flowing in the reference is maintained between 1mA and 5mA. The operating temperature range for this connection is limited to -55° to +85°C.

Reference for CMOS DACs and ADCs

The AD581 is well suited for use with a wide variety of D-to-A converters, especially CMOS DACs. Figure 7 shows a circuit in which an AD7533 10 bit DAC outputs 0 to -10V when using a +10V reference. For a positive DAC output, the AD581 is configured as a 2-terminal -10V reference (Figure 6) and connected to the DAC's V_{REF} input.

In Figure 8, an AD7574 CMOS A/D converter uses an AD581 for its -10V reference input. The input range for the A/D converter is 0V to +10V.

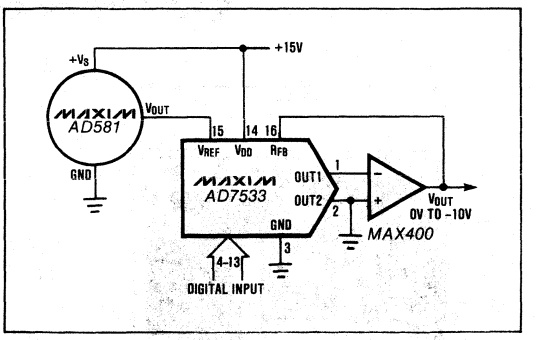


Figure 7. Low Power 10 Bit CMOS DAC Connection

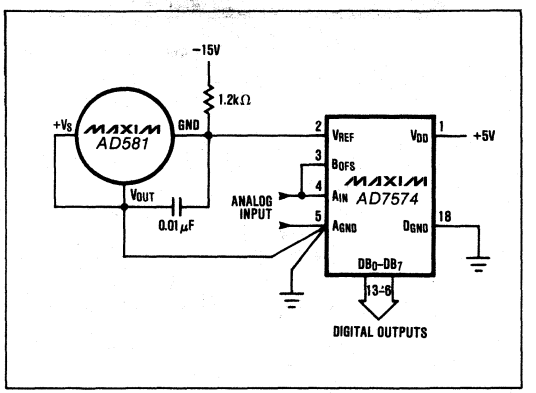


Figure 8. Negative 10V Reference for CMOS A/D Converter

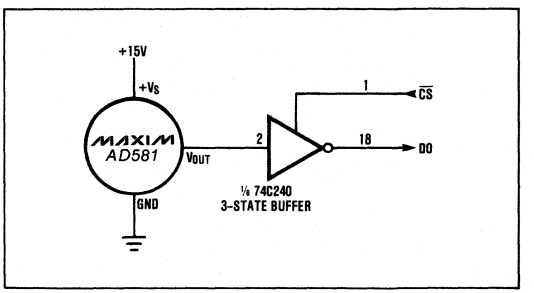
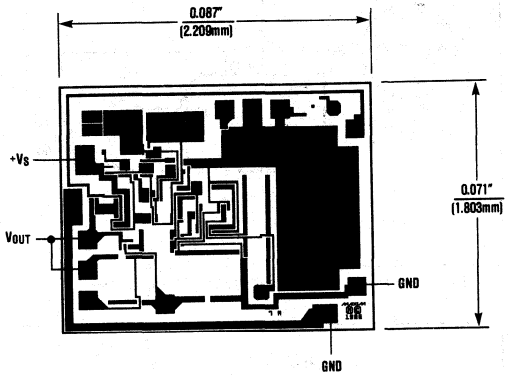


Figure 9. AD581 Microprocessor Interface

High Precision 10 Volt Reference

Chip Topography



MAXIM

Pin Programmable Precision Voltage Reference

General Description

Maxim's AD584 is a temperature compensated, bandgap voltage reference which provides pin-programmable output voltages of +10.00V, +7.50V. +5.00V, and +2.50V. External components are not required for these outputs, but if other voltages are desired, they can be programmed with external resistors. Laser trimming minimizes output error as well as temperature drift, to as low as 5mV and 5ppm/°C with the AD584L.

The input voltage range of the AD584 is 4.5V to 30V. The reference also includes a STROBE input which shuts down the reference output. Typical current drain when ON is 750μA. This drops to about 100μA when the reference is strobed OFF.

The AD584 is designed for use with 8 to 14 bit A/D and D/A converters as well as data acquisition systems. It is available in 8-lead TO-99 metal cans, plastic DIPs, CERDIPs, and small outline packages.

Applications

CMOS DAC Reference
A/D Converter Reference
Measurement Instrumentation
Data Loggers
Precision Analog Systems
Programmable Offset for PGAs

Features

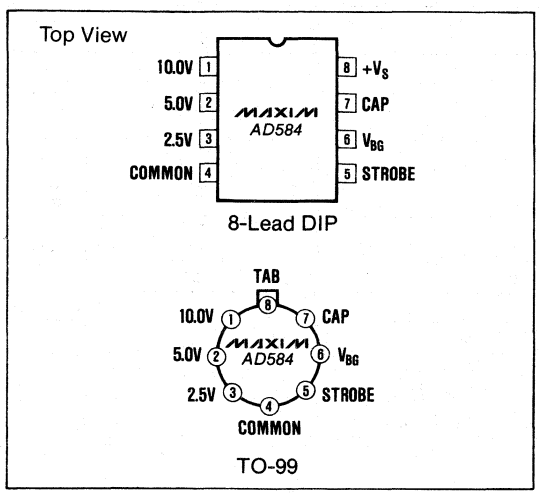
- **Programmable Outputs of: +10.0V, +7.5V, +5.0V, +2.5V**
- **±5mV Tolerance at +10V (AD584L)**
- **Low Tempco: 5ppm/°C Max. (AD584L)**
- **No External Components or Trims**
- **Short Circuit Proof**
- **Output Sources and Sinks Current**
- **10mA Output Current**

Ordering Information

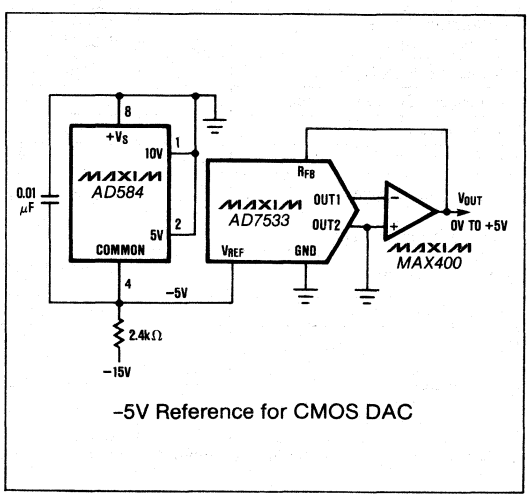
PART	TEMP. RANGE	PACKAGE*	ERROR
AD584JH	0°C to +70°C	TO-99 Can	±30mV
AD584KH	0°C to +70°C	TO-99 Can	±10mV
AD584LH	0°C to +70°C	TO-99 Can	±5mV
AD584JN	0°C to +70°C	Plastic DIP	±30mV
AD584KN	0°C to +70°C	Plastic DIP	±10mV
AD584LN	0°C to +70°C	Plastic DIP	±5mV
AD584JCSA	0°C to +70°C	Small Outline	±30mV
AD584KCSA	0°C to +70°C	Small Outline	±10mV
AD584LCSA	0°C to +70°C	Small Outline	±5mV
AD584JC/D	0°C to +70°C	Dice	±30mV
AD584SH	-55°C to +125°C	TO-99	±30mV
AD584TH	-55°C to +125°C	TO-99	±10mV
AD584SQ	-55°C to +125°C	CERDIP	±30mV
AD584TQ	-55°C to +125°C	CERDIP	±10mV

** All devices — 8 Lead Packages*

Pin Configuration



Typical Operating Circuit



Pin Programmable Precision Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Common ..... -0.3V, +40V
Power Dissipation
- Metal Can (Derate 6.7mW/ above +60°C) 600mW
- CERDIP (Derate 8mW/ above +75°C) 600mW
- Plastic DIP (Derate 6mW/ above +75°C) 450mW
- Small Outline (Derate 5.3mW/ above +75°C) 400mW

Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
- Commercial (J, K, L) ..... 0°C to +70°C
- Military (S, T, U) ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +300°C
Dice Junction Temperature (T_J) ..... -55°C to +150°C
Thermal Resistance, Junction to Ambient
- Metal Can ..... 150°C/W
- CERDIP ..... 125°C/W
- Plastic DIP ..... 160°C/W
- Small Outline ..... 170°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

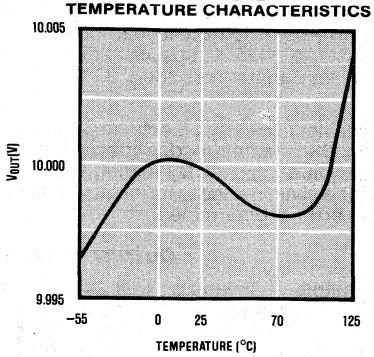
PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Tolerance			I_L = 0mA, At Pin 1	V_{OUT} = +10V, AD584J/S			±30	mV
				AD584K/T			±10	
				AD584L			±5	
				V_{OUT} = +7.5V, AD584J/S			±22	
				AD584K/T			±8	
				AD584L			±4	
				V_{OUT} = +5.0V, AD584J/S			±15	
				AD584K/T			±6	
				AD584L			±3	
				V_{OUT} = +2.5V, AD584J/S			±7.5	
				AD584K/T			±3.5	
				AD584L			±2.5	
Output Voltage Temperature Coefficient			AD584L, +10V, +7.5V, +5V Out				5	ppm/°C
			+2.5V Out				10	
			AD584J/S, All Outputs				30	
			AD584K, All Outputs				15	
			AD584T, +10V, +7.5V, +5V Out				15	
			+2.5V Out				20	
Differential Tempco Between Outputs			AD584K/L/T			3		ppm/°C
			AD584J/S			5		
Quiescent Supply Current		I_Q	I_L = 0mA			750	1000	µA
Quiescent Current Tempco						1.5		µA/°C
Turn-on Settling Time		t_{ON}	To ±1%			200		µs
Noise		e_{NP-P}	0.1Hz to 10Hz			50		μV_{P-P}
Long-Term Stability			(Non-Cumulative)			25		ppm/ kHrs
Short Circuit Current		I_{SC}				30		mA
Line Regulation			No Load, $(V_{OUT} + 2.5V) < V_{IN} < +15V$			0.005		%/V
			+15V < V_{IN} < +30V			0.002		
Load Regulation			I_L = 0mA to 5mA			20	50	ppm/mA
Output Current	Source	I_L	$V_{IN} > V_{OUT}$ +2.5V	T_A = +25°C	10			mA
				T_{MIN} to T_{MAX}	5			
	Sink			T_{MIN} to T_{MAX}, AD584J/K/L	5			
				AD584S/T	0.2			
				-55°C to +85°C, AD584S/T	5			

Note 1: Absolute Maximum power dissipation must not be exceeded.

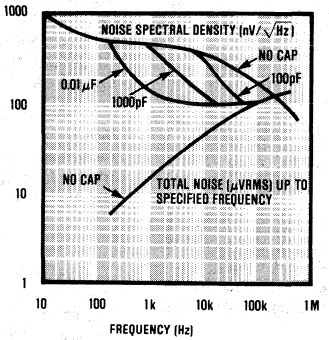
Pin Programmable Precision Voltage Reference

Typical Operating Characteristics

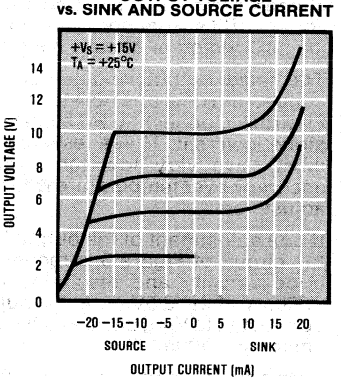
TYPICAL TEMPERATURE CHARACTERISTICS



SPECTRAL NOISE DENSITY AND RMS NOISE vs. FREQUENCY



OUTPUT VOLTAGE vs. SINK AND SOURCE CURRENT



POWER-ON SETTLING CHARACTERISTICS

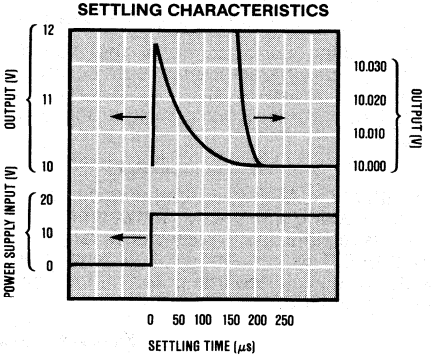


Table 1. Programming Pin Connections

OUTPUT VOLTAGE	PROGRAMMING (OUTPUT ON PIN 1)
10V	Pins 2 and 3 are unconnected.
7.5V	Connect pins 2 and 3 together.
5.0V	Connect pins 2 and 1 together.
2.5V	Connect pins 3 and 1 together.

3

Detailed Description

As shown in Figure 1, most applications of the AD584 require no external components. Connections to $+V_S$, and COMMON (COMMON is also tied to the case in the TO-99 metal package) with all other pins unconnected result in a buffered +10.00V output at pin 1. The other pretrimmed voltages are obtained by strapping pins as shown in Table 1. If one or more external buffer amplifiers are connected to the programming pins (pin 2,3), multiple outputs can be obtained from one reference.

Other Output Voltages

The AD584 can be adjusted to a different output voltage by adding one or more resistors as in Figure 2. As the diagram shows, the reference can be thought of as a 1.215V band-gap followed by a noninverting amplifier. If R1 and R2 are used alone, the adjustment range is widest but the resolution of the trim may be too coarse, even when a muti-turn trim pot is used.

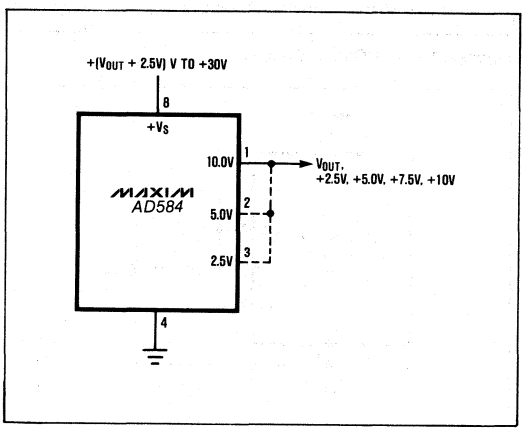


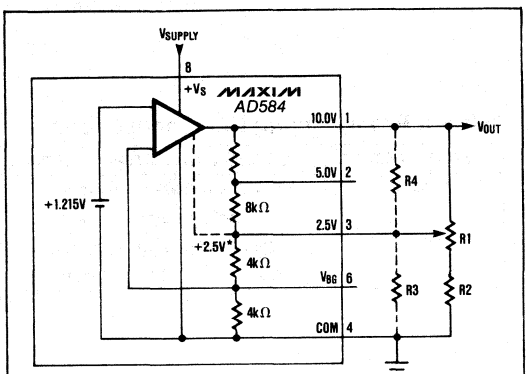
Figure 1. Basic Connection for Positive Outputs

Pin Programmable Precision Voltage Reference

When adding external resistors, output voltages well above 10V can be obtained. R2 should therefore be chosen carefully since it sets the maximum output voltage. R2's resistance should not be so low as to jeopardized other circuits if R1 is misadjusted.

The fixed output voltages can also be varied by connecting only one resistor, as in the dashed lines in Figure 2. Connecting R3 alone raises V_{OUT} while R4 alone lowers it. These resistors (or potentiometers) must have very low temperature coefficients if accuracy over temperature is to be unaffected by the adjustment.

If fine adjustment of the output is all that is required, the circuit of Figure 3 is recommended. It provides good stability and resolution for a trim range of ±200mV. If the 2.5V output is adjusted, R2 should be connected to V_{BG}, pin 6, and the trim range should be limited to ±100mV.



* The 2.5V tap (Pin 3) is used internally as a bias point and should not be changed by more than 100mV in any trim configuration.

Figure 2. Variable Output Options

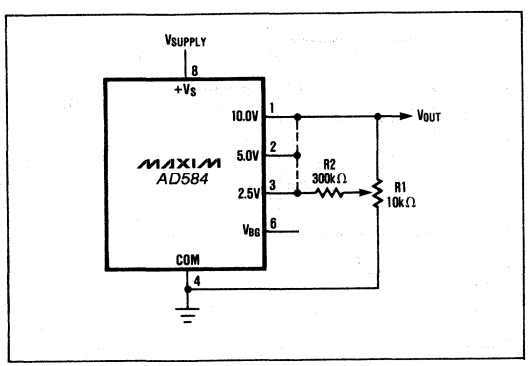


Figure 3. Fine Adjustment of Output Voltage (±200mV)

Voltage Temperature Coefficient

The temperature characteristic of the AD584 consistently follows an "S-curve" as shown in the Typical Charcteristics. A five-point 100% test guarantees compliance with -55°C to +125°C specifications and a three-point 100% test guarantees the 0°C to +70°C specifications.

The tolerance specifications in the Electrical Characteristics table state the maximum deviation from the reference's initial value at 25°C. By adding the maximum deviation for a given device to its initial tolerance, the total possible error is determined.

Output Current

The AD584 is capable of sinking as well as sourcing current. The circuit is also protected for output shorts to either $+V_S$ or ground (COMMON). The output's voltage-versus-current characteristic is shown in the Typical Characteristics section.

Dynamic Performance

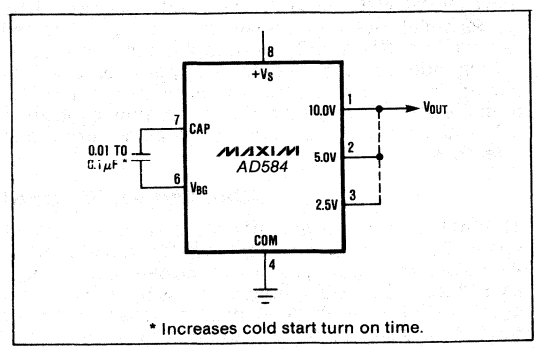
The turn-on settling performance of the AD584 is shown in the Typical Characteristics. Both coarse and fine transient response is shown. The reference typically settles to 1mV (10V output) within 180μs after power is applied.

Noise Filtering

The bandwidth of the AD584's output amplifier can be limited by connecting a capacitor between the CAP and V_{BG} pins (see Figure 4). Typical values range from 0.01μF to 0.1μF. The reduction of wideband and feedthrough noise is plotted in a graph in the Typical Characteristics section.

Strobe Input

The STROBE input, pin 5, zeroes the reference output when it is pulled LOW. If no current is pulled from STROBE, operation is normal. The threshold of the input is 200mV, so an open-drain N-channel FET or open-collector transistor driven from logic is re-



* Increases cold start turn on time.

Figure 4. Additional Noise Filtering with an External Capacitor

Pin Programmable Precision Voltage Reference

commended (see Figure 5). The current sinking ability should be at least 500μA and the leakage current should be 5μA or less. While shut down, the AD584 should not be required to source or sink current unless a 0.7V residual output is acceptable. If the reference is required to sink transient current while shut down, the current flowing out of STROBE should be limited with 100Ω as shown in the dashed connection in Figure 5.

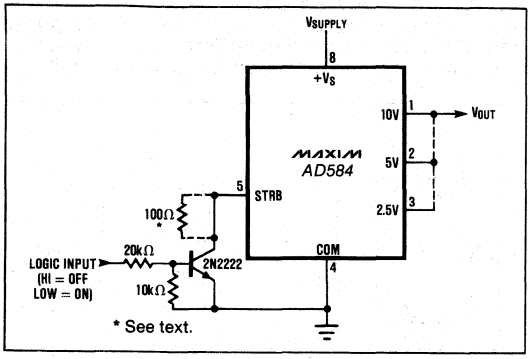


Figure 5. Use of Strobe Terminal

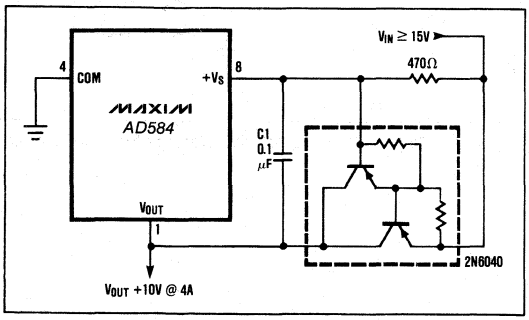


Figure 6. High Current Precision Supply

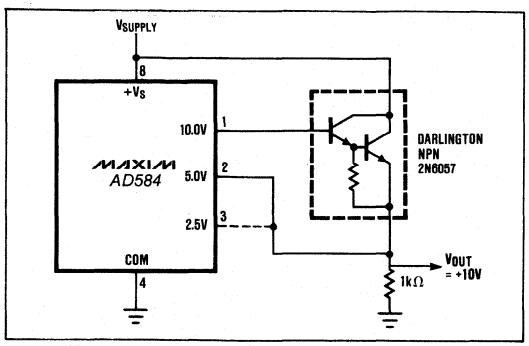


Figure 7. NPN Output Current Booster

Applications

Precision High Current Reference

A PNP power transistor, or Darlington, is easily connected to the AD584 to greatly increase its output current. The circuit in Figure 6 provides a +10V output at up to 4 Amps. If the load has a significant capacitive component, C1 should be added. If the load is purely resistive, high frequency supply rejection is improved without C1. An NPN output transistor or Darlinton can also be used to boost output current as shown in Figure 7.

Current Limiter

By adding a single resistor as shown in Figure 8, the AD584 is turned into a precision current limiter for applications where the driving voltage is 5V to 40V. The programmed current ranges from 0.75mA to 5mA.

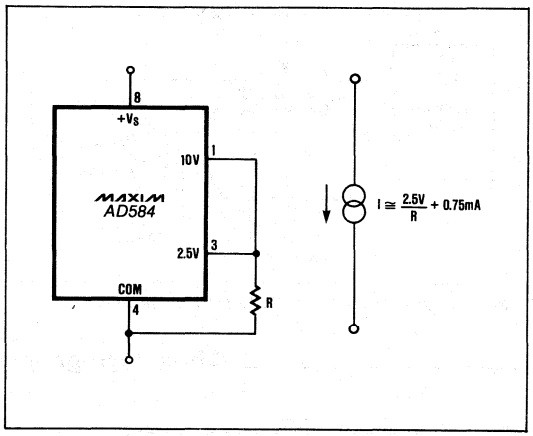


Figure 8. Precision Current Limiter

Negative 10V Reference

In applications which require a -10V, -7.5V, -5.0V, or -2.5V reference, the AD584 can be connected as a two-terminal device and biased like a zener diode. The circuit is shown in Figure 9. $+V_S$ and V_{OUT} are connected to the analog ground bus, and the AD584's COMMON pin is connected, through a resistor, to the negative supply. With 1mA flowing in the reference, the output is typically 2mV greater than what is obtained with a conventional, positive, hook-up.

When using the 2-terminal connection, the load and the bias resistor must be selected so that the current flowing in the reference is maintained between 1mA and 5mA. The operating temperature range for this connection is limited to -55° to +85°C.

Pin Programmable Precision Voltage Reference

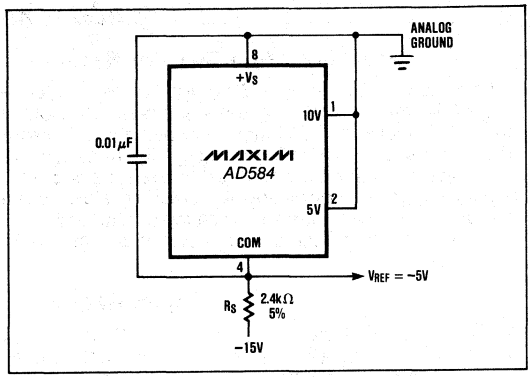


Figure 9. Two-Terminal -5 Volt Reference

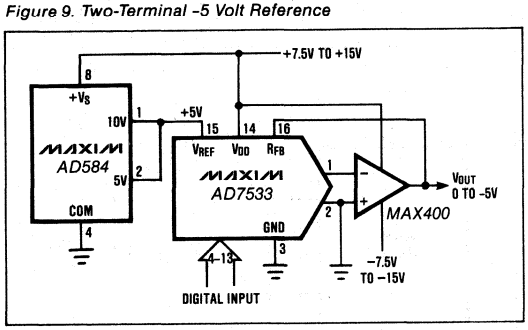


Figure 10. Low Power 10 Bit CMOS DAC Connection

Reference for DACs and ADCs

The AD584 is well suited for use with a wide variety of D-to-A converters, especially CMOS DACs. Figure 10 shows a circuit in which an AD7533 10 bit DAC outputs 0 to -5V when using a +5V reference. For a positive DAC output, the AD584 can be configured as a 2-terminal negative reference as well by using the connection of Figure 9.

In Figure 11, an AD7574 CMOS A/D converter uses an AD584, connected for -2.5V, as its reference input so that the system can operate from ±5V power. The analog input range for the circuit is 0V to +2.5V.

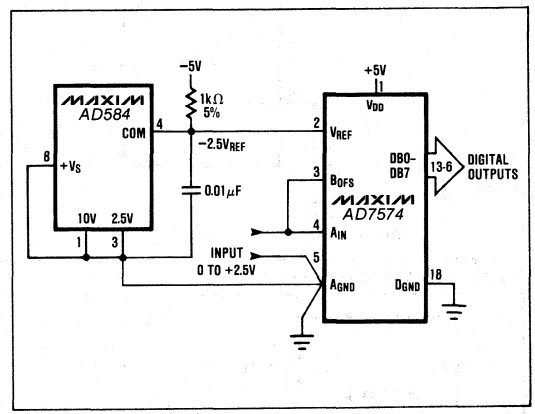
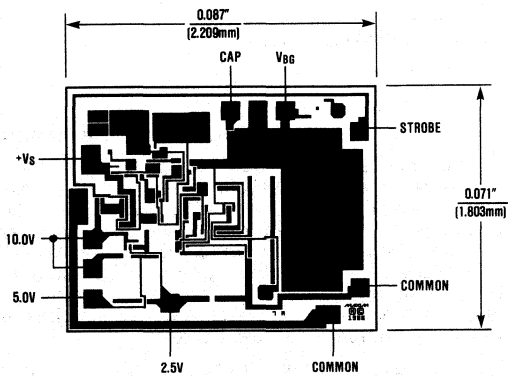


Figure 11. AD584 as Negative 2.5 Volt Reference for a CMOS ADC

Chip Topography



10 Volt Precision References

General Description

The AD2700 series of precision 10 volt reference sources offers excellent accuracy and stability. Laser trimming of both initial accuracy and temperature drift ensures high precision over the commercial (0°C to +70°C), industrial (-25°C to +85°C) and military (-55°C to +125°C) temperature ranges. The guaranteed absolute accuracy allows the user to configure systems without the need for ovens or chip heaters for temperature regulation. The AD2700 is a +10 volt output reference while the AD2701 is a -10 volt output. Both devices are guaranteed to 3ppm/°C max with 2.5mV initial accuracy. The AD2710, with a +10 volt output, is guaranteed to 1ppm/°C max with 1mV initial accuracy. These products are designed to interface with high accuracy, high resolution A to D and D to A converters, precision instrumentation, and data acquisition systems.

Features

- **Pin-for-Pin 2nd Source!**
- **Excellent Initial Accuracy**
- **Low Temperature Coefficient**
- **Excellent Long-Term Stability, 50ppm/1000hrs.**
- **10mA Output Current Capability**
- **Superior Line Regulation: 100μV/V max.**
- **Standard Ceramic Side Brazed DIP**

Ordering Information

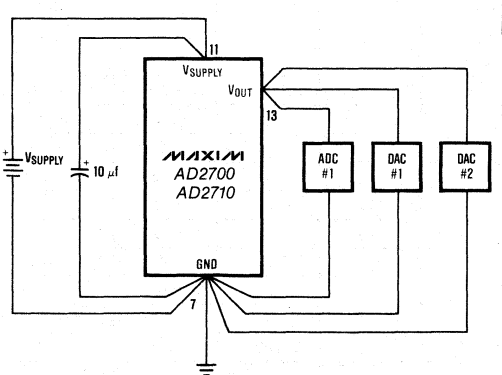
PART	OUTPUT VOLTAGE	TEMP. RANGE
AD2700JD	+10V, 10 ppm/°C	-25°C to +85°C
AD2700LD	+10V, 3 ppm/°C	-25°C to +85°C
AD2700SD	+10V, 3 ppm/°C	-55°C to +125°C
AD2700UD	+10V, 3 ppm/°C	-55°C to +125°C
AD2701JD	-10V, 10 ppm/°C	-25°C to +85°C
AD2701LD	-10V, 3 ppm/°C	-25°C to +85°C
AD2701SD	-10V, 3 ppm/°C	-55°C to +125°C
AD2701UD	-10V, 3 ppm/°C	-55°C to +125°C
AD2710LD	+10V, 1 ppm/°C	0°C to +70°C
AD2710KD	+10V, 2 ppm/°C	0°C to +70°C

All devices are available in a 14 lead ceramic side brazed DIP.

Applications

Precision D/A and A/D Converter Reference
Digital Voltmeters
Precision Test and Measurement Systems
Precision Calibrated Voltage Reference Standard
High Accuracy Transducers

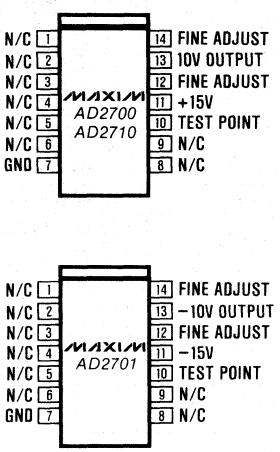
Typical Operating Circuit



Precision +10V System Reference

Pin Configuration

Top View



10 Volt Precision References

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... +20V
Power Dissipation 400mW
Operating Temperature Range
AD2700JD, LD, AD2701JD, LD ..... -25°C to +85°C
AD2700SD, UD, AD2701SD, UD ..... -55°C to +125°C
AD2710KD, LD ..... 0°C to +70°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature ..... +300°C
(soldering, 10 seconds)
Short Circuit to GND ..... Continuous

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V for AD2700 and AD2710, V_{IN} = -15V for AD2701, T_A = +25°C, R_L = 2kΩ, unless otherwise noted)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Initial Output Voltage	AD2700JD, SD		9.9950	10.0000	10.0050	V
	AD2700LD, UD		9.9975	10.0000	10.0025	V
	AD2701JD, SD		-10.0050	-10.0000	-9.9950	V
	AD2701LD, UD		-10.0025	-10.0000	-9.9975	V
	AD2710KD, LD		9.9990	10.0000	10.0010	V
Output Voltage Drift	AD2700,01JD	$T_A = T_{MIN}$ to T_{MAX}			10	ppm/°C
	AD2700,01LD, SD, UD	$T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
	AD2710KD	T_A = +25°C to +70°C			2	ppm/°C
	AD2710LD	T_A = +25°C to +70°C			1	ppm/°C
	AD2710KD	T_A = 0°C to +25°C			5	ppm/°C
	AD2710LD	T_A = 15°C to +25°C			2	ppm/°C
	AD2710LD	T_A = 0°C to +15°C			5	ppm/°C
Output Voltage Range	AD2700JD, AD2701JD	$T_A = T_{MIN}$ to T_{MAX}			±11.0	mV
	AD2700LD, AD2701LD	$T_A = T_{MIN}$ to T_{MAX}			±4.3	mV
	AD2700SD, AD2701SD	$T_A = T_{MIN}$ to T_{MAX}			±8.0	mV
	AD2700UD, AD2701UD	$T_A = T_{MIN}$ to T_{MAX}			±5.5	mV
Output Current	T_A = 25°C, for Specified Load Regulation				10	mA
	$T_A = T_{MIN}$ to T_{MAX} V_{IN} = +13V to +18V (2700, 2710) V_{IN} = -13V to -18V (2701)				5	mA
Line Regulation	V_{IN} = +13.5V to +16.5V (2700, 2710)				100	μV/V
	V_{IN} = -13.5V to -16.5V (2701)				100	μV/V
Load Regulation	0 to 10mA to GND				50	μV/mA
Output Resistance	0 to 10mA to GND				0.05	Ω
Input Voltage Range	AD2700, AD2710		+13		+18	V
	AD2701		-13		-18	V
Quiescent Current	No Load			9	14	mA
Noise (Note 1)	0.1 to 10Hz			6	50	μV_{P-P}
Long Term Stability	T_A = +55°C			50		ppm/1000 hrs.
Output Adjust Range	See Figure 1 and 2			±20		mV
Output Adjust Temperature Drift Effect				±4		μV/°C per mV of adjust

Note 1: QA sample tested.

Theory of Operation

A zener voltage of approximately 6.3V is applied to the non-inverting input of an operational amplifier. This voltage is accurately amplified to produce a precise 10.000V output. The amplifier's gain setting resistors are actively laser-trimmed to produce the desired output voltage. The zener operating current is derived from the regulated output voltage, and actively laser-trimmed to produce the lowest drift over temperature at the output of the amplifier.

Discussion of Performance

The Maxim AD2700 and AD2701 are designed for applications requiring a precision voltage reference, where initial accuracy at room temperature and drift over temperature are of prime importance.

The drift specification of the AD2700 and AD2701 are guaranteed by making precise voltage measurements at -55°C, -25°C, +25°C, +85°C, and -125°C, while maintaining unit identity. In this way, three key specifications are guaranteed: initial accuracy, absolute accuracy over temperature, and drift. The upper and lower bound limits of absolute accuracy over temperature are established by the sum of the maximum initial output voltage error and the maximum drift from +25°C to T_{MAX}. For example, the AD2700LD limit of 4.3mV is calculated from the addition of 2.5mV initial output voltage error plus the temperature drift error of 1.8mV [3ppm/°C x 10V x (85°C - 25°C)].

The drift specification is defined using the "box method" (Fig. 3). The "box" is formed by the T_{MAX} and T_{MIN} temperatures and a diagonal with a slope equal to the maximum specified drift. The maximum and minimum output voltages must meet the following conditions:

$$\frac{(V_{OUTMAX} - V_{OUTMIN})/10V}{T_{MAX} - T_{MIN}} \times 10^6 \leq \text{drift specification}$$

This assures that the output voltage variation over the temperature change is contained within the box with V_{OUTMAX} and V_{OUTMIN} limits.

For example, the AD2700LD maximum drift specification of 3ppm/°C from -25°C to +85°C restricts ($V_{OUTMAX} - V_{OUTMIN}$) to less than 3.3mV.

The AD2710 drift specification is defined over the temperature range of 0°C to +70°C using the "butterfly" method (Fig. 4), where endpoint measurements are tested for temperature coefficient from 25°C independent of the nominal voltage. Each device is tested at 0°C, +15°C, +25°C, and +70°C with the output voltage data recorded at each temperature. After the initial accuracy is checked for 1mV deviation from +10.000V at +25°C, the devices are graded according to temperature coefficient (TC). The AD2710K has a temperature coefficient less than or equal to 2ppm/°C from +25°C to +70°C and 5ppm/°C from 0°C to +25°C. These temperature coefficients correspond to a maximum change of 0.90mV and 1.25mV respectively (see Fig. 4a).

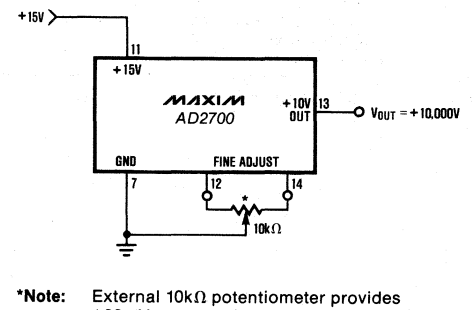
$$10V \times (70°C - 25°C) \times 2\times10^{-6} = 0.90mV$$
$$10V \times (25°C - 0°C) \times 5\times10^{-6} = 1.25mV$$

Similarly, the AD2710L is tested for 1ppm/°C from +25°C to +70°C, 2ppm/°C from +15°C to +25°C, and 5ppm/°C from 0°C to +15°C (see Fig. 4b). The corresponding voltage limits are 0.45mV from 25°C to +70°C, 0.2mV from +15°C to +25°C, and 0.75mV from 0°C to +15°C which, when added to the 0.2mV at +15°C, allows for 0.95mV change at 0°C.

Application Information

The Typical Operating Circuit shown on the front page shows the proper connection for the AD2700/2710. Special attention to layout is required to achieve the specified performance. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply.

The output voltage of the AD2700 and AD2710 can be trimmed, as shown in Figure 1, by connecting an external potentiometer between pins 12 and 14 with the wiper connected to ground. This external potentiometer provides typically ±20mV of output adjustment. The voltage drift will change by approximately 0.4ppm/°C (or 4μV/°C) per mV of adjustment.



***Note:** External 10kΩ potentiometer provides ±20mV output adjustment. Temperature effect is ±4μV/°C per mV of output adjustment.

Figure 1. Fine Trim Connection, AD2700 and AD2710

10 Volt Precision References

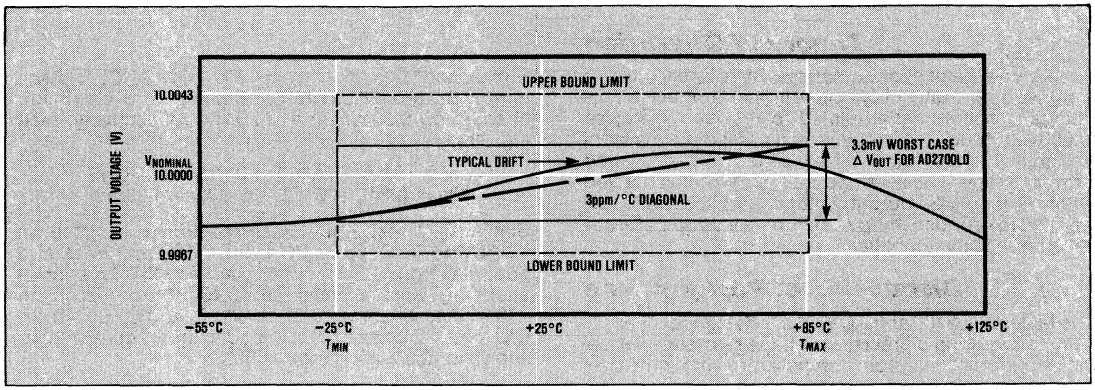
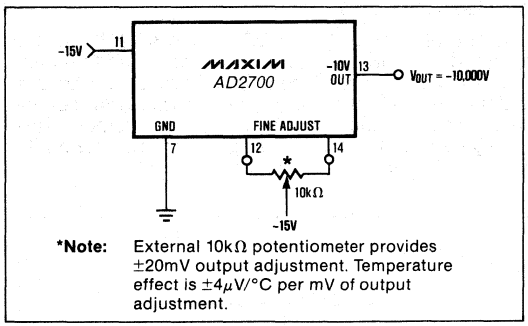


Figure 3. AD2700 Output Voltage Drift

The fine trim adjustment of the AD2701 is achieved by connecting the wiper of the potentiometer to V⁻, as shown in Figure 2.



***Note:** External 10kΩ potentiometer provides ±20mV output adjustment. Temperature effect is ±4μV/°C per mV of output adjustment.

Figure 2. Fine Trim Connection, AD2701

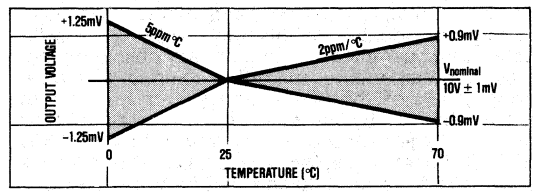


Figure 4a. AD2710K Output Voltage Drift

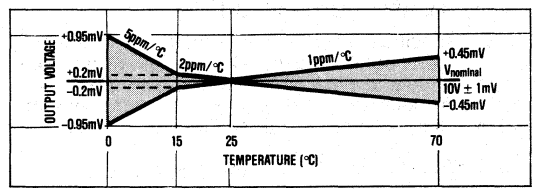


Figure 4b. AD2710L Output Voltage Drift

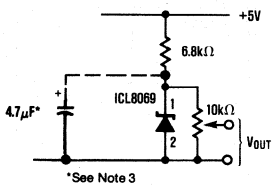
General Description

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Maxim's ICL8069 also features excellent stability, freedom from oscillation.

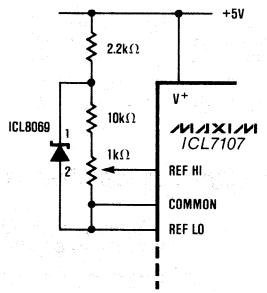
Applications

Analog to Digital Converters
Digital to Analog Converters
Threshold Detectors
Voltage Regulators
Portable Instruments

Typical Operating Circuits



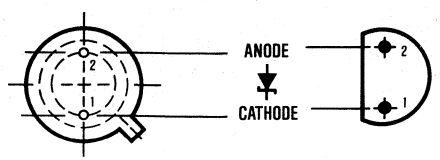
(a) Simple Reference (1.2 Volts or Less)



(b) Double Regulated 100mV Reference for ICL7107 One-Chip DPM Circuit.

Pin Configuration

Bottom View



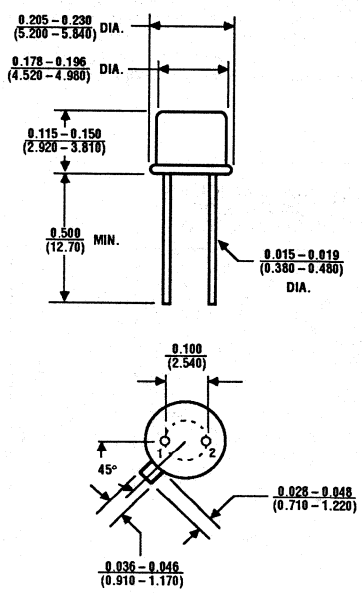
Features

- **Temperature Coefficient Guaranteed to 10ppm/°C Max.**
- **Low Bias Current . . . 50 μA Min.**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

Ordering Information

PART	TEMP. STABILITY	TEMP. RANGE
TO-92 Plastic:		
ICL8069CCZQ2	0.005%/°C	0°C to +70°C
ICL8069DCZQ2	0.01%/°C	0°C to +70°C
TO-52 Can:		
ICL8069ACSQ2	0.001%/°C	0°C to +70°C
ICL8069BCSQ2	0.0025%/°C	0°C to +70°C
ICL8069CCSQ2	0.005%/°C	0°C to +70°C
ICL8069DCSQ2	0.01%/°C	0°C to +70°C
ICL8069CMSQ2	0.005%/°C	-55°C to +125°C
ICL8069DMSQ2	0.01%/°C	-55°C to +125°C

Package Information



2 Lead TO-52
Can (SQ)

Low Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Reverse Voltage ..... See Note 1
Forward Current 10mA
Reverse Current 10mA
Power Dissipation .... Limited by Max Forward/Reverse Current
Storage Temperature Range ..... -65°C to +150°C

Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... -55°C to +125°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	I_R = 500μA	1.20	1.23	1.25	V
Reverse Breakdown Voltage Change	50μA ≤ I_R ≤ 5mA		15	20	mV
Reverse Dynamic Impedance	I_R = 50μA I_R = 500μA		1 0.6	2 2	Ω
Forward Voltage Drop	I_F = 500μA		0.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I_R = 500μA		5		μV
Breakdown Voltage Temperature Coefficient: ICL8069A ICL8069B ICL8069C ICL8069D	 I_R = 500μA T_A = Operating Temperature Range (Note 2)			 .001 .0025 .005 .01	%/°C
Reverse Current Range		.050		5	mA

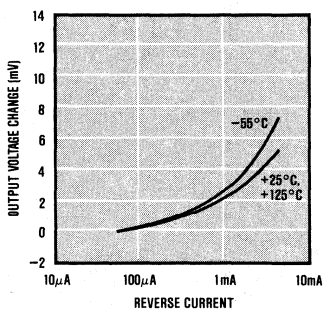
Note 1: In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.

Note 2: For the military devices, measurements are made at 25°C, -55°C, and 125°C, while for the commercial devices measurements are made at 25°C, 0°C and 70°C. The unit is then classified as a function of the worst case TC. Sample tested to 0.1% AQL.

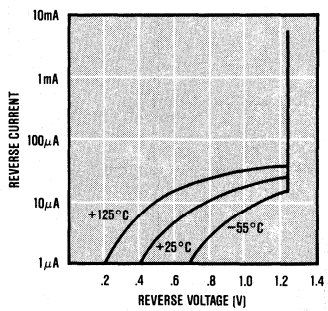
Note 3: If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.

Typical Operating Characteristics

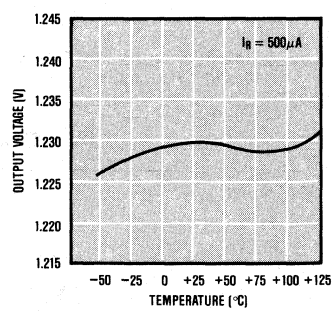
VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



REVERSE VOLTAGE AS A FUNCTION OF CURRENT



REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

+5V, +10V Precision Voltage References

General Description

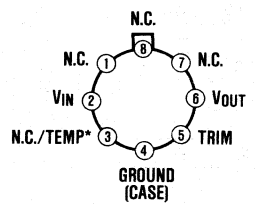
The REF01 and REF02 are precision voltages references that are pretrimmed to within ±.3% of 10V and 5V respectively. Both references feature excellent temperature stability (as low as 8.5 ppm/°C worst case), low current drain and low noise. The REF02 also provides a TEMP pin whose output voltage varies linearly with temperature, making this device suitable for a wide variety of temperature sensing and control applications. Both devices are available from Maxim in the space-saving Small Outline package, as well as the standard 8 pin TO-99 and MINI-DIP packages.

Applications

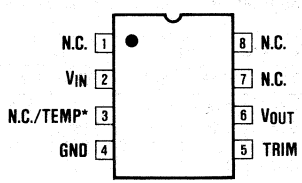
A to D Converters
D to A Converters
Digital Voltmeters
Voltage Regulators
Threshold Detectors

Pin Configuration

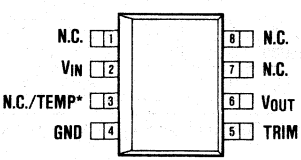
Top View



8 Lead TO-99 Metal Can



8 Lead DIP



8 Lead Small Outline

***NOTE:** Pin 3 is N.C. (No Connection) on REF01, TEMP Output on REF02

Features

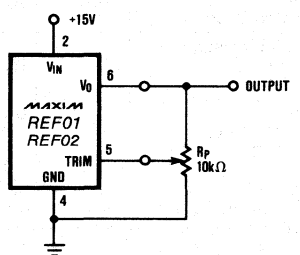
- **Pretrimmed to +5V, +10V ±0.3%**
- **Excellent Temperature Stability: 3ppm/°C**
- **Low Noise: 10μV_{p-p} (REF02)**
- **Low Supply Current: 1.4mA Max**
- **Short Circuit Proof**
- **Linear Temperature Transducer O/P (REF02)**

Ordering Information

PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C		
REF01EJ	10V ± 30mV	TO-99
REF01HJ	10V ± 50mV	TO-99
REF01CJ	10V ± 100mV	TO-99
REF01EZ	10V ± 30mV	Hermetic DIP
REF01HZ	10V ± 50mV	Hermetic DIP
REF01CZ	10V ± 100mV	Hermetic DIP
REF01HP	10V ± 50mV	Plastic DIP
REF01CP	10V ± 100mV	Plastic DIP
REF01HCSA	10V ± 50mV	Small Outline
REF01CCSA	10V ± 100mV	Small Outline
TEMP RANGE: -55°C TO +125°C		
REF01AJ	10V ± 30mV	TO-99
REF01J	10V ± 50mV	TO-99
REF01AZ	10V ± 30mV	Hermetic DIP
REF01Z	10V ± 50mV	Hermetic DIP

(Ordering information continued on last page.)

Typical Operating Circuit



Reference with Trimmed Output

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS—REF01

Input Voltage
- REF01, A, E, H, All DICE 40V
- REF01C 30V

Power Dissipation
- T099 (J) 500mW
  (Derate at 7.1mW/°C above 80°C)
- CERDIP (Z) 500mW
  (Derate at 6.7mW/°C above 75°C)
- Plastic DIP (P) 500mW
  (Derate at 5.6mW/°C above 36°C)
- Small Outline (S) 300mW
  (Derate at 5.0mW/°C above 55°C)

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- REF01A, REF01 ..... -55°C to +125°C
- REF01E, REF01H, REF01C ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... -65°C to +150°C

Lead Temperature (Soldering, 60 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01A/E			REF01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, -55°C ≤ T_A ≤ +125°C for REF01A and REF01, 0°C ≤ T_A ≤ +70°C for REF01E and REF01H, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01A/E			REF01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13V to 33V)(Note 4)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA)(Note 4)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

Note 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

Note 2: ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
Note 3: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 4: Line and Load Regulation specifications include the effect of self heating.
Note 5: Sample tested.

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01C			UNITS
			MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0mA	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.009	0.015	%/V
Load Regulation (Note 4)		I_L = 0 to 8mA I_L = 0 to 4mA	— —	0.006 0.006	0.015 0.015	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	mA

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01C			UNITS
			MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	ppm/%
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.011	0.018	%/V
Load Regulation (Note 4)		I_L = 0 to 5mA	—	0.008	0.018	%/mA

Notes: See previous page.

Output Adjustment

The REF01 trim terminal can be used to adjust the voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V, including 10.240V for binary applications (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/°C for 100mV of output adjustment.

Burn-in Circuit

The burn-in circuit of Figure 1 is used for both the REF01 and the REF02. All Maxim REF01s and REF02s are 100% burned-in for a minimum of 24hrs at 150°C (except for Small Outline package), which is equivalent to 25 years of operation at 25°C. This substantially improves the long term stability of the part, and allows Maxim to offer a product with a F.I.T. rate of better than 10 (See Product Reliability Report RR-1A).

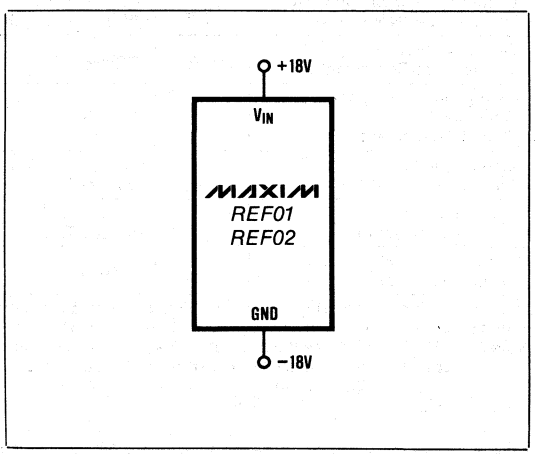


Figure 1. Burn-in circuit

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS—REF02

Input Voltage
- REF02, A, E, H, All DICE 40V
- REF02C, D 30V

Power Dissipation
- T099 (J) 500mW
  (Derate at 7.1mW/°C above 80°C)
- CERDIP (Z) 500mW
  (Derate at 6.7mW/°C above 75°C)
- Plastic DIP (P) 500mW
  (Derate at 5.6mW/°C above 36°C)
- Small Outline (S) 300mW
  (Derate at 5.0mW/°C above 55°C)

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- REF02A, REF02 ..... -55°C to +125°C
- REF02E, REF02H ..... 0°C to +70°C
- REF02C, REF02D ..... 0°C to +70°C

Lead Temperature (Soldering, 60 sec.) ..... +300°C

DICE Junction Temperature (T_j) ..... -65°C to +150°C

Output Short-Circuit Duration
(to Ground or V_{IN}) ..... Indefinite

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02A/E			REF02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3	±6	—	±3	±6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	10	15	—	10	15	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 8V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 1)		I_L = 0 to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 2)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, -55°C ≤ T_A ≤ +125°C for REF02A and REF02, 0°C ≤ T_A ≤ +70°C for REF02E and REF02H, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02A/E			REF02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 3, 4)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 5)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 8V to 33V)(Note 1)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA)(Note 1)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	—	2.1	—	mV/°C

Note 1: Line and Load Regulation specifications include the effect of self heating.
Note 2: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
Note 3: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

Note 4: ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
Note 5: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 6: Sample tested.

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02C			REF02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±6.0	—	±2.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	12	18	—	12	—	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 8V to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 1)		I_L = 0 to 8mA I_L = 0 to 4mA	— —	0.006 —	0.015 —	— —	— 0.015	— 0.04	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 2)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02C			REF02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 3 and 4)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 5)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 1)		V_{IN} = 8V to 30V	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 1)		I_L = 0 to 5mA	—	0.008	0.018	—	0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	—	2.1	—	mV/°C

Notes: See previous page.

Output Adjustment

The REF02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

Temperature Voltage Output

The REF02 provides a temperature dependent output voltage on the TEMP pin. This voltage is proportional to the absolute temperature, and has a scale factor of approximately 2.1mV/°C (Figure 2).

Output Voltage = 2.1(T + 273)mV
where T = Temperature in °C

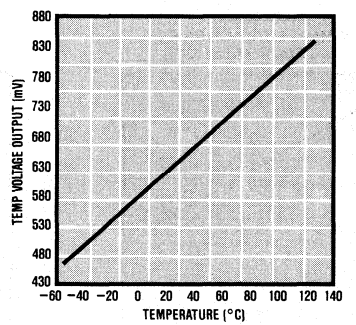
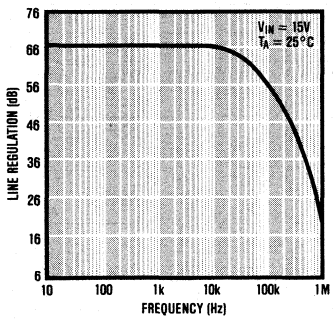


Figure 2. REF02 Temperature Voltage Output vs. Temperature.

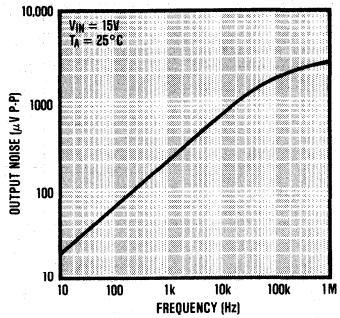
+5V, +10V Precision Voltage References

Typical Operating Characteristics

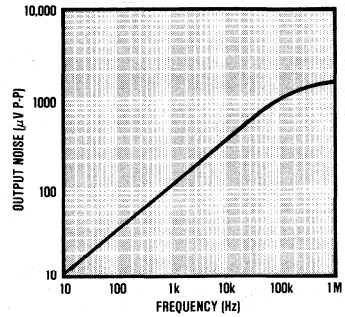
LINE REGULATION vs FREQUENCY



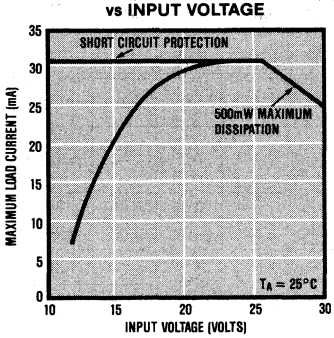
REF01 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



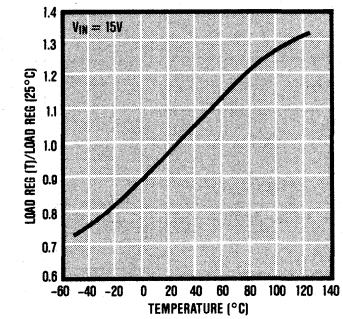
REF02 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



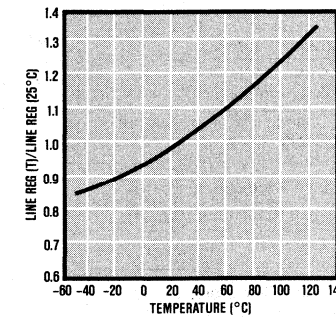
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



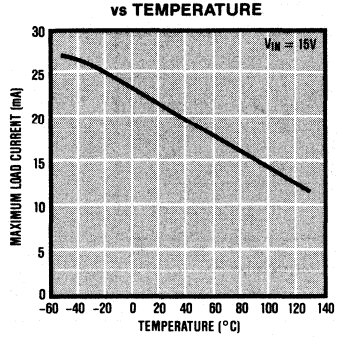
NORMALIZED LOAD REGULATION (ΔI_L = 10 mA) vs TEMPERATURE



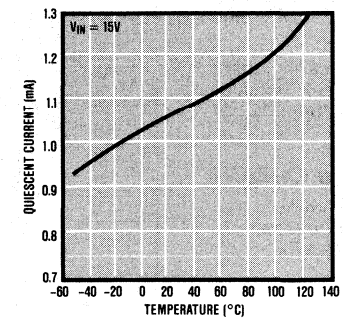
NORMALIZED LINE REGULATION vs TEMPERATURE



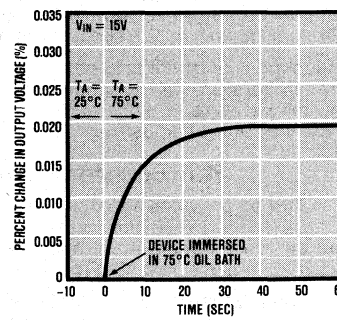
MAXIMUM LOAD CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



OUTPUT CHANGE DUE TO THERMAL SHOCK



Typical Applications

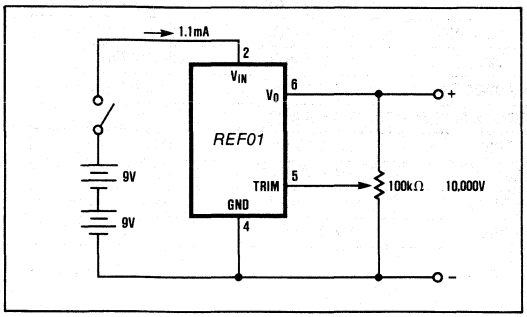


Figure 3. Precision Calibration Standard

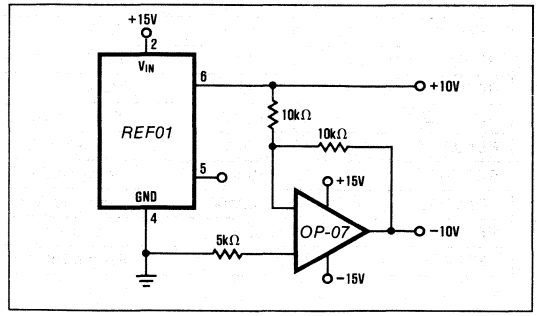


Figure 4. ±10V Reference

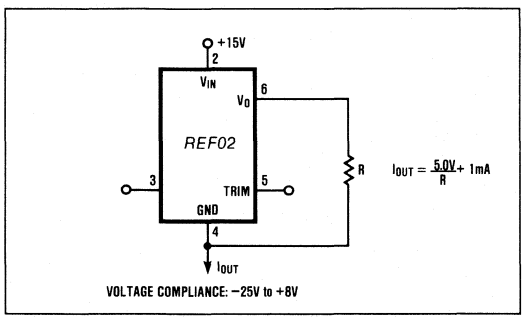


Figure 5. Current Source

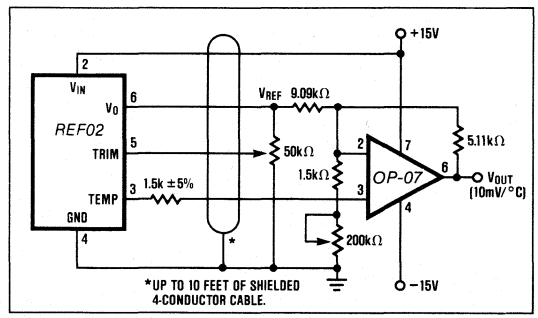
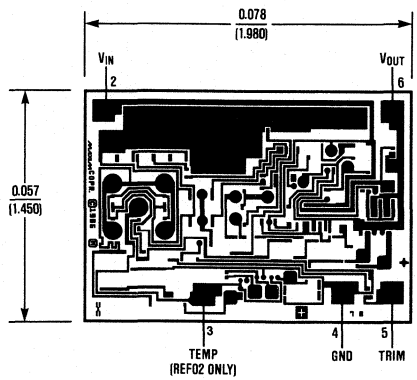


Figure 6. Precision Temperature Transducer with Remote Sensor

Chip Topography



+5V, +10V Precision Voltage References

Ordering Information

(Continued from first page)

PART	V_{OUT} @ 25°C	PACKAGE	PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C			**TEMP RANGE: 0°C TO +70°C**		
REF02EJ	5V ± 15mV	TO-99	REF02DP	5V± 100mV	Plastic DIP
REF02HJ	5V ± 25mV	TO-99	REF02HCSA	5V ± 25mV	Small Outline
REF02CJ	5V ± 50mV	TO-99	REF02CCSA	5V ± 50mV	Small Outline
REF02DJ	5V ± 100mV	TO-99	REF02DCSA	5V ± 100mV	Small Outline
REF02EZ	5V ± 15mV	Hermetic DIP	**TEMP RANGE: -55°C TO +125°C**		
REF02HZ	5V ± 25mV	Hermetic DIP	REF02AJ	5V ± 15mV	TO-99
REF02CZ	5V ± 50mV	Hermetic DIP	REF02J	5V ± 25mV	TO-99
REF02DZ	5V ± 100mV	Hermetic DIP	REF02AZ	5V ± 15mV	Hermetic DIP
REF02HP	5V ± 25mV	Plastic DIP	REF02Z	5V ± 25mV	Hermetic DIP
REF02CP	5V ± 50mV	Plastic DIP			

True RMS-to-DC Converters

4

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

True RMS-to-DC Converter

General Description

The AD536A and AD636 are true RMS-to-DC converters. They feature low power and are designed to accept low level input signals from 0 to $7V_{rms}$ for the AD536A and 0 to $200mV_{rms}$ for the AD636. Both devices accept complex input waveforms containing AC and DC components. They can be operated from either a single supply or dual supplies. Both devices draw less than 1mA of quiescent supply current making them ideal for battery powered applications.

Input and output offset, positive and negative waveform symmetry (DC reversal), and full-scale accuracy are laser trimmed, so that no external trims are required to achieve full rated accuracy.

Applications

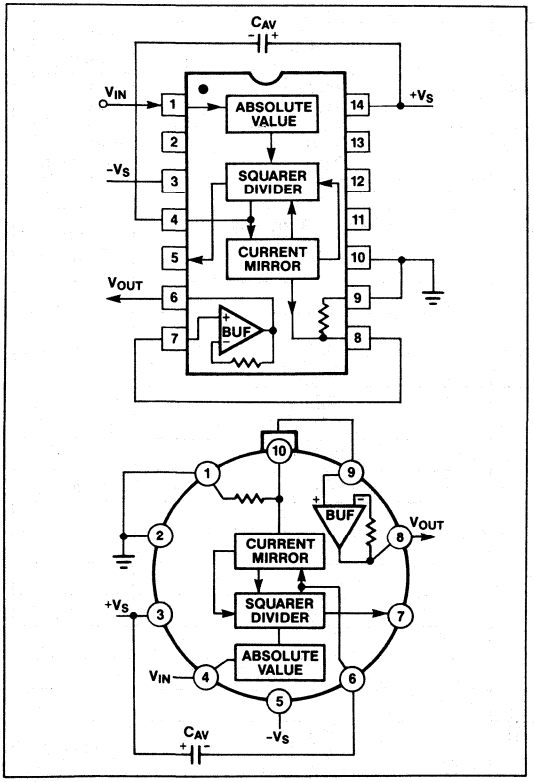
Digital Multimeters

Battery Powered Instruments

Panel Meters

Process Control

Typical Operating Circuit



Features

- **True RMS-to-DC Conversion**
- **Computes RMS of AC and DC Signals**
- **Wide Response:**
  2MHz Bandwidth for V_{rms} >1V (AD536A)
  1MHz Bandwidth for V_{rms} >100mV (AD636)
- **Auxiliary dB Output: 60dB range for AD536A**
  50dB range for AD636
- **Single or Dual Supply Operation**
- **Low Power: 1.2mA typ for AD536A**
  800μA typ for AD636

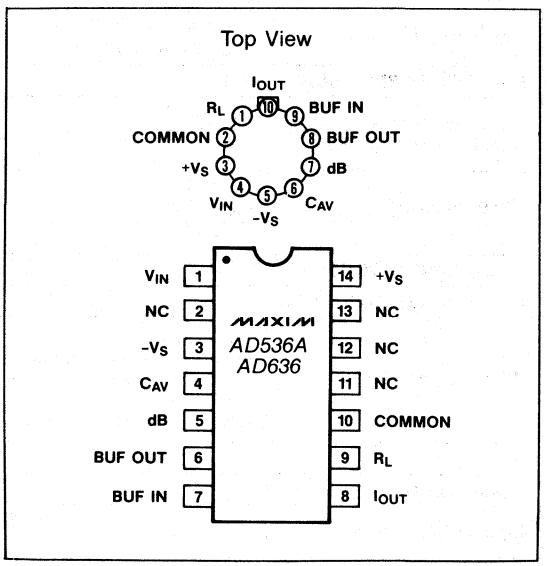
Ordering Information

PART	TEMP. RANGE	PACKAGE*
AD536AJC/D	0°C to +70°C	Dice
AD536AJCWE	0°C to +70°C	16 Lead Wide S.O.
AD536AJD	0°C to +70°C	14 Lead Ceramic
AD536AJH	0°C to +70°C	10 Lead TO-100
AD536AJN	0°C to +70°C	14 Lead Plastic DIP
AD536AJQ*	0°C to +70°C	14 Lead CERDIP
AD536AKCWE	0°C to +70°C	16 Lead Wide S.O.
AD536AKD	0°C to +70°C	14 Lead Ceramic
AD536AKH	0°C to +70°C	10 Lead TO-100
AD536AKN	0°C to +70°C	14 Lead Plastic DIP

Ordering Information continued on last page.

** Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages*

Pin Configuration



True RMS-to-DC Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage: Dual Supplies (AD536A) ..... ±18V
(AD636) ..... ±12V
Single Supply (AD536A) ..... +36V
(AD636) ..... +24V
Input Voltage (AD536A) ..... ±25V
(AD636) ..... ±12V
Power Dissipation (Package)
Plastic DIP (Derate 12mW/°C above +75°C) 450mW
Small Outline (Derate 10mW/°C above +75°C) ... 400mW
Power Dissipation (Package) (continued)
Ceramic (Derate 10mW/°C above +75°C) 500mW
TO-100 metal can (Derate 7mW/°C above +75°C) .. 450mW
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range:
Commercial (J,K) ..... 0°C to +70°C
Military (S) ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS—AD536A (T_A = 25°C, $+V_S$ = +15V, $-V_S$ = -15V, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSFER EQUATION				$V_{OUT} = [avg.(V_{IN})^2]^{½}$		
CONVERSION ACCURACY						
Total Error, Internal Trim (Note 1)		AD536AJ,AS AD536AK			±5 ±0.5 ±2 ±0.2	mV ±% of Reading
Total Error vs. Temperature	T_{MIN} to +70°C	AD536AJ AD536AK AD536AS			±0.1 ±0.01 ±0.05 ±0.005 ±0.1 ±0.005	mV ±% of Reading/°C
	+70°C to +125°C	AD536AS			±0.03 ±0.005	
Total Error vs. Supply				±0.1 ±0.01		mV ±% of Reading/V
Total Error vs. DC Reversal		AD536AJ,AS AD536AK		±0.2 ±0.1		% of Reading
Total Error, External Trim (Note 1)		AD536AJ,AS AD536AK		±3 ±0.3 ±2 ±0.1		mV ±% of Reading
ERROR vs. CREST FACTOR (Note 2)						
Additional Error	Crest Factor 1 to 2 Crest Factor = 3 Crest Factor = 7			Specified Accuracy -0.1 -1.0		% of Reading
FREQUENCY RESPONSE (Note 3)						
Bandwidth for 1% Additional Error (0.09dB)	V_{IN} = 10mV V_{IN} = 100mV V_{IN} = 1V			5 45 120		kHz
±3dB Bandwidth	V_{IN} = 10mV V_{IN} = 100mV			90 450		kHz
	V_{IN} = 1V			2.3		MHz
AVERAGING TIME CONSTANT (Fig. 3)				25		ms/μF C_{AV}
INPUT CHARACTERISTICS						
Input Signal Range	±15V Supplies Continuous rms			0 to 7		V_{rms}
	Peak Transient				±20	V_{PK}
	±5V Supplies Continuous rms			0 to 2		V_{rms}
	Peak Transient				±7	V_{PK}
Safe Input	All Supplies				±25	V_{PK}
Input Resistance			13.33	16.7	20.00	kΩ
Input Offset Voltage		AD536AJ,AS AD536AK		0.8 0.5	±2 ±1	mV

ELECTRICAL CHARACTERISTICS—AD536A (Continued)

(T_A = 25°C, $+V_S$ = +15V, $-V_S$ = -15V, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Offset Voltage	T_A = +25°C	AD536AJ AD536AK AD536AS		±1 ±0.5	±2 ±1 ±2	mV
	T_{MIN} to T_{MAX}	AD536AJ,AK AD536AS		±0.1	±0.2	mV/°C
	Supply Voltage	AD536AJ,AK AD536AS		±0.1 ±0.2		mV/V
Output Voltage Swing	±15V Supplies ±5V Supplies		0 to +11 0 to +2	+12.5		V
Output Current	Source Sink		+5 -130			mA µA
Short Circuit Current				20		mA
Output Resistance					0.5	Ω
dB OUTPUT						
Error	V_{IN} = 7mV to $7V_{rms}$, 0dB = $1V_{rms}$	AD536AJ AD536AK AD536AS		±0.4 ±0.2 ±0.5	±0.6 ±0.3 ±0.6	dB
Scale Factor				-3		mV/dB
Scale Factor TC (Uncompensated)				+0.33		% of Reading/°C
I_{REF}	0dB = $1V_{rms}$		5	20	80	µA
I_{REF} Range			1		100	µA
I_{OUT} TERMINAL						
I_{OUT} Scale Factor				40		$\mu A/V_{rms}$
I_{OUT} Scale Factor Tolerance				±10	±20	%
Output Resistance			20	25	30	kΩ
Voltage Compliance				$-V_S$ to $(+V_S - 2.5V)$		V
BUFFER AMPLIFIER						
Input and Output Voltage Range			$-V_S$ to $(+V_S - 2.5V)$			V
Input Offset Voltage	R_S = 25kΩ			±0.5	±4	mV
Input Bias Current				20	60	nA
Input Resistance				10^8		Ω
Output Current	Source Sink		+5 -130			mA µA
Short Circuit Current				20		mA
Small Signal Bandwidth				1		MHz
Slew Rate (Note 4)				5		V/µs

Note 1: Accuracy is specified for 0 to $7V_{rms}$, DC or 1kHz sinewave input with the AD536A connected as in Figure 2.
Note 2: Error vs. crest factor is specified as an additional error for $1V_{rms}$ rectangular pulse stream, pulse width = 200µs.
Note 3: Input voltages are expressed in volts rms, and error as % of reading.
Note 4: With 2kΩ external pulldown resistor.

True RMS-to-DC Converter

ELECTRICAL CHARACTERISTICS—AD536A (Continued)

(T_A = 25°C, $+V_S$ = +15V, $-V_S$ = -15V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Dual Supplies	Rated Performance	±3.0		±18	V
Single Supply	Rated Performance	+5		+36	V
Quiescent Current	Total V_S, 5V to 36V T_{MIN} to T_{MAX}		1.2	2	mA

ELECTRICAL CHARACTERISTICS—AD636 (T_A = 25°C, $+V_S$ = +3V, $-V_S$ = -5V, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSFER EQUATION				$V_{OUT} = [avg.(V_{IN})^2]^{½}$		
CONVERSION ACCURACY						
Total Error, Internal Trim (Notes 5,6)		AD636J AD636K			±0.5 ±0.6 ±0.2 ±0.3	mV ±% of Reading
Total Error vs. Temperature (0°C to +70°C)		AD636J AD636K			±0.1 ±0.01 ±0.1 ±0.005	mV ±% of Reading/°C
Total Error vs. Supply				±0.1 ±0.01		mV ±% of Reading/V
Total Error vs. DC Reversal	V_{IN} = 200mV	AD636J AD636K		±0.2 ±0.1		% of Reading
Total Error, External Trim (Note 5)		AD636J AD636K		±0.3 ±0.1 ±0.1 ±0.1		mV ±% of Reading
ERROR vs. CREST FACTOR (Note 3)						
	Crest Factor 1 to 2 Crest Factor = 3 Crest Factor = 6			Specified Accuracy -0.2 -0.5		% of Reading
FREQUENCY RESPONSE (Notes 6,8)						
Bandwidth for 1% Additional Error (0.09dB)	V_{IN} = 10mV V_{IN} = 100mV V_{IN} = 200mV			14 90 130		kHz
±3dB Bandwidth	V_{IN} = 10mV V_{IN} = 100mV			100 900		kHz
	V_{IN} = 200mV			1.5		MHz
AVERAGING TIME CONSTANT (Fig. 3)				25		ms/μF C_{AV}
INPUT CHARACTERISTICS						
Input Signal Range	Continuous rms, All Supplies			0 to 200		mV_{rms}
	Peak Transient +3V, -5V Supplies ±2.5V Supplies ±5V Supplies				±2.8 ±2 ±5	V_{PK}
Safe Input	All Supplies				±12	V_{PK}
Input Resistance			5.33	6.7	8.00	kΩ
Input Offset Voltage		AD636J AD636K			±0.5 ±0.2	mV

ELECTRICAL CHARACTERISTICS—AD636 (Continued)

(T_A = 25°C, $+V_S$ = +3V, $-V_S$ = -5V, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS (Note 5)						
Offset Voltage	T_A = +25°C	AD636J AD636K			±0.5 ±0.2	mV
	T_{MIN} to T_{MAX}			±10		µV/°C
	With Supply Voltage			±0.1		mV/V
Output Voltage Swing	+3V, -5V Supplies		0 to 1			V
	±5V to ±16.5V Supplies		0 to 1	+1.4		
Output Resistance			8	10	12	kΩ
dB OUTPUT						
Error	7mV ≤ V_{IN} ≤ 300mV	AD636J AD636K		±0.3 ±0.1	±0.5 ±0.2	dB
Scale Factor				-3		mV/dB
Scale Factor Tempco				+0.33 -0.033		%/°C dB/°C
I_{REF}	0dB = $1V_{rms}$		2	4	8	µA
I_{REF} Range			1		50	µA
I_{OUT} TERMINAL						
I_{OUT} Scale Factor				100		$\mu A/V_{rms}$
I_{OUT} Scale Factor Tolerance			-20	±10	+20	%
Output Resistance			8	10	12	kΩ
Voltage Compliance				$-V_S$ to $(+V_S - 2.0V)$		V
BUFFER AMPLIFIER						
Input and Output Voltage Range			$-V_S$ to $(+V_S - 2V)$			V
Input Offset Voltage	R_S = 10kΩ	AD636J AD636K		±0.8 ±0.5	±2 ±1	mV
Input Current				20	60	nA
Input Resistance				10^8		Ω
Output Current	Source Sink		+5 -130			mA µA
Short Circuit Current				20		mA
Small Signal Bandwidth				1		MHz
Slew Rate (Note 9)				5		V/µs
POWER SUPPLY						
Rated Performance Dual Supplies Single Supply			 +2/-2.5 +5	+3/-5	 ±16.5 +24	V
Quiescent Current (Note 10)				0.8	1	mA

Note 5: Accuracy is specified for 0 to 200mV, DC or 1kHz sinewave input. Accuracy is degraded at higher rms signal levels.
Note 6: Measured at pin 8 of DIP and S.O. (I_{OUT}), with pin 9 tied to COMMON.
Note 7: Error vs. crest factor is specified as an additional error for $200mV_{rms}$ rectangular pulse input, pulse width = 200µs.
Note 8: Input voltages are expressed in volts rms.
Note 9: With 10kΩ external pulldown resistor from pin 6 (BUF OUT) to $-V_S$.
Note 10: With BUF input tied to COMMON.

True RMS-to-DC Converter

Detailed Description

The AD536A/636 uses an implicit method of RMS computation that overcomes the dynamic range as well as other limitations inherent in a straightforward computation of the RMS. The actual computation performed by the AD536A/636 follows the equation:

$$V_{rms} = \text{Avg.}\ [V_{IN}^2 / V_{rms}]$$

The input voltage, V_{IN}, applied to the AD536A/636 is processed by an absolute value/voltage to current converter that produces a unipolar current I_1 (see Figure 1). This current drives one input of a squarer/divider that produces a current I_4 that has a transfer function:

$$I_4 = \frac{I_1^2}{I_3}$$

The current I_4 drives the internal current mirror through a low pass filter formed by R_1 and an external capacitor, C_{AV}. As long as the the time constant of this filter is greater than the longest period of the input signal, I_4 is averaged. The current mirror returns a current, I_3, to the square/divider to complete the circuit. The current I_4 is then a function of the average of (I_1^2/I_4) which is equal to I_1rms.

The current mirror also produces a $2 \cdot I_4$ output current, I_{OUT}, that can be used directly or converted to a voltage using resistor R2 and the internal buffer to provide a low impedance voltage output. The transfer function for the AD536A/636 is:

$$V_{OUT} = 2 \cdot R2 \cdot I_{rms} = V_{IN}$$

The dB output is obtained by the voltage at the emitter of Q3 which is proportional to the -log V_{IN}. The emitter follower Q5 buffers and level shifts this voltage so that the dB output is zero when the externally set emitter current for Q5 approximates I_3.

Standard Connection (Figure 2)

The standard rms connection requires only one external component, C_{AV}. In this configuration the AD536A/636 measures the rms of the AC and DC levels present at the input, but shows an error for low frequency inputs as a function of the C_{AV} filter capacitor. Figure 3 gives practical values of C_{AV} for various values of averaging error over frequency for the standard rms connections (no post filtering). If a 3μF capacitor is chosen, the additional error at 100Hz will be 1%. If the DC error can be rejected, a capacitor should be connected in series with the input, as would typically be the case in single supply operation.

The input and output signal ranges are a function of the supply voltages. Refer to the electrical characteristics for guaranteed performance. The buffer amplifier can be used either for lowering the output impedance of the circuit, or for other applications such as buffering high impedance input signals. The AD536A/636 can be used in current output mode by disconnecting the internal load resistor R_L from ground. The current output is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 40μA/Volt rms input for the AD536A and 100μA/Volt rms input for the AD636. The output is positive.

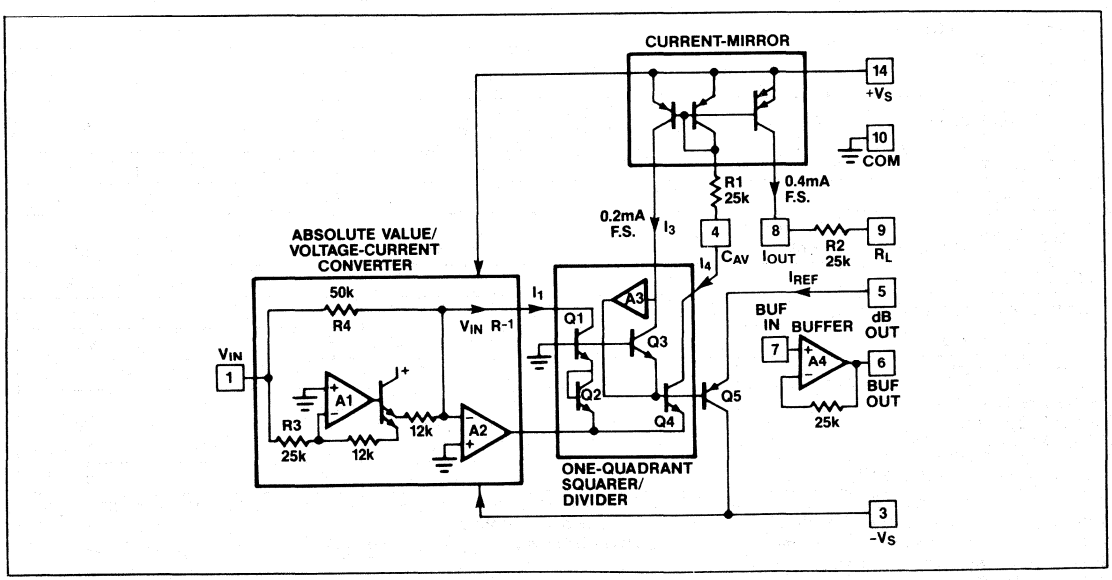


Figure 1. AD536A Simplified Schematic

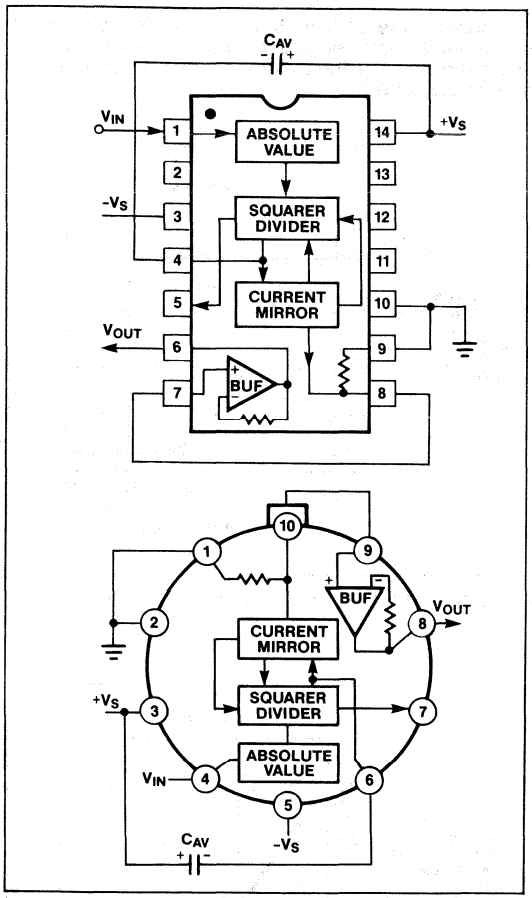


Figure 2. AD536A/AD636 Standard rms Connection

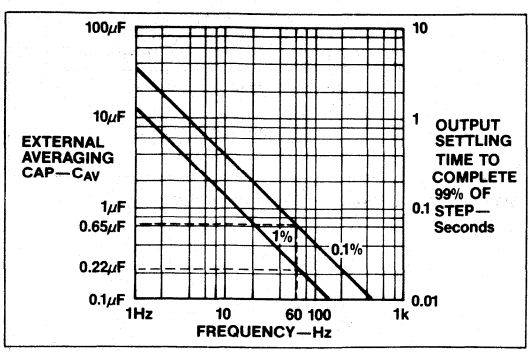
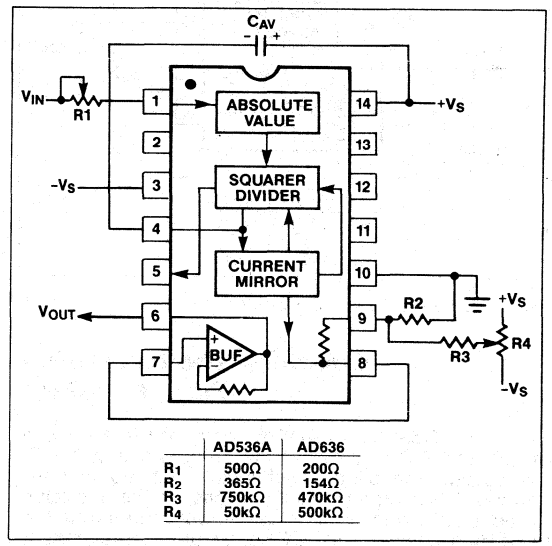


Figure 3. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 2

High Accuracy Adjustments

The accuracy of the AD536A/636 can be improved by the addition of external trims as shown in Figure 4. R4 trims the offset. The input should be grounded and R4 adjusted to give zero volts output from pin 6. R1 is trimmed to give the correct value for either a calibrated DC input or a calibrated AC signal. For example: 200mV DC input should give 200mV DC output, a ±200mV peak to peak sinewave should give 141mV DC output.



	AD536A	AD636
R_1	500Ω	200Ω
R_2	365Ω	154Ω
R_3	750kΩ	470kΩ
R_4	50kΩ	500kΩ

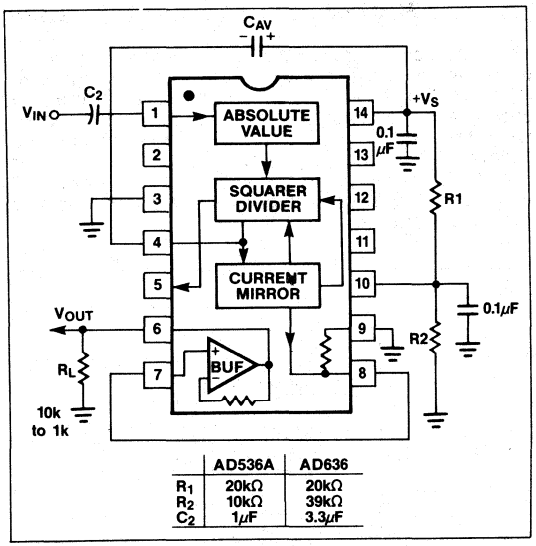
Figure 4. Optional External Gain and Output Offset Trims

Single Supply Operation

Both the AD536A and AD636 can be used with single supplies down to +5V. See Figure 5. The major limitation of this connection is that only AC signals can be measured since the differential input stage must be biased off ground for proper operation. The load resistor is necessary to provide output sink current. The input signal is coupled through C2 and the value chosen so that the desired low frequency break point is obtained with the input resistance of 16.7k ohms for the AD536A and 6.7k ohms for the AD636.

Figure 5 shows how to bias pin 10 within the range of the supply voltage (pin 2 on "H" packages). It is critical that no extraneous signals are coupled into this pin. A capacitor connected between pin 10 and ground is recommended. The common pin requires less than 5μA of input current, and if the current flowing through the resistors R1 and R2 is chosen to be approximately 10 times the common pin current, or 50μA, the resistor values can easily be calculated.

True RMS-to-DC Converter



	AD536A	AD636
R_1	20kΩ	20kΩ
R_2	10kΩ	39kΩ
C_2	1µF	3.3µF

Figure 5. Single Supply Operation

Choosing the Averaging Time Constant

Both the AD536A and AD636 compute the rms value of AC and DC signals. At low frequencies and DC, the output tracks the input exactly; at higher frequencies, the average output approaches the rms value of the input signal. The actual output differs from the ideal by an average (or DC) error plus some amount of ripple.

The DC error term is a function of the value of C_{AV} and the input signal frequency. The output ripple is inversely proportional to the value of C_{AV}. Waveforms with high crest factors, such as a pulse train with low duty cycle, should have an average time constant chosen to be at least ten times the signal period.

Using a large value of C_{AV} to remove the output ripple increases the settling time for a step change in the input signal level. Figure 3 shows the relationship between C_{AV} and settling time, where 115ms settling equals 1µF of C_{AV}. The settling time, or time for the rms converter to settle to within a given percent of the change in rms level, is set by the averaging time constant, which varies approximately 2:1 between increasing and decreasing input signals. For example, increasing input signals require 2.3 time constants to settle to within 1% and 4.6 time constants for decreasing signals levels.

In addition, the settling time also varies with input signal levels, increasing as the input signal is reduced, and decreasing as the input is increased as shown in figures 6(a) and 6(b).

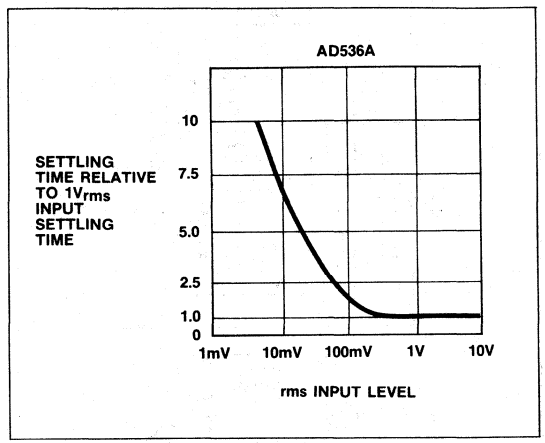


Figure 6A. AD536A Settling Time vs. Input Level

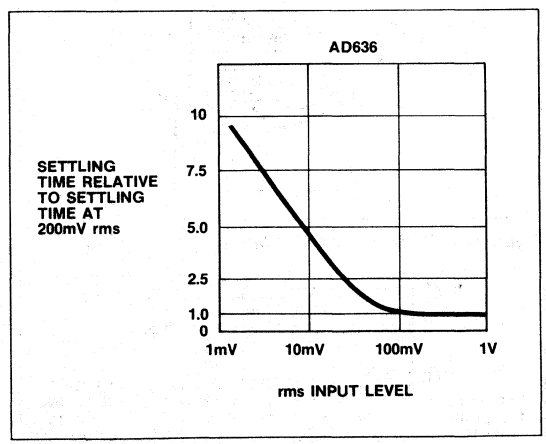


Figure 6B. AD636 Settling Time vs. Input Level

Using Post Filters

A post filter allows a smaller value of C_{AV}, and reduces ripple and improves the overall settling time. The value of C_{AV} should be just large enough to give the maximum DC error at the lowest frequency of interest. The post filter is used to remove excess output ripple. Figures 7, 8 and 9 give recommended filter connections and values for both the AD536A and AD636. Table 1 lists the number of time constants required for the rms section to settle to within different percentages of the final value for a step change in the input signal.

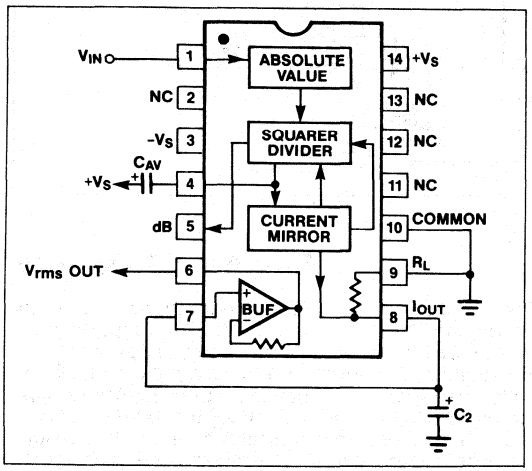


Figure 7. AD536A/AD636 with a 1 Pole Output Filter

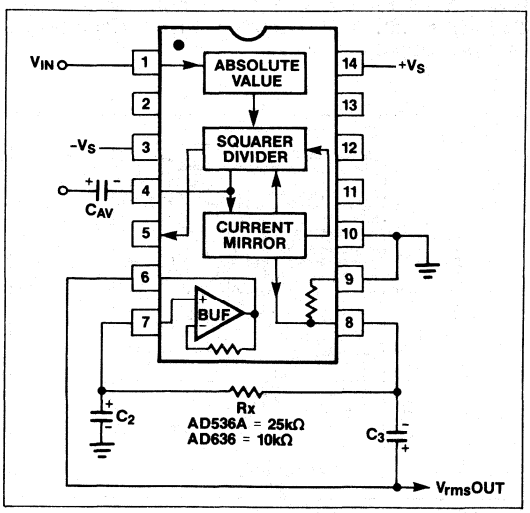
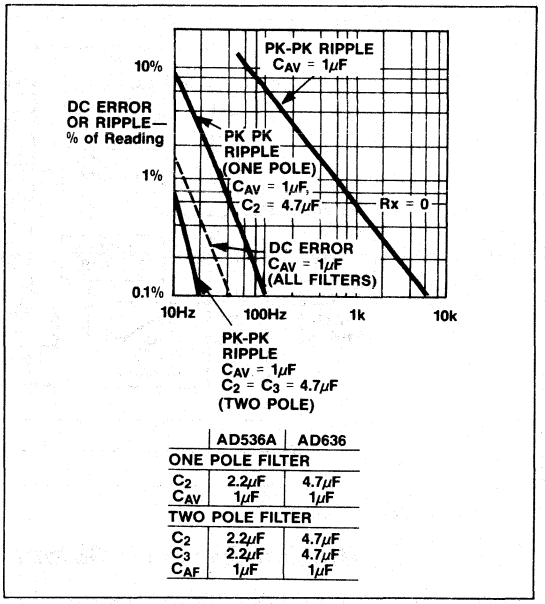


Figure 8. AD536A/AD636 with a 2 Pole Output Filter



	AD536A	AD636
ONE POLE FILTER		
C_2	2.2μF	4.7μF
C_{AV}	1μF	1μF
TWO POLE FILTER		
C_2	2.2μF	4.7μF
C_3	2.2μF	4.7μF
C_{AF}	1μF	1μF

Figure 9. Performance Features of Various Filter Types for AD536A/AD636

Table 1. Number of RC Time Constants (τ) Required for AD536A, AD636, rms Converters to Settle to Within Stated % of Final Value

	For Increasing Amplitudes	For Decreasing Amplitudes
Basic Formulas	$\Delta V\sqrt{1-e^{-T/RC}}$	$\Delta V\sqrt{e^{-T/RC}}$
Settling Time to Within Stated % of New rms Level		
1%	2.0τ (4.6τ)	4.6τ (4.6τ)
0.1%	3.1τ (6.9τ)	6.9τ (6.9τ)
0.01%	4.2τ (9.2τ)	9.2τ (9.2τ)
(τ) Settling Times for Linear RC Filter		

True RMS-to-DC Converter

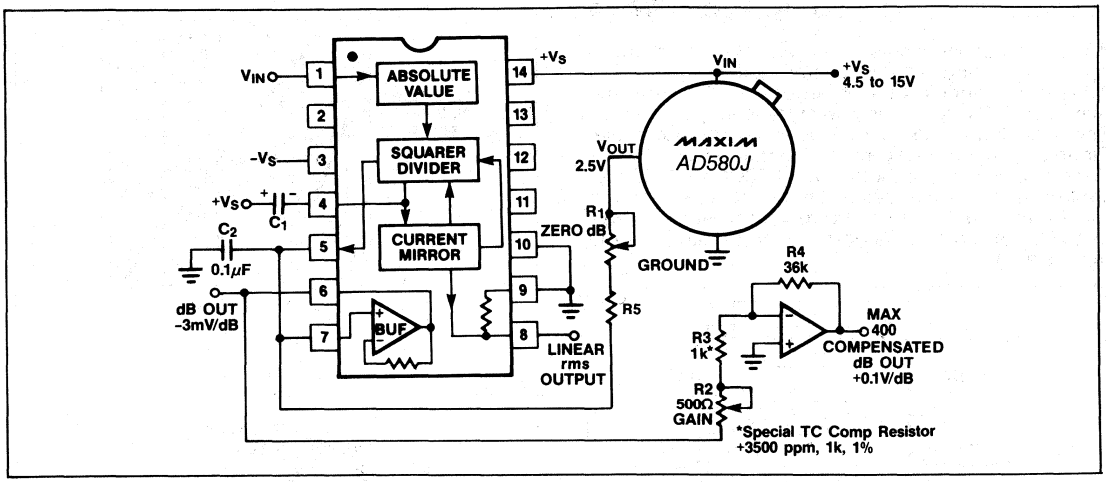


Figure 10. dB Connection

The Decibel (dB) Output

The dB output of the AD536A/636 originates in the squarer/divider section and works well over a 60dB range. The connection for dB measurements is shown in Figure 10. The dB output has a temperature drift of 0.03dB/°C and in some applications may need to be compensated. Figure 10 shows a compensation scheme. The amplifier can be used to scale the output for a particular application. The values used in Figure 10 give an output of +100mV/dB.

Frequency Response

The AD536A/636 utilizes a logarithmic circuit in performing the rms computation of the input signal. The bandwidth of the rms converters are proportional to signal level. Figures 11 and 12 represent the frequency response of the converters from 10mV to 7V_{rms} for the AD536A and 1mV to 1V for the AD636 respectively. The dashed lines indicate the upper frequency limits for 1%, 10%, and ±3dB of reading additional error. Caution must be used when designing rms measuring systems so that overload does not occur. The input clipping level for the AD636 is ±12V, and for the AD536A it is ±20V. A 7V_{rms} signal with a crest factor of 3 has a peak input of 21 volts!

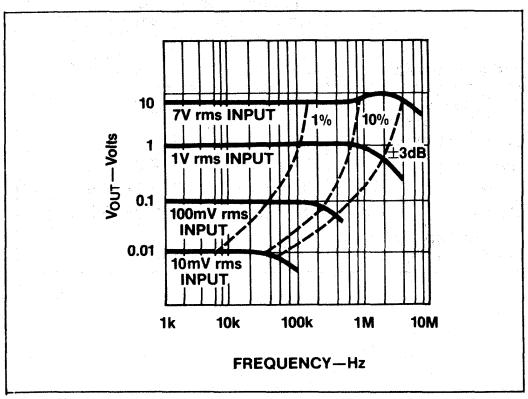


Figure 11. AD536A High Frequency Response

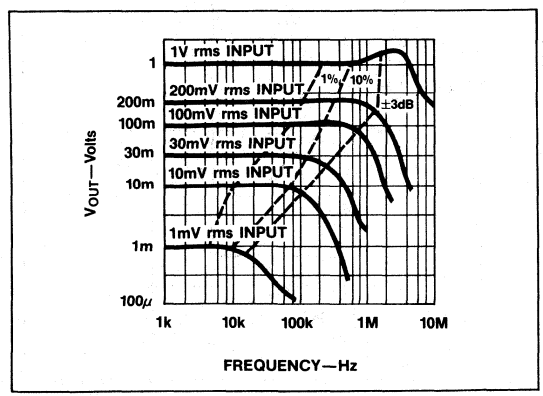


Figure 12. AD636 High Frequency Response

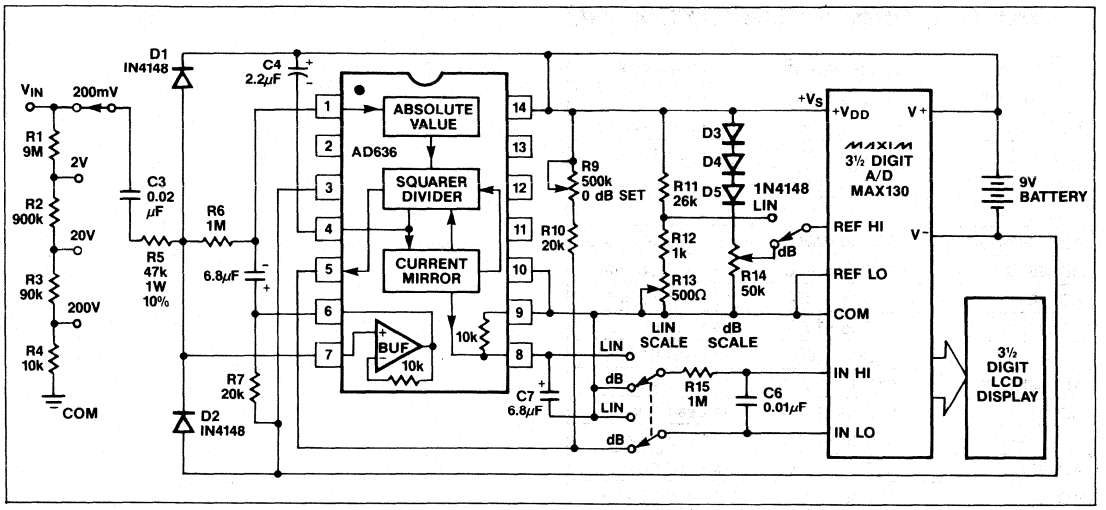


Figure 13. A Portable, High Z Input, rms DPM and dB Meter

Application in a low cost DVM

A low cost digital voltmeter (DVM) using just two integrated circuits plus supporting circuitry and LCD display is shown in Figure 13. The MAX130 is a 3½ digit integrating A/D converter with precision band-gap reference. The 10Mohm input attenuator is AC coupled to pin 6 of the AD636 buffer amplifier. The output from the AD636 is connected to the MAX130 to give a direct reading to the LCD display.

True RMS-to-DC Converter

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*
AD536AKQ*	0°C to +70°C	14 Lead CERDIP
AD536ASD	-55°C to +125°C	14 Lead Ceramic
AD536ASH	-55°C to +125°C	10 Lead TO-100
AD536ASQ*	-55°C to +125°C	14 Lead CERDIP
AD636JC/D	0°C to +70°C	Dice
AD636JCWE	0°C to +70°C	16 Lead Wide S.O.
AD636JD	0°C to +70°C	14 Lead Ceramic
AD636JH	0°C to +70°C	10 Lead TO-100
AD636JN	0°C to +70°C	14 Lead Plastic DIP
AD636JQ*	0°C to +70°C	14 Lead CERDIP
AD636KCWE	0°C to +70°C	16 Lead Wide S.O.
AD636KD	0°C to +70°C	14 Lead Ceramic
AD636KH	0°C to +70°C	10 Lead TO-100
AD636KN	0°C to +70°C	14 Lead Plastic DIP
AD636KQ*	0°C to +70°C	14 Lead CERDIP

** Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages*

MAXIM

Operational Amplifiers and Buffers

Operational Amplifiers

Bipolar, Chopper Stabilized and Programmable Gain

Part Number	Initial V_{OS} (μV max)	V_{OS} Tempcos (μV/°C max)	I_{BIAS} (pA max)	Supply Voltage	Supply Current (mA max)	Noise DC-1Hz (μV pk-pk typ)	Features	Page No.
MAX400	10	0.3	2000	±3V to ±18V	4.0	0.15	Non-Chopped	5-1
MAX420	10	0.05	30	±2.5V to ±16.5V	2.0	0.3	±15V Operation	5-5
MAX421	10	0.05	30	±2.5V to ±16.5V	2.0	0.3	±15V Operation	5-5
MAX422	10	0.05	30	±2.5V to ±16.5V	0.5	0.4	Low Current	5-5
MAX423	10	0.05	30	±2.5V to ±16.5V	0.5	0.4	Low Current	5-5
MAX430	10	0.05	30	±2.5V to ±16.5V	2.0	0.3	No Ext Capacitors	5-17
MAX432	10	0.05	30	±2.5V to ±16.5V	0.5	0.4	No Ext Capacitors	5-17
ICL7650	5	0.05	10	±2.25V to ±8V	2.0	0.7	Low I_{BIAS}	5-65
ICL7650B	10	0.1	20	±2.25V to ±8V	2.0	0.7	Lowest Cost	5-65
ICL7652	5	0.05	30	±2.5V to ±8V	2.0	0.2	Lowest Noise	5-75
LT1001	15	0.6	4000	±3V to ±18V	2.5	0.15	Non-Chopped	5-113
OP07A	25	0.6	2000	±3V to ±18V	4.0	0.15	Non-Chopped	5-117
OP07E	75	1.3	4000	±3V to ±18V	4.0	0.15	Non-Chopped	5-117
PGA100	500	6 typ	1000	+5V and ±8V to ±15V		0.2	Programmed Gain and Input Mux	5-123

CMOS

Part Number	Description	Compensation	Offset Null	V_{OS} Selection (mV max.)	Ios (pA typ.)	I_B (pA typ.)	Page No.
ICL7611	Single, Selectable I_Q	Internal	Yes	2, 5, 15	0.5	1	5-49
ICL7612	Single, Selectable I_Q Extended CMVR	Internal	Yes	2, 5, 15	0.5	1	5-49
ICL7614	Single, Fixed I_Q	External	Yes	2, 5, 15	0.5	1	5-49
ICL7616	Single, Selectable I_Q Extended CMVR	Internal	Yes	2, 5, 15	0.5	1	5-49
ICL7621	Dual, Fixed I_Q	Internal	No	2, 5, 15	0.5	1	5-49
ICL7622	Dual, Fixed I_Q	Internal	Yes	2, 5, 15	0.5	1	5-49
ICL7631	Triple, Selectable I_Q	Internal	No	5, 10, 20	0.5	1	5-49
ICL7632	Triple, Selectable I_Q	None	No	5, 10, 20	0.5	1	5-49
ICL7641	Quad, Fixed I_Q	Internal	No	5, 10, 20	0.5	1	5-49
ICL7642	Quad, Fixed I_Q	Internal	No	5, 10, 20	0.5	1	5-49

Video Amplifiers and Buffers

Part Number	Type	Bandwidth (MHz)	Slew Rate (V/μs)	Output Current (mA)	Features	Page No.
MAX450	Video Op Amp	10	70	30	Drives 75Ω	5-25
MAX451	Video Op Amp	10	70	30	1nA max I_{BIAS}	5-25
MAX452	Video Amp	50	150	20	Drives 75Ω	5-29
MAX453	Video Mux/Amp	50	150	20	2 Ch Input max	5-29
MAX454	Video Mux/Amp	50	150	20	4 Ch Input max	5-29
MAX455	Video Mux/Amp	50	150	20	8 Ch Input max	5-29
MAX460	Video Buffer	100	1500	100	Low I_B and C_{IN}	5-37
AD3554	Video Op Amp	1200	1000	100	High Gain	5-43
BB3553	Video Buffer	300	6000	200	Drive 50Ω	5-95
BB3554	Video Op Amp	1700	1000	100	High Gain	5-43
LH0033	Video Buffer	100	1500	100	Drives 75Ω	5-85
LH0063	Video Buffer	300	6000	200	Drives 50Ω	5-95
LH0101	Power Op Amp	5	10	2000	0.008% THD	5-101

MAXIM

Ultra Low Offset Voltage Operational Amplifier

General Description

The MAX400 guaranteed maximum 10μV offset error is the lowest input offset voltage of any commercially available (nonchopper) monolithic amplifier. The MAX400 represents a 2.5 times improvement over the highest grade OP07 (the OP07A), and a 5 times improvement over the best commercial temperature range device (OP07E). The offset voltage drift is guaranteed to be a maximum of 0.3μV/°C which is also an improvement over the OP07 family.

For the ultimate in DC performance (5μV maximum offset voltage and 0.05μV/°C maximum offset voltage drift) the MAX420 and MAX430 series of ±15V monolithic chopper stabilized amplifiers should be consulted.

Applications

Precision Amplifiers
Thermocouple Amplifiers
Low Level Signal Processing
Medical Instrumentation
Strain Gauge Amplifiers
High Accuracy Data Acquisition

Features

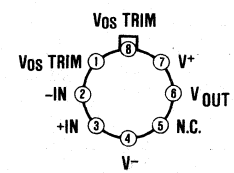
- **Ultra Low Offset Voltage: 10μV (max.)**
- **Ultra Low Offset Voltage Drift: 0.2μV/°C**
- **Ultra Stable vs. Time: 0.2μV/Month**
- **Ultra Low Noise 0.35μV_{p-p}**
- **Wide Supply Voltage: ±3V to ±18V**
- **High Common Mode Input: ±14V**
- **No External Components Required**
- **Fits OP07, AD510, 725, 108A/308A Sockets**

Ordering Information

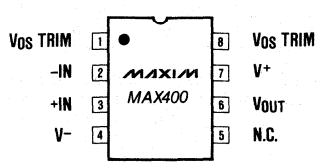
PART	TEMP. RANGE	PACKAGE
MAX400MJA	-55°C to +125°C	8 Lead CERDIP
MAX400MTV	-55°C to +125°C	8 Lead TO-99
MAX400EJA	-40°C to +85°C	8 Lead CERDIP
MAX400ETV	-40°C to +85°C	8 Lead TO-99
MAX400CTV	0°C to +70°C	8 Lead TO-99
MAX400CPA	0°C to +70°C	8 Lead Plastic DIP
MAX400CSA	0°C to +70°C	8 Lead Small Outline

Pin Configuration

Top View

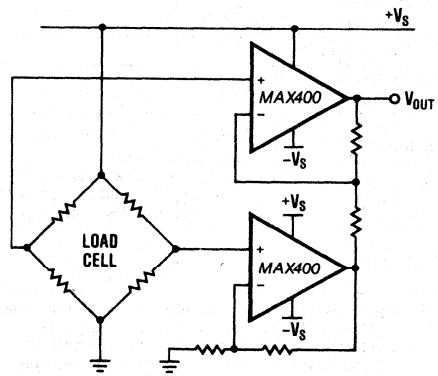


8 Lead TO-99



8 Lead Dip

Typical Operating Circuit



Load Cell Amplifier

5

Ultra Low Offset Voltage Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... ±22V
Internal Power Dissipation 500mW
TO-99(T) — derate at 7.1mW/°C above +80°C
Hermetic Dip(J) — derate at 6.7mW/°C above +75°C
Plastic Dip(P) — derate at 5.6mW/°C above +36°C
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
MAX400M ..... -55°C to +125°C
MAX400E ..... -40°C to +85°C
MAX400C ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Duration of Output Short Circuit ..... Indefinite
Junction Temperature (T_J) ..... -65°C to +160°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX400M			MAX400C/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 2)		4	10		10	15	µV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 3)		0.2	1.0		0.2	1.0	µV/ Month
Input Offset Current	I_{OS}			0.3	2.0		0.3	2.0	nA
Input Bias Current	I_B			±0.7	±2.0		±0.7	±2.0	nA
Input Noise Voltage	$e_{N\,P-P}$	0.1Hz to 10Hz (Note 4)		0.35	0.6		0.35	0.6	μV_{P-P}
Input Noise Voltage Density	e_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	$I_{N\,P-P}$	0.1Hz to 10Hz (Note 4)		14	30		14	30	pA_{P-P}
Input Noise Current Density	I_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance Differential-Mode	R_{IN}	(Note 5)	30	80		20	60		MΩ
Input Resistance Common-Mode	R_{INCM}			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	114	126		114	126		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		4	10		4	10	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O$ = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 5)	500 150	1000 400		500 150	1000 400		V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V

Note 2: V_{OS} is measured one minute after application of power.
Note 3: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV — refer to typical performance curves. Parameter is sample tested.
Note 4: Sample tested.
Note 5: Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX400M			MAX400C/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 6)	0.1	0.3		0.1	0.3		V/μS
Closed-Loop Bandwidth	BW	A_{VCL} = +1V (Note 6)	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0V, I_O = 0		60			60		Ω
Power Consumption	P_D	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		75 4	120 6	mW
Offset Adjustment Range		R_P = 20kΩ		±4			±4		mV

Note 6: Sample tested.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = Full Operating Temperature Range, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX400M			MAX400C/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 7)		20	40		20	40	μV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}	(Note 8)		0.2	0.3		0.2	0.3	μV/°C
Input Offset Current	I_{OS}			0.8	4.0		0.8	4.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 9)		5	25		5	25	pA/°C
Input Bias Current	I_B			±1.0	±4.0		±1.0	±4.0	nA
Average Input Bias Current Drift	TCI_B	(Note 9)		8	25		8	25	pA/°C
Input Voltage Range	IVC		±13	±13.5		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	106	123		106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		5	20		5	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	200	400		200	400		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6		±12.0	±12.6		V

Note 7: Offset Voltage is measured one minute after application of power.
Note 8: 100% tested.
Note 9: Sample tested.

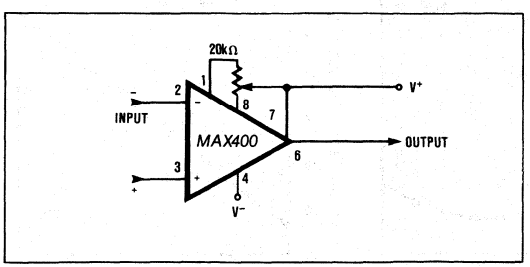


Figure 1. Optional Offset Nulling Circuit.

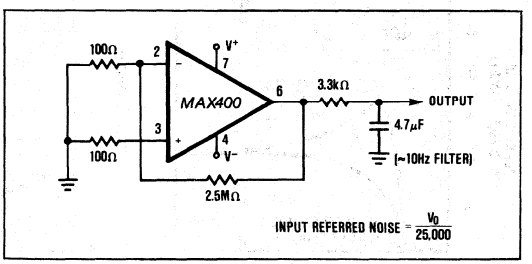
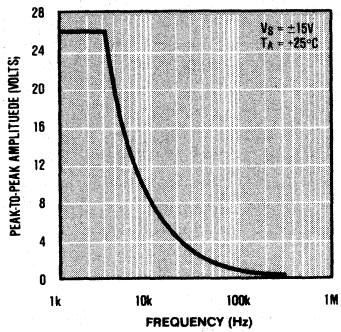


Figure 2. Low Frequency Noise Test Circuit.

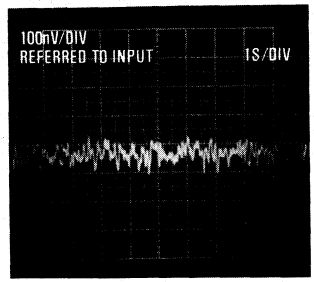
Ultra Low Offset Voltage Operational Amplifier

Typical Operating Characteristics

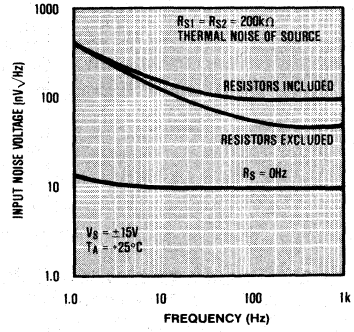
MAXIMUM OUTPUT SWING vs. FREQUENCY



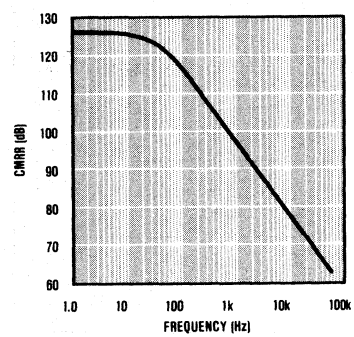
LOW FREQUENCY NOISE



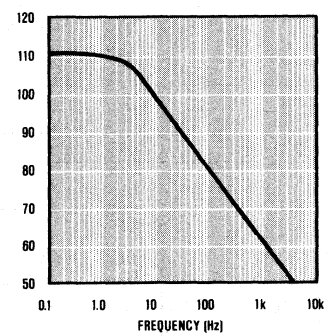
TOTAL INPUT NOISE VOLTAGE vs. FREQUENCY



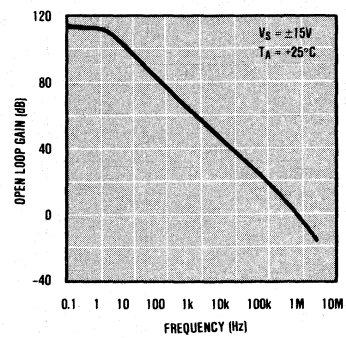
CMRR vs. FREQUENCY



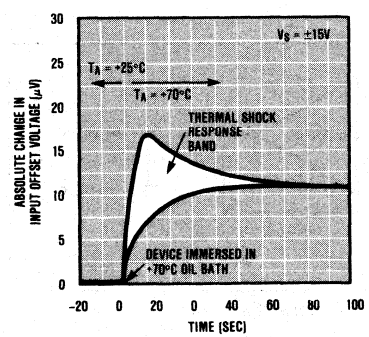
PSRR vs. FREQUENCY



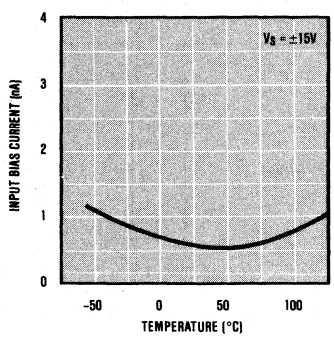
OPEN LOOP FREQUENCY RESPONSE



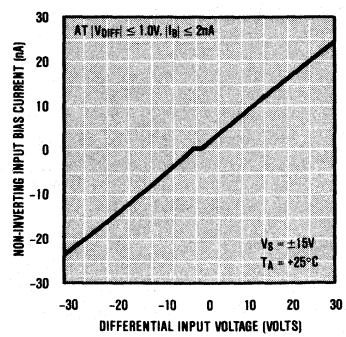
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



INPUT BIAS CURRENT vs. TEMPERATURE



INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



MAXIM

±15 Volt Chopper Stabilized Operational Amplifier

General Description

The MAX420, 421, 422, and 423 are a series of ±15V CMOS chopper-stabilized amplifiers, designed for high accuracy amplification, signal conditioning and instrumentation applications. These devices offer input offset and drift specification superior to previous "precision" bipolar amplifiers and monolithic choppers. The maximum offset is 5.0μV while the guaranteed drift limit is 0.05μV/°C.

The combination of ±15 volt operation, low power, and standard op-amp pin configuration allows these devices to virtually "plug-in" replace conventional lower-performance amplifiers. The only additional components required are two external capacitors. A wide input voltage range specification, that includes the negative supply, allows for the amplification of signals including ground in single-supply applications.

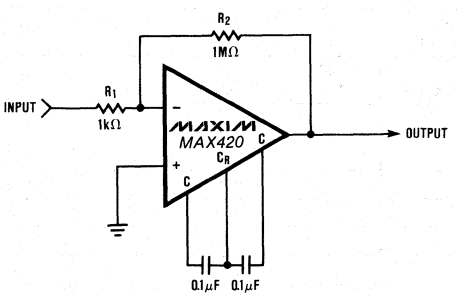
The MAX420 (8 pin) and MAX421 (14 pin) have a maximum supply current of 2mA. The MAX422 (8 pin) and MAX 423 (14 pin) are low power amplifiers with a maximum current of 0.5mA.

Applications

Precision Amplifiers
Signal Conditioning for:
- Thermocouples
- Strain Gauges, Load Cells
- Platinum Temperature Sensors
- Thermistors, Bridges

High Accuracy Data Acquisition
D.C. Stabilization of Amplifiers and Systems

Typical Operating Circuit



Inverting Amplifier

Features

- **5μV Max Offset Voltage**
- **±15V Supply Operation**
- **Input Voltage Range: +12V to -15V**
- **Low Input Noise: $0.3\mu V_{p-p}$ (DC - 1Hz)**
- **High Gain, CMRR, PSRR: 120dB**
- **Low Power CMOS Design: 0.5mA Max Supply Current (MAX422/423)**
- **Low Input Bias Current: 30pA Max**

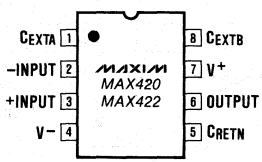
Ordering Information

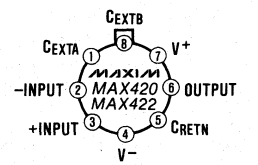
PART	TEMP. RANGE	PACKAGE
MAX420CPA	0°C to +70°C	8 Lead Plastic DIP
MAX420EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX420MTV	-55°C to +125°C	TO-99 Metal Can
MAX421CPD	0°C to +70°C	14 Lead Plastic DIP
MAX421CWE	0°C to +70°C	16 Lead Small Outline
MAX421C/D	0°C to +70°C	Dice
MAX421EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX421MJD	-55°C to +125°C	14 Lead CERDIP

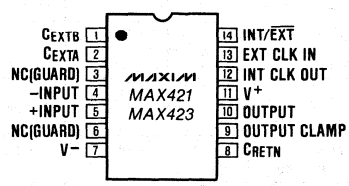
(Ordering information continued on last page)

Pin Configurations

Top View







NC = No internal connection.

(Pin Configurations continued on last page)

±15 Volt Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Voltage ..... (V^+ + 0.3) to (V^- – 0.3) V
Storage Temperature Range ..... –65°C to +160°C
Operating Temperature Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... +300°C
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite

Current Into Any Pin 10mA
Continuous Total Power Dissipation (T_A = +25°C)
CERDIP Package 500mW
Plastic Package 375mW
TO-99 ..... 250mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS MAX420, MAX421

(V^+ = +15V, V^- = –15V, T_A = +25°C. Test circuit unless noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C	C E,M		±1 ±1	±10 ±5	µV
		Over Temperature Range (Note 1, 2)	C E,M		±2 ±2	±20 ±10	µV
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Over Temperature Range (Note 1, 2)	E,M		0.02	0.05	µV/°C
Input Bias Current	I_B	T_A = +25°C	C E,M		10 10	100 30	pA
		Over Temperature Range (Note 1)	C E M		30 35 0.5	 5	pA pA nA
Input Offset Current	I_{OS}	T_A = +25°C	C E,M		15 15	200 60	pA
		Over Temperature Range (Note 1)	C E M		30 50 0.5	 10	pA pA nA
Input Resistance	R_{IN}				10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±10V, T_A = +25°C Over Temperature Range (Note 1)		120 120	150 150		dB
Output Voltage Swing	V_{OUT}	CLAMP not connected (note 3)	R_L = 10kΩ R_L = 100kΩ	±12	±14.5 ±14.95		V
Common-Mode Voltage Range	CMVR			+12, –15	+12.5, –15.1		V
Common-Mode Rejection Ratio	CMRR	CMVR = +12V to –15V, T_A = +25°C Over Temperature Range (Note 1)		120 110	140 140		dB
Power Supply Rejection Ratio	PSRR	±3V to ±16.5V, T_A = 25°C Over Temperature Range (Note 1)		120 110	140 140		dB
Input Noise Voltage (P-P value not exceeded 95% of time)	$e_{N_{p-p}}$	R_S = 100Ω, DC to 1Hz DC to 10 Hz			0.3 1.1		μV_{p-p}
Input Noise Current	I_N	f = 10Hz			0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW				500		kHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ			0.5		V/µs
Rise Time	t_r				0.7		µs
Overshoot					20		%

Note 1: Operating temperature range for "C" parts is 0°C to +70°C, for "E" parts is –40°C to +85°C, and for "M" parts is –55°C to +125°C.
Note 2: Guaranteed by design.
Note 3: The OUTPUT CLAMP, pin 9 on MAX421, when connected to the inverting input (pin 4), reduces the overload recovery time inherent with chopper-stabilized amplifiers (see text).
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883C, Method 3015.2 Test Circuit).

ELECTRICAL CHARACTERISTICS MAX420, MAX421 (continued)

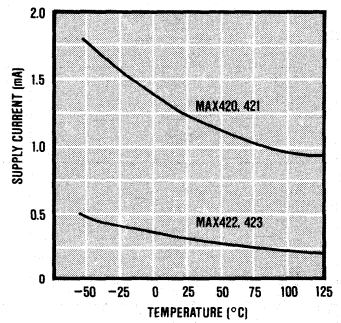
(V^+ = +15V, V^- = -15V, T_A = +25°C. Test circuit unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Supply Range	V^+, V^-		±2.5		±16.5	V
Supply Current	I_S	No Load, T_A = +25°C Over Temperature Range (Note 1)		1.3	2.0 3.5	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (MAX421)		400		Hz
Clamp ON Current (Note 3)	$I_{CLP\ (ON)}$	R_L = 100kΩ	25	100		µA
Clamp OFF Current (Note 3)	$I_{CLP\ (OFF)}$	$-10V \leq V_{OUT} \leq +10V$		1		pA
Offset Voltage vs. Time				100		$nV/\sqrt{month}$

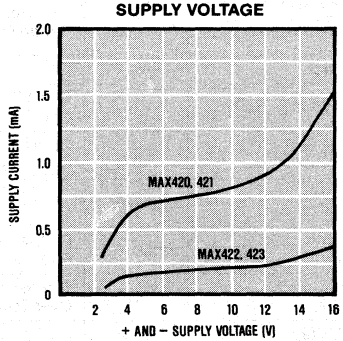
Note 1: Operating temperature range for "C" parts is 0°C to +70°C, for "E" parts is -40°C to +85°C, and for "M" parts is -55°C to +125°C.
Note 2: Guaranteed by design.
Note 3: The OUTPUT CLAMP, pin 9 on MAX421, when connected to the inverting input (pin 4), reduces the overload recovery time inherent with chopper-stabilized amplifiers (see text).
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883C, Method 3015.2 Test Circuit).

Typical Operating Characteristics

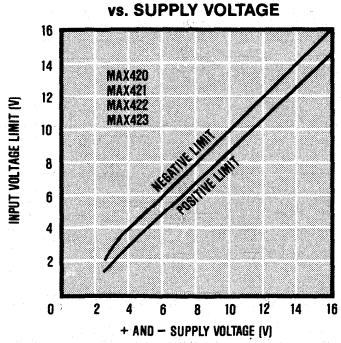
SUPPLY CURRENT vs. TEMPERATURE



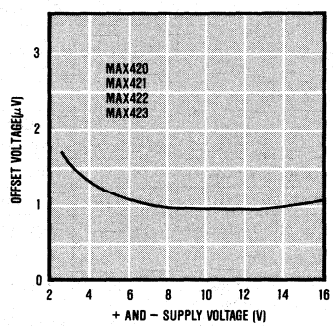
SUPPLY CURRENT vs. SUPPLY VOLTAGE



INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



5

±15 Volt Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS: same as for MAX420, 421

ELECTRICAL CHARACTERISTICS MAX422, MAX423

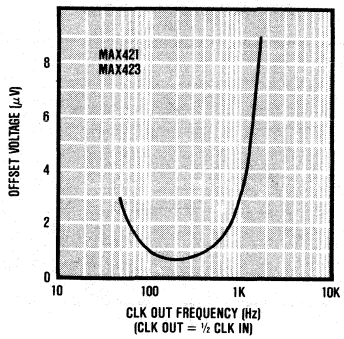
(V^+ = +15V, V^- = -15V, T_A = +25°C. Test circuit unless noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C	C E,M		±1 ±1	±10 ±5	µV
		Over Temperature Range (Note 1, 2)	C E,M		±2 ±2	±20 ±10	µV
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Over Temperature Range (Note 1, 2)	E,M		0.02	0.05	µV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_B	T_A = +25°C	C E,M		10 10	100 30	pA
		Over Temperature Range (Note 1)	C E M		30 35 0.5	 5	pA pA nA
Input Offset Current (Doubles every 10°C above about 60°C)	I_{OS}	T_A = +25°C	C E,M		15 15	200 60	pA
		Over Temperature Range (Note 1)	C E M		30 50 0.5	 10	pA pA nA
Input Resistance	R_{IN}				10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 100kΩ, V_{OUT} = ±10V, T_A = +25°C Over Temperature Range (Note 1)		120 120	150 150		dB
Output Voltage Swing	V_{OUT}	CLAMP not connected (Note 3) R_L = 100kΩ		±14	±14.6		V
Common-Mode Voltage Range	CMVR			+12, -15	+12.5, -15.1		V
Common-Mode Rejection Ratio	CMRR	CMVR = +12V to -15V, T_A = +25°C Over Temperature Range (Note 1)		120 110	140 140		dB
Power Supply Rejection Ratio	PSRR	±3V to ±16.5V, T_A = +25°C Over Temperature Range (Note 1)		120 110	140 140		dB
Input Noise Voltage (P-P value not exceeded 95% of time)	$e_{N_{p-p}}$	R_S = 100Ω, DC to 1Hz DC to 10Hz			0.4 1.2		μV_{p-p}
Input Noise Current	I_N	f = 10Hz			0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW				125		kHz
Slew Rate	SR	C_L = 50pF, R_L = 100kΩ			1.25		V/µs
Rise Time	t_r				2.8		µs
Overshoot					20		%
Operating Supply Range	V^+, V^-			±2.5		±16.5	V
Supply Current	I_S	No Load, T_A = +25°C Over Temperature Range (Note 1)			0.3	0.5 1	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (MAX423)			250		Hz
Clamp ON Current (Note 3)	$I_{CLP\ (ON)}$	R_L = 1MΩ		5	25		µA
Clamp OFF Current (Note 3)	$I_{CLP\ (OFF)}$	$-10V \le V_{OUT} \le +10V$			1		pA
Offset Voltage vs. Time					100		$nV/\sqrt{month}$

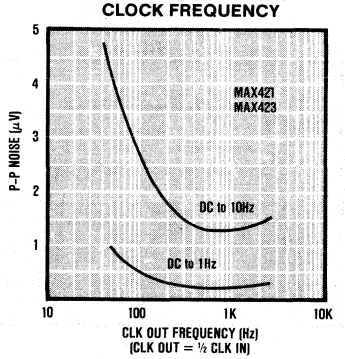
Note 1: Operating temperature range for "C" parts is 0°C to +70°C, for "E" parts is -40°C to +85°C, and for "M" parts is -55°C to +125°C.
Note 2: Guaranteed by design.
Note 3: The OUTPUT CLAMP, pin 9 on MAX423, when connected to the inverting input (pin 4), reduces the overload recovery time inherent with chopper-stabilized amplifiers (see text).
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883C, Method 3015.2 Test Circuit).

Typical Operating Characteristics

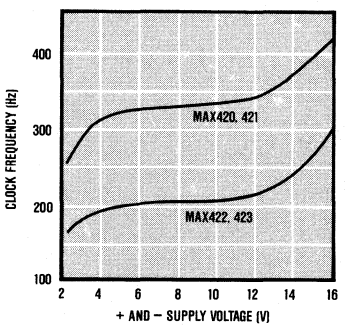
INPUT OFFSET VOLTAGE vs. CLOCK FREQUENCY



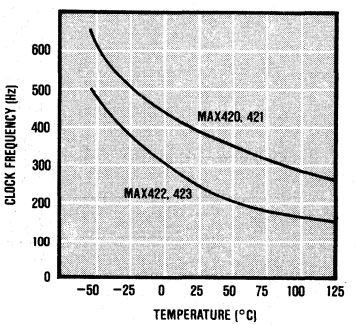
P-P NOISE VOLTAGE vs. CLOCK FREQUENCY



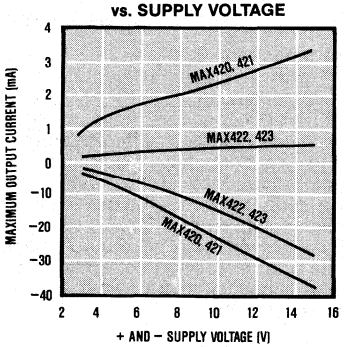
CLOCK FREQUENCY vs. SUPPLY VOLTAGE



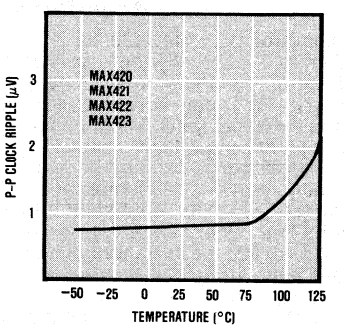
CLOCK FREQUENCY vs. TEMPERATURE



MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



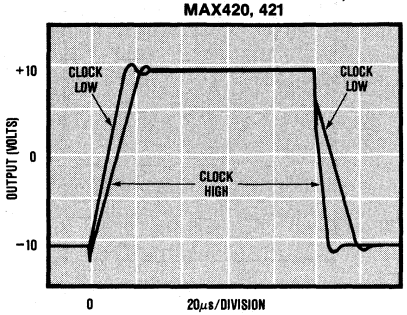
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



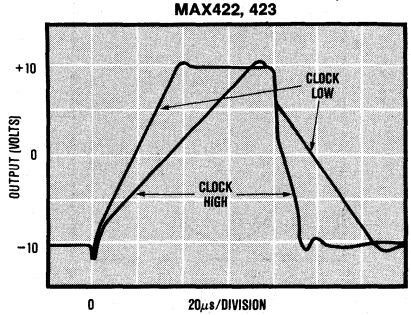
±15 Volt Chopper Stabilized Operational Amplifier

Typical Operating Characteristics

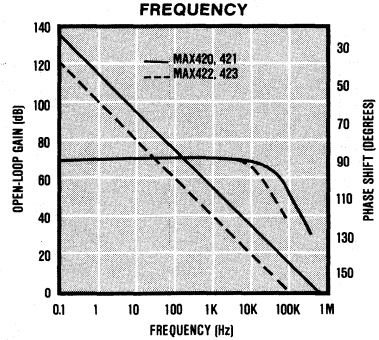
FOLLOWER LARGE SIGNAL PULSE RESPONSE, MAX420, 421



FOLLOWER LARGE SIGNAL PULSE RESPONSE, MAX422, 423



OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



Detailed Description

Amplifier Operation

A block diagram of a MAX420 series amplifier is shown in Figure 2. Internally there are two amplifiers, a main amp and a nulling amp. The main amplifier is in the primary signal path and is continuously connected to the external inputs. The null amp alternately corrects its own offset, and then that of the main amp, as its input switches between the two main amp inputs. Offset correction is accomplished by means of compensating FETs in the input stage's bias circuitry (not shown). The offset values that drive these trim FETs are stored for the duration of the correction cycle on two capacitors, C_{EXTA} and C_{EXTB}. Each cycle is controlled by the clock as shown in the timing diagram of Figure 2. An added benefit of the offset correction scheme is that it also increases CMRR, PSRR, and A_{VOL} at low frequencies ($f_{IN} \ll f_{CLK}$).

Capacitor Selection

Two external capacitors, C_{EXTA} and C_{EXTB}, connected as shown in Figure 1, enable the amplifier to store and correct its own offset errors. The MAX420 series is specified with 0.1μF capacitors, however, other values up to 1.0μF may be optimal if different clock rates are used (MAX421, 423 only). If an external clock is used, the capacitor values should be scaled to roughly maintain the ratio between the nominal self-clock period (2.5ms @ 400Hz) and 0.1μF. For example, if a 200Hz clock were used, then 0.2μF would be best. This relationship is not critical and certainly no change in capacitor value is necessary for part-to-part variations in the internal clock rate.

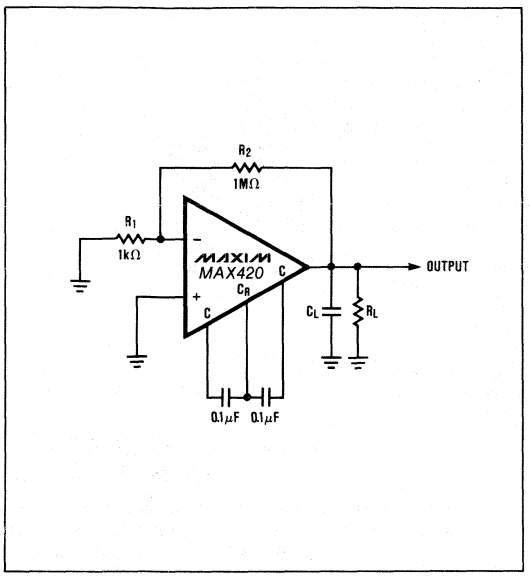


Figure 1. Test Circuit.

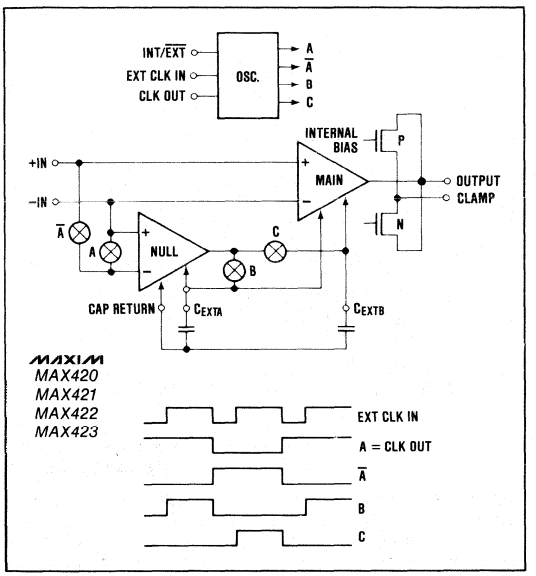


Figure 2. Maxim MAX420 Series Amplifier Block Diagram.

The banded or outer foil end of the correction capacitors should be connected to C_{RETN} as this is a low impedance point. C_{EXTA} and C_{EXTB} are high impedance nodes and so the connections to these pins should be as short as possible to minimize noise pick-up.

Capacitor Types

Precision DC performance can be realized with a wide variety of capacitor types, however those with high leakage will cause excessive clock ripple in the signal path and should not be used. Other low cost capacitors, such as ceramics, may have adequate leakage specifications but often also exhibit high dielectric absorption. This will not harm the amplifier's DC performance but can increase the initial settling time on turn-on to 1 or 2 seconds (to 1μV). If fast settling after power-up is required then higher quality capacitors, such as mylar or polypropylene, should be used.

Clock

An on-chip clock is included on all 420 series amplifiers to control the operation of the offset correction circuitry. This oscillator is completely self contained and needs no external components or connections. The internal clock rate is nominaly 400Hz on the MAX420/421 and is 250Hz on the MAX422/423.

External Clock

The MAX421 and 423 have an INT/$\overline{EXT}$ pin for clock selection (pin 14). The pin has an internal pull-up and, for self-clocked operation, can be left open or connected to V^+. When INT/$\overline{EXT}$ is tied to V^- the internal clock is disabled and an external clock can then be applied to EXT CLK IN. Because of an internal divider, the offset nulling circuitry runs at one half the external clock rate.

Duty Cycle and Thresholds

The duty cycle of the external clock is not critical at low frequencies. For EXT CLK IN frequencies of 500Hz or greater, a 50% to 80% positive duty cycle is recommended to allow transients on the null capacitors to settle. This is necessary because the capacitors are only charged when EXT CLK IN is high. The input threshold for EXT CLK IN is typically $V^+ - 2.5V$ so that an external clock signal can swing from either V^+ to GROUND or V^+ to V^-. The internal chopping frequency is available at the CLK OUT pin with either internal or external clock operation .The nominal output levels for CLK OUT are V^+ for a "High" and $V^+ - 5V$ for a clock "Low".

In some instances, it may be advantageous to synchronize two amplifier clocks, or slave one to another. A simple way to accomplish this is to tie the amplifiers' EXT CLK IN pins together (MAX421 or 423 only) and pull one's INT/$\overline{EXT}$ pin low while allowing the other's to float high. The amplifier with INT/$\overline{EXT}$ high will then provide the clock for both devices (see Figure 9).

±15 Volt Chopper Stabilized Operational Amplifier

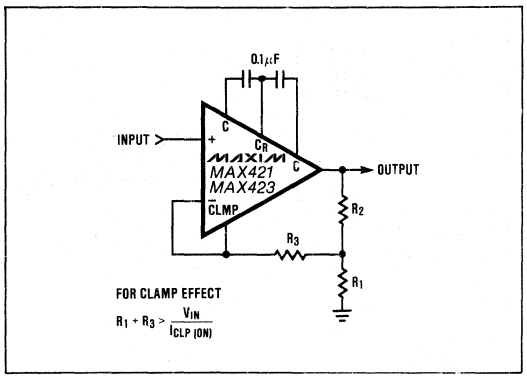


Figure 3. Non-Inverting Amplifier with Optional Clamp.

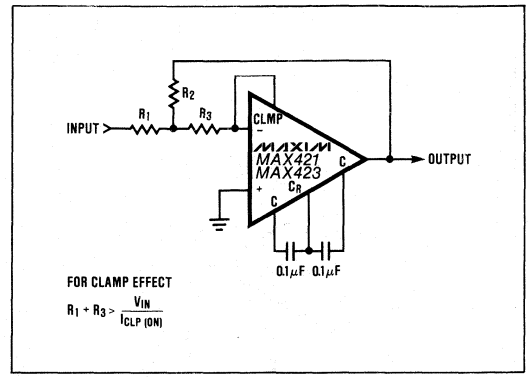


Figure 4. Inverting Amplifier with Optional Clamp.

Plugging into a Conventional Op-Amp Socket

As a result of their ±15V supply capability, the 8-pin MAX420 and 422 can plug directly into a conventional op-amp socket for immediate upgrading of DC specifications. Since the external nulling capacitors occupy what are usually "Offset null" pins (1, 5, and 8), the standard op-amp pin-out is still maintained for input, output, and supply connections. Essentially, C_{EXTA} and C_{EXTB} replace the offset trim pot normally required with conventional op-amps.

Output Clamp/Overload

The OUTPUT CLAMP, when connected to the inverting input, reduces the amplifier's overload recovery time (see Figures 3 and 4). It does this by providing a feedback path that is activated just before the output saturates. The resultant reduction in gain prevents differential input overload and consequent charge build-up on the correction capacitors. If the capacitors are allowed to overcharge, the amplifier will need time to recover (typically 500ms) after the overload is removed. Since the OUTPUT CLAMP activates slightly prior to output saturation there is also a small reduction in output swing when it is used. This reduction is typically 500mV with a 10kΩ output load.

Single Supply Operation

The 420 series amplifiers are well suited for operation in single power supply applications that have system ground connected to V^-. With supply voltages of 10 volts or above the input range is typically from Ground to V^+ – 1.5V. At lower supply voltages the input-range lower limit will be higher (approx. Gnd + 0.5V at 5V supply). The amplifiers' outputs will swing to within approximately 50mV of Ground or V^+ with a 100kΩ load and within 500mV with 10kΩ (MAX420, 421 only).

Applications

Low Voltage Signals

Realizing microvolt offset and nanovolt drift performance goes beyond the selection of a precision amplifier (though it's not a bad start). When trying to amplify very low level signals any number of outside error sources can confuse the measurement. These errors are often indistinguishable from real signal or amplifier error, which of course is why they are a problem.

Thermo-Electric Effect

This property describes how thermocouples measure temperature. In short it states that two dissimilar metals in contact can be expected to generate a voltage. This is fine for thermocouples but is not so useful when pin-to-socket, socket-to-circuit board, and circuit board-to-edge connector junctions all generate signals which can add to input error. The voltage generated in such situations can range from 0.1 to 10's of μV/°C, many times the offset drift of an MAX420. In general such problems are dealt with by minimizing sockets and connectors in low level circuitry and by using components designed for low thermal EMF when connectors, relays, etc. are unavoidable.

Gradients

The presence of heat in low level circuitry is often not so much a problem as are thermal gradients. Gradients can, for example, cause normally balanced amplifier input connections to be at different temperatures. These connections then generate different thermoelectric voltages that can no longer be completely cancelled by the balanced inputs. The moral then is to minimize thermal gradients by keeping power dissipation and air currents in and around low level circuitry and connections at a minimum.

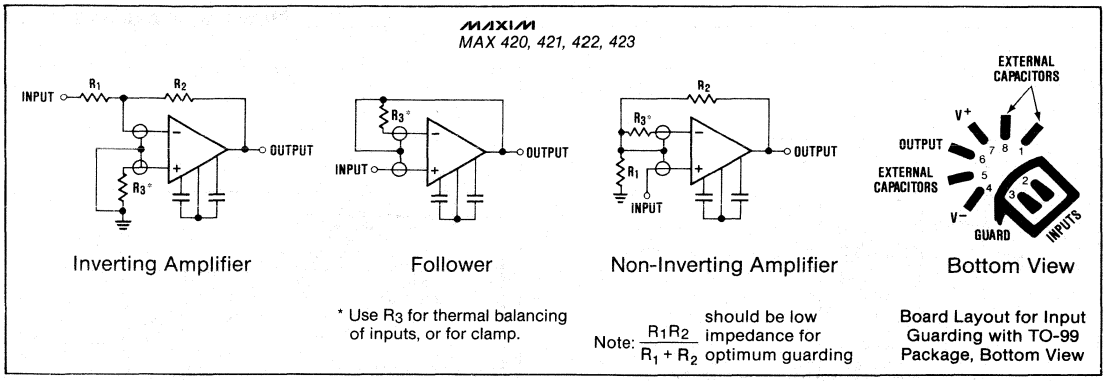


Figure 5. Input Guard Connections.

Thermal Symmetry

Another useful low level technique is to design thermal "symmetry" into the layout. This may mean adding dummy resistors and connections so that the thermal mass, as well as the number of thermoelectric error sources, in an input pair will cancel. It may also involve running input traces near each other and keeping their size the same as well. Thermal "filtering" with small enclosures or even insulation for sensitive areas can also be helpful.

Low Current Signals, Input Guards

Low leakage, high impedance CMOS inputs allow the MAX420 amplifier family to amplify the signals of very high impedance sources. Though the amplifiers' input bias current is measured in picoamps, getting the surrounding connections to live up to that specification requires some attention. In applications where picoamp or nanoamp errors can be significant, board leakage either from surface contamination or through the board material itself may be a problem.

Controlling Leakage

Using low leakage board materials and proper cleaning methods after assembly can provide marked reductions in leakage induced errors. Beyond this, conformal coatings can be used to control later surface contamination. In some cases, Teflon insulators and/or circuit board guard rings may be necessary to protect very high impedance nodes. Guard connections for various amplifier configurations are shown in Figure 5. In each case the guard is connected to a low impedance point that is approximately at the same potential as the inputs. Leakage currents from other points on the board are then absorbed by the guard. For best results, guard rings should be used on both sides of the circuit board. The 14 pin MAX421 and 423 have specifically been designed to ease input guard layout in that the pins adjacent to the inputs are unused in those packages.

Output Characteristics /Open Loop Gain

The MAX420 and 421 can typically drive a 10kΩ load from +14.8V to −14.5V when operating with ±15V power supplies. With a 100kΩ or greater load, however, the output can typically swing to within 50mV of each rail. The output swing with the lower power MAX422 and 423 will be somewhat less for a given load.

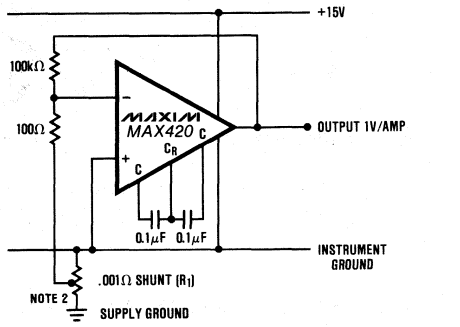
The open loop gain of a MAX420 series amplifier is somewhat load dependent for resistances which are less than 10kΩ. The effect is largely due to the impedance of the amplifier's output stage. The gain is about 17dB lower with a 1kΩ load than it is with 10kΩ. Since even with 1kΩ the gain is still typically 120dB, the reduction is insignificant for low frequency applications. In wideband circuits, however, the best results are achieved with loads of 10kΩ or more where the amplifier's open loop response is a smooth 6dB/octave slope from 0.1Hz to 0.5MHz. Additionally, there is negligible phase shift at the frequency where the null amp is rolled off.

Intermodulation

In some chopper-stabilized amplifier designs, interaction between the input signal and the chopper frequency sometimes produces intermodulation products in the form of sum and difference signals. If the input frequency and the chop rate are near enough to each other, a difference signal may even appear as a DC error at the output. The MAX420 series minimizes these problems with active compensation circuitry that virtually eliminates intermodulation effects and controls the amplifier's open loop gain-phase characteristics as well. With well behaved open loop parameters, the chopper circuitry's impact on the amplifier's dynamic performance can be ignored in most applications.

±15 Volt Chopper Stabilized Operational Amplifier

Typical Applications



Note 1: $R_1 \simeq 3$ cm. #20 solid copper wire.
Note 2: Shunt contact point determined at calibration.

Figure 6. Ultra-low Current Shunt Amp.

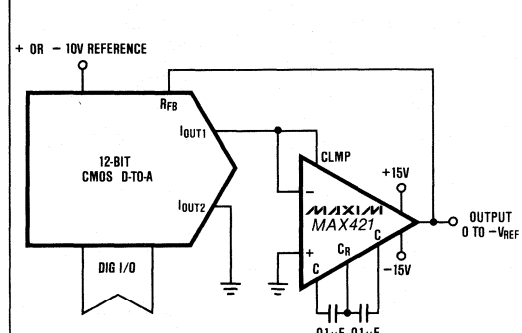
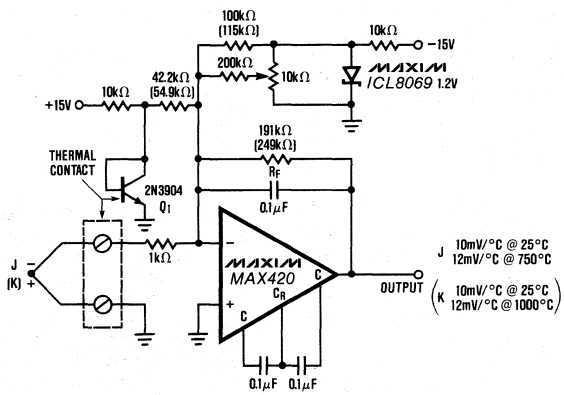


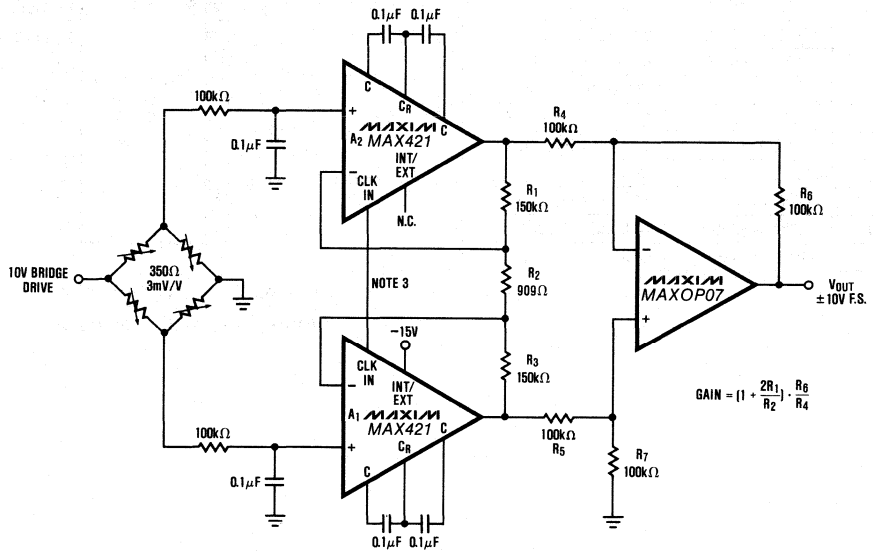
Figure 7. CMOS DAC Output Amplifier. Low offset maintains DAC linearity.



Note 1: Q_1 and connection terminals must be at the same temperature.
Note 2: Values in parentheses are for type K thermocouple.
Note 3: Connections to inverting input of op-amp should be kept as short as possible to reduce noise pickup.
Note 4: All circuit power is ±15V.

Figure 8. Amplifier with Cold-Junction Compensation for Grounded Thermocouples.

Typical Applications



Note 1: Matching rules: $R_1 = R_3$ and $\frac{R_6}{R_7} = \frac{R_4}{R_5}$. Matching determines CMRR, for example 0.1% = 60dB, 0.01% = 80dB.
Note 2: Metal film or wire-wound resistors are recommended.
Note 3: A_1's internal clock is slaved to A_2 via CLK IN pins.
Note 4: All amplifiers powered from ±15V supplies.
Note 5: R_2 is a selected value.

Figure 9. 10μV V_{OS}, 0.1μV/°C Strain Gauge Instrumentation Amplifier.

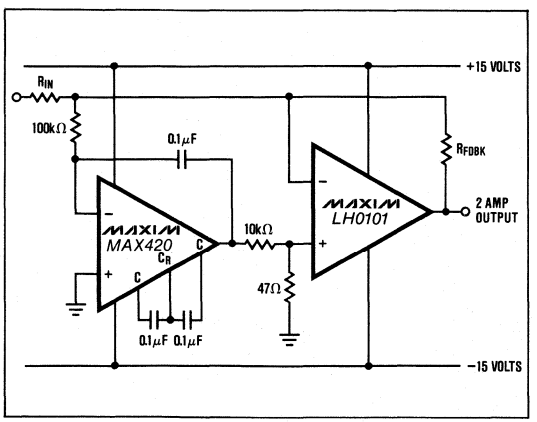
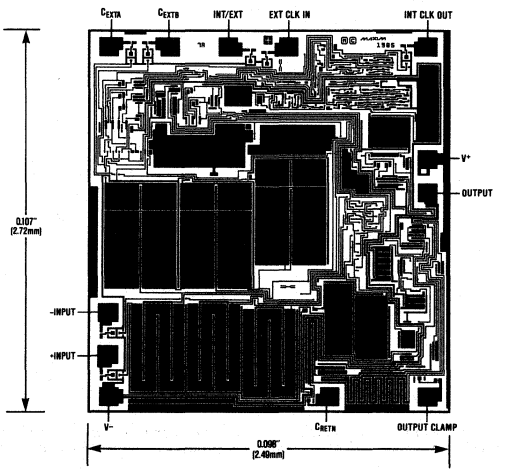


Figure 10. D.C. Stabilized Power Op-Amp. Main amp has 5MHz unity-gain point.

Chip Topography

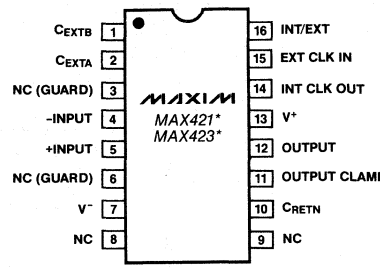


±15 Volt Chopper Stabilized Operational Amplifier

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX421M/D	-55°C to +125°C	Dice
MAX422CPA	0°C to +70°C	8 Lead Plastic DIP
MAX422EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX422MTV	-55°C to +125°C	TO-99 Metal Can
MAX423CPD	0°C to +70°C	14 Lead Plastic DIP
MAX423CWE	0°C to +70°C	16 Lead Small Outline
MAX423C/D	0°C to +70°C	Dice
MAX423EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX423MJD	-55°C to +125°C	14 Lead CERDIP
MAX423M/D	-55°C to +125°C	Dice

Pin Configurations (continued)



NC = No internal connection

* Pinout for small outline package only

±15 Volt Chopper Stabilized Operational Amplifier

General Description

The MAX430 and MAX432 are CMOS ±15V chopper-stabilized amplifiers designed for high accuracy signal conditioning, amplification, and instrumentation applications. They offer input offset and drift specifications superior to previous "precision" bipolar op-amps and monolithic chopper amplifiers. External capacitors, required with previous CMOS chopper amplifiers, are NOT needed with the MAX430/432. Both amplifiers are packaged in 8 pin plastic DIPs.

The combination of ±15V operation, low power, and standard op-amp pin configuration allows these devices to plug directly into almost any OP07/OP77/LM108/μA741 socket regardless of what offset balancing or frequency compensation circuitry might be present. A wide input voltage range that includes the negative supply allows applications not possible with most conventional operational amplifiers.

The MAX430 has a maximum supply current of 2mA and a unity gain frequency of 500kHz; the MAX432 has a maximum supply current of 0.5mA and a unity gain frequency of 125kHz.

Applications

Precision Amplifiers

Signal Conditioning for:

- Thermocouples
- Strain Gauges, Load Cells
- Resistance Temperature Devices (RTDs)

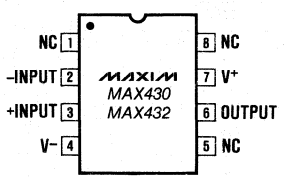
High Accuracy Data Acquisition

D.C. Stabilization of Amplifiers and Systems

4-20mA process control transmitters

Pin Configuration

Top View



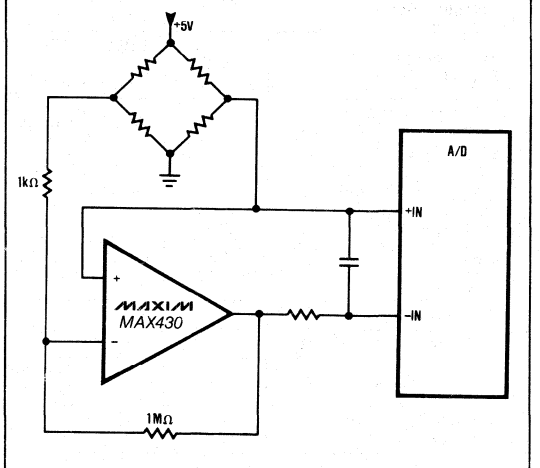
Features

- ♦ No External Capacitors Required
- ♦ 5μV Max Offset Voltage
- ♦ 30pA Input Bias Current
- ♦ Low Input Voltage Noise 0.3μVp-p (DC-1Hz)
- ♦ Low Input Current Noise 0.01pA/$\sqrt{Hz}$ at 10Hz
- ♦ ±15V Supply Operation
- ♦ Input Voltage Range Includes V^-
- ♦ Low Power CMOS Design

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX430CPA	0°C to +70°C	8 Lead Plastic DIP
MAX430EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX432CPA	0°C to +70°C	8 Lead Plastic DIP
MAX432EPA	-40°C to +85°C	8 Lead Plastic DIP

Typical Operating Circuit



Bridge Amplifier

5

±15 Volt Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... +36V
Input Voltage ..... (V^+ +0.3V) to (V^- -0.3V)
Storage Temperature Range ..... -65°C to +160°C
Operating Temperature Range
MAX430C, MAX432C ..... 0°C to +70°C
MAX430E, MAX432E ..... -40°C to +85°C

Lead Temperature (Soldering 10 sec) ..... +300°C
Duration of Output Short Circuit ..... Indefinite
Current into Any Pin 10mA
Continuous Total Power Dissipation 375mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V^- = -15V, T_A = +25°C, Test circuit unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MAX430 MIN.	MAX430 TYP.	MAX430 MAX	MAX432 MIN.	MAX432 TYP.	MAX432 MAX.	UNITS
Input Offset Voltage	$+V_{OS}$	T_A = +25°C	C E		1 2	5 10		1 2	5 10	μV
Average Temperature Coefficient of Input Offset Voltage		Over Temperature Range (Note 1)			0.02	0.05		0.02	0.05	μV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_B	T_A = +25°C Over Temp.			10 35	100		10 35	100	pA
Input Offset Current (Doubles every 10°C above about 60°C)	I_B	T_A = +25°C Over Temp.			15 50	200		15 50	200	pA
Input Resistance	R_{IN}				10^{12}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±10V		120	150		120	150		dB
Output Voltage Swing	V_{OUT}	R_L = 10kΩ R_L = 100kΩ		±12	±14.5 ±14.95		±14	±14.6		V
Common Mode Voltage Range	CMVR	Positive Negative		+12 -15	+12.5 -15.1		+12 -15	+12.5 -15.1		V
Common Mode Rejection Ratio	CMRR	CMVR +12V to -15V, T_A = +25°C Over Temp.		120 110	140 140		120 110	140 140		dB
Power Supply Rejection Ratio	PSSR	±3V to ±16.5V, T_A = +25°C Over Temp.		120 110	140 140		120 110	140 140		dB
Input Noise Voltage (P-P value not exceeded 95% of time)	e_{Np-p}	R_S = 100Ω, DC to 1Hz DC to 10Hz			0.3 1.1			0.4 1.2		μV_{p-p}
Input Noise Current	i_N	f = 10Hz			0.01			0.01		$\frac{pA}{\sqrt{Hz}}$
Unity-Gain Bandwidth	GBW				500			125		kHz
Slew Rate	SR	C_L = 50pF, R_L = 100kΩ			0.5			0.125		V/μs
Rise Time	t_R				0.7			2.8		μs
Overshoot					20			20		%
Operating Supply Range	V^+, V^-			±2.5		±16.5	±2.5		±16.5	V
Supply Current	I_S	No Load, T_A = +25°C Over Temp.			1.3	2.0 3.5		0.3	0.5 1	mA
Internal Chopping Frequency	f_{CH}				400			250		Hz
Offset Voltage vs. Time					100			100		$\frac{nV}{\sqrt{mo.}}$

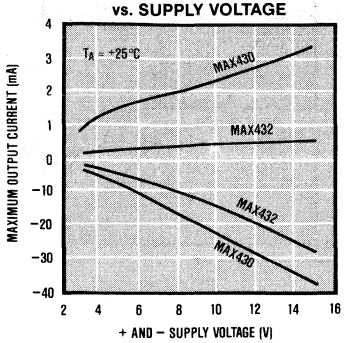
Note 1: Guaranteed by design.

Note 2: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil-Std-883C Method 3015.2 Test Circuit)

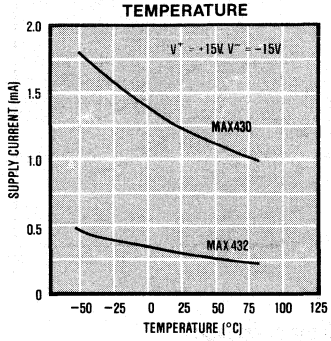
±15 Volt Chopper Stabilized Operational Amplifier

Typical Operating Characteristics

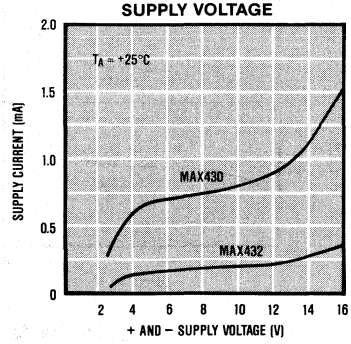
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



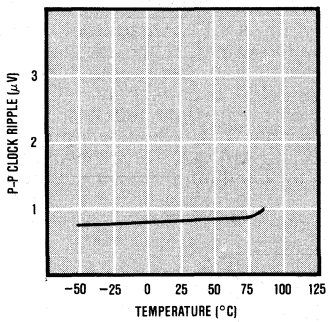
SUPPLY CURRENT vs. TEMPERATURE



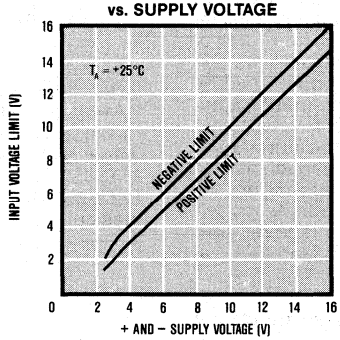
SUPPLY CURRENT vs. SUPPLY VOLTAGE



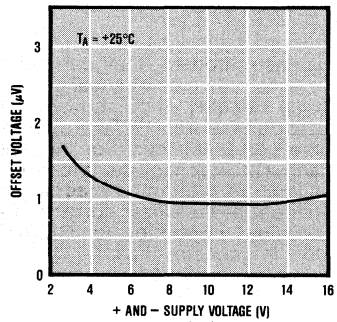
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



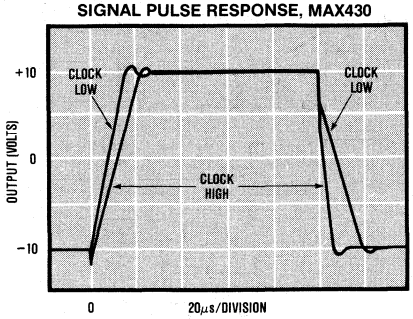
INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



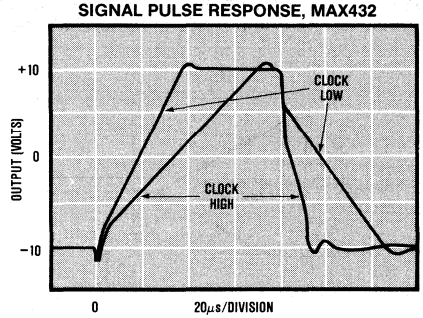
INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



FOLLOWER LARGE SIGNAL PULSE RESPONSE, MAX430



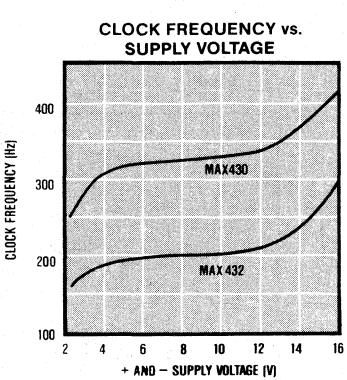
FOLLOWER LARGE SIGNAL PULSE RESPONSE, MAX432

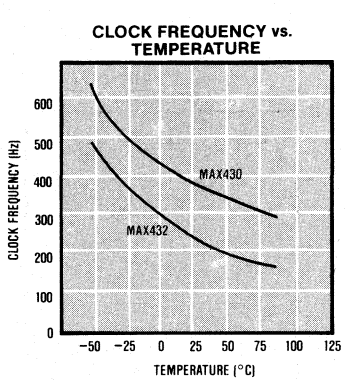


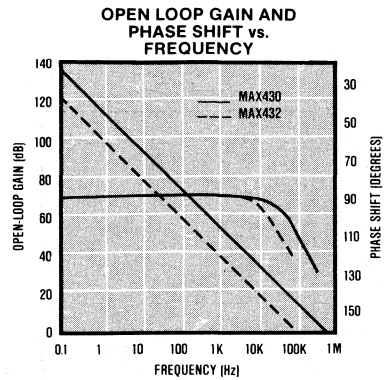
5

±15 Volt Chopper Stabilized Operational Amplifier

Typical Operating Characteristics







Detailed Description

Amplifier Operation

A block diagram of a MAX430/432 is shown in Figure 2. Internally there is a main signal path amplifier and a separate nulling amp. The main amplifier is in the primary signal path and is continuously connected to the external inputs (+IN, -IN). The nulling amplifier alternately corrects its own offset, and then that of the main amp, as its input switches between the two op-amp inputs. Offset correction is accomplished by means of two compensating FETs in the input stage's bias circuitry (not shown). The offset values that drive these trim FETs are stored for the duration of the correction cycle on two internal capacitors, C1 and C2. Each cycle is controlled by the clock as shown in the timing diagram in Figure 2. An added benefit of the offset correction scheme is that it also provides correction for CMRR, PSRR, and A_{VOL} at low frequencies ($f_{IN} \ll f_{CLK}$).

Internal Clock

An on-chip clock is included on the MAX430/432 to control the operation of the offset correction circuitry. This oscillator is completely self-contained and needs no external components or connections. The internal clock rate is nominally 400Hz on the MAX430 and 250Hz on the MAX432 and cannot be adjusted. If other clock frequencies are desired, refer to the MAX421 or MAX423.

Output Characteristics/Open Loop Gain

The MAX430 typically drives a 10kΩ load from +14.8V to -14.5V when operating with ±15V power supplies. With a 100kΩ or greater load, the output typically swings to within 50mV of each supply rail. The MAX432 low power part will drive 100kΩ typically within 0.4V of each supply. The output swing of the MAX432 is less than the MAX430 for a given load because of a factor of 4 reduction in output stage bias current.

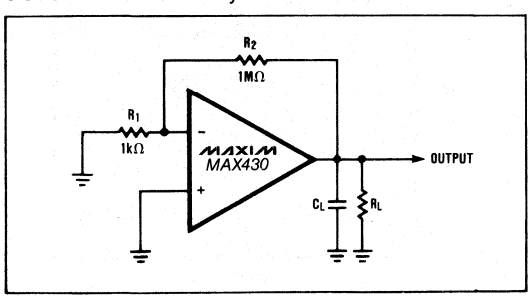


Figure 1. Test Circuit.

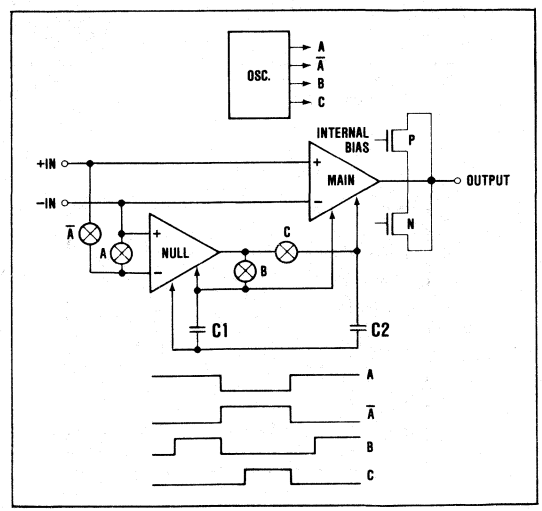


Figure 2. Maxim MAX430 Series Amplifier Block Diagram.

The open loop gain of a MAX430 is load dependent for resistances which are less than 10kΩ. The effect is largely due to the impedance of the amplifier's output stage. The gain is about 17dB lower with a 1kΩ load than it is with 10kΩ (MAX430). Even with 1kΩ the gain is typically 120dB, the reduction is insignificant for low frequency applications. In wide-band circuits, however, the best results are achieved with loads of 10kΩ or more where the amplifier's open loop response is a smooth 6dB/octave slope from 0.1Hz to 0.5MHz. Additionally, there is negligible phase shift at the frequency where the null amp is rolled off.

Clock Ripple and Noise

There are two components to MAX430/432 amplifier noise: wide-band noise and clock related ripple. With conventional op-amps, 1/f noise is often a problem in low level applications. This is the case, even with filtering in low frequency applications, because 1/f noise is difficult to remove. Chopper stabilization techniques eliminate 1/f noise in the MAX430/432 to provide superior low frequency performance.

The chopper generates a small amount of ripple at the internal clock frequency. Typically its peak-to-peak input referred amplitude is 15μV. This signal is easily reduced by band limiting the amplifier's response to below the internal oscillator frequency. In wide band limiting the amplifier's response to below the internal oscillatory frequency. In wide band applications, positive and negative going 5μs pulses, with a typical output amplitude of 15mV, also appear. In circuits which are band limited to 5kHz or less, this noise will not be seen and averages to zero. However, since the pulses are output related, they have little dependence on closed loop gain and are only partially filtered with feedback capacitance around the amplifier. Filtering or band limiting in the circuitry following the amplifier removes this noise.

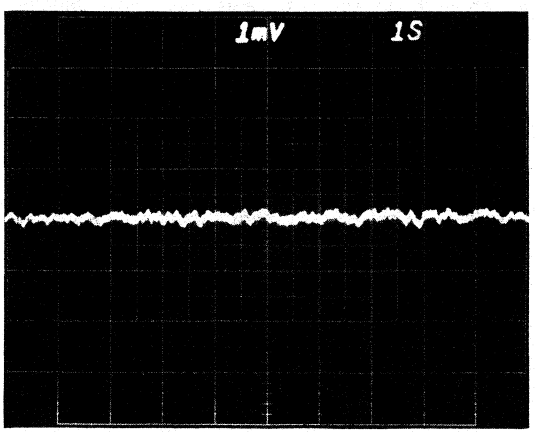


Figure 3. D.C. to 1Hz Noise, 1μV/vert. div. referred to input, 1 second/horiz. div.

Intermodulation

In some chopper-stabilization amplifier designs, interaction between the input signal and the chopper frequency sometimes produces intermodulation products in the form of sum and difference signals. If the input frequency and the chop rate are close enough to each other, a difference signal may appear as a DC error at the output. The MAX430 series minimizes these problems with active compensation circuitry that virtually eliminates intermodulation effects and controls the amplifier's open loop gain-phase characteristics as well. With well-behaved open loop parameters, the chopper's circuitry impact on the amplifier's dynamic performance can be ignored in most applications. If chopper oscillator interaction is a problem, then the MAX421/423, which has an externally controllable oscillator, should be used.

Overload Recovery

The MAX430/432 like most chopper-stabilized amplifiers takes more time to recover from input overloads than a conventional op-amp. The reason for this is that the internal offset nulling capacitors are overcharged during input overloads as the amplifier attempts to "correct" the overload condition via the nulling circuitry. Once these capacitors are overcharged, some time is needed for them to return to the proper level. The length of this delay depends on the duration and amplitude of the overload. The worst case time is about 4 seconds for a severely over-driven MAX430. If the recovery takes too long then a MAX421/423 which provides a "Clamp" input to speed overload recovery, should be used.

Application Hints

Plugging Into A Conventional Op-Amp Socket

The MAX430/432 can be powered from supplies ranging from +5V to ±15V. It can therefore plug into most conventional "741 pinout" op-amp applications. On other op-amps, pins 1, 5, and 8 are used for a variety of functions specific to the amplifier: typically frequency compensation, setting bias, or offset correction. Since the MAX430/432 is internally compensated and its internal chopper removes substantially all of the offset voltage and drift, no connections are required to pins 1, 5 and 8. These pins are not internally connected on the MAX430/432 so that external connections from existing designs will not affect the op-amp's operation.

±15 Volt Chopper Stabilized Operational Amplifier

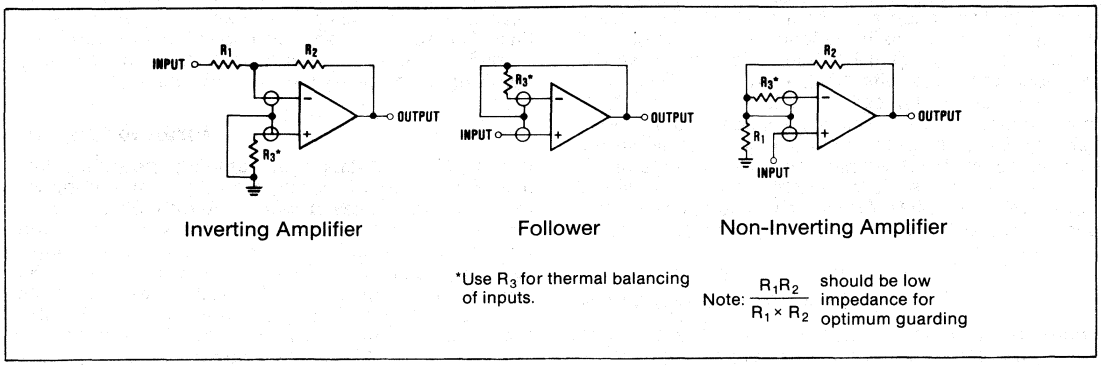


Figure 4. Input Guard Connections.

The MAX432 has the same offset and drift specifications as the MAX430 but is designed for low power operation. As a low power op-amp it has been optimized for driving relatively light loads. With output currents above several hundred microamps, there will be some reduction in open loop gain and output swing. The MAX430, however, is guaranteed to swing ±12V into a 10kΩ load. The MAX432's load driving limitations should, in general, not be a problem in replacement applications because conventional precision amplifiers are not normally used where they must drive heavy loads. This is because the resulting output stage power dissipation often generates thermally induced error voltages elsewhere in the amplifier.

Single Supply Operation

The MAX430/432 is well suited for operation in single power supply applications, i.e. circuits that have system ground connected to V^-. With supply voltages of 10 volts or above, the input range is typically from Ground to V^+ – 1.5V. At lower supply voltages the lower input range limit is higher (approx. GND + 0.5V at 5V supply). With a single power supply, the amplifier's output will swing to within approximately 50mV of ground and V^+ when driving a 100kΩ load.

Low Voltage Signals

Realizing microvolt offset and nanovolt drift performance goes beyond the selection of a precision amplifier (though it's not a bad start). When trying to amplify very low level signals any number of outside error sources can confuse the measurement. These errors are often indistinguishable from real signal or amplifier error, which of course is why they are a problem.

Thermo-Electric Effect

This property describes how thermocouples measure temperature. In short it states that two dissimilar metals in contact can be expected to generate a voltage. This is fine for thermocouples but is not so useful when pin-to-socket, socket-to-circuit board, and circuit board-to-edge connector junctions all generate signals which can add to input error. The voltage generated in such situations can range from 0.1 to 10's of μV/°C, many times the offset drift of a MAX430/432. In general such problems are dealt with by minimizing sockets and connectors in low level circuitry and by using components designed for low thermal EMF when connectors, relays, etc. are unavoidable.

±15 Volt Chopper Stabilized Operational Amplifier

Gradients

The presence of heat in low level circuitry is often not so much a problem as are thermal gradients. Gradients can, for example, cause normally balanced amplifier input connections to be at different temperatures. These connections then generate different thermoelectric voltages that can no longer be completely cancelled by the balanced inputs. The moral then is to minimize thermal gradients by keeping power dissipation and air currents in and around low level circuitry and connections at a minimum.

Thermal Symmetry

Another useful low level technique is to design thermal "symmetry" into the layout. This may mean adding dummy resistors and connections so that the thermal mass, as well as the number of thermoelectric error sources, in an input pair will cancel. It may also involve running input traces near each other and keeping their size the same as well. Thermal "filtering" with small enclosures or even insulation for sensitive areas can also be helpful.

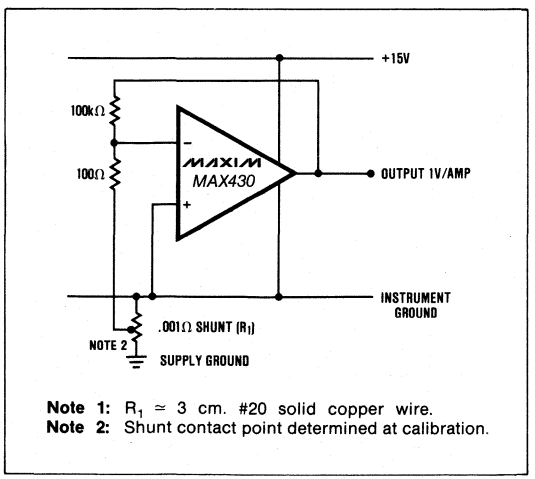
Low Current Signals, Input Guards

Low leakage, high impedance CMOS inputs allow the MAX430 amplifier family to amplify the signals of very high impedance sources. Though the amplifier's input bias current is measured in picoamps, getting the surrounding connections to live up to that specification requires some attention. In applications where picoamp or nanoamp errors can be significant, board leakage either from surface contamination or through the board material itself may be a problem.

Controlling Leakage

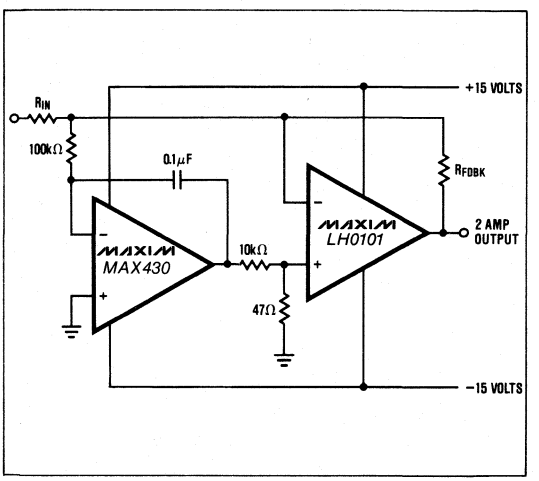
Using low leakage board materials and proper cleaning methods after assembly can provide marked reductions in leakage induced errors. Beyond this, conformal coatings can be used to control later surface contamination. In some cases, Teflon insulators and/or circuit board guard rings may be necessary to protect very high impedance nodes. Guard connections for various amplifier configurations are shown in Figure 4. In each case the guard is connected to a low impedance point that is approximately at the same potential as the inputs. Leakage currents from other points on the board are then absorbed by the guard. For best results, guard rings should be used on both sides of the circuit board.

Typical Applications



Note 1: $R_1 \simeq$ 3 cm. #20 solid copper wire.
Note 2: Shunt contact point determined at calibration.

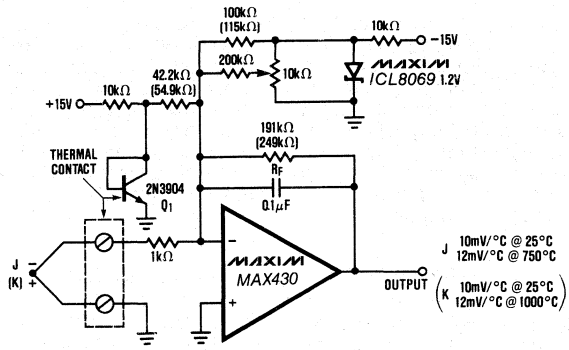
Figure 5. Ultra-low Current Shunt Amp.



D.C. Stabilized Power Op-Amp. Main amp has 5MHz unity-gain point.

±15 Volt Chopper Stabilized Operational Amplifier

Typical Applications



Note 1: Q_1 and connection terminals must be at the same temperature.
Note 2: Values in parentheses are for type K thermocouple.
Note 3: Connections to inverting input of op-amp should be kept as short as possible to reduce noise pickup.
Note 4: Circuit power is ±15V.

Figure 7. Amplifier with Cold-Junction Compensation for Grounded Thermocouples.

CMOS Video Amplifier

General Description

The MAX450 video amplifier is designed to buffer and amplify signals from DC through 10MHz. This monolithic CMOS amplifier has a high impedance CMOS input, while the output can drive 75 ohm loads to greater than ±2V output swing.

Optimized for ±12V supplies, the MAX450 can operate with power supplies ranging from ±10V to ±15V. The MAX450 needs no compensation for gains greater than 20, and provides 4 terminals for two simple RC compensation networks. The MAX450 is "well behaved" and is not prone to oscillations, and the MAX450 is relatively insensitive to variations in printed circuit board layout.

Its 100V/μs slew rate and the ability to drive 75Ω loads make the MAX450 ideally suited for systems which distribute video or other 10MHz bandwidth signals via 75Ω coaxial cables.

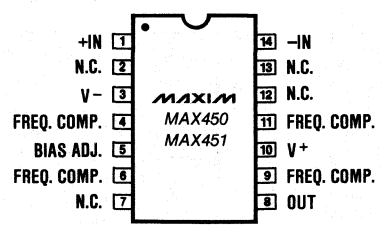
The MAX451 provides all of the features of the MAX450, plus a guaranteed 1nA maximum input bias current. This combination of low bias current and video bandwidth is well suited for vidicon preamps, for photodetector preamps in fiber optics systems up to a 10MHz bit rate, and other applications which demand low input bias current, 10MHz bandwidth, and high current output drive capability.

Applications

Video Amplifiers
PIN Photodiode Amplifiers
Vidicon Amplifiers
Pulse Amplifier
High Input Impedance Video Buffers Amplifiers
CCD Amplifier

Pin Configuration

Top View



Note:
Pin 2 and 13 have internal connections, and should never be connected. Pin 7 may be connected to GND, for compatibility with the NE5539.

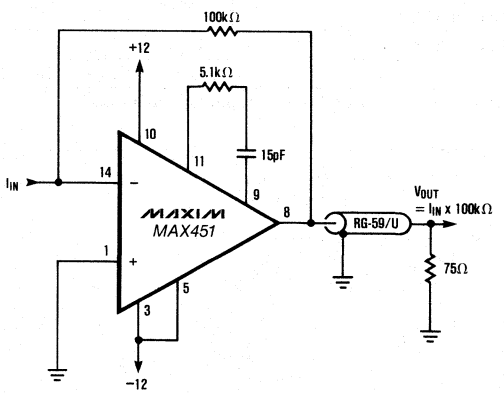
Features

- ◆ **10MHz Power Bandwidth**
- ◆ **±4.0V Output Swing into Back Terminated 75Ω Coax (R_L = 150Ω)**
- ◆ **0.1dB Differential Gain**
- ◆ **0.1° Differential Phase**
- ◆ **400pA (typical) Input Bias Currents**
- ◆ **100V/μs Slew Rate**
- ◆ **53dB Gain at 300kHz**
- ◆ **Output is Short Circuit Protected**
- ◆ **5pA/$\sqrt{Hz}$ Current Noise**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX450CPD	0°C to +70°C	14 Lead Plastic DIP
MAX450CJD	0°C to +70°C	14 Lead CERDIP
MAX450C/D	0°C to +70°C	Dice
MAX451CPD	0°C to +70°C	14 Lead Plastic DIP
MAX451CJD	0°C to +70°C	14 Lead CERDIP
MAX451C/D	0°C to +70°C	Dice

Typical Operating Circuit



Vidicon or PIN Diode Transimpedance Amplifier

(Bandwidth = 5MHz)

CMOS Video Amplifier

ABSOLUTE MAXIMUM RATINGS

V^+ - V^-, pin 3 connected to pin 5 ..... +26.4V
V^+ - V^-, 1kΩ between pin 3 and pin 5 ..... +36V
+IN, -IN, ... (V^+ + 0.3V) to (V^- - 0.3V)
Short Circuit Duration, V_{OUT} .... Continuous with V^+, V^- = ±12V

Power Dissipation at +25°C
Plastic Package 1250mW
(derate 10mW/°C above 25°C)
CERDIP Package 1190mW
(derate 9.5mW/°C above 25°C)
Storage Temperature ..... -65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

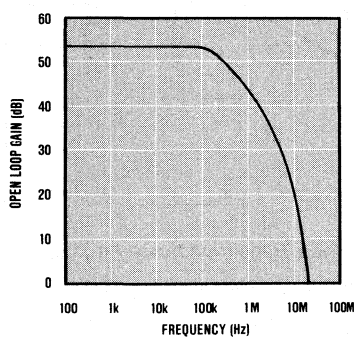
(V_{SUPP} = ±12V, T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MAX450 MIN	MAX450 TYP	MAX450 MAX	MAX451 MIN	MAX451 TYP	MAX451 MAX	UNITS
Input Offset Voltage	V_{OS}	V_{OUT} = 0V, R_S = 100Ω	-30	8	30	-30	8	30	mV
Input Bias Current	I_{BIAS}	V_{IN} = 0		0.4			0.4	1	nA
Common Mode Voltage Range	V_{CMR}			±6			±6		V
Output Voltage Swing	V_{OUT}	f = 1MHz, R_L = 150Ω (Note 1)	±3	±4		±3	±4		V
		f = 1MHz, R_L = 75Ω (Note 1)	±2	±3.5		±2	±3.5		
Large Signal Voltage Gain	A_{VOL}	f = 1MHz, R_L = 150Ω		200			200		V/V
Unity Gain Bandwidth	G_{BW}	V_{OUT} = 1V_{p-p}, R_L = 150Ω		10			10		MHz
Input Capacitance	C_{IN}	Plastic		3			3		pF
		CERDIP		6			6		pF
Input Resistance	R_{IN}	DC to 100kHz		10^7			10^7		Ω
		f = 1MHz		10^6			10^6		
Output Resistance	R_{OUT}	f = 1MHz		5			5		Ω
Common Mode Rej. Ratio	CMRR	V_{CM} = ±1.7, R_S = 100Ω	50	55		50	55		dB
Power Supply Rejection Ratio	PSRR	ΔV_{CC} = ±1V		40			40		mV/V
Supply Current	I_{SUPP}	V_{IN} = 0V		25	35		25	35	mA
Slew Rate	SR	A_V = +1, R_L = 150Ω		100			100		V/μs

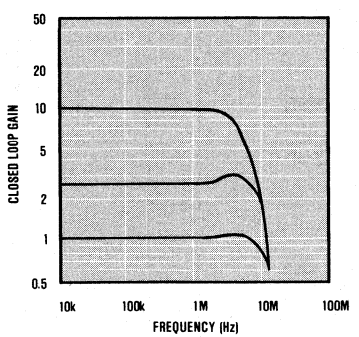
Note 1: Guaranteed by design: not production tested.

Typical Operating Characteristics

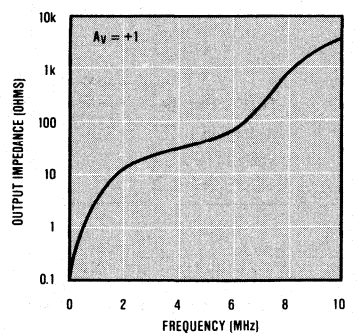
OPEN LOOP GAIN vs. FREQUENCY



CLOSED LOOP GAIN vs. FREQUENCY



OUTPUT IMPEDANCE vs. FREQUENCY



Detailed Description

Compensation, Layout and Bypassing

Figures 1 and 2 show typical applications, including the proper compensation network. Specific compensation component values for different closed loop gains are given in Table 1. For gains above 20, the MAX450/451 does not require any compensation. The easiest way to test for proper compensation is to drive the input with a low amplitude square wave and observe the overshoot. Less than 20% overshoot is normally considered acceptable. The RC network connected between pins 4 and 6 control the negative slew rate, while the RC network connected between pins 9 and 11 control the positive slew rate.

The MAX450/451, unlike many other video amplifiers, is relatively insensitive to printed circuit board layout. $+V_{CC}$ and $-V_{CC}$ should be bypassed to ground with a 0.1µF or 1µF ceramic bypass capacitor. A ground plane should be used to minimize the inductance of the ground connection, and in particular to minimize any ground return inductance that is included in both the input and output return paths.

Power Dissipation and Output Swing

The MAX450/451 operates as a class AB amplifier with the output stage quiescent current being all but 5mA of the total quiescent current. In order to operate in a class A mode for up to ±15mA output current, the MAX450/451 quiescent current is set to approximately 25mA with ±12V supplies and the Bias Adjustment pin connected directly to $-V_{CC}$. This sets the typical power dissipation to 600mW. When output current is drawn, it diverts current from the output stage and actually reduces power dissipation.

For output voltage swings less than ±8V, the output voltage swing is directly proportional to the load resistance, since the MAX450/451 output current capability is nearly independent of the output voltage swing below ±8V. The source follower configuration of the MAX450 output stage limits the no load output voltage to $+V_{CC}$ - 4V.

If operation is desired over the full temperature range, the quiescent current must be reduced by connecting a resistor between $-V_{CC}$ and the Bias Adjustment pin. While reducing the quiescent current, this also creates an output offset as shown in the typical characteristics graphs. Adding a bias adjustment resistor will also reduce the DC output current capability, but the full ±30mA AC output current capability can be maintained by bypassing the bias adjustment resistor with a 0.1µF to 1.0µF ceramic capacitor. The effect of the bias resistor is shown in Table 2.

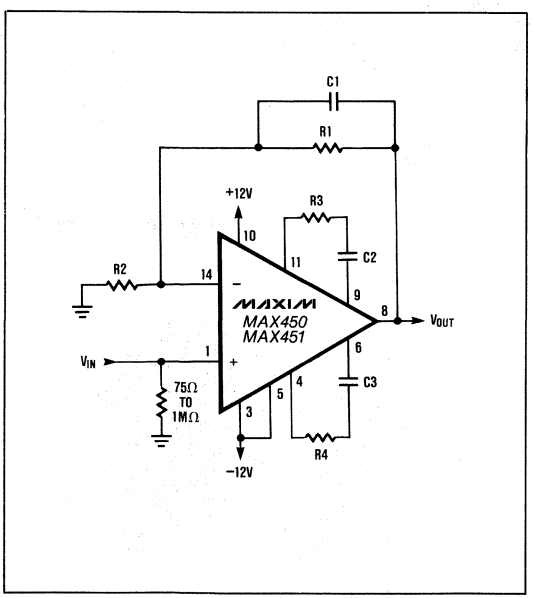


Figure 1. Non-inverting Configuration.

Warmup Effects and High Speed Automatic Testing

The MAX450/451 has a typical power dissipation of 600mW. During high speed automatic testing the package temperature has not stabilized and the die temperature is lower than will be observed in actual operation. The parameters most significantly affected by this heating effect are supply current and input bias current. Maxim measures the input bias current after approximately 2 seconds, using test limits chosen such that the data sheet specification limits will not be exceeded, even after the device has been on for several minutes and has achieved thermal equilibrium.

Table 1: Component Values for Figure 1

	GAIN			
COMPONENT	+1	+2.5	+4	+10
R1	0Ω	1.5kΩ	3kΩ	3kΩ
R2	None	1kΩ	1kΩ	330Ω
R3	2.2kΩ	4.7kΩ	4.7kΩ	5.1kΩ
R4	1.5Ω	1.5kΩ	5.1kΩ	None
C1	None	3pF	3pF	3pF
C2	10pF	5pF	5pF	3pF
C3	10pF	10pF	3pF	None

CMOS Video Amplifier

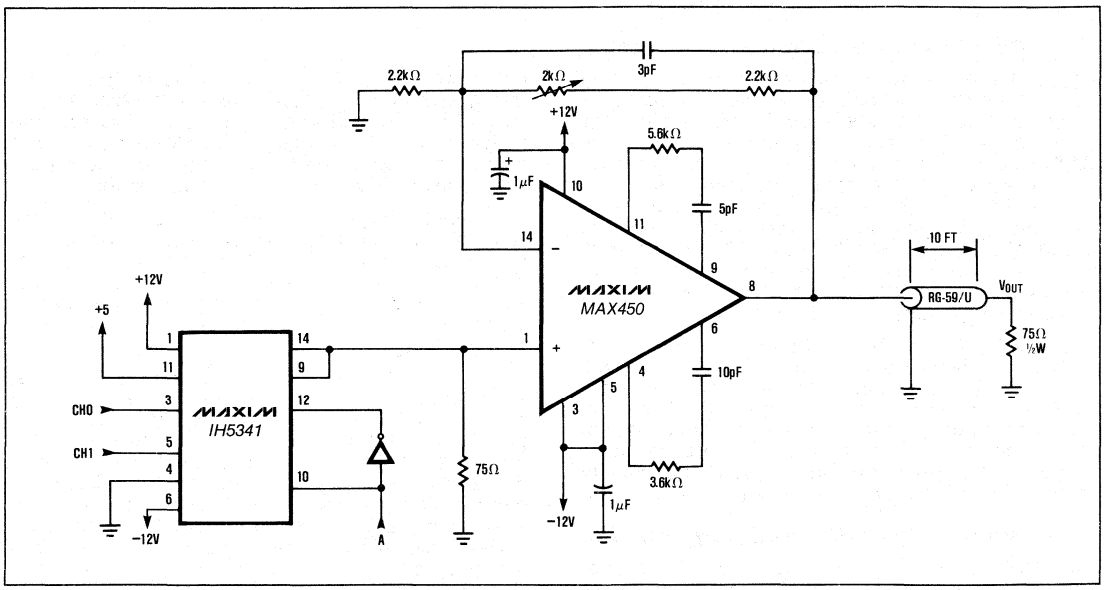


Figure 2. 2 Channel Lossless Video Switch.

Table 2: Effect of Bias Resistor (bypassed with 1μF ceramic capacitor)

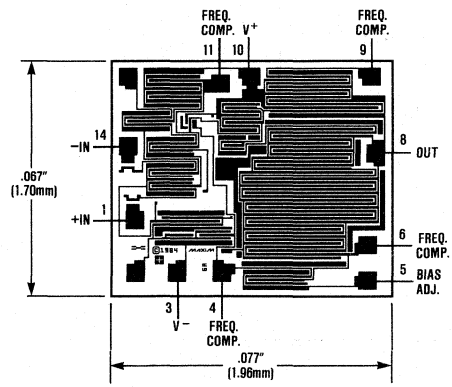
R_{BIAS} (Ω) BETWEEN PINS 3 AND 5	I_Q (mA) V_{CC} = ±12V	V_{OS} (mV)	OUTPUT SWING (V) 1kHz into 75Ω	OUTPUT SWING (V) 1MHz into 75Ω	SLEW RATE (V/μs)	BANDWIDTH (MHz) GAIN = +2
0	25	±10	+4.8, −4.2	±3.5V	+100, −67	10
330	21	+20	+4.8, −4.0	±3.0V	+100, −40	9.5
500	19	+25	+4.8, −3.7	±2.9V	+100, −40	9.3
1k	15	+50	+4.7, −3.4	±2.8V	+100, −20	8.8

Package Information

14 Lead Plastic DIP (Copper)
θ_{JA} = 100°C/W
θ_{JC} = 60°C/W

14 Lead CERDIP
θ_{JA} = 105°C/W
θ_{JC} = 50°C/W

Chip Topography



CMOS Video Multiplexer/Amplifier

General Description

The MAX452 is a unity-gain stable, 50MHz video amplifier capable of driving a 75 ohm load directly. The MAX453, MAX454, and MAX455 combine the 50MHz video amplifier, of the MAX452, with an on-board multiplexer offering 2, 4, or 8 channels respectively. All of the MAX452 family devices operate from ±5V supplies and typically consume only 250mW.

Optimized for video applications, these amplifiers will directly drive a 150 ohm load to ±2V, and will swing ±1V into a 75 ohm load. All amplifiers are unity-gain stable and do not require external frequency compensation components. The MAX453/454/455 operate as positive-gain amplifiers, gain being set by two external resistors. Since they are connected as non-inverting amplifiers, their minimum closed-loop gain is 0dB. In most applications the amplifier's closed-loop gain will be set at 0dB or +6dB (1 V/V or 2 V/V), which guarantees a minimum bandwidth of 25MHz.

Applications

Video signal multiplexing

75 ohm cable drivers

Driving flash converters

Video Crosspoint Switches

Features

- **Unity-gain bandwidth of 50MHz typ.**
- **Low input capacitance: 7pF typ.**
- **No frequency-compensation required**
- **Low power operation: 250mW typ.**
- **Low bias current: 10pA typ.**
- **Directly drives 75 ohm cable**
- **70 dB typical OFF isolation at 4 MHz**

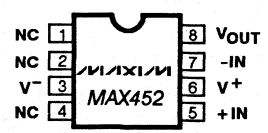
Ordering Information

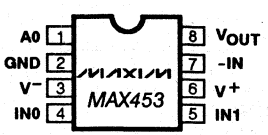
PART	TEMP. RANGE	PACKAGE
MAX452CPA	0°C to +70°C	8 lead plastic DIP
MAX452CSA	0°C to +70°C	8 lead small-outline
MAX452C/D	0°C to +70°C	Dice
MAX452EPA	-40°C to +85°C	8 lead plastic DIP
MAX452EJA	-40°C to +85°C	8 lead CERDIP
MAX452MJA	-55°C to +125°C	8 lead CERDIP
MAX453CPA	0°C to +70°C	8 lead plastic DIP
MAX453CSA	0°C to +70°C	8 lead small-outline
MAX453EPA	-40°C to +85°C	8 lead plastic DIP
MAX453EJA	-40°C to +85°C	8 lead CERDIP
MAX453MJA	-55°C to +125°C	8 lead CERDIP
MAX454CPD	0°C to +70°C	14 lead plastic DIP
MAX454CSD	0°C to +70°C	14 lead small-outline
MAX454EPD	-40°C to +85°C	14 lead plastic DIP
MAX454EJD	-40°C to +85°C	14 lead CERDIP

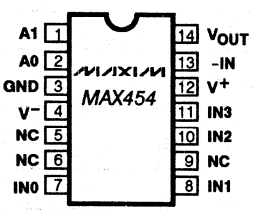
(Ordering Information Continued on Last Page.)

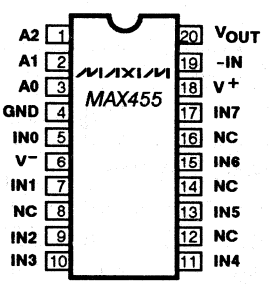
Pin Configurations

Top View









CMOS Video Multiplexer/Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... 12 V
Positive Supply Voltage, V^+ (rel. GND) ..... +12V
Negative Supply Voltage, V^- (rel. GND) ..... -12V
Analog Input Voltage ..... (V^+) + 0.3 V to (V^-) -0.3 V
Digital Input Voltage ..... -0.3 V to (V^+) + 0.3 V
Storage Temperature Range ..... -65°C to +160°C
Operating Temperature Range
MAX452C,MAX453C,
MAX454C,MAX455C ..... 0°C to +70°C
MAX452E,MAX453E,
MAX454E,MAX455E ..... -40°C to +85°C
MAX452M,MAX453M,
MAX454M,MAX455M ..... -55°C to +125°C

Lead temperature (Soldering, 10 sec) ..... 300°C
Duration of Output Short-Circuit to ground ..... Indefinite
Input Current, power on or off
Digital Inputs ..... ±20 mA
All other pins ..... ±50 mA
Continuous Total Power Dissipation (T_A = +70°C)
8 Pin CERDIP (derate 8.0mW/°C above 70°C) 640mW
14 Pin CERDIP (derate 9.5mW/°C above 70°C) 760mW
20 Pin CERDIP (derate 11.1mW/°C above 70°C) 890mW
8 Pin Plastic DIP (derate 8.3mW/°C above 70°C) 660mW
14 Pin Plastic DIP (derate 10.0mW/°C above 70°C) 800mW
20 Pin Plastic DIP (derate 11.1mW/°C above 70°C) 890mW
8 Pin Small-Outline (derate 5.9mW/°C above 70°C) 320mW
14 Pin Small-Outline (derate 8.7mW/°C above 70°C) 480mW
20 Pin Small-Outline (derate 10.0mW/°C above 70°C) 550mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS MAX452/3/4/5

(V^+ = +5V, V^- = -5V, -2V ≤ Vin ≤ +2V, Output Load Resistor = 150Ω, T_A = +25°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VIDEO AMPLIFIER (MAX452/3/4/5)						
Input Voltage Range	V_{IN}	Over Temperature Range (Note 2)	-2		2	V
Input Offset Voltage	V_{OS}			2	5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	(Note 5)		20	100	µV/°C
Input Bias Current	I_B	T_A = +25°C (Note 1)		0.01	10	nA
		Over Temperature Range (Notes 1,2) C		1	10	
		E		3	30	
		M		50	500	
Input Resistance	R_{IN}			10^{11}		Ω
Open-Loop Voltage Gain	A_{VOL}	R_L = 1000Ω	180	260		V/V
		R_L = 150Ω	45	70		
		R_L = 75Ω	25	38		
Open-Loop Gain Drift	$\Delta A_{VOL}/\Delta T$	R_L = 150Ω		0.5		%/°C
Common-Mode Rejection Ratio	CMRR	-2V ≤ V_{IN} ≤ +2V	60	80		dB
Power Supply Rejection Ratio	PSRR	±4.5V to ±5.5V	54	66		dB
Slew Rate	SR	(Note 5)	150	300		V/µs

Note 1: Input bias current includes the multiplexer's ON-state leakage current for the MAX453, MAX454 and MAX455.
Note 2: Operating temperature range for "C" devices is 0°C to 70°C, for "E" devices is -40°C to +85°C, and for "M" devices is -55°C to +125°C.
Note 3: Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.
Note 4: Guaranteed over the voltage range, $V^- < V_{IN} < V^+$.
Note 5: Guaranteed by design.

(Continued on next page)

ELECTRICAL CHARACTERISTICS MAX452/3/4/5 (Continued)

($V^+ = +5V$, $V^- = -5V$, $-2V < Vin < +2V$, Output Load Resistor = 150Ω, $T_A = +25°C$ unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VIDEO AMPLIFIER (MAX452/3/4/5)						
-3dB Bandwidth	GBW1	$A_V = 0dB$, $R_L = 75Ω$ (Note 5)	30	50		MHz
-3dB Bandwidth	GBW2	$A_V = 6dB$, $R_L = 150Ω$ (Note 5)	25	40		MHz
Differential Phase Error	DP	MAX452 (Notes 3, 5) MAX453/4/5 (Notes 3, 5)		0.2 1.2		deg
Differential Gain Error	DG	(Notes 3, 5)		0.5		%
Settling-Time to 1%	t_S	$\Delta V = 1V$, $R_L = 150Ω$, $A_V = 6dB$		50		ns
Output Impedance	R_{OUT}	$f = 100kHz$, $A_V = 0dB$		2		Ω
Full-Scale Output Current	I_{OUT}	$R_L = 150Ω$	±14	±20		mA
Output Voltage Swing	V_{OUT}	$R_L = 150Ω$	±2.1	±3.0		V
Input Noise, dc to 40MHz	Vn	(Note 5)		0.15	0.5	mV_{rms}
Operating Supply Voltage	V^+, V^-		±4.5		±5.5	V
Supply Current	I_S	$V_{IN} = 0V$	20	25	30	mA
MULTIPLEXER (MAX453/4/5)						
Input Voltage Range	V_{IN}	Over Temperature	-2		2	V
OFF Input Leakage Current	I_{OFF}	$T_A = +25°C$ (Note 4) Over Temperature Range (Notes 2, 4) C E M		0.01 1 3 50	10 10 30 500	nA
Logic Low Threshold	V_{IL}				0.8	V
Logic High Threshold	V_{IH}		2.4			V
Input Pullup/down Current	$I_{IL/IH}$			5	20	µA
Turn-ON Time	t_{ON}	(Note 5)		75	120	ns
Turn-OFF Time	t_{OFF}	(Note 5)		25	60	ns
Break-Before-Make Delay	t_D	(Note 5)	10	50		ns
Channel "ON" Capacitance	C_{ON}	(Note 5)		7	15	pF
Channel "OFF" Capacitance	C_{OFF}	(Note 5)		3.5	12	pF
Channel "OFF" Isolation	OIRR	$f_{IN} = 4MHz$, $R_S = 75Ω$ (Note 5) Channel 2 to Channel 3 All other Channels	45 60	55 70		dB

Note 1: Input bias current includes the multiplexer's ON-state leakage current for the MAX453, MAX454 and MAX455.

Note 2: Operating temperature range for "C" devices is 0°C to 70°C, for "E" devices is -40°C to +85°C, and for "M" devices is -55°C to +125°C.

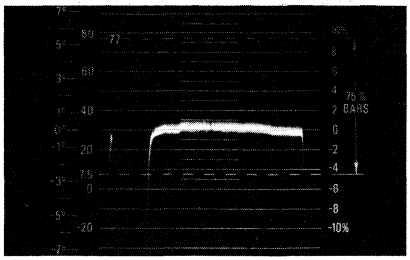
Note 3: Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.

Note 4: Guaranteed over the voltage range, $V^- < V_{IN} < V^+$.

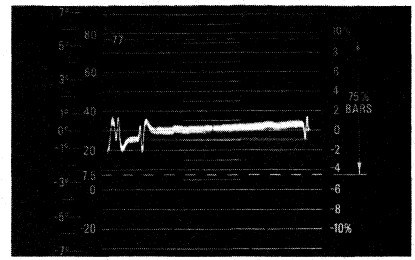
Note 5: Guaranteed by design.

CMOS Video Multiplexer/Amplifier

MAX452 AND MAX455 DIFFERENTIAL GAIN

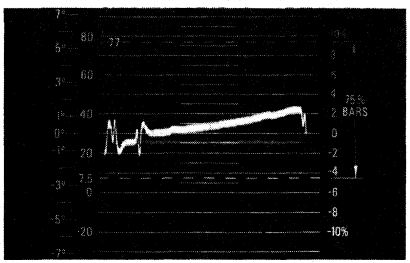


MAX452 DIFFERENTIAL PHASE

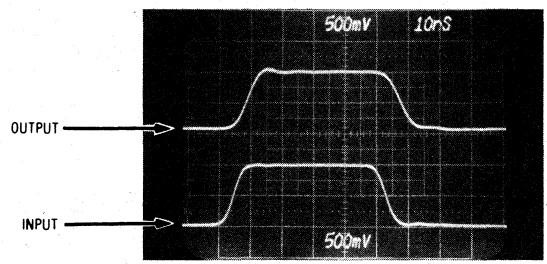


Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.

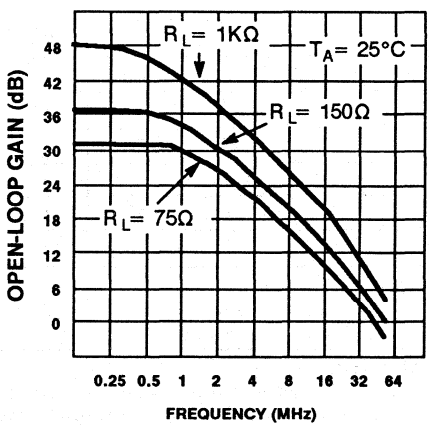
MAX455 DIFFERENTIAL PHASE



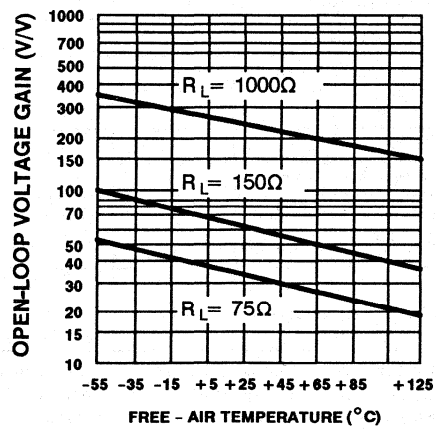
MAX455 PULSE RESPONSE



OPEN-LOOP GAIN vs. FREQUENCY



OPEN-LOOP GAIN vs. TEMPERATURE



Pin Description

PIN NAME	PIN NUMBER				FUNCTION
	MAX452	MAX453	MAX454	MAX455	
V^+	6	6	12	18	Positive Supply, +5V
V^-	3	3	4	6	Negative Supply, -5V
V_{OUT}	8	8	14	20	Amplifier output
-IN	7	7	13	19	Amplifier's inverting input
+IN	5	-	-	-	Amplifier's non-inv. input
IN0	-	4	7	5	Analog input, channel 0
IN1	-	5	8	7	Analog input, channel 1
IN2	-	-	10	9	Analog input, channel 2
IN3	-	-	11	10	Analog input, channel 3
IN4	-	-	-	11	Analog input, channel 4
IN5	-	-	-	13	Analog input, channel 5
IN6	-	-	-	15	Analog input, channel 6
IN7	-	-	-	17	Analog input, channel 7
A2	-	-	-	1	Channel select, MSB
A1	-	-	1	2	Channel select
A0	-	1	2	3	Channel select, LSB
GND	-	2	3	4	Logic Ground

Detailed Description

The video amplifier is a low gain, wideband op-amp optimized for driving low impedance loads. Open-loop gain is about 40V/V with a 75 ohm load which introduces a small gain error. However, this can readily be trimmed by adjusting the gain-setting resistors.

The MAX452/3/4/5 series are unity-gain stable when driving resistive loads. They are optimized for driving 75 ohms at unity gain or 150 ohms at a gain of 2V/V with no frequency compensation components required. Generally, for the best transient response, the load resistance should be (in ohms) 75 x GAIN(V/V). Thus, at a gain of +6dB (2V/V), the amplifier's optimal load is 150 ohms. If a higher resistive load is used, the amplifier will show peaking near its -3dB frequency. If a capacitive load is being driven, such as the input to a flash converter, the load should be "isolated" by a series resistor to limit amplifier ringing, see Figure 4.

The bandwidth of the amplifier is affected by both the closed-loop gain and the load resistor. Table 1 lists the -3dB rolloff frequency for a MAX453/4/5 with different gains and optimal resistive loads. The MAX452, which doesn't have the input multiplexer, runs about 20% higher in bandwidth.

Table 1.
Gain and Load Resistor Selection

GAIN (V/V)	f-3dB (MHz)	R1 (Ω)	R2 (Ω)	R_{load} (Ω)
1	50	0	∞	75
2	40	1k	1k	150
5	30	1k	4k	390
10	18	1k	9k	750

The multiplexers feature break-before-make switches to insure that no two channels are ever connected together. Low DC offset voltage and high bandwidth allow the MAX455 to be cascaded to form a 64 channel system while retaining video signal fidelity.

Figure 1 shows a typical application of the MAX455. The circuit is being used to drive a back terminated 75 ohm cable. R3 and R4 terminate the cable at both ends. R3 also attenuates the signal by a factor of two, so to make up for the signal loss, the amplifier is run at a gain of 2V/V. This arrangement provides unity gain from signal input to

CMOS Video Multiplexer/Amplifier

cable output. Amplifier closed-loop gain is set by R1 and R2 giving,

$$\frac{V_{OUT}}{V_{IN}} = \frac{G \times (R1 + R2)}{(G \times R2) + (R1 + R2)}$$

Where G is the open-loop gain of the amplifier, about 70V/V with a 150 ohm load. Capacitors C1 and C2 are power supply bypass capacitors.

Multiplexer channels are selected by the A0, A1, and A2 pins. These logic pins are compatible with either TTL or CMOS logic. The GND pin (which is a logic ground, NOT an analog ground) should be connected to digital ground. Table 2 shows selected channels for the different states of the control lines. If A0, A1, and A2 are left floating, internal pullup/pulldown sources will hold A0 and A1 low, and A2 high. Thus, channel 0 is the default channel for the MAX453 and MAX454, while channel 4 is the default channel for the MAX455. Pullup/pulldown currents are typically around 5µA.

Table 2. Channel Selection

MAX453		MAX454			MAX455			
A0	Channel	A1	A0	Channel	A2	A1	A0	Channel
L	0*	L	L	0*	L	L	L	0
H	1	L	H	1	L	L	H	1
		H	L	2	L	H	L	2
		H	H	3	L	H	H	3
					H	L	L	4*
					H	L	H	5
					H	H	L	6
					H	H	H	7

*Default channel if selection pins are left floating.

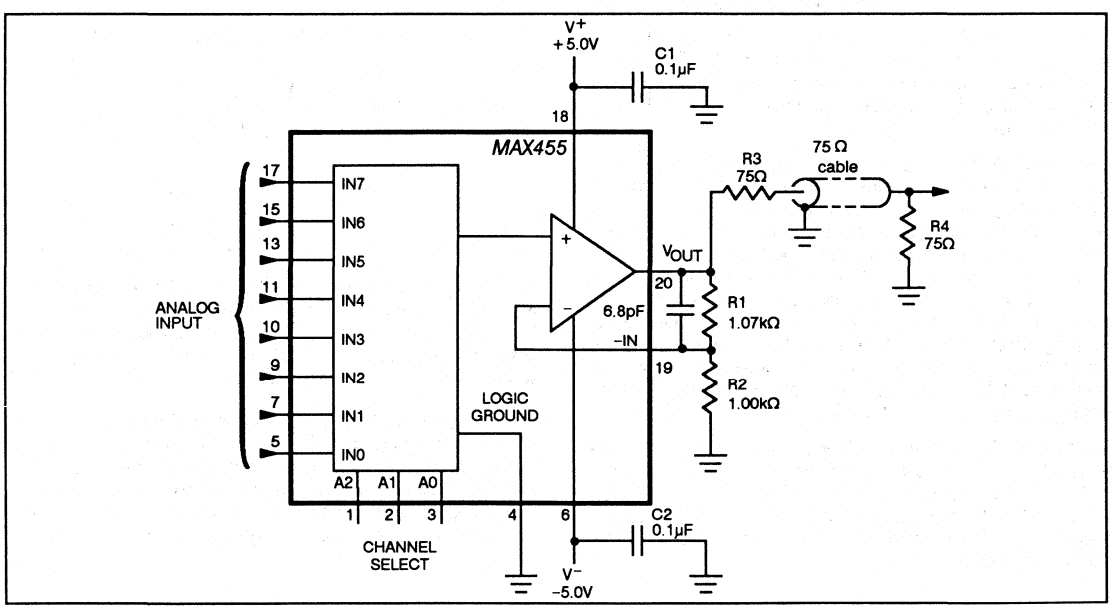


Figure 1. Typical Application

Typical Applications

Figure 2 shows the connections for a unity-gain amplifier. R1 and R2 adjust the gain to be nominally 1.00V/V. R3 is a 75 ohm load resistor. If precise unity-gain is not needed, R1 and R2 can be omitted and -IN can be connected directly to V_{OUT}.

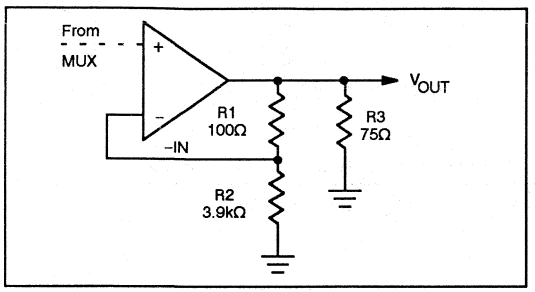


Figure 2. Unity-Gain Connections

Figure 3 shows how 64 channels can be multiplexed together. Eight MAX455s select 8 out of 64 channels, and a final MAX455 selects one of the 8 intermediate channels. The first eight MAX455s are connected as unity-gain amplifiers with 150 ohm load resistors. This results in a voltage gain of about 0.99V/V. The 150 ohm loads will also cause these unity-gain amplifiers to peak around 40MHz which tends to cancel the rolloff of the final amplifier running at a gain of 2V/V. The overall gain is adjusted by R1. The -3dB frequency is about 35MHz.

Figure 4 shows the amplifier driving a capacitive load. The 27 ohm resistor provides isolation between the capacitive load and the amplifier output. This minimizes signal peaking at high frequencies. As a rule, the resistor should be chosen such that the RC product is 10ns or longer. This scheme shouldn't be used if R is greater than 150 ohms (or C is less than 100pF). The amplifier can drive 100pF directly without an isolation resistor.

The video amplifier is similar to a transconductance amplifier in that the output is a current proportional to the difference of the input voltage and the feedback voltage. Gm is about 0.5 mA/mV. The output impedance of the amplifier is around 1k ohms. This gives an unloaded voltage gain of,

$$Gm \times Ro = 500\ V/V$$

or about 54 dB.

Video signals are often of one polarity, e.g., ranging from 0 to +1V full scale. When amplifying these signals, phase distortion can be reduced by biasing the output stage of the video amplifier as shown in Figure 5. Here a signal is driven 0 to +2V into a 150 ohm load. R2 provides 6.5 mA of drive to the load at mid scale (1V). The amplifier, instead of supplying 0 to 13mA, supplies a more symmetric ±8mA which reduces phase distortion to about 1 degree at 4 MHz. Because of the amplifier's finite gain of 0.5mA/mV, the current from R2 introduces an offset voltage. Adding R1 compensates for this offset. R3 and R4 set the closed-loop gain of the amplifier.

Care should be taken in laying out the printed circuit board connections to minimize cross-talk between channels. This can be augmented by using ground traces between the signal paths.

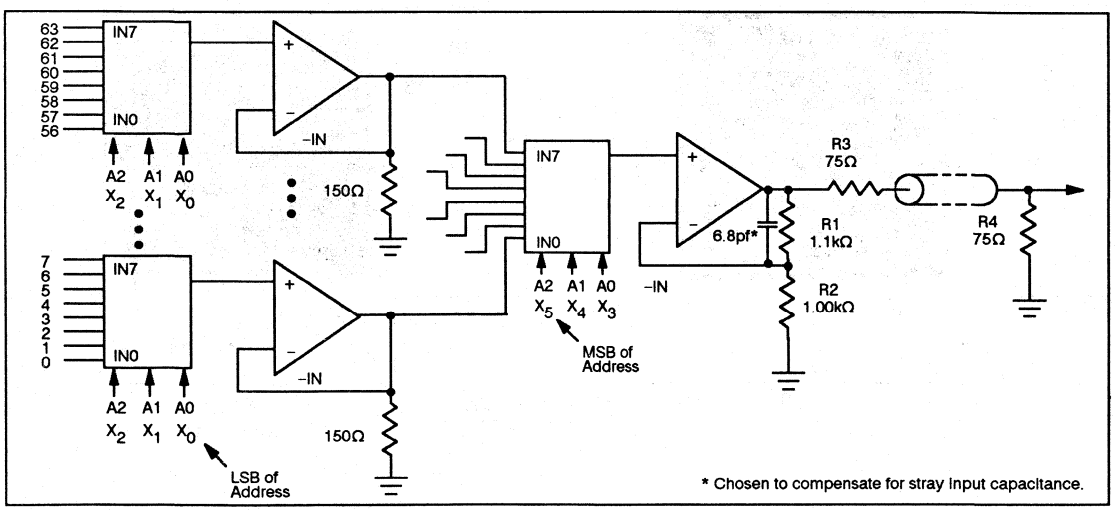


Figure 3. Nine MAX455s Used to Multiplex 64 Channels.

CMOS Video Multiplexer/Amplifier

Power supply voltages should be maintained to within ± 5% of the nominal ± 5.00V values for optimum performance.

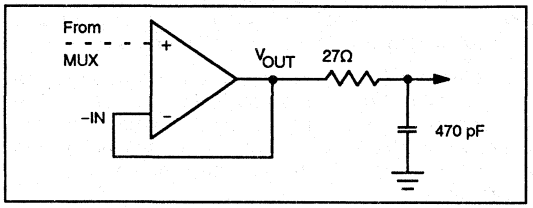


Figure 4. Isolating a Large Capacitive Load.

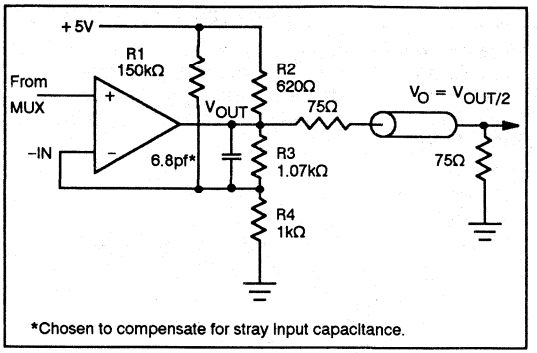
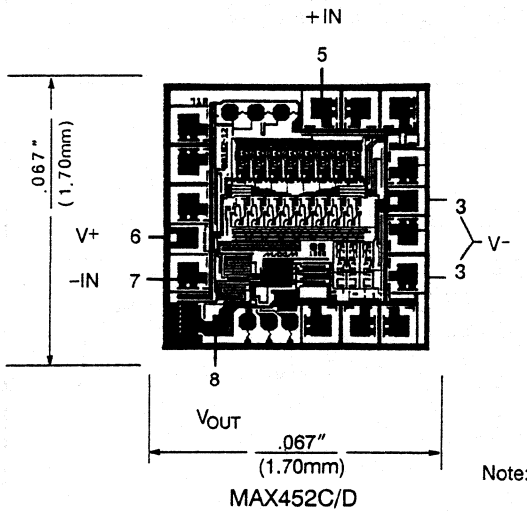


Figure 5. Minimizing Phase Distortion

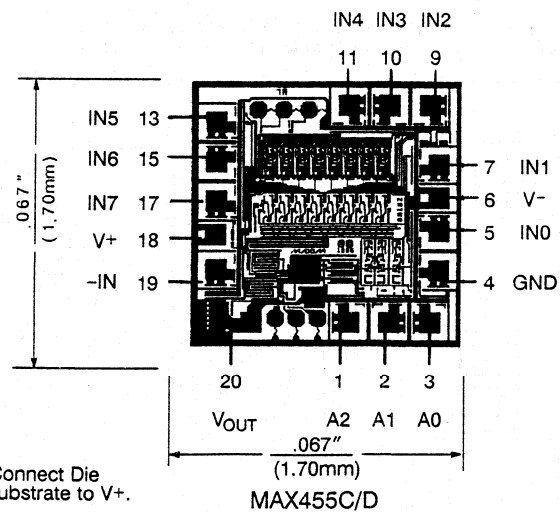
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX454MJD	-55°C to +125°C	14 lead CERDIP
MAX455CPP	0°C to + 70°C	20 lead plastic DIP
MAX455CWP	0°C to + 70°C	20 lead small-outline
MAX455C/D	0°C to + 70°C	Dice
MAX455EPP	-40°C to +85°C	20 lead plastic DIP
MAX455EJP	-40°C to +85°C	20 lead CERDIP
MAX455MJP	-55°C to +125°C	20 lead CERDIP

Chip Topographies



Note: Connect Die Substrate to V+.



General Description

The MAX460 is a high speed, JFET input voltage follower similar and pin compatible to the LH0033, but with input specifications significantly improved over the older device. This device is a direct pin-for-pin replacement for the EL2005. The cascode input stage maintains a constant high input resistance over the full ±10V input voltage range. The input loading can be characterized as a 1000GΩ resistance in parallel with a 3pF capacitor to ground. In most practical applications this can be considered a negligible load.

Applications

Fast Sample/Hold Amplifiers
High Source Impedance Accurate Buffering
Flash A/D Input Buffering
Video Distribution
CRT Drive
Coaxial Line Driver

Features

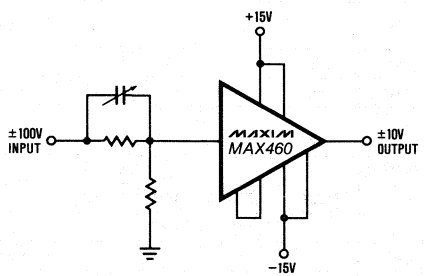
- **Pin for Pin Second Source!**
- **Pin Compatible with LH0033 and EL2005**
- **Low Input Current 50pA**
- **Low Offset Voltage 2mV**
- **Low Offset Drift 25μV/°C**
- **High Slew Rate 1500V/μs**
- **Fast Rise & Fall Times 2.5ns**
- **High Input Resistance 1000GΩ**
- **Wide Bandwidth 140MHz**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX460MGC	-55°C to +125°C	12 Lead TO-8
MAX460IGC	-25°C to +85°C	12 Lead TO-8
EL2005G	-55°C to +125°C	12 Lead TO-8
EL2005CG	-25°C to +85°C	12 Lead TO-8

(Note: The EL2005G is equivalent to the MAX460MGC, and the EL2005CG is equivalent to the MAX460IGC.

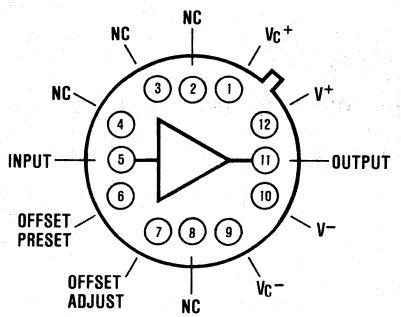
Typical Operating Circuit



High Speed
High Voltage Attenuator
(Detailed Circuit Diagram — Figure 5)

Pin Configuration

Top View



High Accuracy Fast Buffer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$) 40V
Maximum Power Dissipation ..... 1.5W (See Graph)
Maximum Junction Temperature ..... +175°C
Input Voltage Range ..... $\pm V_S$
Continuous Output Current ..... ±100mA
Peak Output Current ..... ±250mA
Operating Temperature Range
MAX460MGC ..... -55°C to +125°C
MAX460IGC ..... -25°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V_S = \pm15V$, $V_{IN} = 0V$, $T_{MIN} \le T_A \le T_{MAX}$) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MAX460MGC			MAX460IGC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Offset Voltage	V_{OS}	$R_S = 100\Omega$, $T_J = +25°C$		2	5		3	10	mV
		$R_S = 100\Omega$			10			15	
Offset Tempco	$\Delta V_{OS}/\Delta T$	$R_S = 100\Omega$ (Note 3)		25			25		µV/°C
Supply Rejection	PSRR	$\pm10V < V_S < \pm20V$	66	75		60	75		dB
Input bias current	I_B	$T_J = +25°C$ (Notes 2 and 7)		2	50		5	100	pA
		$T_A = +25°C$, (Notes 4 and 7)		50	500		100	1000	
		$T_J = T_A = T_{MAX}$		2	5		0.5	5	nA
Voltage Gain	A_V	$R_L = 1k\Omega$	0.97	0.98	1	0.96	0.98	1	V/V
		$R_L = 100\Omega$	0.92	0.95	0.98	0.91	0.95	0.99	
Input Impedance	R_{IN}	-10V to +10V	2	1000		2	1000		GΩ
		$T_J = +25°C$	10	1000		10	1000		
Output Resistance	R_{OUT}	$V_{IN} = \pm1V$		4	8		4	8	Ω
Output Voltage Swing	V_{OUT}	$V_{IN} = \pm14V$, $R_L = 1k\Omega$	12	12.5		12	12.5		V
		$V_{IN} = \pm10.5V$, $R_L = 100\Omega$, $T_A = +25°C$	9	9.8		9	9.8		
External Offset Resistance	R_{EXT}	$V_{OS} = 0mV$, $T_A = +25°C$ (Note 6)	0	75	200	0	75	200	Ω
Supply Current	I_S	$V_{IN} = 0V$ (Note 5)		19	22		19	24	mA
Power Consumption	P_S	$V_{IN} = 0V$		570	660		570	720	mW

AC ELECTRICAL CHARACTERISTICS ($T_C = +25°C$, $V_S = \pm15V$, $R_S = 50\Omega$, $R_L = 1k\Omega$)

PARAMETER	SYMBOL	CONDITIONS	MAX460MGC			MAX460IGC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$V_{IN} = \pm10V$, $V_{OUT} = \pm5V$	1000	1500		1000	1500		V/µs
Bandwidth	BW	$V_{IN} = 1V_{RMS}$		140			140		MHz
Phase Non-Linearity		BW = 1 to 20MHz		2			2		deg.
Rise Time	t_r	$\Delta V_{IN} = 0.5V$		2.5			2.5		ns
Fall Time	t_f	$\Delta V_{IN} = 0.5V$		1			1		ns
Distortion	HD	F = 1kHz		< 0.1			< 0.1		%
Voltage Gain	A_V	$R_S = 100\Omega$, $V_{IN} = 1V_{RMS}$, F = 1kHz	0.97	0.99	1	0.96	0.99	1	V/V
Output Resistance	R_{OUT}	$V_{IN} = 1V_{RMS}$, F = 1kHz		4	8		4	8	Ω

Note 1: The MAX460MGC is 100% tested at +25°C, +125°C and -55°C. The MAX460IGC is 100% production tested at +25°C only. Specifications at temperature extremes are verified by sample testing to 10% LTPD, but these limits are not used to calculate outgoing quality level.
Note 2: Specification is at +25°C junction temperature due to requirements of high speed automatic testing.
Note 3: Temperature coefficient measured from +25°C to T_{MAX}.
Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.
Note 5: Guaranteed through correlated automatic pulse testing at $T_J = +25°C$.
Note 6: Offset adjust resistor connects between device pin 7 and V^-.
Note 7: Input bias current is guaranteed for $-10V \le V_{IN} \le +10V$.

Circuit Description

The MAX460 combines a cascode JFET input stage with a high current bipolar output stage to form an analog buffer amplifier with very high input impedance and very low output resistance over a wide range of conditions.

In normal operation, the source of Q1 wil be offset from the input voltage by the Vgs of Q1. The output is offset from the Q1 source voltage by the IR drop across R1 and the Vbe of Q5. The total of these offsets has been actively trimmed during the assembly process to be nearly zero.

Q8 sets the drain to source voltage of Q1 to a low voltage that is virtually independent of input voltage, so that the input bias current only changes slightly when the input voltage is changed. (This is the primary difference between the MAX460 and the LH0033.)

Q4, Q7 and Q9 are devices similar to Q1, Q5 and Q8. The current forced by the drain of Q9 will have the proper temperature coefficient to balance the temperature coefficient of the main amplifier stage, Q1.

Diode connected transistors Q2 and Q3 provide a two Vbe voltage difference between the bases of the two output transistors, setting the quiescent current through Q5 and Q6. Resistors R3 and R4 provide a small amount of degeneration to stabilize the quiescent current over temperature.

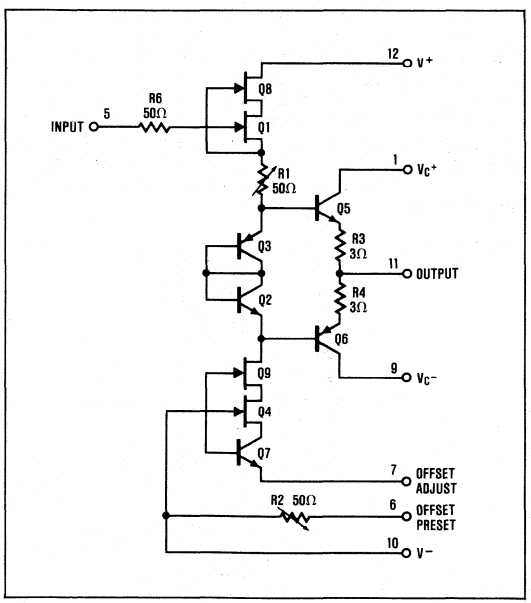


Figure 1.

Applications

Layout Precautions

The MAX460 should be treated as a high frequency amplifier when designing a printed circuit layout. Power supply bypassing to a ground plane with low inductance capacitors should be within a half inch of the device. For applications where the input capacitance is critical, connect the case of the device to the output so that the case capacitance is bootstrapped. For most applications, the case may be left unconnected or grounded. There is no internal connection to the case.

In addition to the high frequency concerns, one must consider the effects of any possible leakage paths if the full input resistance of the MAX460 is to be utilized. Ordinary printed circuit board materials may need a coating to prevent board leakage at high humidities or when dirty. The input in some situations may not even go to the printed circuit board, but instead be connected directly to a sensor or input connector. Lastly, consider the possibility of a guard structure surrounding the input node connected to the MAX460 output: since there will be little or no voltage differential between the input and output, there can be little input current flow even if there is some parasitic leakage resistance.

Offset Voltage Adjustment

For most normal applications of the MAX460, connect pin 6 to pin 7 and use the internally adjusted and guaranteed offset adjustment. When this is not acceptable, or there is a system offset to be absorbed, an external 200 ohm trim pot may be connected from pin 7 to V^-.

Power Dissipation Considerations

The MAX460 package is rated for 0.5W in still air at 125°C and 0.75W with an infinite heat sink, Since the quiescent power is in the neighborhood of 600mW, a heat sink is needed for most 125°C applications and some heavy load applications at lower temperatures. Note that several degrees rise in device temperature can have an adverse effect on the input current and resistance. Several suitable commercial heat sinks are available including the Thermalloy 2241, the Wakefield 215CB and the IERC UP-TO8-48CB. Please note that the can diameter is 0.55 inches nominal as opposed to the JEDEC TO-8 can which is 0.45 inches nominal. (See the outline drawing for detailed dimensions.)

High Accuracy Fast Buffer

Operation from Single or Asymmetrical Power Supplies

Since the MAX460 has no ground pin, an asymmetrical power supply is indistinguishable from a symmetrical supply with a DC level on the input. The single supply case is simply the asymmetrical case taken to the extreme of one of the supplies being zero. In either case, an offset error will be generated corresponding directly to the gain of the circuit times the apparent DC level with respect to a pseudo ground point halfway between the supplies.

$$\text{Output Offset} = 0.5(1 - \text{gain})(|V^+| - |V^-|)$$

For example, a device operating on supplies of +5V and -12V would have an apparent offset error due to the gain of about -35mV. This could easily be corrected with an offset adjust pot connected from pin 7 to V^- as discussed in the offset voltage adjustment section.

Capacitive Loading

The MAX460 is designed to drive heavy capacitive loads without susceptibility to oscillation. Note that the absolute maximum current rating must still be observed, thus the output slew rate times the load capacitance must be less than 250mA. For example, a 1000V/μs slew rate with a 250pF load would fall just within the absolute maximum peak current specification. If a heavier capacitive load needs to be driven, the slew rate must be externally limited. Power dissipation resulting from capacitive load currents must be considered independently. The real power dissipated in a circuit driving a sine wave into a pure capacitive load is:

$$P_{ac} = (V_{p-p})^2 \times \text{Frequency} \times C_1$$

This dissipation adds directly to the device's quiescent power and any DC load power that might be present. The sum of all these terms must be less than the absolute maximum power rating at the temperature of operation. For example, a 250pF load driven to 20V peak to peak at 1MHz adds a reactive power dissipation in the MAX460 of:

$$(20)^2 \times 10^6 \times 250 \times 10^{-12} = 100\text{mW}.$$

This additional power is not often a severe application problem with the MAX460.

Short Circuit Protection

The MAX460 is not internally short circuit protected as most of the possiblities involve some compromise in output swing or transient response. The output stage collectors are available separately, so there are several options open to the user. The simplest and most commonly used is the simple resistor in each output stage collector. For worst case protection these resistors may be calculated by:

R_{LIM} = V+/100mA = V-/100mA = 150Ω for 15V supplies

Unfortunately, a resistor this large severely restricts the voltage swing into a heavy load and the slew rate into a capacitive load. Decoupling the V_C^+ and V_C^- pins with capacitors will retain full output swing for transient pulses, but if the capacitors are made too large (to hold up long pulses) the protection is lost. A better but more complex circuit is shown in figure 4. Here, each output stage collector is driven by a current source set to a safe current, in this case, about 70mA. Ordinarily, the actual output current demand is less than that, so the current source saturates, applies $+V_S$ and $-V_S$ to the output collectors and the MAX460 behaves normally. In the event of a short on the output, however, the current source comes into play and reduces the output stage collector voltage as required to keep the current to a safe level. The output stage collectors may be bypassed with a small capacitor to give additional current capacity for short periods, as would be required in driving a capacitive load.

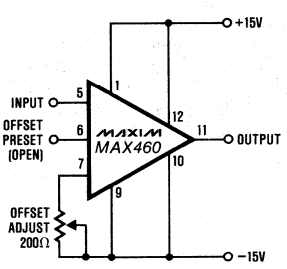


Figure 2. Offset Zero Adjust

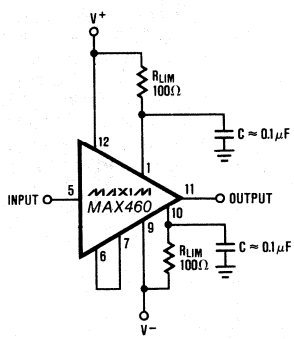


Figure 3. Using Resistor Current Limiting

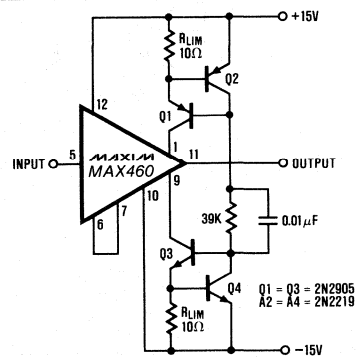


Figure 4. Current Limiting Using Current Sources

Typical Applications

High Resistance Compensated Divider to Monitor ±100V

The circuit in Figure 5 is intended to interface an A/D converter with a maximum input voltage of ±10V to an input signal of ±100V with a minimum of loading on the signal. Resistors R1 and R2 and capacitor C1 form a frequency compensated 10:1 voltage divider so that the buffer never sees more than its rated ±10V. For optimum transient response, C1 should be adjusted to compensate for variations in stray capacitance.

Note that this circuit will work with the LH0033 device, but there will be a tendency for the negative gain to be in error due to the rise in the input current for negative input voltages. (See the curve of input bias current vs. input voltage on the LH0033 data sheet.) This non-linearity at the input can cause apparent offset voltage changes in response to an AC signal that would cause the input current to be higher at some parts of the cycle than at others.

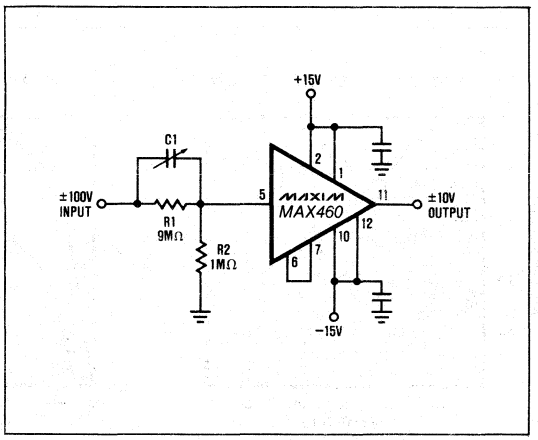
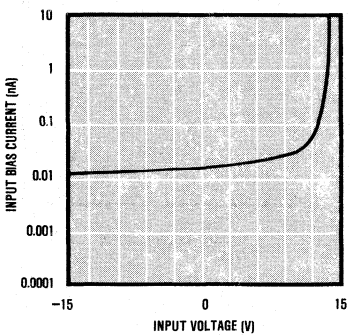


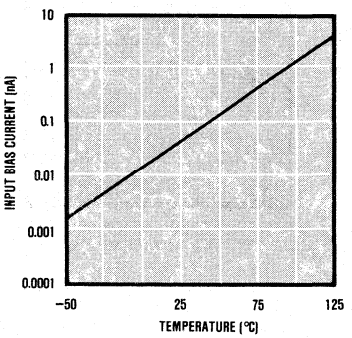
Figure 5. High Speed High Voltage Attenuator

Typical Operating Characteristics

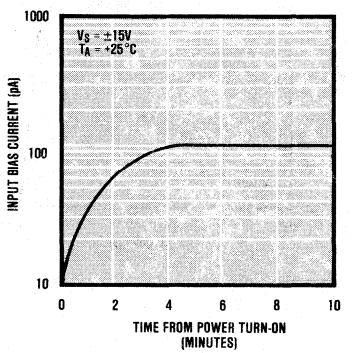
INPUT BIAS CURRENT vs INPUT VOLTAGE



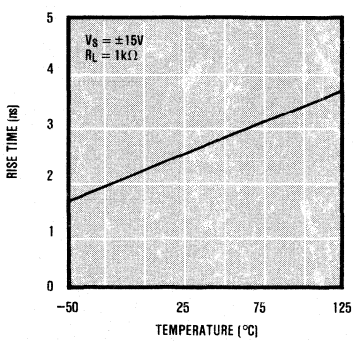
INPUT BIAS CURRENT vs TEMPERATURE



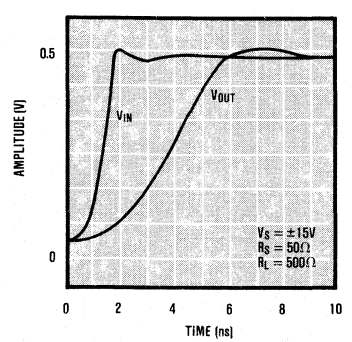
INPUT BIAS CURRENT DURING WARM-UP



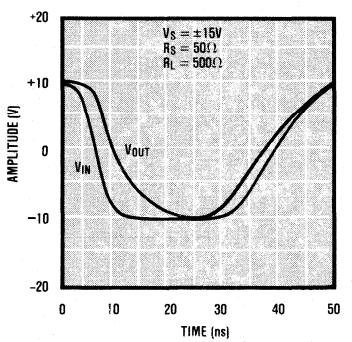
RISE TIME vs TEMPERATURE



SMALL SIGNAL PULSE RESPONSE



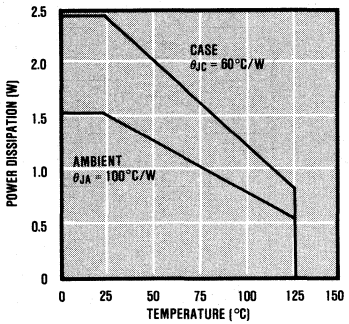
LARGE SIGNAL PULSE RESPONSE



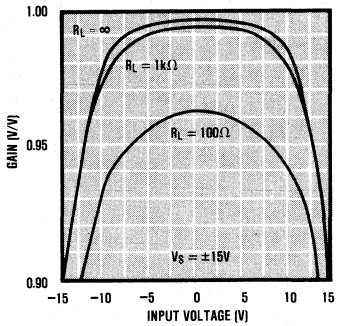
High Accuracy Fast Buffer

Typical Operating Characteristics

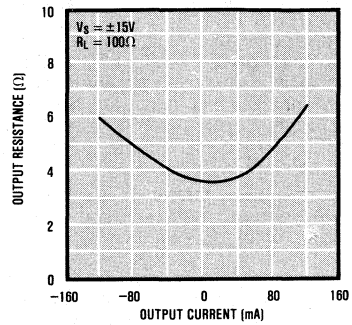
MAXIMUM POWER DISSIPATION



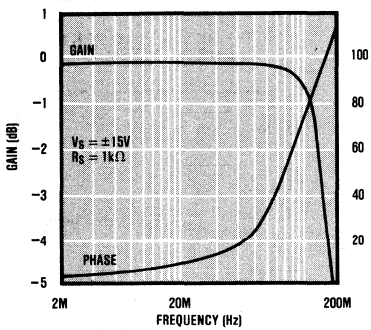
GAIN vs INPUT VOLTAGE



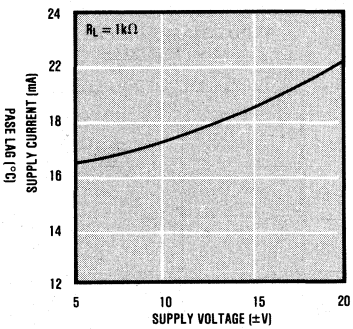
OUTPUT RESISTANCE vs OUTPUT CURRENT



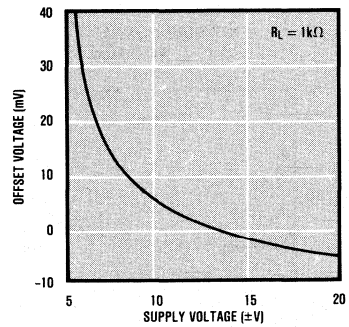
FREQUENCY RESPONSE



SUPPLY CURRENT vs SUPPLY VOLTAGE



OFFSET VOLTAGE vs SUPPLY VOLTAGE



MAXIM

Wideband Fast-Settling Operational Amplifier

General Description

The BB3554/AD3554 is a very high performance Hybrid operational amplifier with JFET inputs and high-speed high-drive bipolar output. The combination of respectable DC specifications with unusually complete AC, noise, and transient specifications guaranteed over a wide range of conditions results in an amplifier that can be used in a wide variety of applications.

The BB3554/AD3554 slews at 1000V/μs and outputs up to ±100mA at ±10V. As a fast-settling amplifier, the BB3554/AD3554 reaches its final value within 150ns to a ±0.05% error band.

Applications

Baseband Video Amplifiers
Test Equipment
Waveform Generators
Pulse Amplifiers
Fast A/D and D/A Converters

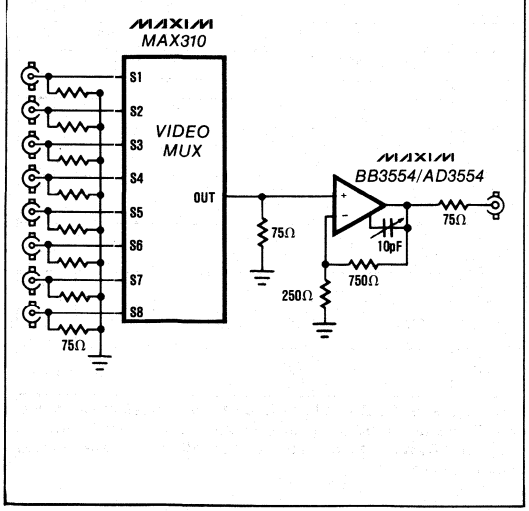
Features

- **1000 V/μs Slew Rate**
- **Settling-Time 150ns Max**
- **Full Differential Input**
- **100mA Minimum Output Current**
- **Drives Coaxial Cable Directly**

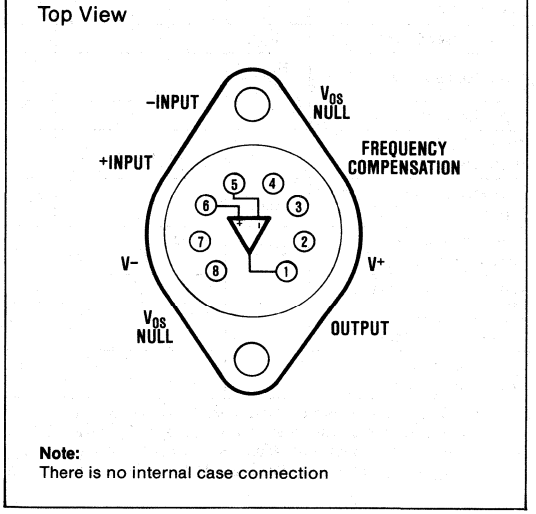
Ordering Information

PART	TEMP. RANGE	PACKAGE
BB3554AM	-25° C to +85° C	8 Lead TO-3
BB3554BM	-25° C to +85° C	8 Lead TO-3
BB3554SM	-55° C to +125° C	8 Lead TO-3
AD3554AM	-25° C to +85° C	8 Lead TO-3
AD3554BM	-25° C to +85° C	8 Lead TO-3
AD3554SM	-55° C to +125° C	8 Lead TO-3

Typical Operating Circuit



Pin Configuration



Note:
There is no internal case connection

5

Wideband Fast-Settling Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 40V
Input Voltage ..... V^+ to V^-
Continuous Output Current ..... ±150mA
Peak Output Current ..... ±250mA
Power Dissipation (See Curves) 3.5W
(Derate linearly above +50°C at 36°C/W to zero at +75°C)

Operating Temperature Range
BB3554SM and AD3554SM ..... $-55°C \le T_A \le +125°C$
BB3554AM, BB3554BM,
AD3554AM, AD3554BM ..... $-25°C \le T_A \le +85°C$
Junction Temperature ..... +175°C
Storage Temperature ..... $-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_S = ±15V; T_{CASE} = +25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	BB3554AM/ AD3554AM			BB3554BM/ AD3554BM			BB3554SM/ AD3554SM			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Open-Loop Voltage Gain	A_{VOL}	V_{OUT} = ±10V R_L = 100Ω	100 90	106 96		100 90	106 96		100 90	106 96		dB
Output Voltage Swing	V_{OUT}	I_{OUT} = ±100mA	±10	±11		±10	±11		±10	±11		V
Output Current Swing	I_{OUT}	V_O = ±10V	±100	±125		±100	±125		±100	±125		mA
Output Resistance	R_{OUT}	f = 10MHz		20			20			20		Ω
Input Offset Voltage	V_{OS}	T_A = +25°C		0.5	2.0		0.2	1.0		0.2	1.0	mV
Average Temperature Coefficient of Offset Voltage		$T_{MIN} < T_C < T_{MAX}$		20	50		8	15		12	25	µV/°C
Power Supply Rejection Ratio	PSRR	±7V to ±18V $T_{MIN} < T_C < T_{MAX}$		80	300		80	300		80	300	µV/V
Input Bias Current	I_B	(Note 1) $T_{MIN} < T_C < T_{MAX}$	0	-10 -0.64	-50	0	-10 -0.64	-50	0	-10 -10	-50	pA nA
I_B vs Supply				1			1			1		pA/V
Input Offset Current	I_{OS}			2	10		2	10		2	10	pA
Input Resistance	R_{DIFF} R_{CM}			10^{11} 10^{11}			10^{11} 10^{11}			10^{11} 10^{11}		Ω
Input Capacitance	C_{IN}			2.0			2.0			2.0		pF
Common-Mode Input Range	V_{CM}	Linear Operation		±(V_{CC} -4)			±(V_{CC} -4)			±(V_{CC} -4)		V
Maximum Safe Input Voltage	$V_{CM(MAX)}$		V^-		V^+	V^-		V^+	V^-		V^+	V
Common-Mode Rejection Ratio	CMR	f = DC, V_{CM} = +7V to -10V	60	78		60	78		60	78		dB
Rated Supply Voltage				±15V			±15V			±15V		V
Voltage Range, Derated Performance			±5V		±18V	±5V		±18V	±5V		±18V	V
Supply Current, Quiescent			17	28	45	17	28	45	17	28	45	mA

Note 1: Specification is at +25°C case temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at T_J = +25°C. When supply voltages are ±15V, no-load operating junction temperature without a heat sink may rise 20-30°C above ambient, and more under heavy load conditions. Accordingly, I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

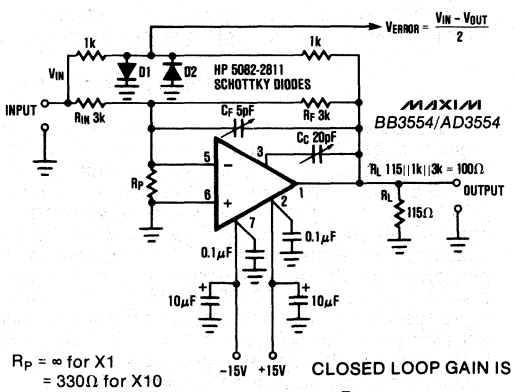
AC ELECTRICAL CHARACTERISTICS

(T_{CASE} = +25°C, V_S = ±15V, R_S = 50Ω, R_L = 50Ω)

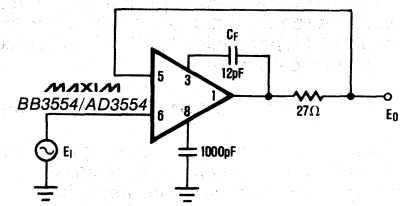
PARAMETER	SYMBOL	CONDITIONS	BB3554AM AD3554AM MIN.	TYP.	MAX.	BB3554BM AD3554BM MIN.	TYP.	MAX.	BB3554SM AD3554SM MIN.	TYP.	MAX.	UNITS
Bandwidth (Note 2)	BW	0dB Small Signal, C_F = 0	70	90		70	90		70	90		MHz
Gain-Bandwidth Product (Note 3)	GBW	C_F = 0, Gain = 10 V/V C_F = 0, Gain = 100 V/V C_F = 0, Gain = 1000 V/V	150 425 1000	225 725 1700		150 425 1000	225 725 1700		150 425 1000	225 725 1700		MHz
Full Power Bandwidth (Note 3)	BW	R_L = 100Ω, V_{IN} = ±10V, C_F = 0	16	19		16	19		16	19		MHz
Slew Rate (Note 3)	SR	R_L = 100Ω, V_{IN} = ±10V, C_F = 0	1000	1200		1000	1200		1000	1200		V/μs
Settling Time (Note 3)		to 1%, Gain = -1 to 0.1%, Gain = -1 to 0.05%, Gain = -1 to 0.01%, Gain = -1		60 120 140 200	 150 250		60 120 140 200	 150 250		60 120 140 200	 150 250	ns
Input Noise Voltage (Note 2)	e_N	R_S = 100Ω, f_0 = 1Hz R_S = 100Ω, f_0 = 10Hz R_S = 100Ω, f_0 = 100Hz R_S = 100Ω, f_0 = 1KHz R_S = 100Ω, f_0 = 10KHz R_S = 100Ω, f_0 = 100KHz R_S = 100Ω, f_0 = 1MHz R_S = 100Ω, f_0 = 0.3Hz to 10Hz R_S = 100Ω, f_0 = 10Hz to 1MHz		125 50 25 15 10 8 7 2 8	450 160 90 50 35 25 25 7 25		125 50 25 15 10 8 7 2 8	450 160 90 50 35 25 25 7 25		125 50 25 15 10 8 7 2 8	450 160 90 50 35 25 25 7 25	nV√Hz μV_{P-P} μV_{RMS}
Input Noise Current (Note 2)	I_N	f_0 = 0.3Hz to 10Hz f_0 = 10Hz to 1MHz		45 2			45 2			45 2		fA, P-P pA, RMS

Note 2: These parameters are untested and not guaranteed. This specification is established to a 90% confidence level.
Note 3: These parameters are sample tested to 10% LTPD.

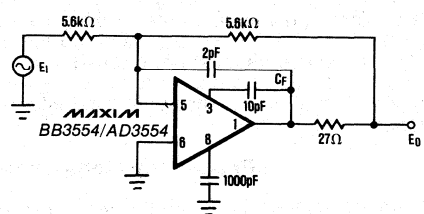
Test Circuits



Settling Time Test Circuit Schematic



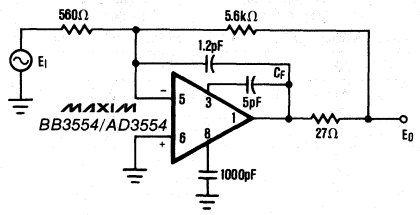
X1 Non-Inverter



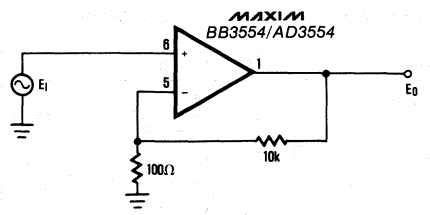
X1 Inverter

Wideband Fast-Settling Operational Amplifier

Test Circuits (continued)



X10 Inverter



X100 Non-Inverter

Application Hints

Layout Considerations

Layout is one of the most important areas of high frequency circuit design. An excellent circuit design may yield only marginal performance if insufficent attention is paid to circuit layout. Operating very high bandwidth devices, such as the BB3554/AD3554, at low closed-loop gains will generally exacerbate the problem.

A ground plane is highly recommended for all applications using high-speed amplifiers. The low resistance, low inductance, and high frequency shielding attainable with a ground plane are advantageous in almost any application.

IC sockets should generally be avoided, as they cause parasitic inductances and capacitances to appear at all pins. If it is required that the device be removable, use individual Hypertronics YSK0102-004 sockets for each of the device pins used.

Power Supply Decoupling

The positive and negative power supply terminals of the BB3554/AD3554 must be well bypassed to ground. Maxim suggests solid tantalum capacitors of about 4.7μf backed-up with high-frequency capacitors such as monolithic ceramics with good performance at 100MHz. The high frequency decoupling capacitors should be placed as close as possible to the device pins. These capacitors must be returned to the same ground point on the ground plane or connected by a short, wide circuit board trace of low inductance and resistance.

Frequency Compensation

The BB3554/AD3554 is internally compensated for closed-loop gains above 50 so the user can optimise bandwidth, slew-rate, and/or settling-time at lower gains by selection of external compensation capacitors. Compensation capacitance is connected between pins 1 and 3, a value of 10pF provides unity-gain stability. For gains up to 50 the value is decreased to zero. The exact value depends on a number of factors including closed-loop gain, layout, and load capacitance.

Settling-time performance into a capacitive load of 1000pF or more may be improved by isolating the load capacitance from the amplifier with a low value resistor of the order of 27Ω. The compensation capacitor remains connected directly from pins 1 to 3, but the output and feedback connections are made to the other end of the new resistor. A 1000pF capacitor from pin 8 to ground can also be beneficial.

High-speed operational amplifiers ordinarily need some capacitance across the feedback resistor to compensate for the inevitable shunt capacitance at the inverting input. The value required is small (typically 2pF) and is repeatable from device to device, so it may be practical to incorporate the feedback capacitor into the PC layout as planned stray capacitance.

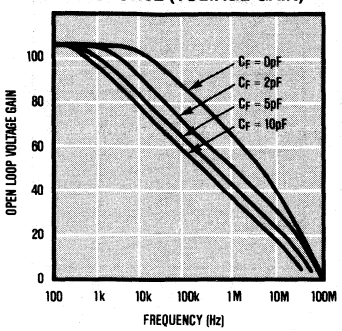
Offset Voltage Adjustment

The BB3554/AD3554 is laser trimmed for minimum offset voltage. The residual offset error may be trimmed by a 10kΩ or 20kΩ linear potentiometer connected between pins 4 and 8 with the wiper connected to V^+. Note that pins 4 and 8 are very sensitive to capacitively coupled pickup. The effect can be minimized by connecting series resistors between the null pins and the null potentiometer, the resistors must be placed close to the BB3554/AD3554. The value of these resistors should be as high as possible consistent with adequate adjustment range, at least 1kΩ is recommended. It is generally undesirable to absorb system offsets by adjusting the amplifier's offset away from zero as this may cause the amplifier's temperature coefficient to be degraded. It is preferable to adjust the system offset in some other manner such as offsetting the non-inverting input of the amplifier or summing a correction signal at the inverting input.

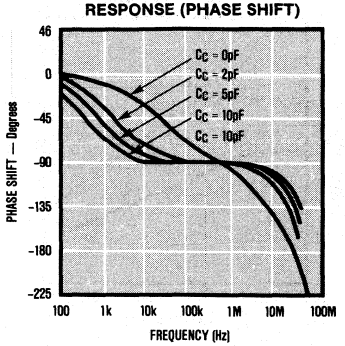
Wideband Fast-Settling Operational Amplifier

Typical Operating Characteristics

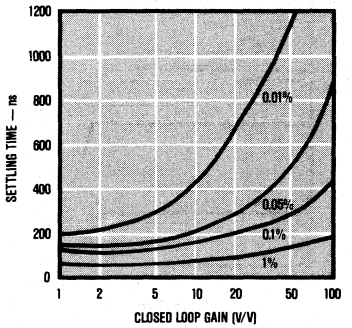
OPEN LOOP FREQUENCY RESPONSE (VOLTAGE GAIN)



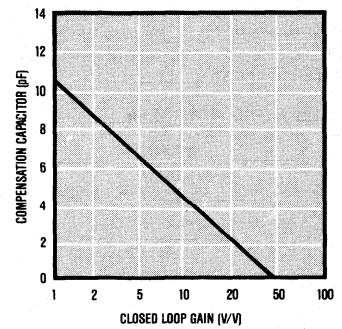
OPEN LOOP FREQUENCY RESPONSE (PHASE SHIFT)



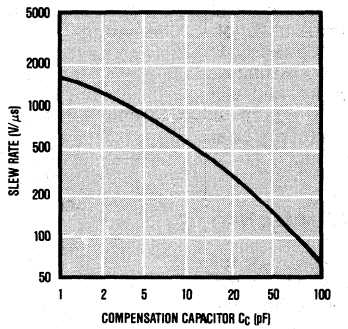
SETTLING TIME vs. CLOSED LOOP GAIN



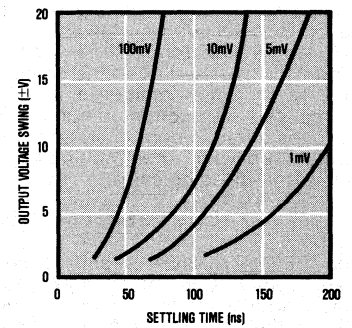
RECOMMENDED COMPENSATION CAPACITOR vs. CLOSED LOOP GAIN



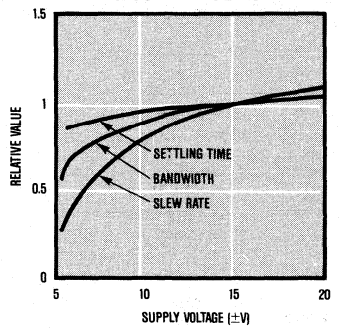
SLEW RATE vs. COMPENSATION



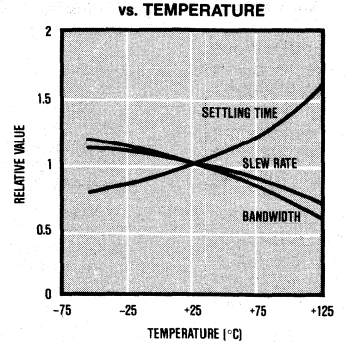
SETTLING TIME vs. OUTPUT VOLTAGE CHANGE



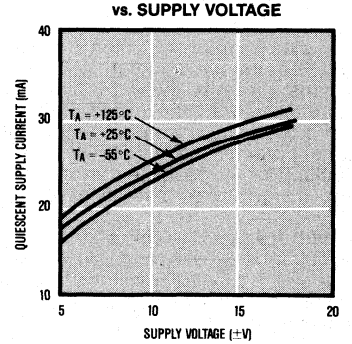
DYNAMIC CHARACTERISTICS vs. SUPPLY VOLTAGE



DYNAMIC CHARACTERISTICS vs. TEMPERATURE



QUIESCSENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



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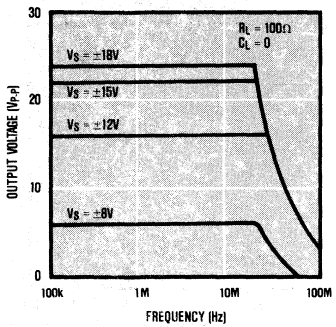
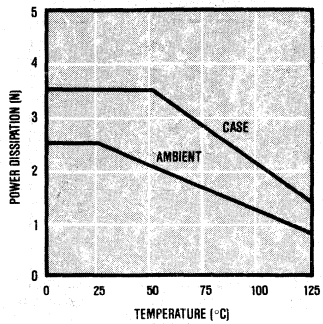
Wideband Fast-Settling Operational Amplifier

Typical Operating Characteristics (continued)

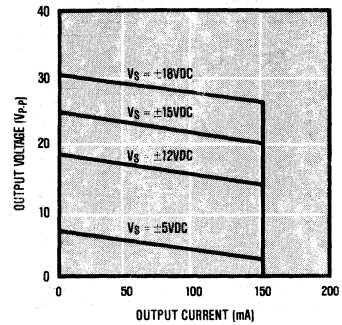
OUTPUT VOLTAGE vs. FREQUENCY



POWER DISSIPATION vs. TEMPERATURE



OUTPUT VOLTAGE vs. OUTPUT CURRENT



Common-Mode Voltage Range

Note that while it is safe to apply common-mode voltage up to and including both the positive and negative power supplies, the common-mode rejection ratio is specified from -10V to +7V. When the BB3554/AD3554 is operated up to the common-mode limit of -11V to +11V the common-mode rejection ratio will be reduced. The common-mode voltage range must be considered when operating with assymetrical power supplies or when running large voltage swings at low non-inverting gains.

Short-Circuit Protection

The BB3554/AD3554 is short-circuit protected for continuous output shorts to ground, but not to the power supplies. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

Guarding

Low bias current and high impedance applications may require the addition of guard rings to divert leakage currents away from the BB3554/AD3554's input terminals. The guard should completely surround the amplifier inputs and should be held at the same potential as the input signal. In addition to blocking board leakage currents the guard will also reduce signal pickup at the inputs.

In high-frequency applications the increase in input capacitance caused by guarding may be undesirable. However, a small capacitor placed across the feedback resistor will compensate for the increased input capacitance.

Heat Sinking

The BB3554/AD3554 does not require heat sinking for most light load applications. For heavy loads and/or high temperature conditions a heat sink will be necessary. Table 1 lists some representative heatsinks for the 8 lead TO3 package.

Table 1. Heat Sinks for BB3554/AD3554

Manufacturer	Part #
Thermalloy	6002-19
IERC	LAIC3B4CB HPI-TO3-33CB
AAVID	5423B,5426B,5327B 5791,5197B-15

Ordinarily, the heat sink will be in electrical contact with the case. The case of the BB3554/AD3554 is not internally connected, so the user is free to connect the case/heat sink to ground, to the output or to simply leave it floating as dictated by the application.

IERC
135 W. Magnolia Bl.
Burbank, CA 91502
(818) 786-1182

Thermalloy
P.O. Box 34829
Dallas, TX 75234
(214) 243-4321

AAVID Engineering
One Kool Path
Box 400
Laconia, NH 03247
(603) 524-4443

Hypertronics
16 Brent Dr.
Hudson, MA 01749
(617) 568-0541

MAXIM

Single/Dual/Triple/Quad Operational Amplifiers

General Description

The ICL761X/762X/763X/764X family of monolithic CMOS op amps combine ultra low input current with low power operation over a wide supply voltage range. With pin selectable quiescent currents of 10, 100, or 1000 μA per amplifier, these op amps will operate from ±1V to ±8V power supplies, or from single supplies from 2V to 16V. The CMOS outputs swing to within millivolts of the supply voltages.

The ultra low bias current of 1 pA makes this family of op amps ideal for long time constant integrators, picoammeters, low droop rate sample/hold amplifiers and other applications where input bias and offset currents are critical. A low noise current of 0.01 pA/$\sqrt{Hz}$ and an input impedance of 10^{12} ohms ensure optimum performance with very high source impedances in such applications as pH meters and photodiode amplifiers.

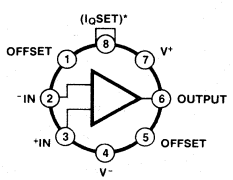
Applications

Battery Powered Instruments
Low Leakage Amplifiers
Long Time Constant Integrators
Low Frequency Active Filters
Hearing Aids and Microphone Amplifiers
Low Droop Rate Sample/Hold Amplifiers
Picoammeters

Pin Configuration

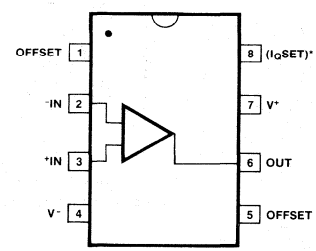
Top View

SINGLES—ICL7611/12/14/16
TO—99



*PIN 7 CONNECTED TO CASE

8 PIN DIP



*EXTERNAL COMPENSATION (ICL7614)

Features

- **Pin-for Pin 2nd Source!**
- **1 pA Typical Bias Current—4 nA Maximum @ 125°C**
- **Wide Supply Voltage Range ±1V to ±8V**
- **Industry Standard Pinouts**
- **Programmable Quiescent Currents of 10, 100 and 1000 μA**
- **Monolithic, Low Power CMOS Design**

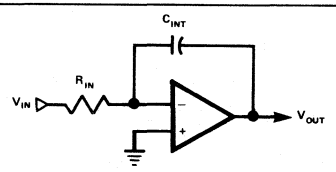
Ordering Information

ICL76XX M N OP

V_{OS} SELECTION	TEMP. RANGE	PACKAGE CODE
A=2mV	C=0°C to 70°C	TV - 8 PIN TO-99
B=5mV	M=-55°C to +125°C	PA - 8 PIN PLASTIC DIP
C=10mV		SA - 8 PIN SMALL S.O.
D=15mV		JD - 14 PIN CERDIP
E=20mV		PD - 14 PIN PLASTIC DIP
		SD - 14 PIN SMALL S.O.
		JE - 16 PIN CERDIP
		PE - 16 PIN PLASTIC DIP
		SE - 16 PIN SMALL S.O.
		WE - 16 PIN WIDE S.O.

	Singles				Duals			Triples		Quads	
	ICL7611	ICL7612	ICL7614	ICL7616	ICL7621	ICL7622	ICL7631	ICL7632	ICL7641	ICL7642
Compensated	X	X		X	X	X	X		X	X
Externally Compensated			X							
Extended CMVR		X		X						
Offset null capability	X	X	X	X		X				
Programmable I_Q	X	X		X			X	X		
Fixed I_Q 10μA										X
Fixed I_Q 100μA			X		X	X				
Fixed I_Q 1mA									X	

Typical Operating Circuit



Long Time Constant Integrator
(Detailed Circuit Diagram — Figure 10)

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Single/Dual/Triple/Quad Operational Amplifiers

Ordering Information

Single & Dual

PART	TEMP. RANGE	PACKAGE
ICL761XACPA	0°C to +70°C	8 Lead Plastic DIP
ICL761XACSA	0°C to +70°C	8 Lead Slim S.O.
ICL761XACTV	0°C to +70°C	TO-99 Metal Can
ICL761XAMTV	-55°C to +125°C	TO-99 Metal Can
ICL761XBCPA	0°C to +70°C	8 Lead Plastic DIP
ICL761XBCSA	0°C to +70°C	8 Lead Slim S.O.
ICL761XBCTV	0°C to +70°C	TO-99 Metal Can
ICL761XBMTV	-55°C to +125°C	TO-99 Metal Can
ICL761XDCPA	0°C to +70°C	8 Lead Plastic DIP
ICL761XDCSA	0°C to +70°C	8 Lead Slim S.O.
ICL761XDCTV	0°C to +70°C	TO-99 Metal Can
ICL761XDC/D	0°C to +70°C	Dice
ICL7621ACPA	0°C to +70°C	8 Lead Plastic DIP
ICL7621ACSA	0°C to +70°C	8 Lead Slim S.O.
ICL7621ACTV	0°C to +70°C	TO-99 Metal Can
ICL7621AMTV	-55°C to +125°C	TO-99 Metal Can
ICL7621BCPA	0°C to +70°C	8 Lead Plastic DIP
ICL7621BCSA	0°C to +70°C	8 Lead Slim S.O.

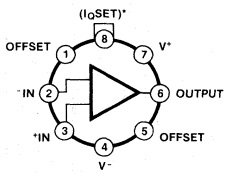
PART	TEMP. RANGE	PACKAGE
ICL7621BCTV	0°C to +70°C	TO-99 Metal Can
ICL7621BMTV	-55°C to +125°C	TO-99 Metal Can
ICL7621DCPA	0°C to +70°C	8 Lead Plastic DIP
ICL7621DCSA	0°C to +70°C	8 Lead Slim S.O.
ICL7621DCTV	0°C to +70°C	TO-99 Metal Can
ICL7621DC/D	0°C to +70°C	Dice
ICL7622ACPD	0°C to +70°C	14 Lead Plastic DIP
ICL7622ACSD	0°C to +70°C	14 Lead Slim S.O.
ICL7622ACJD	0°C to +70°C	14 Lead CERDIP
ICL7622AMJD	-55°C to +125°C	14 Lead CERDIP
ICL7622BCPD	0°C to +70°C	14 Lead Plastic DIP
ICL7622BCSA	0°C to +70°C	14 Lead Slim S.O.
ICL7622BCJD	0°C to +70°C	14 Lead CERDIP
ICL7622BMJD	-55°C to +125°C	14 Lead CERDIP
ICL7622DCPD	0°C to +70°C	14 Lead Plastic DIP
ICL7622DCSD	0°C to +70°C	14 Lead Slim S.O.
ICL7622DCJD	0°C to +70°C	14 Lead CERDIP
ICL7622DC/D	0°C to +70°C	Dice

(X above is replaced by: 1, 2, 4, 6)

Pin Configuration

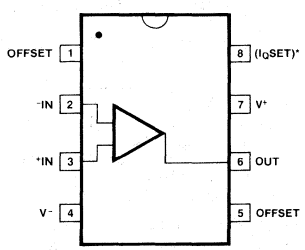
Top View

SINGLES—ICL7611/12/14/16
TO—99



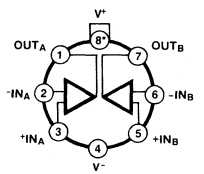
*PIN 7 CONNECTED TO CASE

8 Lead

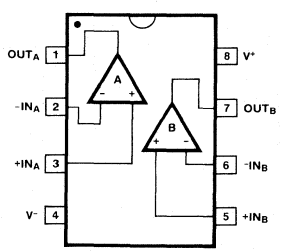


*EXTERNAL COMPENSATION (ICL7614)

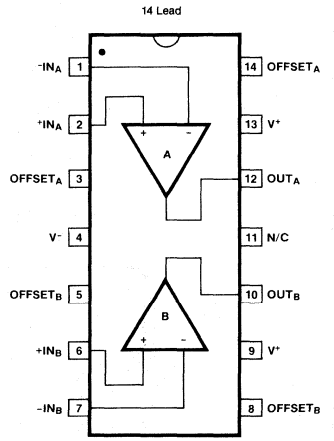
DUALS—ICL7621/22
TO—99



8 Lead



14 Lead



Note: PINS 9 & 13 ARE INTERNALLY CONNECTED

ABSOLUTE MAXIMUM RATINGS[1] — Single & Dual

Total Supply Voltage V^+ to V^- 18V
Input Voltage . . . . . $V^+ + 0.3$ to $V^- - 0.3V$
Differential Input Voltage[2] . . . . . $\pm\lvert(V^+ + 0.3) - (V^- - 0.3)\rvert$V
Duration of Output Short Circuit[3] . . . . . Unlimited
Continuous Power Dissipation @ 25°C — Above 25°C derate as follows:

TO-99 Metal Can	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead CERDIP	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead CERDIP	500mW	4mW/°C

Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
M Series . . . . . −55°C to +125°C
C Series . . . . . 0°C to +70°C
Lead Temperature Soldering, 10 sec . . . . . 300°C

Notes:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS — Single & Dual

($V_{SUPP} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		10			15		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		0.5	30 300		0.5	30 300	pA
Input Bias Current	I_{BIAS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		1.0	50 500		1.0	50 500	pA
Common Mode Voltage Range (Except ICL7612, ICL7616)	V_{CMR}		−0.4		+0.6	−0.4		+0.6	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		−1.1		+0.6	−1.1		+0.6	V
Extended Common Mode Voltage Range (ICL7616 Only)	V_{CMR}	$I_Q = 10\mu A$	−1.3		−0.3	−1.3		−0.3	V
Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$, $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		±0.98 ±0.96			±0.98 ±0.96		V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 0.1V$, $R_L = 1M\Omega$ $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		90 80			90 80		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$		80			80		dB
Input Referred Noise Voltage	e_n	$R_S = 100\Omega$, f = 1kHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S = 100\Omega$, f = 1kHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Slew Rate	SR	$A_{VOL} = 1$, $C_L = 100pF$, $V_{IN} = 0.2V_{p-p}$ $R_L = 1M\Omega$		0.016			0.016		V/μs
Rise Time	t_r	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5			5		%

Single/Dual/Triple/Quad Operational Amplifiers

ELECTRICAL CHARACTERISTICS — Single & Dual
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, T_A = 25°C $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7			15 20	mV mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		10			15			25		µV/°C
Input Offset Current	I_{OS}	T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
Common Mode Voltage Range (Except ICL7612, ICL7616)	V_{CMR}	I_Q = 10µA[1]	+4.4 −4.0			+4.4 −4.0			+4.4 −4.0			V
		I_Q = 100µA[1]	+4.2 −4.0			+4.2 −4.0			+4.2 −4.0			
		I_Q = 1mA[1]	+3.7 −3.7			+3.7 −3.7			+3.7 −3.7			
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	I_Q = 10µA	±5.3			±5.3			±5.3			V
		I_Q = 100µA	+5.3 −5.1			+5.3 −5.1			+5.3 −5.1			
		I_Q = 1mA	+5.3 −4.5			+5.3 −4.5			+5.3 −4.5			
Extended Common Mode Voltage Range (ICL7616 Only)	V_{CMR}	I_Q = 10µA	−5.3 +3.7			−5.3 +3.7			−5.3 +3.5			V
		I_Q = 100µA	−5.1 +3.0			−5.1 +3.0			−5.1 +2.7			
		I_Q = 1mA	−4.5 +2.0			+4.5 +2.0			−4.5 +1.7			
Output Voltage Swing	V_{OUT}	(1) I_Q = 10µA, R_L = 1MΩ T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			V
		I_Q = 100µA, R_L = 100kΩ T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			
		(1) I_Q = 1mA, R_L = 10kΩ T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			
Large Signal Voltage Gain	A_{VOL}	V_O = ±4.0V, R_L = 1MΩ I_Q = 10µA, T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 86 80 74	 104		 80 75 68	 104		 80 75 68	 104		dB
		V_O = ±4.0V, R_L = 100kΩ I_Q = 100µA, T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 86 80 74	 102		 80 75 68	 102		 80 75 68	 102		
		V_O = ±4.0V, R_L = 10kΩ I_Q = 1mA,[1] T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 80 76 72	 83		 76 72 68	 83		 76 72 68	 83		
Unity Gain Bandwidth	G_{BW}	I_Q = 10µA[1] I_Q = 100µA I_Q = 1mA[1]		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz

Note 1: ICL7611, 7612, 7616 only
Note 2: ICL7614; 39 pF from pin 6 to pin 8.

ELECTRICAL CHARACTERISTICS — Single & Dual (Continued)
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	UNITS
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$, $I_Q = 10\mu A$[1]	76	96		70	96		70	96		dB
		$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	76	91		70	91		70	91		
		$R_S \leq 100k\Omega$, $I_Q = 1mA$[1]	66	87		60	87		60	87		
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$, $I_Q = 10\mu A$[1]	80	94		80	94		80	94		dB
		$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	80	86		80	86		80	86		
		$R_S \leq 100k\Omega$, $I_Q = 1mA$[1]	70	77		70	77		70	77		
Input Referred Noise Voltage	e_n	$R_S = 100\Omega$, f = 1kHz		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S = 100\Omega$, f = 1kHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load										mA
		$I_Q = 10\mu A$[1]		0.01	0.02		0.01	0.02		0.01	0.02	
		$I_Q = 100\mu A$		0.1	0.25		0.1	0.25		0.1	0.25	
		$I_Q = 1mA$[1]		1.0	2.5		1.0	2.5		1.0	2.5	
Channel Separation	V_{O1}/V_{O2}	$A_{VOL} = 100$		120			120			120		dB
Slew Rate[2]	SR	$A_{VOL} = 1$, $C_L = 100pF$ $V_{IN} = 8V_{p-p}$										V/μs
		$I_Q = 10\mu A$,[1] $R_L = 1M\Omega$		0.016			0.016			0.016		
		$I_Q = 100\mu A$, $R_L = 100k\Omega$		0.16			0.16			0.16		
		$I_Q = 1mA$,[1] $R_L = 10k\Omega$		1.6			1.6			1.6		
Rise Time[2]	t_r	$V_{IN} = 50mV$, $C_L = 100pF$										μs
		$I_Q = 10\mu A$,[1] $R_L = 1M\Omega$		20			20			20		
		$I_Q = 100\mu A$, $R_L = 100k\Omega$		2			2			2		
		$I_Q = 1mA$,[1] $R_L = 10k\Omega$		0.9			0.9			0.9		
Overshoot Factor[2]		$V_{IN} = 50mV$, $C_L = 100pF$										%
		$I_Q = 10\mu A$,[1] $R_L = 1M\Omega$		5			5			5		
		$I_Q = 100\mu A$, $R_L = 100k\Omega$		10			10			10		
		$I_Q = 1mA$,[1] $R_L = 10k\Omega$		40			40			40		

Note 1: ICL7611, 7612, 7616 only.
Note 2: ICL7614; 39 pF from pin 6 to pin 8.

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Single/Dual/Triple/Quad Operational Amplifiers

Ordering Information

Triple & Quad

PART	TEMP. RANGE	PACKAGE
ICL763XBCPE	0°C to +70°C	16 Lead Plastic DIP
ICL763XBCSE	0°C to +70°C	16 Lead Slim S.O.
ICL763XCCPE	0°C to +70°C	16 Lead Plastic DIP
ICL763XCCSE	0°C to +70°C	16 Lead Slim S.O.
ICL763XECPE	0°C to +70°C	16 Lead Plastic DIP
ICL763XECSE	0°C to +70°C	16 Lead Slim S.O.
ICL763XBCJE	0°C to +70°C	16 Lead CERDIP
ICL763XCCJE	0°C to +70°C	16 Lead CERDIP
ICL763XECJE	0°C to +70°C	16 Lead CERDIP
ICL763XBMJE	-55°C to +125°C	16 Lead CERDIP
ICL763XCMJE	-55°C to +125°C	16 Lead CERDIP
ICL763XEC/D	0°C to +70°C	Dice

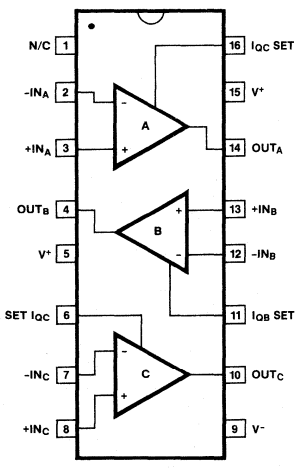
PART	TEMP. RANGE	PACKAGE
ICL764XBCPD	0°C to +70°C	14 Lead Plastic DIP
ICL764XBCWE	0°C to +70°C	16 Lead Wide S.O.
ICL764XCCPD	0°C to +70°C	14 Lead Plastic DIP
ICL764XCCWE	0°C to +70°C	16 Lead Wide S.O.
ICL764XECPD	0°C to +70°C	14 Lead Plastic DIP
ICL764XECWE	0°C to +70°C	16 Lead Wide S.O.
ICL764XBCJD	0°C to +70°C	14 Lead CERDIP
ICL764XCCJD	0°C to +70°C	14 Lead CERDIP
ICL764XECJD	0°C to +70°C	14 Lead CERDIP
ICL764XBMJD	-55°C to +125°C	14 Lead CERDIP
ICL764XCMJD	-55°C to +125°C	14 Lead CERDIP
ICL764XEC/D	0°C to +70°C	Dice

(X above is replaced by: 1, 2)

Pin Configuration

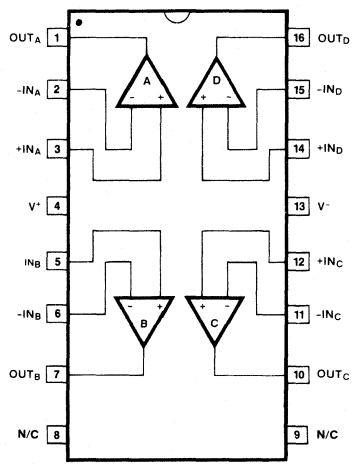
Top View

ICL7631/32
16 Lead

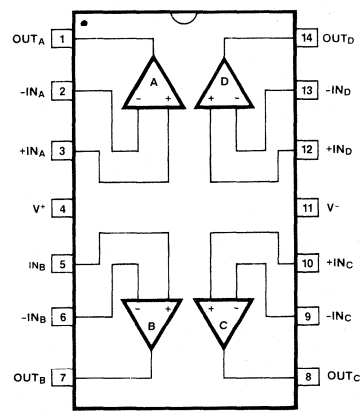


Note: Pins 5 & 15 are internally connected

ICL7641/42
16 Lead Wide S.O.



ICL7641/42
14 Lead



ABSOLUTE MAXIMUM RATINGS[1] — Triple & Quad

Total Supply Voltage V^+ to V^- 18V
Input Voltage . . . . . $V^+ + 0.3$ to $V^- - 0.3V$
Differential Input Voltage[2] . . . . . $\pm|(V^+ + 0.3) - (V^- - 0.3)|V$
Duration of Output Short Circuit[3] . . . . . Unlimited

Continuous Power Dissipation @ 25°C		Above 25°C derate as follows:
TO-99 Metal Can	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead CERDIP	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead CERDIP	500mW	4mW/°C

Storage Temperature Range . . . . . −55°C to +150°C

Operating Temperature Range
M Series . . . . . −55°C to +125°C
C Series . . . . . 0°C to +70°C
Lead Temperature Soldering, 10 sec . . . . . 300°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS — Triple & Quad

($V_{SUPP} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless noted)
Specs apply to ICL7631/7632/7642 only.

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			5 7			10 12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		15			20		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		0.5	30 300		0.5	30 300	pA
Input Bias Current	I_{BIAS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		1.0	50 500		1.0	50 500	pA
Common Mode Voltage Range	V_{CMR}		−0.4		+0.6	−0.4		+0.6	V
Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$, $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		±0.98 ±0.96			±0.98 ±0.96		V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 0.1V$, $R_L = 1M\Omega$ $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		90 80			90 80		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR			80			80		dB
Input Referred Noise Voltage	e_n	$R_S = 100\Omega$, f = 1kHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S = 100\Omega$, f = 1kHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Channel Separation	V_{O1}/V_{O2}	$A_{VOL} = 100$		120			120		dB
Slew Rate	SR	$A_{VOL} = 1$, $C_L = 100pF$, $V_{IN} = 0.2V_{p-p}$ $R_L = 1M\Omega$		0.016			0.016		V/μs
Rise Time	t_r	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5			5		%

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Single/Dual/Triple/Quad Operational Amplifiers

ELECTRICAL CHARACTERISTICS — Triple & Quad
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, T_A = 25°C			5			10			20	mV
		$T_{MIN} \leq T_A \leq T_{MAX}$			7			15			25	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		15			20			30		µV/°C
Input Offset Current	I_{OS}	T_A = 25°C		0.5	30		0.5	30		0.5	30	pA
		0°C≤T_A≤+70°C			300			300			300	
		−55°C≤T_A≤+125°C			800			800			800	
Input Bias Current	I_{BIAS}	T_A = 25°C		1.0	50		1.0	50		1.0	50	pA
		0°C≤T_A≤+70°C			500			500			500	
		−55°C≤T_A≤+125°C			4000			4000			4000	
Common Mode Voltage Range	V_{CMR}	I_Q = 10µA[1]	+4.4 −4.0			+4.4 −4.0			+4.4 −4.0			V
		I_Q = 100µA[3]	+4.2 −4.0			+4.2 −4.0			+4.2 −4.0			V
		I_Q = 1mA[2]	+3.7 −3.7			+3.7 −3.7			+3.7 −3.7			V
Output Voltage Swing	V_{OUT}	(1) I_Q = 10µA, R_L = 1MΩ										
		T_A = 25°C	±4.9			±4.9			±4.9			V
		0°C≤T_A≤+70°C	±4.8			±4.8			±4.8			
		−55°C≤T_A≤+125°C	±4.7			±4.7			±4.7			
		I_Q = 100µA, R_L = 100kΩ										
		(3) T_A = 25°C	±4.9			±4.9			±4.9			V
		0°C≤T_A≤+70°C	±4.8			±4.8			±4.8			
		−55°C≤T_A≤+125°C	±4.5			±4.5			±4.5			
		(2) I_Q = 1mA, R_L = 10kΩ										
		T_A = 25°C	±4.5			±4.5			±4.5			V
		0°C≤T_A≤+70°C	±4.3			±4.3			±4.3			
		−55°C≤T_A≤+125°C	±4.0			±4.0			±4.0			
Large Signal Voltage Gain	A_{VOL}	V_O = ±4.0V, R_L = 1MΩ[1]										
		I_Q = 10µA,[1] T_A = 25°C	86	104		80	104		80	104		dB
		0°C≤T_A≤+70°C	80			75			75			
		−55°C≤T_A≤+125°C	74			68			68			
		V_O = ±4.0V, R_L										
		I_Q = 100µA, T_A = 25°C	86	102		80	102		80	102		dB
		0°C≤T_A≤+70°C	80			75			75			
		−55°C≤T_A≤+125°C	74			68			68			
		V_O = ±4.0V, R_L = 10kΩ[2]										
		I_Q = 1mA,[1] T_A = 25°C	86	98		80	98		80	98		dB
		0°C≤T_A≤+70°C	80			75			75			
		−55°C≤T_A≤+125°C	74			68			68			
Unity Gain Bandwidth	G_{BW}	I_Q = 10µA[1]		0.044			0.044			0.044		MHz
		I_Q = 100µA[3]		0.48			0.48			0.48		
		I_Q = 1mA[2]		1.4			1.4			1.4		
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$, I_Q = 10µA[1]	76	96		70	96		70	96		dB
		$R_S \leq 100k\Omega$, I_Q = 100µA	76	91		70	91		70	91		
		$R_S \leq 100k\Omega$, I_Q = 1mA[2]	66	87		60	87		60	87		
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$, I_Q = 10µA[1]	80	94		80	94		80	94		dB
		$R_S \leq 100k\Omega$, I_Q = 100µA	80	86		80	86		80	86		
		$R_S \leq 100k\Omega$, I_Q = 1mA[2]	70	77		70	77		70	77		

Note 1: Does not apply to 7641.
Note 2: Does not apply to 7642.
Note 3: ICL7631/32 only.
Note 4: Does not apply to 7632.

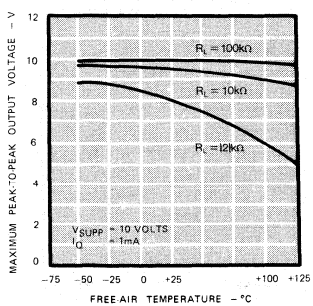
ELECTRICAL CHARACTERISTICS — Triple & Quad (Continued)
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Referred Noise Voltage	e_n	R_S = 100Ω, f = 1kHz		100			100			100		nV/√Hz
Input Referred Noise Current	i_n	R_S = 100Ω, f = 1kHz		0.01			0.01			0.01		pA/√Hz
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load I_Q = 10μA[1] I_Q = 100μA I_Q = 1mA[2]		 0.01 0.1 1.0	 0.022 0.25 2.5		 0.01 0.1 1.0	 0.022 0.25 2.5		 0.01 0.1 1.0	 0.022 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_{VOL} = 100		120			120			120		dB
Slew Rate[4]	SR	A_{VOL} = 1, C_L = 100pF V_{IN} = 8V_{p-p} I_Q = 10μA,[1] R_L = 1MΩ I_Q = 100μA, R_L = 100kΩ I_Q = 1mA,[1] R_L = 10kΩ[2]		 0.016 0.16 1.6			 0.016 0.16 1.6			 0.016 0.16 1.6		V/μs
Rise Time[4]	t_r	V_{IN} = 50mV, C_L = 100pF I_Q = 10μA,[1] R_L = 1MΩ I_Q = 100μA, R_L = 100kΩ I_Q = 1mA,[2] R_L = 10kΩ		 20 2 0.9			 20 2 0.9			 20 2 0.9		μs
Overshoot Factor[4]		V_{IN} = 50mV, C_L = 100pF I_Q = 10μA,[1] R_L = 1MΩ I_Q = 100μA, R_L = 100kΩ I_Q = 1mA,[2] R_L = 10kΩ		 5 10 40			 5 10 40			 5 10 40		%

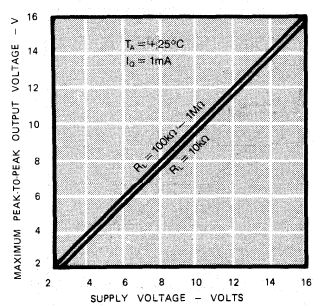
Note 1: Does not apply to 7641.
Note 2: Does not apply to 7642.
Note 3: ICL7631/32 only.
Note 4: Does not apply to 7632.

Typical Operating Characteristics

MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



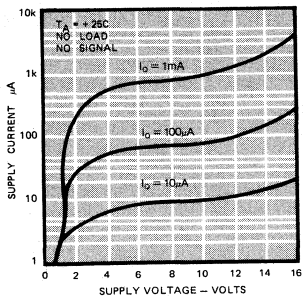
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



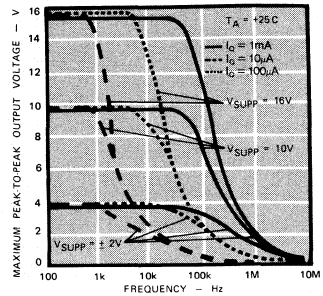
Single/Dual/Triple/Quad Operational Amplifiers

Typical Operating Characteristics

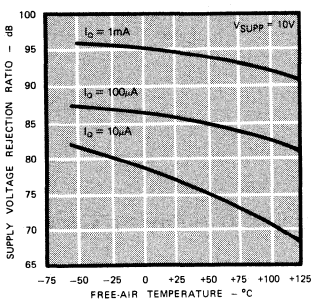
SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE



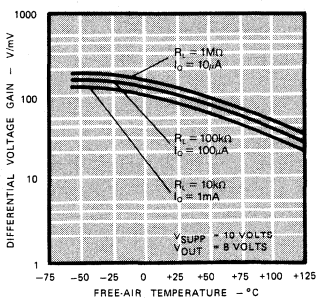
PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



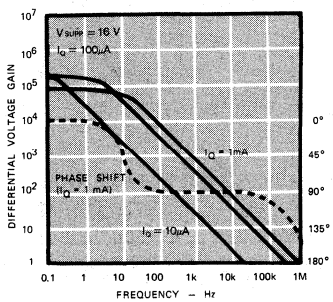
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



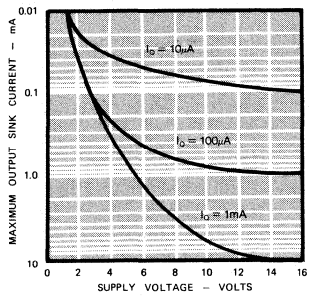
LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE



LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY

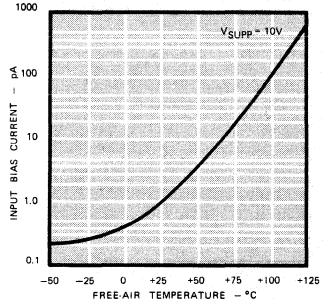


MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

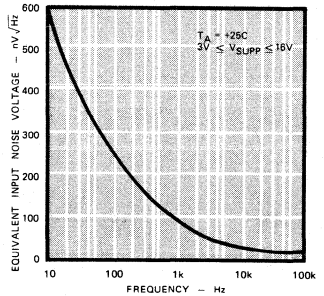


Typical Operating Characteristics

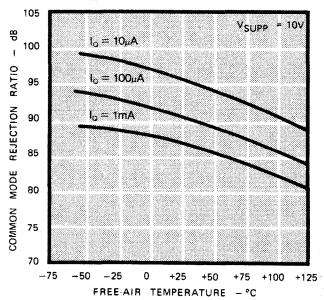
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



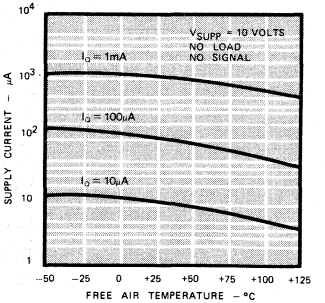
EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



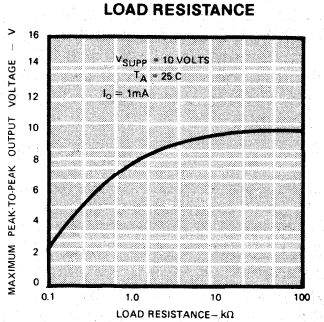
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



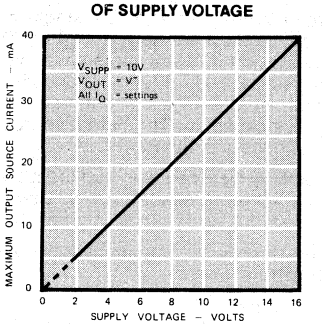
SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



MAXIMUM OUTPUT/SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

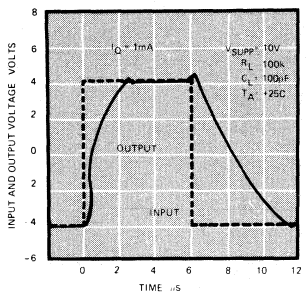


5

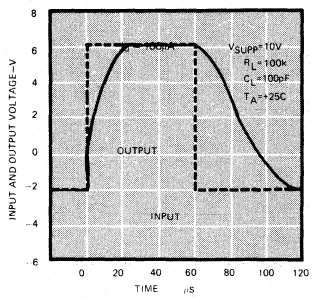
Single/Dual/Triple/Quad Operational Amplifiers

Typical Operating Characteristics

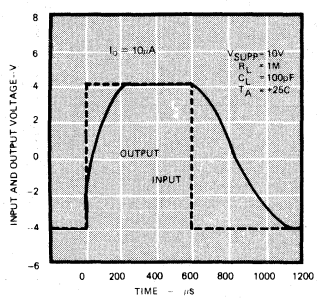
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



Detailed Description

Quiescent Current Selection

The voltage input to the I_Q pin of the single and triple amplifiers selects a quiescent current (I_Q) of 10, 100 or 1000 µA. The dual and quad amplifiers have fixed quiescent current (I_Q) settings. Unity gain bandwidth and slew rate increase with increasing quiescent current, as does output sink current capability. The output source current capability is independent of quiescent current.

The lowest I_Q setting that results in sufficient bandwidth and slew rate should be selected for each specific application.

The I_Q pin of the single and triple amplifiers controls the quiescent current as follows:

I_Q = 10 µA..... I_Q pin to V^+
I_Q = 100 µA..... I_Q pin between V^- +0.8V and V^+ −0.8V
I_Q = 1 mA..... I_Q pin to V^-

Input Offset Nulling

The input offset can be nulled by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1 mA and 100 µA, the nulling range provided is adequate for all V_{OS} selections. However with higher values of V_{OS}, and an I_Q of 10 µA, nulling may not be possible.

Frequency Compensation

All of the ICL7611 and ICL7621 Series except the ICL7614 are internally compensated for unity gain operation. The ICL7614 is externally compensated by a capacitor connected between COMP and OUT pins, with 39 pF being sufficient compensation for a unity gain buffer. For gains greater than unity, the compensation capacitor value may be reduced to increase the bandwidth and slew rate. The ICL7132 is not compensated and does not have frequency compensation pins. Use only at gains ≥20 at I_Q of 1mA; at gains ≥10 at I_Q of 100µA; at gains ≥5 at I_Q of 10µA.

Output Loading Considerations

Approximately 70% of the amplifier's quiescent current flows in the output stage. The output swing can approach the supply rails for output loads of 1M, 100k and 10k, using the output stage in a highly linear class A mode. Crossover distortion is avoided and the voltage gain is maximized in this mode. The output stage, however, can also be operated in Class AB, which supplies higher output currents. (See graphs under Typical Operating Characteristics). The voltage gain decreases and the output transfer characteristic is non-linear during the transition from Class A to Class B operation.

The output stage, with a gain that is directly proportional to load impedance, approximates a transconductance amplifier. Approximately the same open loop gains are obtained at each of the I_Q settings if corresponding loads of 10k, 100k, and 1M are used.

The maximum output source current is higher than the maximum sink current, and is independent of I_Q.

Like most amplifiers, there are output loads for which the amplifier stability is not guaranteed. In particular, avoid capacitive loads greater than 100 pF; and while on the 1mA I_Q setting, avoid loads less than 5 kΩ. Since the output stage is a transconductance output, very large (>10 μF) capacitive loads will create a dominant pole and the output will be stable, even with loads that are less than 5 kΩ.

Extended Common Mode Voltage Range, ICL7612 and ICL7616

A common mode voltage range that includes both V^+ and V^- is often desirable, especially in single supply operation. The ICL7612 and ICL7616 extended common mode range op amps are designed specifically to meet this need. The ICL7612 input common mode voltage range (CMVR) extends beyond both power supply rails when operated with at least 3V total supply and an I_Q of 10μA or 100μA. The ICL7616 CMVR includes the negative supply voltage (or ground when operated with a single supply) at an I_Q of 10μA or 100μA.

Printed Circuit Board Layout

Careful PCB layout techniques must be used to take full advantage of the very low bias current of the ICL7611 family. The inputs should be encircled with a low impedance trace, or guard, that is at the same potential as the inputs. In an inverting amplifier this is normally ground; in a unity gain buffer connect the guard to the ouput. A convenient way of guarding the 8 pin TO-99 version of the ICL7611 is to use a 10 pin circle, with the two extra pads on either side of the input pins to provide space for a guard ring (see Figure 8). Assembled boards should be carefully cleaned, and if a high humidity environment is expected, conformally coated.

Single Supply Operation

The ICL7611 family will operate from a single 2V to 16V power supply. The common mode voltage range of the standard amplifier types when operated from a single supply is 1.0V to ($V^+ - 0.6V$) at 10 μA I_Q. At 100 μA I_Q the CMVR is 1.0V to ($V^+ - 0.8V$), and at 1 mA I_Q the CMVR is 1.3V to ($V^+ - 1.3V$). If this CMVR range is insufficient, use the ICL7612, whose CMVR includes both ground and V^+, or the ICL7616, whose CMVR includes ground.

A convenient way to generate a psuedo-ground at $V^+/2$ is to use one op amp of a quad to buffer a $V^+/2$ voltage from a high impedance resistive divider.

Low Voltage Operation

Operation at $V_{SUPP} = \pm 1.0V$ is only guaranteed at I_Q = 10 μA. Output swings to within a few millivolts of the supply rails are achievable for R_L (> or =) 1 MΩ. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to −0.7V at $V_{SUPP} = \pm 1.0V$. For applications where greater common mode range is desirable, refer to description of ICL7612 and ICL7616 above.

Applications

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

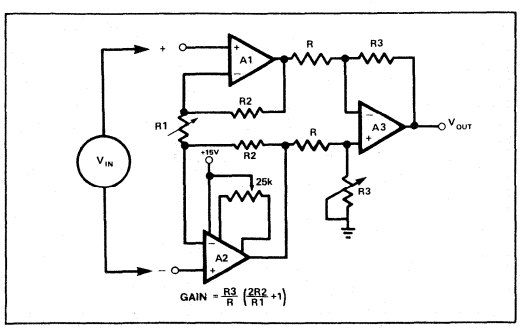


Figure 1. Instrumentation Amplifier—Adjust R3 to improve CMRR. The offset of all three amplifiers is nulled by the offset adjustment of A2.

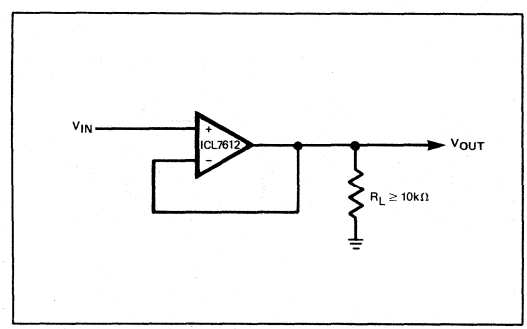


Figure 2. Simple Follower—By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

Single/Dual/Triple/Quad Operational Amplifiers

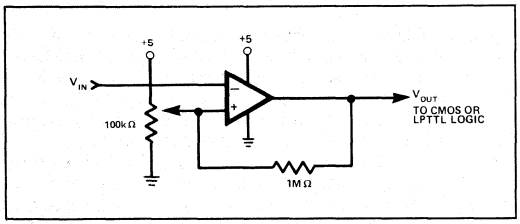


Figure 3. Level Detector—By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

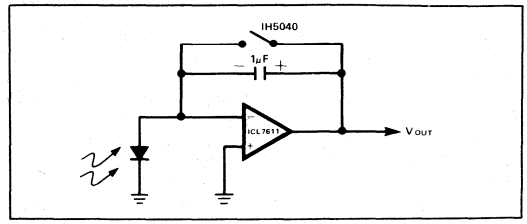


Figure 4. Photocurrent Integrator—Low leakage currents allow integration times up to several hours.

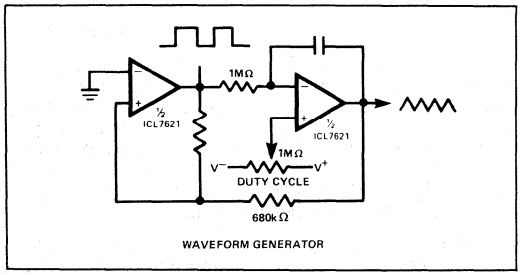


Figure 5. Precise Triangle/Square Wave Generator—The frequency and duty cycle are virtually independent of power supply.

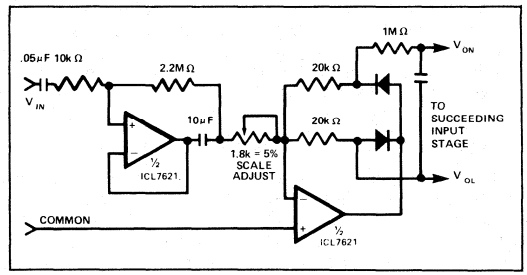


Figure 6. Averaging AC to DC Converter—Recommended for Maxim's ICL7106/07/09 A/D Converters.

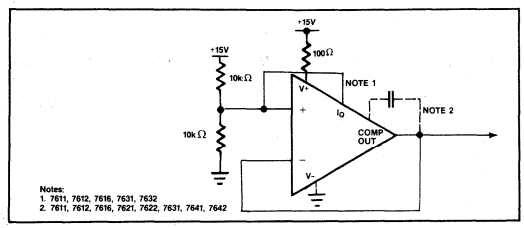


Figure 7. Burn-In and Life Test Circuit

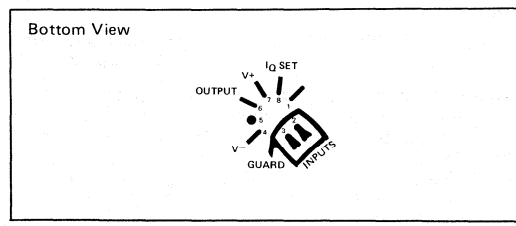


Figure 8. Input Guard for TO-99

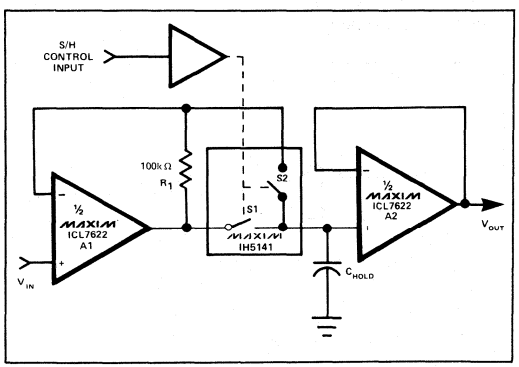


Figure 9. Low Droop Rate Sample & Hold—S2 improves accuracy and acquisition time by including the voltage drop across S1 inside the feedback loop. R1 closes the feedback loop of A1 during the hold phase. The droop rate is $[I_{BIAS(AZ)} + I_{LEAK(S1)} + I_{LEAK(S2)}]/C_{HOLD}$.

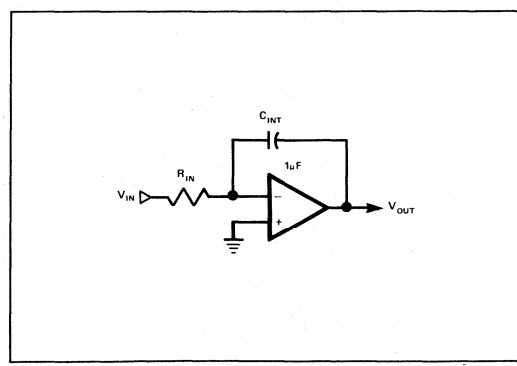


Figure 10. Long Time Constant Integrator—With R_{IN} = 10" ohm, the time constant of this integrator is 100,000 seconds. Since the input voltage is converted to a current by R_{IN}, the input voltage can far exceed the power supply voltage.

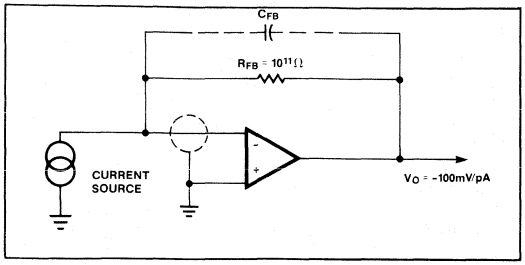


Figure 11. Pico Ammeter—The response time of this circuit is $R_{FB} \times C_{FB}$, where C_{FB} is the stray capacitance between the output and the inverting terminal of the amplifier.

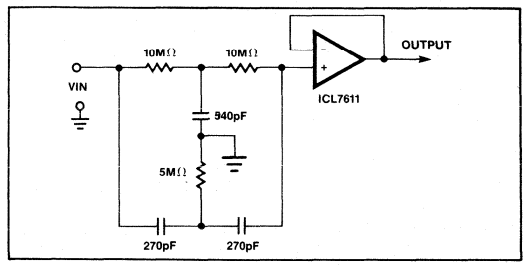
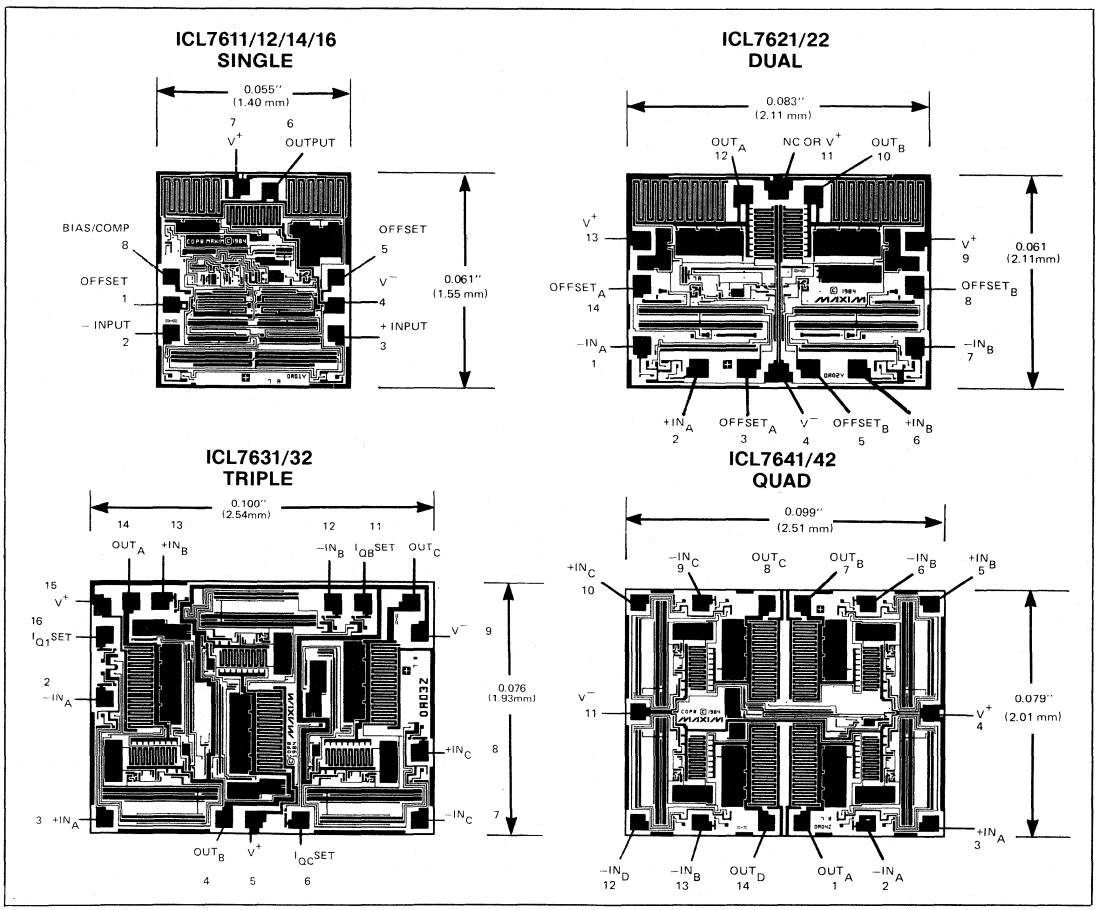


Figure 12. 60 Hz Twin "T" Notch Filter—The low, 1 pA bias current of the ICL7611 allows use of small 540 pF and 270 pF capacitors, even with a notch frequency of 60 Hz. The 60 Hz rejection is approximately 40 dB.

Chip Topographies



MAXIM
Chopper Stabilized Operational Amplifier

General Description

The Maxim ICL7650 is a chopper-stabilized amplifier, ideal for low-level signal processing applications. Featuring high performance and versatility, this device combines low input offset voltage, low input bias current, wide bandwidth and exceptionally low drift over time and temperature. Low offset is achieved through a nulling scheme that provides continuous error correction. A nulling amplifier alternately nulls itself and the main amplifier. The result is an input offset voltage that is held to a minimum over the entire operating temperature range.

The ICL7650B is an exact replacement for the Intersil ICL7650B. This device has a maximum offset voltage of 10μV, a maximum input offset voltage temperature coefficient of 0.1μV/°C, and a maximum bias current of 20 pA; all specified over the commercial temperature range.

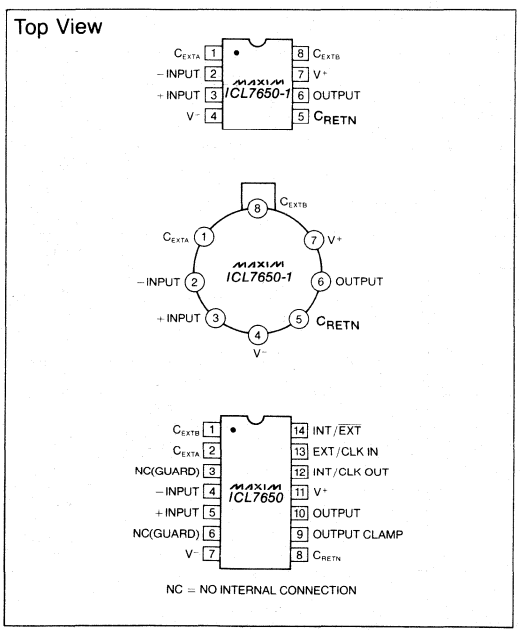
A 14 lead version is available which can be used with either an internal or external clock. The 14 lead version has an output voltage clamp circuit to minimize overload recovery time.

Applications

Condition Amplifier	Thermocouples
Precision Amplifier	Thermistors
Instrumentation Amplifier	Strain Gauges

Pin Configuration

Top View



NC = NO INTERNAL CONNECTION

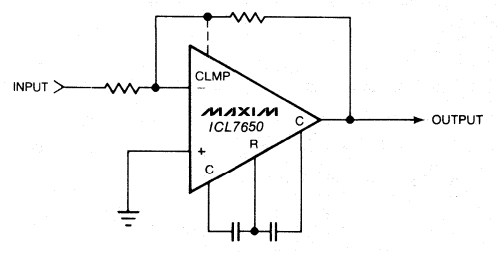
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Lower Supply Current: 2.0 mA**
- **Low Offset Voltage: 1 μV**
- **No Offset Voltage Trimming Needed**
- **High Gain, CMRR and PSRR (120 dB min)**
- **Lower Offset Drift With Time and Temperature**
- **Extended Common Mode Voltage Range**
- **Low DC Input Bias Current: 10 pA**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7650CPD	0°C to +70°C	14 Lead Plastic DIP
ICL7650CSD	0°C to +70°C	14 Lead Slim S.O.
ICL7650IJD	-20°C to +85°C	14 Lead CERDIP
ICL7650MJD	-55°C to +125°C	14 Lead CERDIP
ICL7650CPA-1	0°C to +70°C	8 Lead Plastic DIP
ICL7650CSA-1	0°C to +70°C	8 Lead Slim S.O.
ICL7650CTV-1	0°C to +70°C	8 Lead TO-99 Metal Can
ICL7650IJA-1	-20°C to +85°C	8 Lead CERDIP
ICL7650MTV-1	-55°C to +125°C	8 Lead CERDIP
ICL7650C/D	0°C to +70°C	Dice
ICL7650BCPD	0°C to +70°C	14 Lead Plastic DIP
ICL7650BCSD	0°C to +70°C	14 Lead Slim S.O.
ICL7650BCPA-1	0°C to +70°C	8 Lead Plastic DIP
ICL7650BCSA-1	0°C to +70°C	8 Lead Slim S.O.
ICL7650BCTV-1	0°C to +70°C	8 Lead TO-99 Metal Can
ICL7650BC/D	0°C to +70°C	Dice

Typical Operating Circuit



Inverting Amplifier with Optional Clamp

(Detailed Circuit Diagram—Figure 5)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18Volts
Input Voltage ..... (V^+ + 0.3) to (V^- - 0.3) Volts
Storage Temp. Range ..... -65°C to 160°C
Operating Temp. Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on oscillator control pins ..... V^+ to V^-
except EXT CLOCK IN: ..... (V^+ + 0.3) to (V^+ - 6.0) Volts
Duration of Output short circuit ..... Indefinite
Current into any pin 10mA
—while operating (Note 4) 100μA

Cont. Total Power Dissipation (T_A = 25°C)
CERDIP Package 500mW
Plastic Package 375mW
TO-99 Metal Can 250mW
Small Outline 350mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS — ICL7650

(V^+ = +5V, V^- = -5V, T_A = 25°C, Test Circuit, Unless Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input Offset Voltage	V_{OS}	T_A = +25°C -55°C < T_A < +85°C -55°C < T_A < +125°C		±0.7 ±1.0	±5 5.0	μV
Average Temp. Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	-20°C < T_A < +85°C		0.01 50	0.05	μV/°C
Input Bias Current (doubles every 10°C)	I_{BIAS}	T_A = +25°C 0°C < T_A < +70°C -20°C < T_A < +85°C		1.5 35 100	10	pA
Input Offset Current	I_{OS}	T_A = 25°C		0.5		pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ	1×10^6	5×10^6		V/V
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ R_L = 100kΩ	±4.7	±4.85 ±4.95		V
Common Mode Voltage Range	CMVR		-5.0	-5.2 to +2.0	1.6	V
Common Mode Rejection Ratio	CMRR	CMVR = -5V to +1.6	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	120	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω 0 to 10Hz		2		μVp-p
Input Noise Current	I_n	f = 10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slow Rate	SR	C_L = 50pF, R_L = 10kΩ		2.5		V/μs
Rise Time	t_r			0.2		μs
Overshoot				20		%
Operating Supply Range	V+ to V-		4.5		16	V
Supply Current	I_{SUPP}	no load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	pins 12–14 open (DIP)	120	200	375	Hz
Clamp ON Current (note 2)		R_L = 100kΩ	25	70	200	μA
Clamp OFF Current (note 2)		-4.0V < V_{OUT} < +4.0V		1		pA
Offset Voltage vs Time				100		nV/√month

NOTE 1: Operating temperature range for M series parts is -55°C to +125°C, for I series is -20°C to +85°C, for C series is 0°C to +70°C
NOTE 2: See OUTPUT CLAMP under detailed description.
NOTE 3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
NOTE 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
NOTE 5: $I_{OS} = 2 \bullet I_{BIAS}$

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Chopper Stabilized Operational Amplifier

- **Lower Supply Current**
- **Key Parameters Guaranteed over Temperature**
- **Extended Common Mode Voltage Range**
- **Characterized over Military Temperature Range**
- **Significantly Enhanced "ESD" Protection (Note 6)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS This device conforms to the Absolute Maximum Ratings on adjacent page.

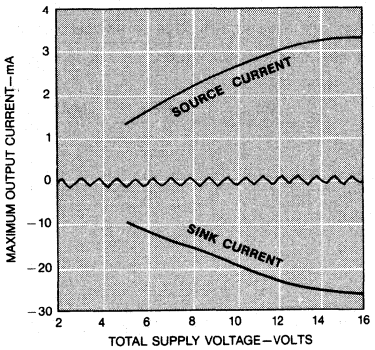
ELECTRICAL CHARACTERISTICS The ICL7650 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, T_A = 25°C, Test Circuit, unless Noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C, ICL7650		±0.7	±5.0	µV
		T_A = +25°C, ICL7650B		±1.0	±10	µV
		0°C ≤ T_A ≤ +70°C, ICL7650 (Note 7)		±1.0	±10	µV
		-20°C ≤ T_A ≤ +85°C, ICL7650 (Note 7)		±1.0	±10	µV
		-55°C ≤ T_A ≤ +125°C, ICL7650 (Note 7)		±10	±50	µV
Average Temperature Coefficient of Input Offset Voltage (Note 7)	$\frac{\Delta V_{OS}}{\Delta T}$	0°C ≤ T_A ≤ +70°C, ICL7650		0.01	0.05	µV/°C
		0°C ≤ T_A ≤ +70°C, ICL7650B		0.01	0.1	µV/°C
		-20°C ≤ T_A ≤ +85°C, ICL7650		0.01	0.05	µV/°C
		-55°C ≤ T_A ≤ +85°C, ICL7650		**0.01**	**0.05**	**µV/°C**
		+85°C ≤ T_A ≤ +125°C, ICL7650		**0.25**	**1.5**	**µV/°C**
Input Bias Current	I_B	T_A = +25°C, ICL7650		4	10	pA
		T_A = +25°C, ICL7650B		12	20	pA
		0°C ≤ T_A ≤ +70°C		**20**	**100**	**pA**
		-20°C ≤ T_A ≤ +85°C		**50**	**200**	**pA**
		-55°C ≤ T_A ≤ +125°C		**0.3**	**10**	**nA**
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ T_A = +25°C	1 x 10^6	5 x 10^6		V/V
		0°C ≤ T_A ≤ +70°C	**0.5 x 10^6**			**V/V**
		-20°C ≤ T_A ≤ +85°C	**0.5 x 10^6**			**V/V**
		-55°C ≤ T_A ≤ +125°C	**0.2 x 10^6**			**V/V**
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
Common Mode Voltage Range	**CMVR**	**0°C ≤ T_A ≤ +70°C**	**-5.0**	**-5.2 to 3.0**	**2.5**	**V**
		-20°C ≤ T_A ≤ +85°C	**-5.0**	**-5.2 to 3.0**	**2.5**	**V**
		-55°C ≤ T_A ≤ +125°C	**-4.5**	**-4.8 to 3.0**	**2.5**	**V**
Common Mode Rejection Ratio	**CMRR**	**CMVR = -5V to +2.5V**	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	120	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_s = 100Ω 0 to 10Hz		2		μV_{p-p}
Input Noise Current	i_n	f = 10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		2.5		V/µs
Rise Time	t_r			0.2		µs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		4.5		16	V
Supply Current	I_{SUPP}	**no load**		**1.2**	**2.0**	**mA**
Internal Chopping Frequency	f_{CLKOUT}	pins 13 and 14 open (DIP)	120	200	375	Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	70	200	µA
Clamp OFF Current (Note 2)		-4.0V ≤ V_{OUT} ≤ +4.0V		1		pA
Offset Voltage vs Time				100		nV/√month

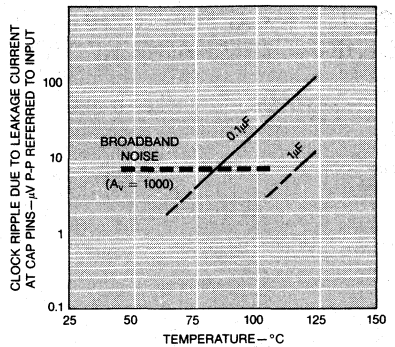
NOTE 1: Operating temperature range for M series parts is −55°C to +125°C, for I series is −20°C to +85°C, for C series is 0°C to +70°C
NOTE 2: See OUTPUT CLAMP under detailed description.
NOTE 3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
NOTE 4: Limiting input current to 100µA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
NOTE 5: $I_{OS} \approx 2 \bullet I_{BIAS}$
NOTE 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883B Method 3015.1 Test Circuit)
NOTE 7: Sample tested. Limits are not used to calculate outgoing quality level.

Chopper Stabilized Operational Amplifier

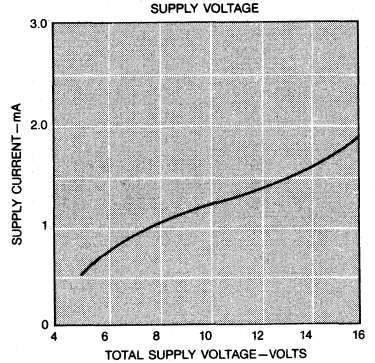
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



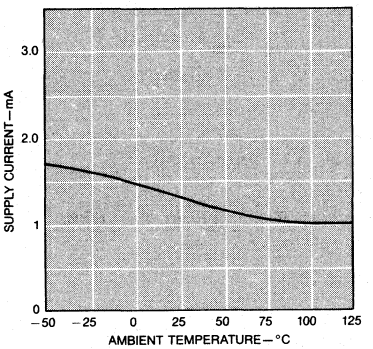
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



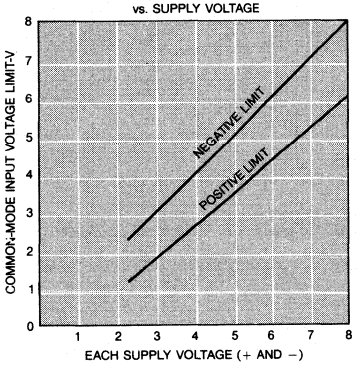
SUPPLY CURRENT vs. SUPPLY VOLTAGE



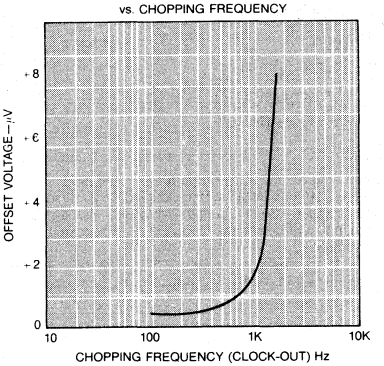
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



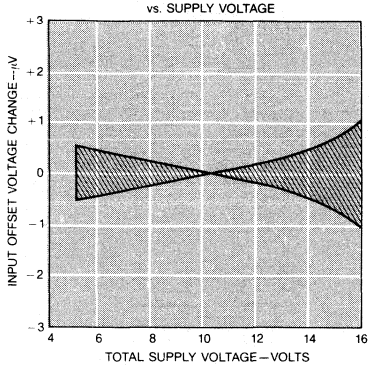
COMMON-MODE INPUT-VOLTAGE RANGE vs. SUPPLY VOLTAGE



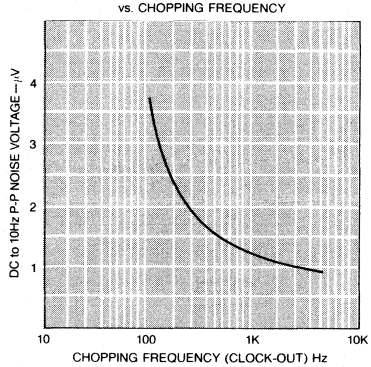
INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY



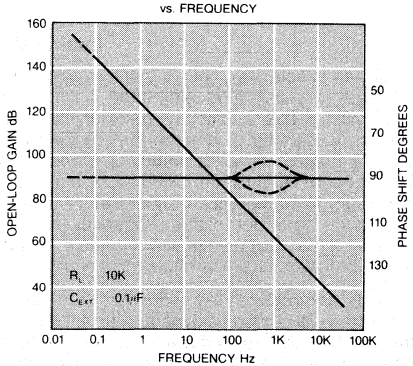
INPUT OFFSET VOLTAGE CHANGE
vs. SUPPLY VOLTAGE



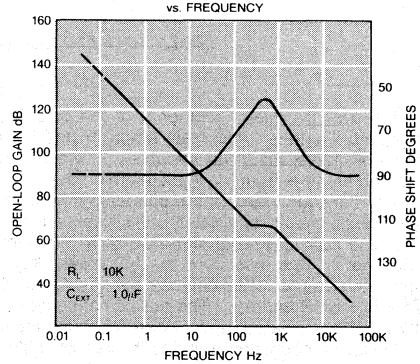
10Hz P-P NOISE VOLTAGE
vs. CHOPPING FREQUENCY



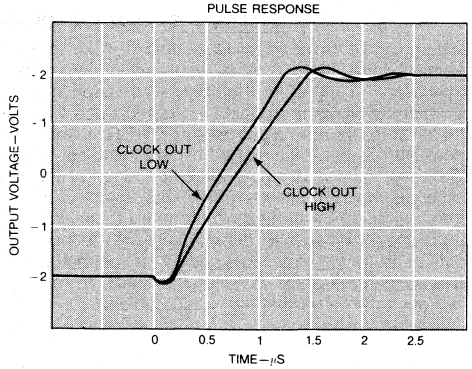
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



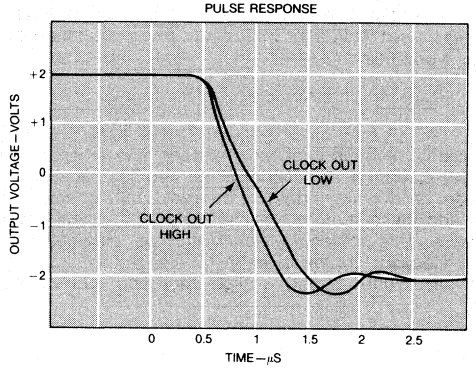
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



Chopper Stabilized Operational Amplifier

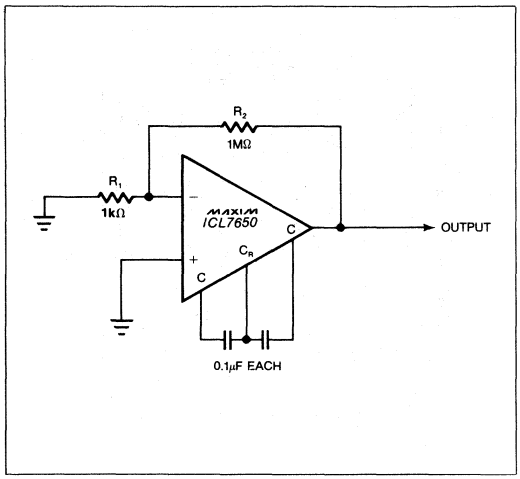


Figure 1. Maxim ICL7650 Test Circuit

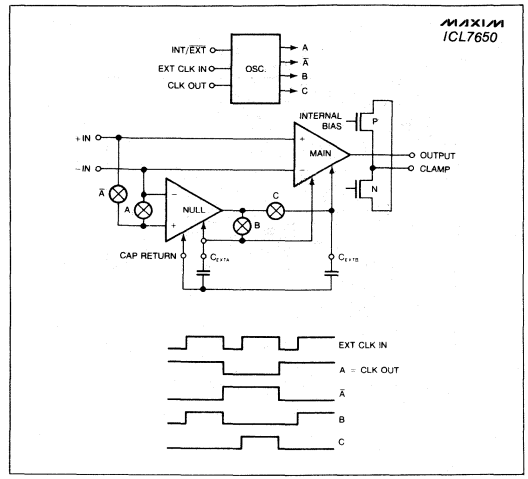


Figure 2. Block Diagram

Detailed Description

Amplifier

Figure 2 shows the major elements of the ICL7650. Two amplifiers are illustrated, the main amplifier and the nulling amplifier, both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling arrangement, which is independent of the output level, operates over the full power supply and common mode ranges. This device exhibits an exceptionally high CMRR, PSRR and A_{VOL}. The nulling connections, which are MOSFET back gates, have inherently high impedance. The two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants.

The chopper frequency charge injection at the input terminals is minimized by careful balance of the input switches. The feed forward-type injection into the compensation capacitor is also minimized. This is the main cause of spikes at the output in this type of circuit.

Output Clamp

The clamp reduces overload recovery time inherent with chopper-stabilized amplifiers. When tied to the summing junction, or inverting input pin, a current path between this point and the output occurs just before the output device saturates. This prevents uncontrolled input differential and the consequent charge build-up on the correction-storage capacitors. There is only a slight reduction in the output swing.

Intermodulation

Intermodulation effects have been a problem with older chopper stabilized amplifier modules. Intermodulation occurs since the amplifier has a finite AC gain, and therefore will have a small AC signal at the input. In a chopper stabilized module this small AC signal is detected, chopped, and fed into the offset correction circuit. This results in spurious outputs at the sum and difference frequencies of the chopping frequency and the input signal frequency. Other intermodulation effects in chopper stabilized modules include gain and phase anomalies near the chopping frequency.

These effects are substantially reduced in the ICL7650 by adding into the nulling circuit a dynamic current that compensates for the AC on the inputs due to the amplifiers finite gain. Unlike the modules, the ICL7650 can precisely compensate for the finite AC gain since both the AC gain rolloff and the intermodulation compensation current are controlled by matched capacitors onboard the ICL7650.

Nulling Capacitor Connection

Separate pins are provided for C_{RETN} and CLAMP in the 14 lead version of the ICL7650. With the 8 lead version, a choice must be made. If the clamp feature is not used, the "-1" version with the C_{RETN} pin should be ordered since it will give slightly lower noise and improved AC CMRR. If the clamp feature is used, order the standard ICL7650 and connect the external capacitors to V^-. To prevent load current IR drops and other extraneous signals from being injected into the capacitors, a separate printed circuit board trace should be used to connect the capacitor commons directly to the V^- pin. The outside foil of the capacitors should be connected to the low impedance side of the null storage circuit, V^- or C_{RETN}. This will act as an electro-static voltage shield.

Clock Operation

A frequency of 200Hz is generated by the internal oscillator of the ICL7650. This is available at the CLK OUT pin on the 14-pin devices. The use of an external clock is also optional on these parts. The INT/$\overline{\text{EXT}}$ pin may be left open for normal operation due to the internal pull-up. However, the internal clock must be disabled and this pin must be tied to V− if an external clock is desired. An external clock signal may then be applied to the EXT CLK IN pin. The duty cycle of the external clock is not critical at low frequencies. However, a 50% to 80% positive duty cycle is preferred for frequencies above 500 Hz, since the capacitors are charged only when EXT CLK IN is HIGH. This ensures that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between GROUND and (V^+) for power supplies up to ±6 volts, and between (V^+) and (V^+ −6V) for higher supply voltages.

To avoid a capacitor imbalance during overload, a strobe signal may be used. Neither capacitor will be charged if a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier. A typical amplifier will drift less than 10 μV/s since the leakage of the capacitor pins is quite low at room temperature. Relatively long measurements may be made with little change in offset.

Applications

Device Selection

In many applications Maxim's interchangeable ICL 7652 is preferred over the ICL 7650. The ICL7650 has a higher gain-bandwidth product and lower input bias currents, while the ICL7652 has less noise. The major change in the ICL7652 to reduce the noise is an increase in the size of the input FETs. This, however, increases the leakage at the ICL7652's external null pins. This means the ICL7650 can operate to a higher temperature with 0.1μF capacitors before the clock ripple (due to leakage at the null capacitor pins) becomes excessive and 1.0μF external capacitors are required.

Output Stage/Load Driving

The ICL7650 is in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. This behavior is apparent when loads are less than the high impedance stage (approximately 18KΩ for 1 output circuit. The open loop gain, for example, will be 17dB lower with a 1KΩ load than with a 10KΩ load. This lower gain is of little consequence if the amplifier is used strictly for DC, since the DC gain is typically greater than 120 dB even with a 1KΩ load. For wideband applications, however, the best frequency response will be achieved with a load resistor of 10kΩ or higher. The result will be a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Component Selection

C_{EXTA} and C_{EXTB}, the two required capacitors, have optimum values depending on the clock or chopping frequency. The correct value is 0.1μF for the preset internal clock. This component value should be scaled proportionally to the relationship between the chopping frequency and the nulling time constant if an external clock is used. A low leakage ceramic capacitor may prove suitable for many applications, however, a high-quality film-type capacitor such as mylar is preferred. Low dielectric absorption capacitors (such as polypropylene) should be used for lowest settling on initial turn-on. With low dielectric absorption capacitors, the ICL7650 will settle to 1μV offset in 100 ms, but several seconds may be required if ceramic capacitors are used.

Thermo-electric Effects

Thermo-electric effects developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc., ultimately limit precision DC measurements. Unless all junctions are at the same temperature, thermoelectric voltages typically around 10μV/°C, but up to hundreds of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide it is essential to take special precautions to avoid temperature gradients. To eliminate air movement, all components should be enclosed (particularly those caused by power dissipating elements in the system). Power supply voltages and power dissipation should be kept to a minimum, and low thermo-electric coefficient connections should be used where possible. Separation from surrounding heat dissipating elements is advised, and high impedance loads are preferable.

Chopper Stabilized Operational Amplifier

Input Guarding

Low leakage, high impedance, CMOS inputs allow the ICL7650 to make measurements of high impedance sources. Stray leakage paths can decrease input resistance and increase input currents unless inputs are guarded. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. The board should be coated with epoxy or silicone after cleaning to prevent contamination.

Leakage currents may cause trouble even with properly cleaned and coated boards, particularly since the input pins are adjacent to pins that are at supply potentials. A significant reduction in leakage can be accomplished by using guarding to lower the voltage difference between inputs and adjacent metal runs. By using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board, input guarding of the 8-lead T0-99 package is accomplished. A conductive ring surrounding the inputs, the guard, is connected to a low-impedance point that is approximately the same voltage as the inputs. The guard then absorbs the leakage current from the high voltage pins. Typical guard connections are shown in Figure 3.

The 14-pin dip configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are not used.

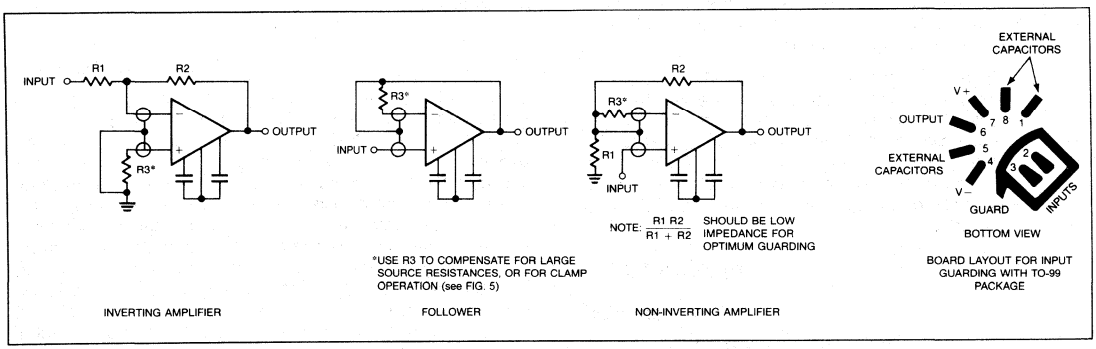


Figure 3. Input Guard Connection

Pin Compatibility

The 8-lead pin-out of the ICL7650 generally corresponds to that of the industry standard 8-pin devices, LM741, LM101, etc. However, the external null storage capacitors are connected to pins 1 and 8, whereas on most operational amplifiers these are left open or used for offset null or compensation capacitors.

The OP-05 and OP-07 operational amplifiers can be converted for ICL7650 operation. This can be accomplished by replacing the offset-null pot between pins 1 and 8, and V^+ by two capacitors from these pins to V^-. For LM 108 devices, the compensation capacitor is replaced by the external nulling capacitors. Pin 5 is the output clamp connection on the ICL7650. By removing any circuit connections from this pin, the LM101/748/709 devices can undergo a similar conversion.

Typical Applications

Figure 4 shows the ICL7650 automatically nulling the offset voltage of a high speed amplifier. The ICL7650 continuously monitors the voltage at the inverting input of the high speed amplifier, integrates the error, and drives the high speed amplifier's non-inverting input to correct for the offset voltage detected at the inverting input. The DC offset characteristics of the circuit are determined by the ICL7650, while the AC performance is determined by the high speed amplifier. While this circuit continuously and automatically adjusts the offset of the high speed amplifier to less than 5μV, it does not correct for errors caused by the input bias current, and R_F should be as low as is practical. This technique can be used with any operational amplifier that is configured as an inverting amplifier.

Figures 5 and 6 illustrate basic inverting and non-inverting amplifier circuits. An output clamping circuit is used in both circuits to enhance the overload recovery performance. The supply voltage (± 8V max) and the output drive capability (10KΩ load for full swing) are the only limitations on the replacement of other operational amplifiers by the ICL7650. By using a simple booster circuit, these limitations may be overcome (Figure 7). This enables the full output capabilities of the LM118 (or any other standard device) to be combined with the input capabilities of the ICL7650. The loop gain stability should be watched carefully when the feedback network is added, particularly when a slower amplifier such as the 741 is used.

A lower voltage supply is required when mixing the ICL7650 with circuits that operate at ±15V supplies. One approach is to use a highly-efficient voltage divider. This is illustrated in Figure 8 where the ICL7660 voltage converter is used to convert +15V to 7.5V.

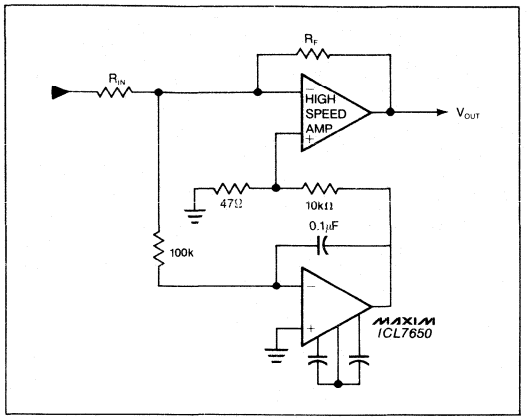


Figure 4. Nulling a High Speed Amplifier

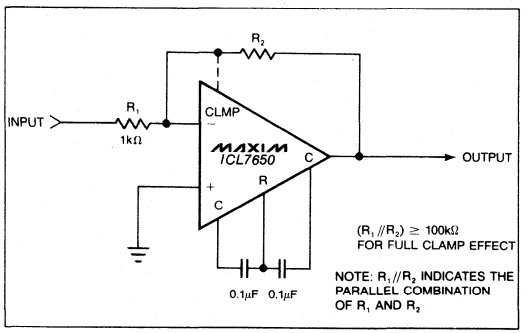


Figure 5. Inverting Amplifier with Optional Clamp

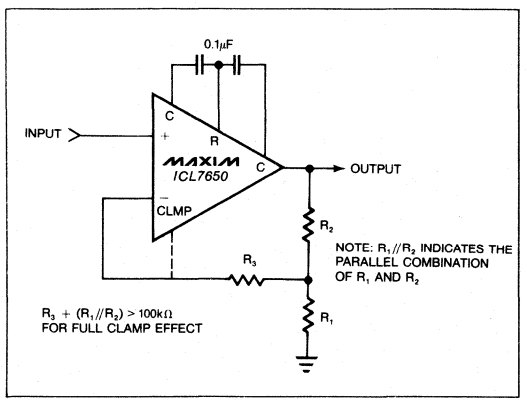


Figure 6. Non-Inverting Amplifier with Optional Clamp

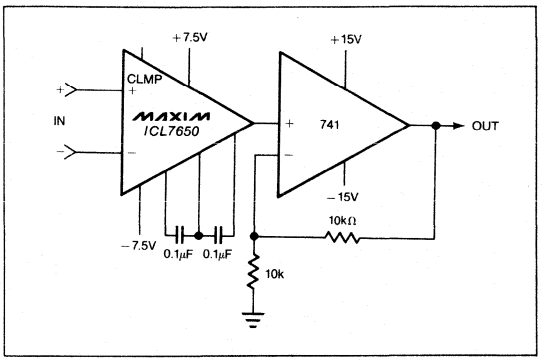


Figure 7. Using 741 to boost Output Drive Capability

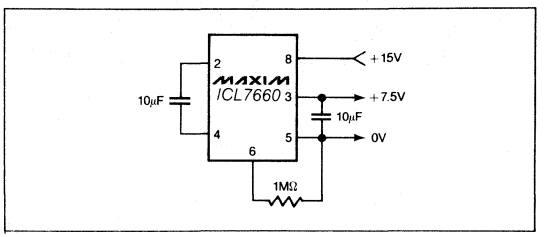
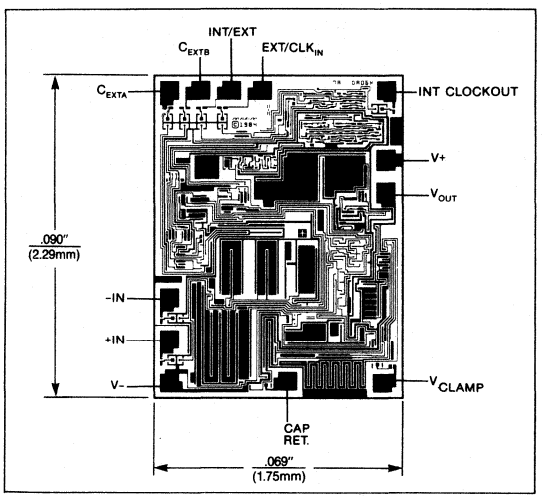


Figure 8. Splitting +15V with ICL7660. Same for -15V (95% Efficiency).

Chip Topography



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Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

Chopper Stabilized Operational Amplifier

General Description

The Maxim ICL7652 is a chopper-stabilized amplifier, ideal for applications requiring low-level signal amplification and conditioning. This device offers distinct performance advantages over the ICL7650, including improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are slightly reduced.

The ICL7652 virtually eliminates the V_{OS} error term in system error calculations, eliminating the reliability and cost problems associated with potentiometer adjustments. In addition, the 0.01μV/°C V_{OS} drift specification and the excellent long term offset stability eliminate the need for periodic V_{OS} trimming.

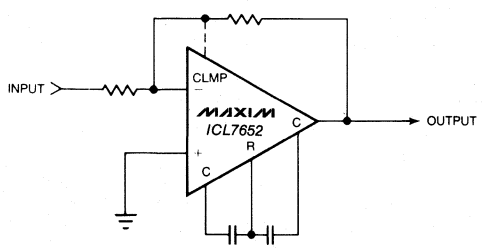
The offset nulling circuit for the 8-lead ICL7652 is controlled by an internal oscillator circuit. The 14-lead version offers the capability of connecting an external oscillator to control the V_{OS} nulling operation. The 14-lead device has an output voltage clamp circuit to minimize overload recovery time.

Applications

The ICL7652 is ideal for all preamplifier circuit applications where low offset voltage is critical and periodic adjustment of the offset is difficult or inaccessible.

Precision Amplifier
Instrumentation Amplifier
Thermocouple Amplifier
Thermistor Amplifier
Strain Gauge Amplifier

Typical Operating Circuit



Inverting Amplifier
with Optional Clamp

(Detailed Circuit Diagram — Figure 5)

Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Low Input Noise Voltage 0.2μV_{p-p}(DC-1Hz)**
- **Low Offset Voltage: 5μV Max.**
- **Low DC Input Bias Current: 30pA Max.**
- **High Gain, CMRR and PSRR (110dB Min.)**
- **Compensated for Unity Gain Operation**
- **Excellent Long Term Offset Stability (<100nV/$\sqrt{month}$)**
- **Monolithic, Low Power CMOS Design**

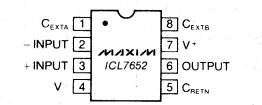
Ordering Information

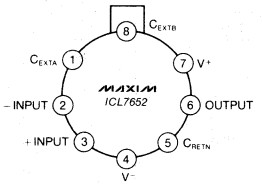
PART	TEMP. RANGE	PACKAGE
ICL7652CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7652CPD	0°C to +70°C	14 Lead Plastic DIP
ICL7652CTV	0°C to +70°C	TO-99 Metal Can
ICL7652IJA	-20°C to +85°C	8 Lead CERDIP
ICL7652IJD	-20°C to +85°C	14 Lead CERDIP
ICL7652ITV	-20°C to +85°C	TO-99 Metal Can
ICL7652C/D	0°C to +70°C	Dice
ICL7652CWE	0°C to +70°C	16 Lead Wide S.O.

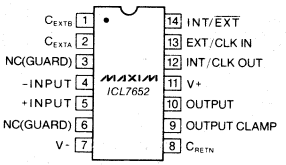
NOTE: All devices listed above are available in B versions. Order part number ICL7652B ___.

Pin Configurations

Top View







NC = NO INTERNAL CONNECTION

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3) to (V^- - 0.3) V
Storage Temperature Range ..... -65°C to 160°C
Operating Temperature Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite

Current into Any Pin 10mA
— while operating (Note 4) 100μA
Continuous Total Power Dissipation (T_A = +25°C)
CERDIP Package (Maxim) 500mW
Plastic Package 375mW
TO-99 Metal Can 250mW
Small Outline 350mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - ICL7652

(V^+ = +5V, V^- = -5V, T_A = +25°C, Test circuit unless noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{OS}	T_A = +25°C		±0.7	±5	μV
		Over Operating Temperature Range (Note 1)		±1.0		
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Operating Temperature Range (Note 1)		0.01	0.05	μV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_{BIAS}	T_A = +25°C		15	30	pA
		0°C ≤ T_A ≤ +70°C		35		
		-20°C < T_A < +85°C		100		
Input Offset Current	I_{OS}	T_A = +25°C		25	60	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±4V,	120	150		dB
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
Common-Mode Voltage Range	CMVR		-4.3	-4.8 to +4.0	3.5	V
Common-Mode Rejection Ratio	CMRR	CMVR = -4.3V to +3.5V	110	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	110	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω, DC to 1Hz		0.2		μV_{p-p}
		DC to 10Hz		0.7		
Input Noise Current	i_n	f = 10Hz		0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		0.5		V/μs
Rise Time	t_r			0.8		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	I_{SUPP}	No Load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	100		μA
Clamp OFF Current (Note 2)		-4.0V < V_{OUT} < +4.0V		1		pA
Offset Voltage vs Time				100		$nV/\sqrt{month}$

Note 1: Operating temperature range for I series parts is -20°C to +85°C, for C series is 0°C to +70°C.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs. clamp current characteristics.
Note 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this not guaranteed.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Chopper Stabilized Operational Amplifier

- **Key Parameters Guaranteed Over Temperature**
- **Lower Supply Current**
- **Improved ESD Protection (Note 5)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS This device conforms to the Absolute Maximum Ratings on adjacent page.

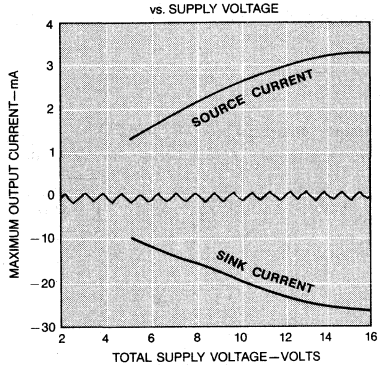
ELECTRICAL CHARACTERISTICS The ICL7652 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, T_A = +25°C, Test circuit, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	**V_{OS}**	T_A = +25°C ICL7652 — Over Temperature Range ICL7652B (below) **-20°C ≤ T_A ≤ +40°C (Note 1)** **-20°C ≤ T_A ≤ +70°C (Note 1, 7)** **+70°C ≤ T_A ≤ +85°C (Note 1, 7)**		±0.7 ±1.0 **±1.0** **±2.0** **±5.0**	±5.0 **±6.25** **±7.25** **±15**	μV
Average Temperature Coefficient of Input Offset Voltage (Note 1)	$\frac{\Delta V_{OS}}{\Delta T}$	ICL7652 — Over Temperature Range ICL7652B (below) -20°C ≤ T_A ≤ +40°C -20°C ≤ T_A ≤ +70°C (Note 1, 7) +70°C ≤ T_A ≤ +85°C (Note 1, 7)		0.01 0.01 0.01 0.1	0.05 0.05 0.1 0.5	μV/°C
Input Bias Current (Note 6) (Doubles every 10°C above approximately 60°C)	**I_{BIAS}**	T_A = +25°C **0°C ≤ T_A ≤ +70°C** **-20°C ≤ T_A ≤ +85°C**		15 **35** **100**	30 **100** **200**	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	**A_{VOL}**	R_L = 10kΩ, V_{OUT} = ±4V, T_A = +25°C **0°C ≤ T_A ≤ +70°C** **-20°C ≤ T_A ≤ +85°C**	120 **114** **114**	150 **140** **140**		dB
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ R_L = 100kΩ	±4.7	±4.85 ±4.95		V
Common-Mode Voltage Range	**CMVR**	**Over Temperature Range (Note 1)**	**-4.3**	**-4.8 to +4.0**	**3.5**	V
Common-Mode Rejection Ratio	**CMRR**	CMVR = -4.3V to +3.5V, T_A = +25°C **Over Temperature Range (Note 1)**	110 **104**	130 **125**		dB
Power Supply Rejection Ratio	**PSRR**	±3V to ±8V, T_A = +25°C **Over Temperature Range (Note 1)**	110 **104**	130 **125**		dB
Input Noise Voltage	en_{p-p}	R_S = 100Ω, DC to 1Hz DC to 10Hz		0.2 0.7		μV_{p-p}
Input Noise Current	i_n	f = 10Hz		0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		0.5		V/μs
Rise Time	t_r			0.8		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	**I_{SUPP}**	**No Load, T_A = +25°C** **Over Temperature Range (Note 1)**		**1.5** **2.0**	**2.0** **3.5**	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	100		μA
Clamp OFF Current (Note 2)		-4.0V ≤ V_{OUT} ≤ +4.0V		1		pA
Offset Voltage vs Time				100		$nV/\sqrt{month}$

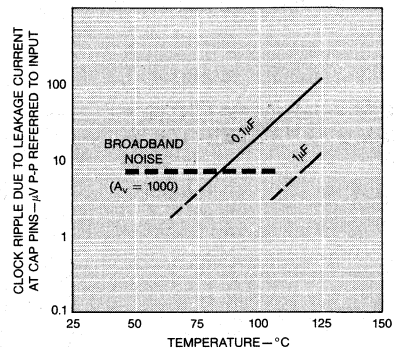
Note 1: Operating temperature range for "I" series parts is -20°C to +85°C, for C series is 0°C to +70°C. This parameter is guaranteed by test correlation.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs. clamp current characteristics.
Note 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
Note 5: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)
Note 6: $I_{OS} = 2 \cdot I_{BIAS}$.
Note 7: With $C_{EXTA} = C_{EXTB} = 1.0\mu F$

Chopper Stabilized Operational Amplifier

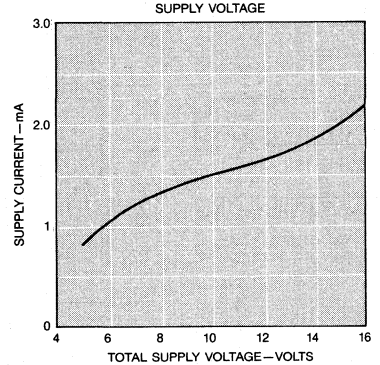
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



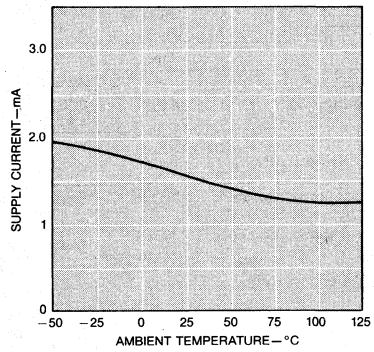
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



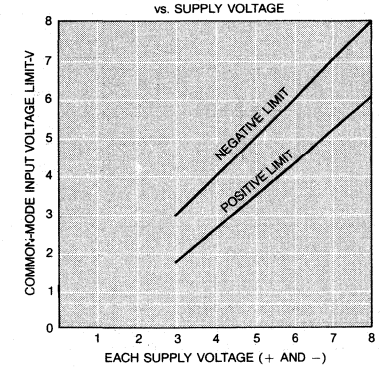
SUPPLY CURRENT vs. SUPPLY VOLTAGE



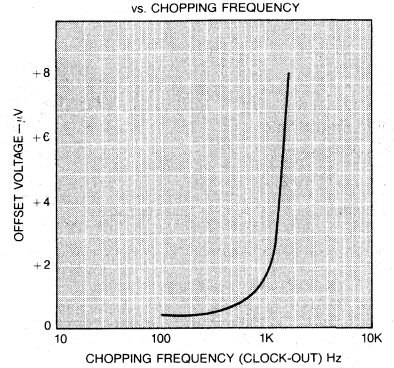
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



COMMON-MODE INPUT-VOLTAGE RANGE vs. SUPPLY VOLTAGE

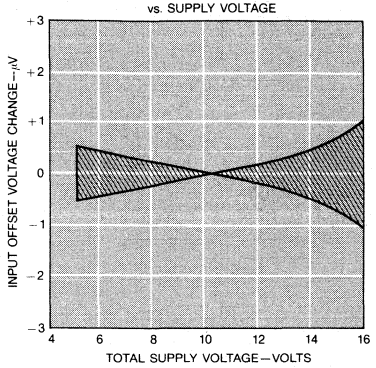


INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY

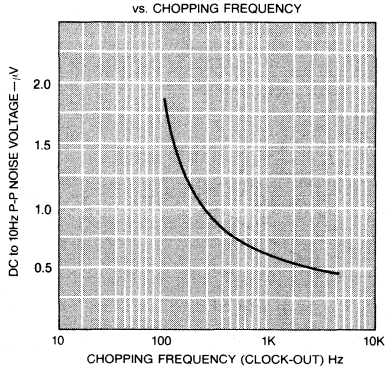


Chopper Stabilized Operational Amplifier

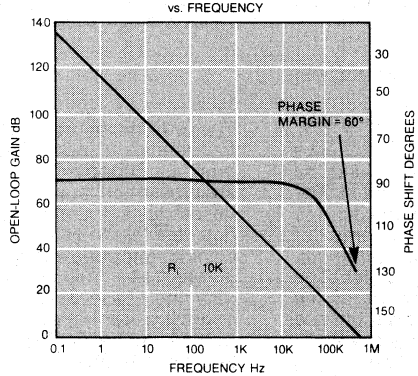
INPUT OFFSET VOLTAGE CHANGE
vs. SUPPLY VOLTAGE



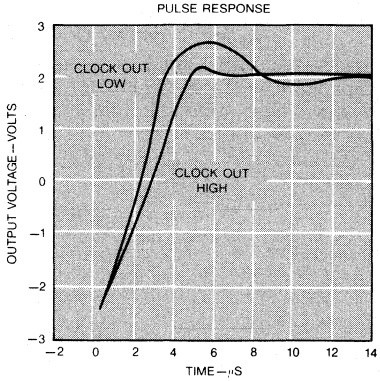
10Hz P-P NOISE VOLTAGE
vs. CHOPPING FREQUENCY



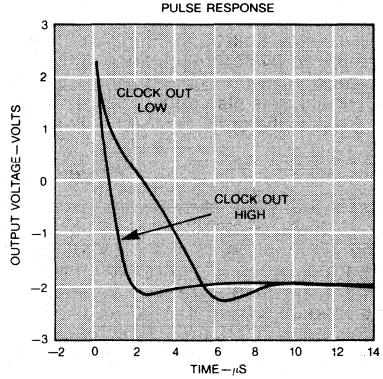
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



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Chopper Stabilized Operational Amplifier

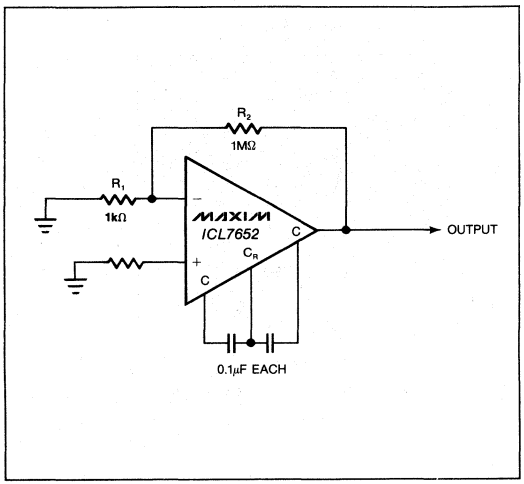


Figure 1. Maxim ICL7652 Test Circuit

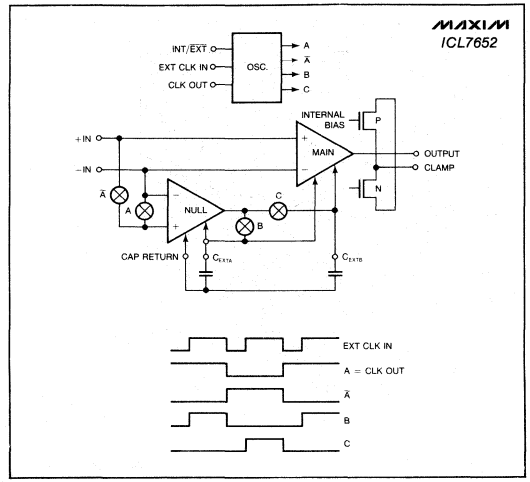


Figure 2. Maxim ICL7652 Block Diagram

Detailed Description

Amplifier

Figure 2 shows the major elements of the ICL7652. Two amplifiers are illustrated, the main amplifier and the nulling amplifier, both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling arrangement, which is independent of the output level, operates over the full power supply and common mode ranges. This device exhibits exceptionally high CMRR, PSRR and A_{VOL}. The nulling connections, which are MOSFET back gates, have inherently high impedance. The two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants.

The chopper frequency charge injection at the input terminals is minimized by careful balance of the input switches. The feed forward-type injection into the compensation capacitor is also minimized. This is the main cause of spikes at the output in this type of circuit.

Output Clamp

This pin allows for reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the summing junction, or to the inverting input pin, a current path between this point and the output occurs just before the output device saturates. This avoids uncontrolled input differential and the consequent charge build-up on the correction-storage capacitors. There is only a slight reduction in the output swing.

Intermodulation

The effects of intermodulation between chopper frequency and input signals have been a problem with previous chopper stabilized amplifiers. These effects are present because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is detected by the zeroing circuit as an error signal. This signal is chopped and fed back, thus injecting sum and difference frequencies. This causes disturbances in the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7652. This reduction is achieved by feeding the nulling circuit with a dynamic current which corresponds to the compensation capacitor current. The intermodulation and gain/phase disturbances in the ICL7652 are held to very low values, and generally can be ignored.

Nulling Capacitor Connection

The C_{EXTA} and C_{EXTB} pins should be connected to the null-storage capacitors, with the common connection made to the C_{RETN}. The outside foil of the capacitors should be connected to C_{RETN}.

Clock Operation

A frequency of 400Hz is generated by the internal oscillator of the ICL7652. This is available at the CLK OUT pin on the 14-lead device. The use of an external clock is also available on these parts. The INT/EXT pin may be left open for normal operation due to the internal pull-up. However, the internal clock must be disabled and this pin must be tied to V^- if an external clock is desired. An external clock signal may then be applied to the EXT CLK IN pin. The duty cycle of the external clock is not critical at low frequencies, since an internal divide by two provides the desired 50% switching duty cycle. However, a 50% to 80% positive duty cycle is preferred for frequencies above 500Hz, since the capacitors are charged only when EXT CLK IN is HIGH. This ensures that any transients have time to settle before the capacitors are turned OFF. The external clock can swing between V^+ and GROUND or V^+ and V^-, and has a logic threshold of about $V^+ - 2.5V$.

To avoid a capacitor imbalance during overload, a strobe signal may be used. Neither capacitor will be charged if a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier. A typical amplifier will drift less than 10μV/s since the leakage of the capacitor pins is quite low at room temperature. Relatively long measurements may be made with little change in offset.

Applications

Output Stage/Load Driving

The ICL7652 is in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. This behavior is apparent when loads are less than the high impedance stage of the output (approximately 18kΩ). The open loop gain, for example, will be 17dB lower with a 1kΩ load than with a 10kΩ load. This lower gain is of little consequence if the amplifier is used strictly for DC, since the DC gain is typically greater than 120dB even with a 1kΩ load. For wideband applications, however, the best frequency response will be achieved with a load resistor of 10kΩ or higher. The result will be a smooth 6dB/octave response from 0.1Hz to 0.5MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Component Selection

C_{EXTA} and C_{EXTB}, the two required external capacitors, have optimum values depending on the clock or chopping frequency. The correct value is 0.1 to 1μF for the preset internal clock frequency. The capacitor value should be scaled proportionally to the relationship between the chopping frequency and the nulling time constant if an external clock is used. A ceramic or other low grade capacitor may prove suitable for many applications, however, a high-quality film-type capacitor such as mylar is preferred. Low dielectric absorption capacitors (such as polypropylene) should be used for lowest settling on initial turn-on. Several seconds may be required to settle to 1μV with ceramic capacitors.

Static Protection

Input diodes provide static protection for all device pins. Strong static fields and discharges, however, should be avoided, as they can cause degraded diode junction characteristics which may result in increased input leakage currents.

Latch-up Avoidance

A parasitic four-layer (p-n-p-n) structure which has characteristics similar to an SCR is a characteristic of a junction-isolated CMOS circuit. This junction may be triggered into a low impedance state under certain circumstances which results in excessive supply current. In an effort to avoid this condition, no voltages greater than 0.3V beyond the supply rails should be applied to any pin. Generally the amplifier supplies should be established either at the same time or before any input signals are applied. However, if this is not possible, the drive circuits should limit the input current flow to under 1mA to avoid latch-up, even under fault conditions.

Thermo-electric Effects

Thermo-electric effects developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc., ultimately limit precision DC measurements. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide it is essential to take special precautions to avoid temperature gradients. All components should be shielded from air movement, especially that caused by power dissipating elements. Power supply voltages and power dissipation should be kept to a minimum, and low thermo-electric coefficient connections should be used where possible. Separation from surrounding heat dissipating elements is advised, and high impedance loads are preferable.

Chopper Stabilized Operational Amplifier

Input Guarding

Low leakage, high impedance, CMOS inputs allow the ICL7652 to make measurements of high impedance sources. Stray leakage paths can decrease input resistance and increase input currents unless inputs are guarded. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. The board should be coated with epoxy or silicone rubber after cleaning to prevent contamination.

Leakage currents may cause trouble even with properly cleaned and coated boards, particularly since the input pins are adjacent to pins that are at supply potentials. A significant reduction in leakage can be accomplished by using guarding to lower the voltage difference between the inputs and adjacent metal runs. By using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board, input guarding of the 8-lead TO-99 package is accomplished. A conductive ring surrounding the inputs, forming a guard, is connected to a low-impedance point that is approximately the same voltage as the inputs. The guard then absorbs the leakage current from the high voltage pins. Typical guard connections are shown in Figure 3.

The 14-lead DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are not used.

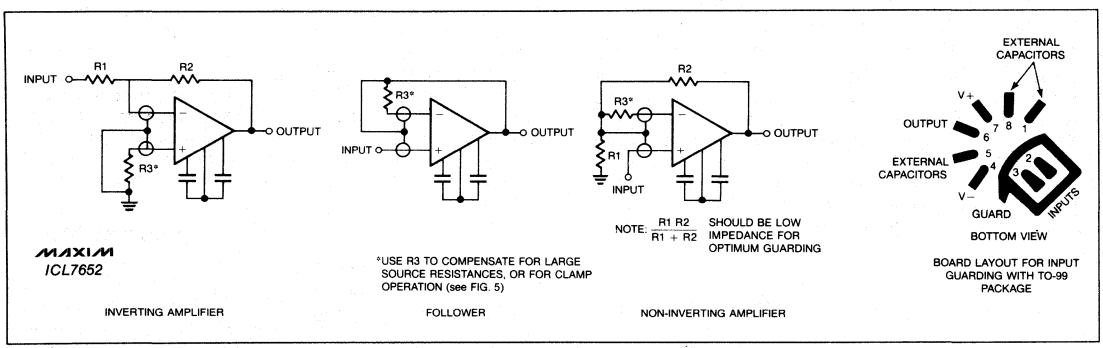


Figure 3. Input Guard Connection

Pin Compatibility

The 8-pin dip of the ICL7652 generally corresponds to that of the industry standard 8-pin devices, μA741, LM101, etc. However, the external null storage capacitors are connected to pins 1 and 8, whereas on most operational amplifiers these are left open or used for offset null or compensation capacitors.

The OP-05 and OP-07 operational amplifiers can also be converted for ICL7652 operation. This can be accomplished by replacing the offset-null potentiometer between pins 1 and 8, and V^+ by two capacitors from those pins to V^-. For LM108 pinout devices, the compensation capacitor is replaced by the external nulling capacitors.

Typical Applications

The ICL7652 is the optimal circuit solution whenever the performance of the system requires significant improvements in the reduction of the input offset voltage and bias currents. Figure 6 illustrates the use of a clamp circuit in a non-inverting amplifier. Since the clamp circuit forces the inverting input to follow the input signal, the usual problems in using a chopper-stabilized amplifier in this application are avoided.

Figures 5 and 6 illustrate basic inverting and non-inverting amplifier circuits. An output clamping circuit is used in both circuits to enhance the overload recovery performance. The supply voltage (± 8V max) and the output drive capability (10kΩ load for full swing) are the only limitations on the replacement of other operational amplifiers by the ICL7652. By using a simple booster circuit, these limitations may be overcome (Figure 7). This enables the full output capabilities of the μA741 (or any other standard device) to be combined with the input capabilities of the ICL7652. Because these devices form a composite amplifier, the loop gain stability should be watched carefully when the feedback network is added.

The provision for lower supply voltages is required when interfacing the ICL7652 with circuits that operate at ± 15V supplies. One approach is to use a highly-efficient voltage divider. This is illustrated in Figure 8 where Maxim's ICL7660 voltage converter is utilized in a backwards fashion.

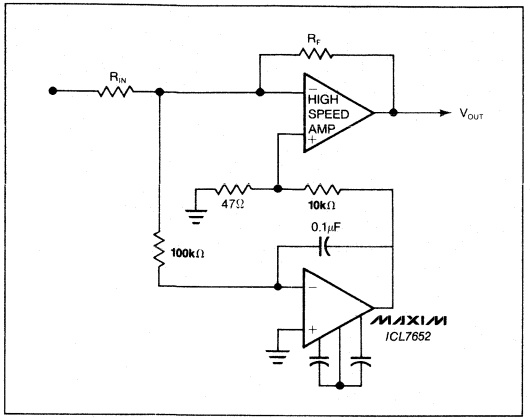


Figure 4. Nulling a High Speed Amplifier

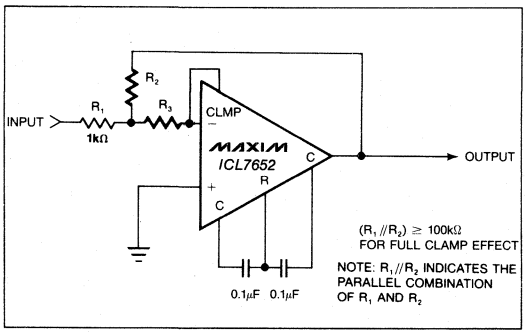


Figure 5. Inverting Amplifier with Optional Clamp

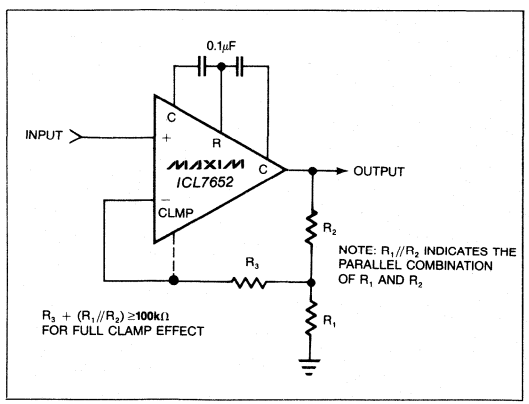


Figure 6. Non-Inverting Amplifier with Optional Clamp

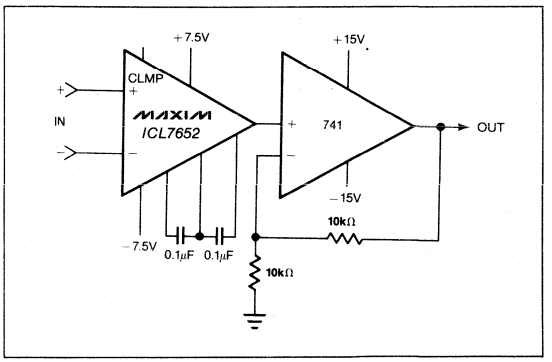


Figure 7. Using 741 to boost Output Drive Capability

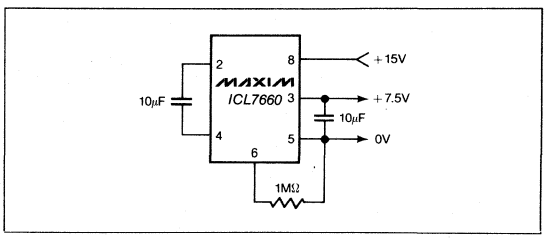
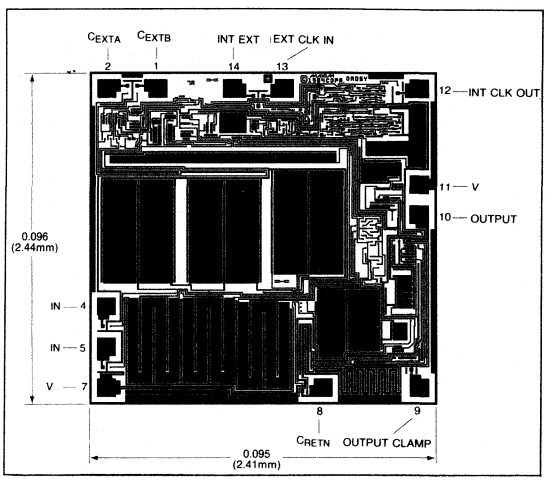


Figure 8. Splitting +15V with ICL7660. Same for -15V (95% Efficiency).

Chip Topography



MAXIM
Fast Buffer Amplifier

General Description

The LH0033A and LH0033 are high speed JFET input voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. With a slew rate of 1500 V/μsec when driving 1kΩ loads, the LH0033 will provide 100 mA output drive (250 mA peak), and can drive loads as low as 50Ω. In addition, phase linearity is characterized up to 20 MHz for video applications. Specifications are included for driving heavy coaxial cable loads not only at the normal 15 volt supplies, but also for 5V supplies.

The LH0033 family is intended to fulfill a wide range of buffer applications such as high-speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, operational amplifier isolation buffers for driving reactive loads and high input impedance buffers for high-speed analog to digital converters and comparators.

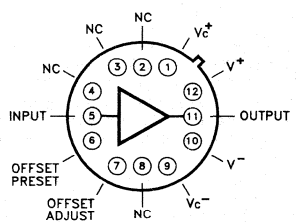
Guaranteed operation over temperature of the LH0033 family is achieved by using specially selected junction field effect transistors along with state-of-the art active laser trim techniques. They are available in the industry standard hermetic 12 Lead TO-8 metal Can.

Applications

Fast Sample/Hold Amplifiers
Flash A/D Input Buffering
Video Distribution
CRT Drive
Coaxial Line Driver

Pin Configuration

Top View



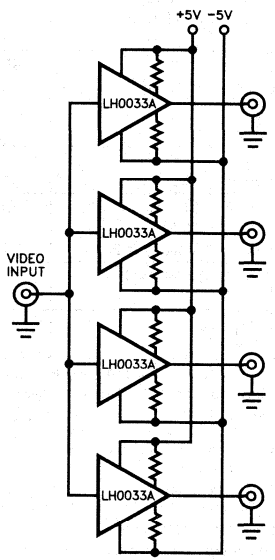
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Guaranteed operation at ±5V supplies**
- **1500 V/μs Slew Rate**
- **100 MHz Bandwidth**
- **2.9 ns Rise and Fall Times**
- **10^{11}Ω Input Impedance**
- **±5V to ±18V Supply Operation**

Ordering Information

PART	TEMP. RANGE	PACKAGE
LH0033AG	−55°C to +125°C	12 Lead TO-8
LH0033ACG	−25°C to + 85°C	12 Lead TO-8
LH0033G	−55°C to +125°C	12 Lead TO-8
LH0033CG	−25°C to + 85°C	12 Lead TO-8

Typical Operating Circuit



Low Loss 75Ω video distribution amplifier

(Detailed Circuit Diagram—Figure 7)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Fast Buffer Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$) 40V
Maximum Power Dissipation (See Curves)
LH0033A/LH0033AC/LH0033/LH0033C 1.5W
Maximum Junction Temperature 175°C
Input Voltage $\pm V_S$
Continuous Output Current
LH0033A/LH0033AC/LH0033/LH0033C ±100 mA
Peak Output Current
LH0033A/LH0033AC/LH0033/LH0033C ±250 mA
Operating Temperature Range
LH0033A/LH0033 −55°C to +125°C
LH0033AC/LH0033C −25°C to +85°C
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) +300°C

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (Note 2)		1	5		6	15		5.0	10		12	20	mV
	$R_S = 100\Omega$			10			20			15			25	mV
Offset Tempco	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100		50	100		50	100		50	100	µV/°C
Input Bias Current	$V_{IN} = 0V$													
	$T_J = 25°C$ (Note 2)			100			250			250			500	pA
	$T_A = 25°C$ (Note 4)			1.5			2.5			2.5			5.0	nA
	$T_J = T_A = T_{MAX}$			7.5			10			10			20	nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0\ k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1.0\ k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k\Omega$		6.0	10		6.0	10		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k\Omega$	±12			±12			±12			±12			V
	$V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.0			±9.0			±9.0			±9.0			V
Supply Current	$V_{IN} = 0V$ (Note 5)		20	22		21	24		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720		600	660		630	720	mW

Note 1: LH0033A and the LH0033 are 100% production tested as specified at 25°C, 125°C, and −55°C. LH0033AC and LH0033C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: LH0033A and LH0033 are 100% production tested for this parameter. LH0033AC and LH0033C are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Fast Buffer Amplifier

- ◆ Full DC specifications at ±5V supplies
- ◆ Low Input Capacitance
- ◆ Guaranteed Offset Adjust Range
- ◆ 75Ω load specifications
- ◆ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

DC ELECTRICAL CHARACTERISTICS Specifications below satisfy or exceed all "tested" parameters on adjacent page.

V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage (Note 2)	R_S = 100Ω, T_J = 25°C, V_{IN} = 0V R_S = 100Ω, V_{IN} = 0V		1 	5 10		6 	15 20		5 	10 15		12 	20 25	mV mV
Offset Tempco	R_S = 100Ω, V_{IN} = 0V (Note 3)		50	100		50	100		50	100		50	100	µV/°C
Input Bias Current	V_{IN} = 0V, T_J = 25°C (Note 2) T_A = 25°C (Note 4) T_J = T_A = T_{MAX}			100 1.5 7.5			250 2.5 10			250 2.5 10			500 5.0 20	pA nA nA
Voltage Gain	V_O = ±10V, R_S = 100Ω, R_L = 1 kΩ V_{IN} = ±10.5V, R_S = 100Ω, R_L = 100Ω V_{IN} = ±2V, R_S = 100Ω, R_L = 75Ω	0.97 0.86 0.84	0.98 0.95 0.95	1.00 1.00 1.00	0.96 0.86 0.84	0.98 0.95 0.95	1.00 1.00 1.00	0.97	0.98	1.00	0.96	0.98	1.00	V/V V/V V/V
Input Impedance	V_{IN} = ±1V, R_L = 1 kΩ, T_A = 25°C	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	V_{IN} = ±1V, R_L = 1 kΩ		6	10		6	10		6	10		6	10	Ω
Output Voltage Swing	V_{IN} = ±14V, R_L = 1 kΩ V_{IN} = ±10.5V, R_L = 100Ω, T_A = 25°C	±12 ±9			±12 ±9			±12 ±9			±12 ±9			V V
External Offset Resistance	V_{OS} = 0 mV, T_A = 25°C (Note 7)	0	75	200	0	75	200							Ω
Supply Current (Note 5)	V_{IN} = 0V		20	22		21	24		20	22		21	24	mA
Power Consumption	V_{IN} = 0V		600	660		630	720		600	660		630	720	mW

DC ELECTRICAL CHARACTERISTICS

V_S = ±5V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage (Note 2)	R_S = 100Ω, T_J = 25°C, V_{IN} = 0V		10	15		12	20							mV
Input Bias Current	V_{IN} = 0V, T_J = 25°C (Note 2) V_{IN} = 0V, T_A = 25°C (Note 4)			100 300			250 750							pA pA
Voltage Gain	V_O = ±1V, R_S = 100Ω, R_L = 1kΩ V_O = ±1V, R_S = 100Ω, R_L = 75kΩ	0.92 0.84	0.96 0.91	1.00 1.00	0.92 0.84	0.96 0.91	1.00 1.00							V/V V/V
Input Impedance	V_{IN} = ± 1V, R_L = 1kΩ, T_A = 25°C	10^{10}	10^{11}		10^{10}	10^{11}								Ω
Output Impedance	V_{IN} = ±1V, R_L = 1kΩ		6	10		6	10							Ω
Output Voltage Swing	V_{IN} = ±4V, R_L = 75Ω, T_A = 25°C	±2	±3.4		±2	±3.4								V
Supply Current	V_{IN} = 0V		16	20		16	20							mA
Power Consumption	V_{IN} = 0V		160	200		160	200							mW

Refer to notes 1-6 on adjacent page.

Note 7: Offset adjust resistor connects between device pin 7 and V — as shown in Figure 2.

Fast Buffer Amplifier

AC ELECTRICAL CHARACTERISTICS

T_C = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 1.0 kΩ (Note 6)

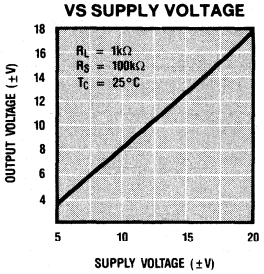
Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1.0 Vrms		100			100			100			100		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0			2.0			2.0			2.0		degrees
Rise Time	ΔV_{IN} = 0.5V		2.9			3.2			2.9			3.2		ns
Propagation Delay	ΔV_{IN} = 0.5V		1.2			1.5			1.2			1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1			<0.1			<0.1			<0.1		%

Refer to notes 1-7 on second and third page of this data sheet.

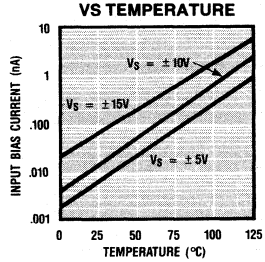
The electrical characteristics above are a reproduction of a portion of National Semiconductor Corporation's copyrighted (1984) Linear data book supplement. This information does not constitute any representation by Maxim that NSC's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Typical Operating Characteristics

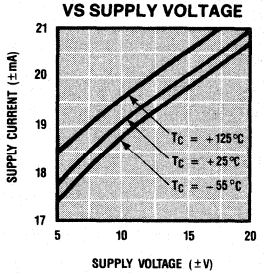
LH0033 OUTPUT VOLTAGE VS SUPPLY VOLTAGE



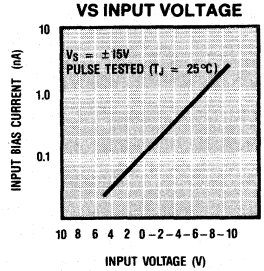
LH0033 INPUT BIAS CURRENT VS TEMPERATURE



LH0033 SUPPLY CURRENT VS SUPPLY VOLTAGE



LH0033 INPUT BIAS CURRENT VS INPUT VOLTAGE



AC ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

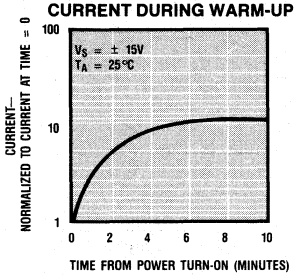
T_C = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 1.0 kΩ (Note 6)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1.0 Vrms		100			100			100			100		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0			2.0			2.0			2.0		degrees
Rise Time	ΔV_{IN} = 0.5V		2.9			3.2			2.9			3.2		ns
Propagation Delay	ΔV_{IN} = 0.5V		1.2			1.5			1.2			1.5		ns
Harmonic Distortion	f = 1kHz		<0.1			<0.1			<0.1			<0.1		%

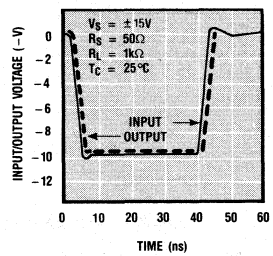
Refer to notes 1-7 on second and third page of this data sheet.

Typical Operating Characteristics

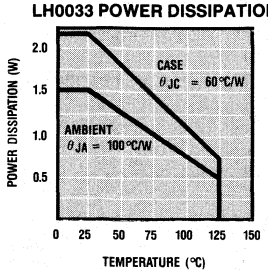
LH0033 NORMALIZED INPUT BIAS CURRENT DURING WARM-UP



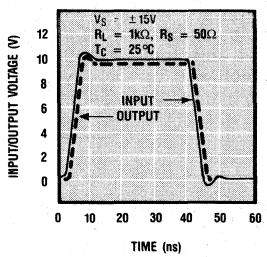
LH0033 NEGATIVE PULSE RESPONSE



LH0033 POWER DISSIPATION



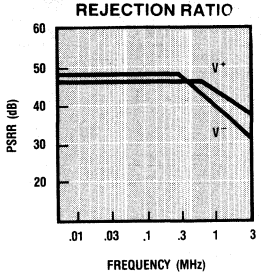
LH0033 POSITIVE PULSE RESPONSE



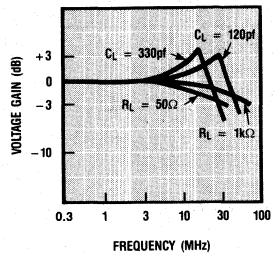
Fast Buffer Amplifier

Typical Operating Characteristics

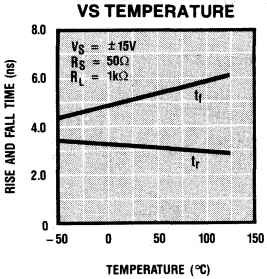
LH0033 POWER SUPPLY REJECTION RATIO



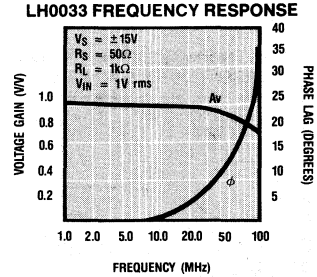
LH0033 FREQUENCY RESPONSE FOR VARIOUS LOADS



LH0033 RISE AND FALL TIME VS TEMPERATURE



LH0033 FREQUENCY RESPONSE



Detailed Description

The LH0033 combines a JFET input stage with a high current bipolar output stage. Also included is the biasing network and laser trimmed resistors for supply current and offset voltage adjustments.

The n-channel JFET Q1 has very low input current, less than 10 nA at V_{IN} = 0V and T_J = 125°C. The source of Q1 will be offset from the input voltage by the V_{GS} voltage of Q1. The output is offset from the input voltage by the IR drop across R1 and the V_{BE} of Q5. The output offset voltage has been actively laser trimmed during assembly to meet the guaranteed maximum offset specification.

Transistors Q2 and Q3 provide a two V_{BE} voltage difference between the bases of the two output transistors, setting the quiescent current through Q5 and Q6. Resistors R3 and R4 provide a small amount of degeneration to stabilize the quiescent current over temperature. Q4 is another n-channel JFET, similar to Q1. Q4 acts as a current sink for the current flowing through the input stage (Q1, R1, Q2, and Q3). The voltage drop across diode D1 and resistor R2 is equal to the drop across R1 and the base-emitter junction of Q5.

LH0033/LH0033C

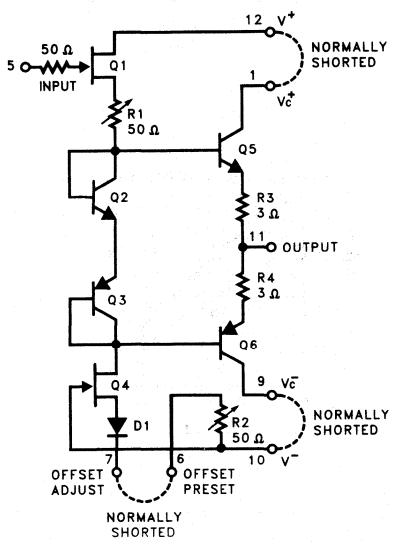


Figure 1. Internal Schematic Diagram

Since Q2 is matched to Q5 and Q3 is matched to Q6, approximately one-half of the quiescent current flows in the input stage, with the remaining quiescent current flowing through the output transistors. This means that the output stage will be operating as a class A amplifier with output currents less than 10 mA. Above this current, the output stage operates in a class B mode, with slightly increased nonlinearity.

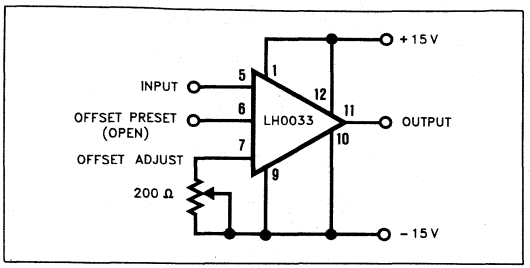


Figure 2. Offset Zero Adjust for LH0033

Applications

Layout Precautions

The LH0033 should be treated as a high frequency amplifier when designing a printed circuit layout. Power supply bypassing to a ground plane with low inductance capacitors should be within a half inch of the device. For applications where the input capacitance is critical, connect the case of the device to the output so that the case capacitance is bootstrapped. For most applications, the case may be left unconnected or grounded. There is no internal connection to the case.

Offset Voltage Adjustment

For most applications, connect pin 6 to pin 7, and the offset voltage will be guaranteed to within the actively trimmed specification. When this is not sufficient, or there is a system offset to be absorbed, an external 200Ω trim pot may be connected from pin 7 to V^-, as illustrated in Figure 2.

Operation Within an Op Amp Loop

The LH0033 may be used as a current booster within the feedback loop of almost any operational amplifier with only a few cautions: remember that the output is not internally short circuit protected, and many applications will require one of the short circuit protection circuits discussed below.

Short Circuit Protection

The LH0033 is not internally short circuit protected as most of the possibilities involve some compromise in output swing or transient response. The output stage collectors are available separately, however, so there are several options open to the user. The simplest and most commonly used is the simple resistor in each output stage collector (Figure 3). For worst case protection these resistors may be calculated by:

$$R_{LIM} = V^+/100\ mA = V^-/100\ mA$$
$$= 150\Omega \text{ for } \pm 15V \text{ supplies}$$

Unfortunately, a resistor that large severely restricts the voltage swing into a heavy load and the slew rate into a capacitive load. Decoupling the V_{C+} and V_{C-} pins with capacitors will retain full output swing for transient pulses, but if the capacitors are made too large, (to hold up long pulses) the protection is lost.

An alternative active current limit circuit is shown in Figure 4. This technique retains full DC output swing. The current sources are set to a safe limit and are normally saturated, thus applying full supply voltage to the V_C pins. In the event of a short on the output, the current source comes into operation and reduces the output stage collector voltage as required to keep the current to a safe level. The output stage collectors may be bypassed with a small capacitor to give additional current capacity for short times, as would be required in driving a capacitive load.

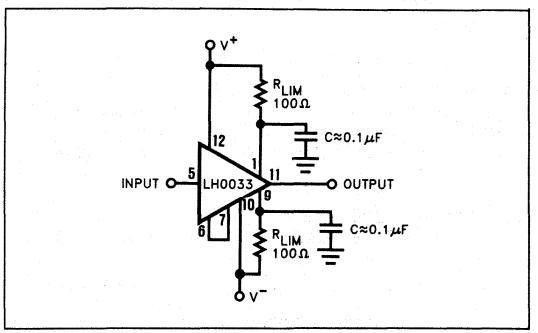


Figure 3. LH0033 Using Resistor Current Limiting

Operation from Single or Asymmetrical Power Supplies

Since the LH0033 has no ground pin, an asymmetrical power supply is indistinguishable from a symmetrical supply with a DC level on the input. (The single supply case is simply the asymmetrical case taken to the extreme of one of the supplies being zero.) In either case, an offset error will be generated corresponding directly to the gain of the circuit times the apparent DC level with respect to a pseudo ground point half-way between the supplies.

$$\text{Offset Voltage} = 0.5(1 - \text{gain})(|V^+| - |V^-|)$$

For example, a device operating on supplies of +5V and −12V would have an apparent offset error due to the gain of about −35 mV. This could be easily corrected with an offset adjust potentiometer connected from pin 6 to V^- as discussed in the offset voltage adjustment section.

Fast Buffer Amplifier

Operation from ±5V Power Supplies

The original LH0033 was characterized and guaranteed to operate at ±15 volt power supplies only, but many applications can save substantial power by operating the device from reduced supplies. The Maxim LH0033A and LH0033AC are specified and tested for gain, swing, offset voltage, bias current and supply current at ±5V power supplies as well as the standard ±15V.

Capacitive Loading

The LH0033 is designed to drive heavy capacitive loads without susceptibility to oscillation. Note that the absolute maximum current rating must still be observed, thus the output slew rate times the load capacitance must be less than 250 mA. For example, a 1000 V/μs slew rate with a 250 pF load would fall just within the absolute maximum peak current specification. If a heavier capacitive load needs to be driven, the slew rate must be externally limited.

$$\text{Slew Rate} \leq I_{OUT(MAX)}/C_{LOAD} \leq \pm 250\ \text{mA}$$

Power dissipation resulting from capacitive load currents must be considered independently. The real power dissipated in a circuit driving a sine wave into a pure capacitive load is:

$$P_{AC} = (V_{P\text{-}P})^2 \times \text{Frequency} \times C_1$$

This dissipation adds directly to the devices quiescent power and any DC load power that might be present. The sum of all these terms must be less than the absolute maximum power rating at the temperature of operation.

$$P_{DC} + P_{AC} \leq P_{DISS(PKG)}$$

For example, a 250 pF load driven to 20V peak to peak at 1 MHz adds a reactive power dissipation in the LH0033 of:

$$P_{AC} = (20)^2 \times 10^6 \times 250 \times 10^{-12} = 100\ \text{mW}$$

This term is not often a severe application problem with the LH0033.

Power Dissipation Considerations

The LH0033 package is rated for 0.5W in still air at 125°C and 0.75W with an infinite heat sink. Since the quiescent power is in the neighborhood of 600 mW, a heat sink is needed for most 125°C applications and some heavy load applications at lower temperatures. Several suitable commercial heat sinks are available including the Thermalloy 2241, the Wakefield 215CB and the IERC UP-TO8-48CB. Please note that the can diameter is 0.55 inches nominal as opposed to the JEDEC TO-8 which is 0.45 inches nominal. (See the outline drawing for detailed dimensions)

Typical Applications

Output Buffer within an Op Amp Loop

The low output impedance, high slew rate, wide power bandwidth, and low phase shift of the LH0033 make it ideally suited for use as an output buffer for operational amplifiers. When using the LH0033 as an op amp buffer, the total phase shift of both the op amp and the LH0033 buffer must be considered when checking for loop stability. With typically only 10 degrees of phase shift at 50 MHz, the LH0033 can be used with all but the very fastest op amps. With an output impedance of less than 10Ω, the LH0033 can drive large inductive or capacitive loads with little additional phase shift.

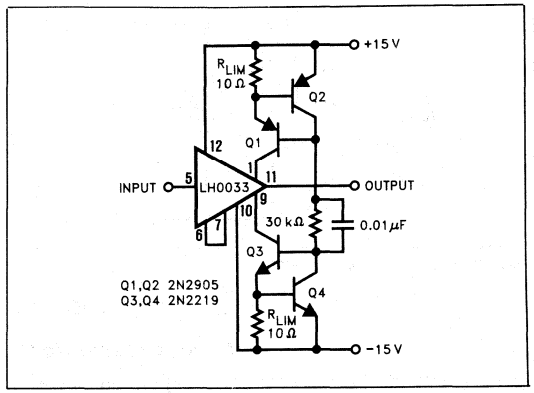


Figure 4. LH0033 Current Limiting Using Current Sources

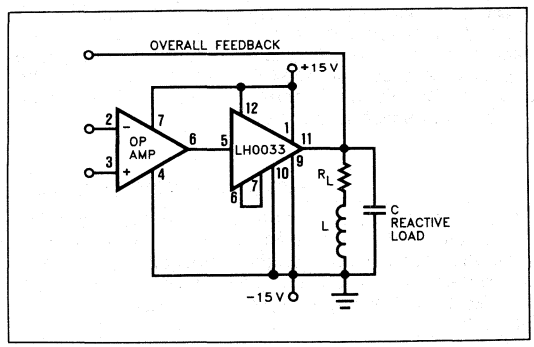


Figure 5. Isolation Buffer

Coaxial Cable Driver

With an input resistance of $10^{11}\Omega$ and input capacitance of 4 pF, the LH0033 places negligible load on a 50 or 75Ω video source. The Maxim LH0033A is guaranteed for operation with ±5V power supplies common in video systems, and is also specified for a minimum ±2V swing into a 75Ω load. The LH0033 typically has only 2 degrees of phase non-linearity over the frequency range of 1 to 20 MHz. The 68Ω resistor on the output can be shorted out if a higher output voltage is required, but this causes a mistermination of the 75Ω cable, and reflections will not be absorbed by the coaxial driver output.

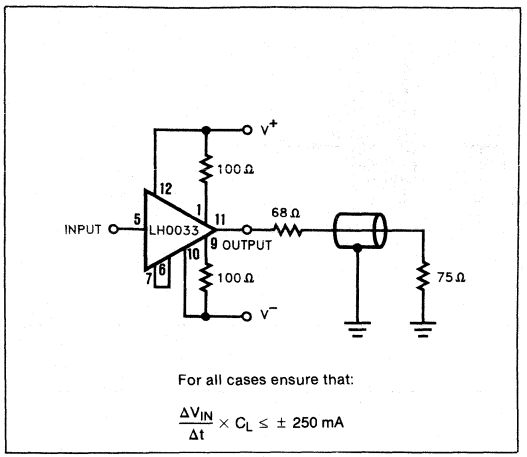


Figure 6. Coaxial Cable Driver

Video Distribution Amplifier

Figure 7 and the front page of this data sheet show a video distribution amplifier capable of driving a number of 75Ω output lines from a single source with very low signal loss. The entire amplifier operates from ±5V supplies with a total power dissipation of 640 mW plus the output power. The input resistance will be in the thousands of megohms and will be negligible in most situations. The input capacitance, however, should be considered as it may result in high frequency misterminations at the input. The voltage gain of the LH0033A and the LH0033AC is specified at 0.91 typ, 0.84 min (±5V supplies and 75Ω load), so the worst case insertion loss of the distribution amplifier is 1.5 dB with a typical under 1dB. Protection resistors are included in series with pins 10 and 12 of each device so that the distribution amplifier will be able to tolerate momentary overloads on the outputs.

Figure 8 is a similar video distribution amplifier which has output resistance of 75Ω to back terminate the outputs. The back termination resistor is selected to be 68Ω to account for the typical 6Ω output resistance of the LH0033. Because each 75Ω load is isolated from the buffer amplifier, each device is able to drive two loads. The voltage loss through this amplifier will be approximately 6 dB. Note that protection resistors are unnecessary in the back terminated configuration, as the LH0033 can safely drive the 68Ω termination resistor even if the cable is shorted.

High Speed Sample/Hold

In Figure 9, the first LH0033 buffers the input and drives the sample capacitor through the FET, Q1, whenever the Sample/Hold logic input is in the sample mode. When the logic input changes to the hold mode, Q1 opens up, isolating the hold capacitor from the input LH0033, and the output voltage no longer follows the input. The second LH0033 buffers and isolates the sample capacitor voltage from the load. Since the input bias current of the LH0033 is typically less than 1 nanoamp, the droop rate of this sample and hold will be less than 1 mV/ms.

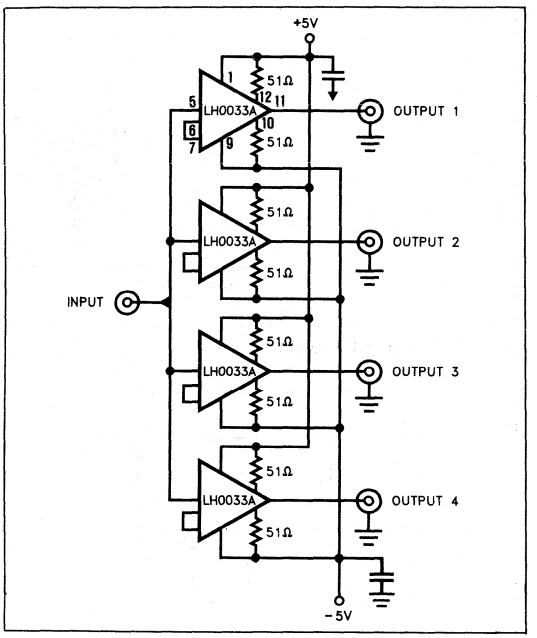


Figure 7. Low Loss 75Ω Video Distribution Amplifier

Since the LH0033 has a slew rate of 1500 V/μs and a 100 MHz bandwidth, this LH0033-based sample and hold is well suited for use with video speed flash A/D converters.

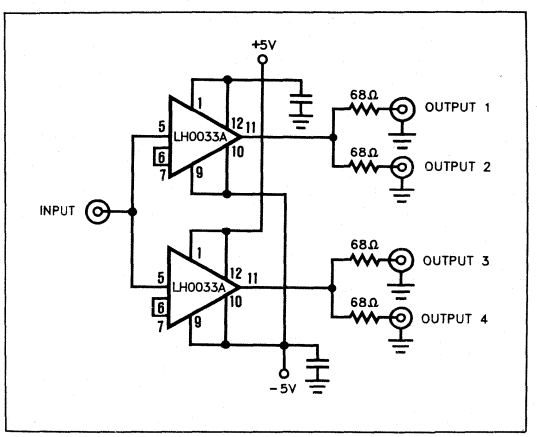


Figure 8. Back Terminated 75Ω Video Distribution Amplifier

Fast Buffer Amplifier

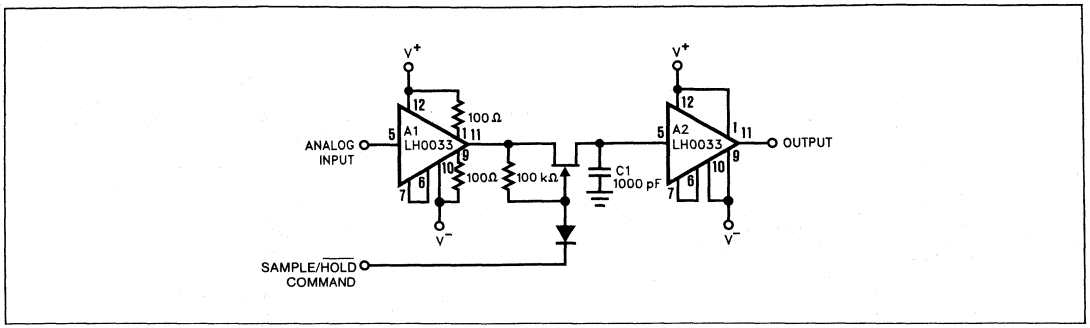


Figure 9. High Speed Sample/Hold

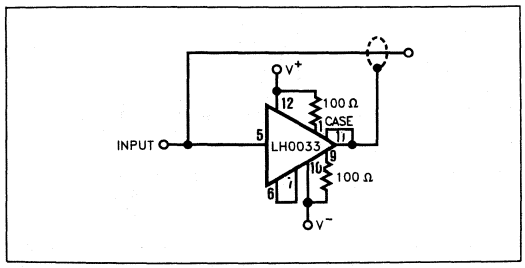


Figure 10. Instrumentation Shield/Line Driver

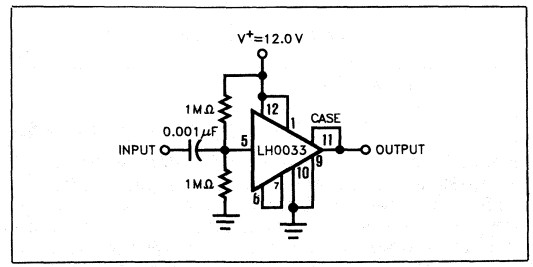


Figure 11. Single Supply AC Amplifier

General Description

The BB3553 and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to 300MHz. Both devices are similar in their slew rate; up to 6000 volts per microsecond with light loads and 2000 volts per microsecond with a 50 ohm load. The LH0063 is not internally current limited, giving added versatility and higher transient drive capability.

Applications

High Speed Line Drivers
Video Drivers/Impedance Transformation
Nuclear Instrumentation Amplifiers
Operational Amplifier Isolation
High Speed A to D Input Buffers
Video Cross Point Switches

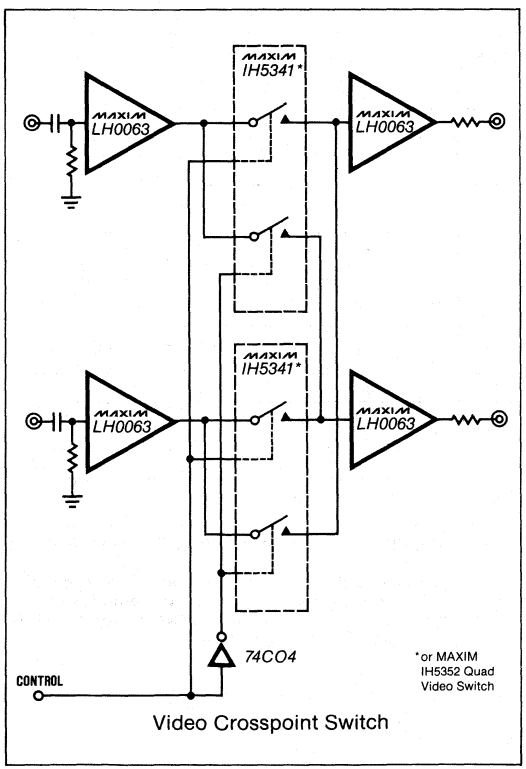
Features

- **Pin for Pin 2nd Source**
- **6000V/μSec Slew Rate**
- **DC to 300MHz Bandwidth**
- **±10V Output Drive Into 50Ω**
- **2ns Rise and Fall Times**
- **Wide Range Single or Dual Supply Operation**
- **10GΩ Input Resistance**

Ordering Information

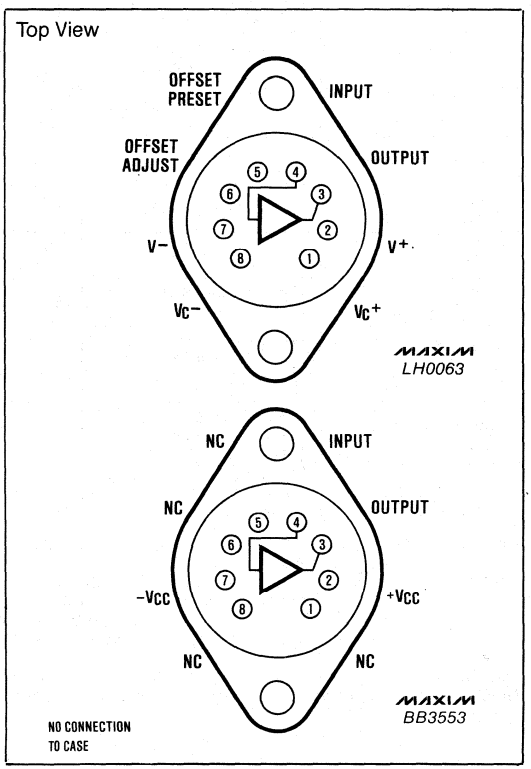
PART	TEMP. RANGE	PACKAGE
LH0063CK	-25°C to +85°C	8 Lead TO-3
LH0063K	-55°C to +125°C	8 Lead TO-3
BB3553AM	-25°C to +85°C	8 Lead TO-3

Typical Operating Circuit



Video Crosspoint Switch

Pin Configurations



Very Fast Buffer Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$) 40V
Maximum Power Dissipation (See Curves) 5W
Maximum Junction Temperature ..... 175°C
Input Voltage ..... V^+ to V^-
Continuous Output Current ..... ±250mA
Peak Output Current ..... ±500mA
Operating Temperature Range
LH0063 ..... -55°C to +125°C
LH0063C and BB3553AM ..... -25°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_S = ±15V, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified) (Note 1)

PARAMETER	CONDITIONS	LH0063			LH0063C			BB3553AM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Offset Voltage	$R_S \leq 100k\Omega$, T_J = 25°C $R_L = 100\Omega$		10	25 100		10	50 100			50	mV mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100k\Omega$ (Note 3)		300			300			300		µV/°C
Input Bias Current	T_J = 25°C (Note 2)		0.1	0.5		0.1	0.5			0.2	nA
Voltage Gain	V_{IN} = ±10V, $R_S \leq 100k\Omega$ $R_L = 1k\Omega$	0.94	0.96	1.00	0.94	0.96	1.00				V/V
Voltage Gain	V_{IN} = ±10V, $R_S \leq 100k\Omega$ $R_L = 50\Omega$, T_J = 25°C	0.92	0.93	0.98	0.91	0.93	0.98	0.92	0.93	0.98	V/V
Input Capacitance	T_A = 25°C (Note 3)		8.0			8.0			8.0		pF
Input Resistance	V_{IN} = ±1V, T_A = 25°C	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	V_{OUT} = ±10V, $R_S \leq 100k\Omega$, $R_L = 50\Omega$		1.0	4.0		1.0	4.0		1.0	4.0	Ω
Output Current Swing	V_{IN} = ±10V, $R_S \leq 100k\Omega$	0.2	0.6		0.2	0.6		0.2	0.4		A
Output Voltage Swing	$R_L = 50\Omega$	10	13		10	13		10			V
Output Voltage Swing	V_S = ±5V, $R_L = 50\Omega$, T_J = 25°C	5.0	7.0		5.0	7.0					V
Supply Current	T_J = 25°C, $R_L = \infty$, V_S = ±15V (Note 4)		35	65		35	65		50	80	mA
Supply Current	V_S = ±5V (Note 4)		50			50					mA
Power Consumption	T_J = 25°C, $R_L = \infty$, V_S = ±15V (Note 4)		1.05	1.95		1.05	1.95		1.5	2.4	W
Power Consumption	V_S = ±5V (Note 4)		500			500					mW
External Offset Resistance	V_{OS} = 0mV, T_A = 25°C (Note 5)	0	300	1000	0	300	1000				Ω

Note 1: All devices are 100% tested at 25°C only. Specifications at temperature extremes are sample tested to 10% LTPD. These limits are not used to calculate outgoing quality level.
Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25°C. When supply voltages are ±15V, no-load operating junction temperature without a heat sink may rise 20-30°C above ambient, and more under heavy load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs. temperature graph for expected values.
Note 3: QA sample tested only.
Note 4: Guaranteed through correlated automatic pulse testing at T_J = 25°C.
Note 5: Offset adjust resistor for LH0063 connects between device pin 6 and V^-.

AC ELECTRICAL CHARACTERISTICS

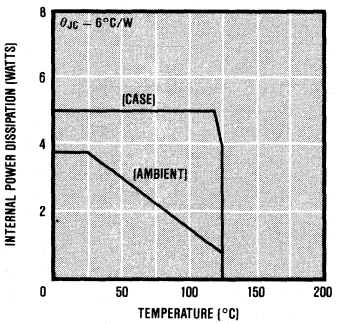
(V_S = ±15V, T_A = 25°C, R_S = 50Ω, R_L = 50Ω (Note 6))

PARAMETER	CONDITIONS	LH0063			LH0063C			BB3553AM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Slew rate	R_L = 1kΩ, V_{IN} = ±10V		6000			6000			6000		V/μS
Slew rate	R_L = 50Ω, V_{IN} = ±10V, T_J = 25°C	2000	2400		2000	2400		2000	2400		V/μS
Bandwidth	V_{IN} = 1.0V_{rms}		300			300			300		MHz
Bandwidth	Full Power, V_{IN} = 10V_{p-p}	32			32			32			MHz

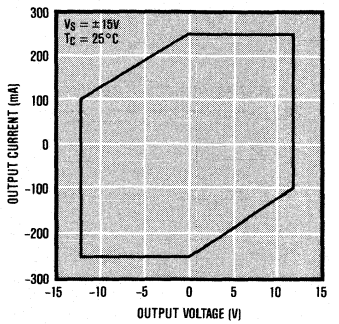
Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Operating Characteristics

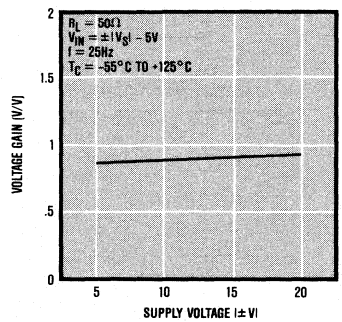
POWER DISSIPATION



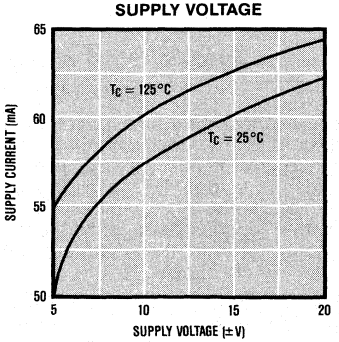
DC SAFE OPERATING AREA



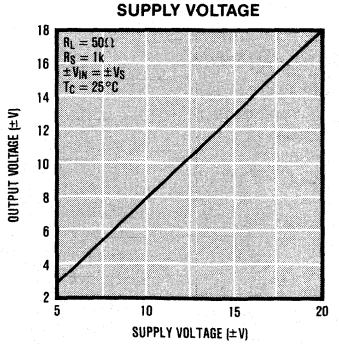
GAIN vs SUPPLY VOLTAGE



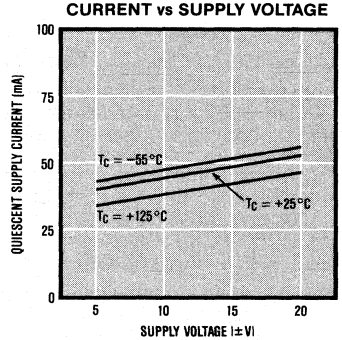
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT VOLTAGE vs SUPPLY VOLTAGE



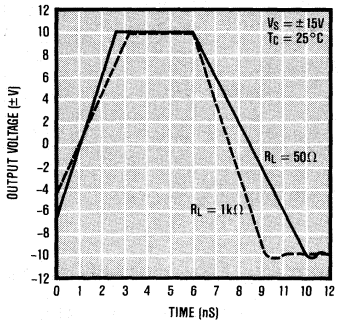
QUIESCENT POWER SUPPLY CURRENT vs SUPPLY VOLTAGE



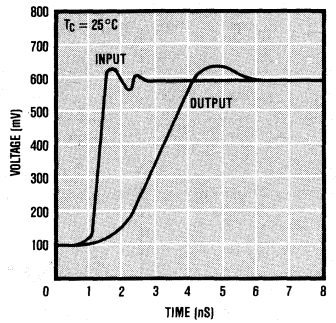
Very Fast Buffer Amplifiers

Typical Operating Characteristics

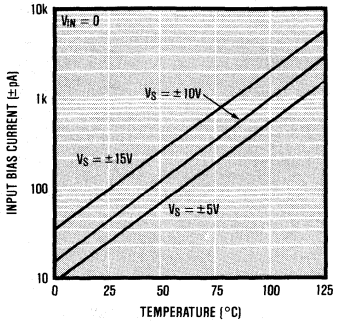
LARGE SIGNAL PULSE RESPONSE



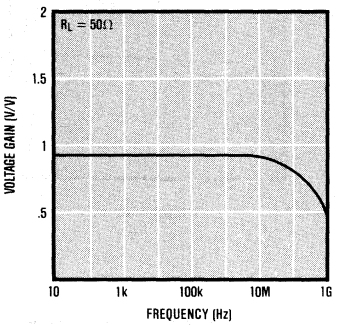
SMALL SIGNAL RISE TIME



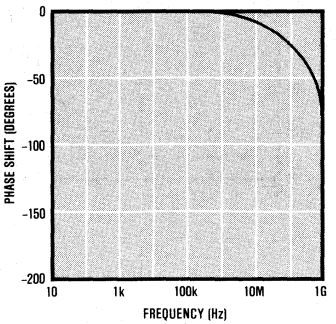
INPUT CURRENT



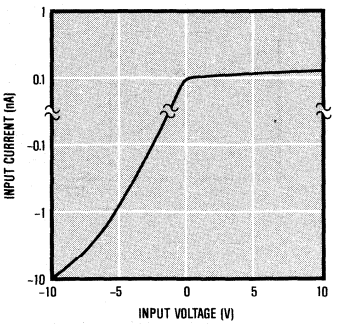
SMALL SIGNAL FREQUENCY RESPONSE



PHASE SHIFT vs FREQUENCY



INPUT CURRENT



Circuit Description

Both the BB3553 and the LH0063 consist of a complementary JFET input stage followed by a bipolar output stage. There is an inherent imbalance between the P and N channel JFETs (Q1 and Q2). Transistors Q3 and Q4 are laser trimmed current sources that correct circuit imbalances to make the offset voltage zero. On the LH0063, the negative current source is made available for optional user adjustment; the BB3553 can only be used at its factory adjusted value.

The BB3553 is internally current limited to 400mA at room temperature. This current limit is based on the V_{BE} of Q8 and Q9, so the limit point will be reduced at high temperatures. The LH0063 has no internal current limit, but has the output stage collectors brought out separately so that external current limiting can be implemented. This has the advantage that more output current is available with the LH0063, as long as the maximum power dissipation limit is not exceeded.

Application Hints

Circuit Layout

Circuit layout is one of the most important areas of high frequency circuit design. Even a good circuit design may yield only marginal performance when insufficient attention is paid to circuit layout. This is especially important with very high bandwidth systems or in a closed loop system with an operational amplifier. To get full performance capability from these buffers the following circuit guidelines are suggested:

1. **Use a ground plane.** It provides a shielded, low-resistance, low-inductance ground reference and reduces undesirable high-frequency coupling.
2. **Avoid IC sockets.** The increased inter-lead capacitance can degrade bandwidth and increase feedback capacitance. Contact resistance can cause offset errors that are difficult to account for.

3. **Keep input and output connections short.** This results in a more compact physical layout and minimizes parasitic coupling.
4. **Minimize capacitance.** When used with an op amp, minimize capacitance from output to feedback point and from feedback summing junction to ground.
5. **Keep wide traces.** Supply and output signal traces should be as wide as practical to minimize inductance and resistance.

Power Supply Decoupling

The positive and negative power supply terminals of the devices must be bypassed to ground with solid tantalum capacitors of about 4.7μF. A somewhat larger aluminum electrolytic can be used if shunted by a high frequency capacitor with good performance at 100 MHz. In any case, the high frequency decoupling capacitors should be placed no more than ¼ to ½ inch from the device pins. These capacitors must be returned to the same ground point on the ground plane or connected by a short, wide circuit board trace of low inductance and resistance.

Compensation

Buffer amplifiers are inherently stable in applications with resistive loads and adequate supply bypassing. However, there may be some tendency towards ringing or oscillation with capacitive loads of 100 pF or greater.

When a buffer amplifier is placed within the feedback loop of a high-gain op amp, the phase margin of the operational amplifier is reduced by an amount equal to the phase lag of the buffer at the amplifier's unity gain frequency. With most monolithic amplifiers, this will be a very small effect, but it should be considered for amplifiers active above 10MHz.

Power Dissipation and Device Rating

The maximum junction temperature of the BB3553 or the LH0063 is 150°C. This is the basic limitation that, in conjunction with the total thermal resistance, sets the maximum allowable power dissipation for either device. Specifically,

$$P_{DISS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where

$T_{J(MAX)}$ is the maximum allowable junction temperature of the device, e.g. 150°C

T_A is the ambient temperature

θ_{JC} is the junction to case thermal resistance, 6°C/W

θ_{CS} is the thermal resistance between the device case and the heatsink in °C/W

θ_{SA} is the thermal resistance for the heatsink to ambient in °C/W.

The θ_{JC} of the BB3553 and the LH0063 is typically 6°C/W; a conservative design should use a value of 10°C/W to allow for device-to-device variaitons in θ_{JC}. The actual power dissipation in a specific application is the sum of the quiescent power dissipation (1.5W typical for the BB3553; 1.05W typical for the LH0063 assuming ±15V power supplies) and the power dissipation in the output transistors. The dissipation in the output stage is the time average of the instantaneous product of the output current times the voltage difference between the output and the supply voltages.

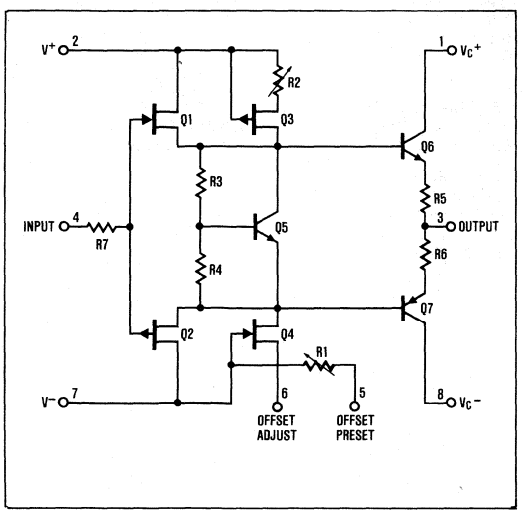


Figure 1. LH0063 Internal Structure

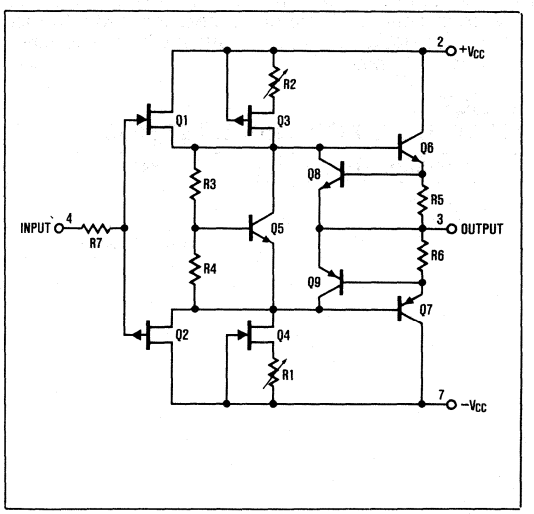


Figure 2. BB3553 Internal Structure

Very Fast Buffer Amplifiers

Operation from Single or Asymmetrical Power Supplies

Buffer amplifiers may be readily operated from single or asymmetrical power supplies with only a few precautions. Since the device has no ground pin and a gain of slightly less than one, an imbalance in the supplies appears to the buffer as a DC signal. It will amplify this DC signal by its gain, and will thus develop an apparent offset voltage different than the one specified in the Electrical Characteristics table. The additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.02(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.96

V^+ = Positive supply voltage

V^- = Negative supply voltage

Offset Voltage Adjustment

The normal definition of an amplifier's offset voltage is that voltage which must be applied to the input to produce zero volts at the output. This definition also applies to a buffer, but there are some other effects to consider. Most important is gain. A device that has a gain of 0.96 will develop nearly a volt of error when the input is taken to plus or minus 10V. In many applications the absolute value of the gain can be compensated.

The LH0063 has provisions for external offset voltage adjustment while the BB3553 is internally committed to its factory trimmed value. When not required, the offset adjust pins of the LH0063 must be shorted together. The external adjustment uses a 1kΩ potentiometer between pin 6 of the LH0063 and V^-. The table of DC electrical characteristics guarantees the MAXIM device to be adjustable to zero volts offset with the specified 1kΩ potentiometer.

TABLE 1.
HEATSINKS FOR LH0063/BB3553

MANUFACTURER	PART #
Thermalloy	6002-19
IERC	LAIC3B4CB HPI-TO3-33CB

Short Circuit Protection

The BB3553 has internal current limiting set at 400mA to protect the output stage against transient overloads. Prolonged overloads can still potentially destroy the device, depending on heat sinking and ambient conditions. The LH0063 is capable of considerably higher peak currents because it does not have the internal current limiting, but it should be externally protected if even a momentary overload is possible.

Input Bias Current vs Input Voltage

The data sheet guarantee for input bias current and input resistance on both devices assumes an input voltage of zero volts. This is the most reasonable condition for small signal applications, but increases dramatically when the input signal swings negative. The curve of typical input current vs. input voltage illustrates the problem. In many applications, the situation can be improved by reducing the positive supply voltage.

TABLE 2. SOCKETS FOR LH0063/BB3553

MANUFACTURER	PART #	COMMENTS
Robinson Nugent, Inc.	0002011	Chassis or heat-sink mounted socket
Midland-Ross Hypertronics	450-3716-01-03-00 YSK0102-004	Low cost socket pins for PCB mounting. 8 socket pins are required to mount one device.

Hypertronics
16 Brent Dr.
Hudson, MA 01749
(617) 568-0451

IERC
135 W. Magnolia Bl.
Burbank, CA 91502
(818) 786-1182

Midland-Ross
Cambion Div.
445 Concord Ave.
Cambridge, MA 02238
(617) 491-5400

Robinson-Nugent Inc.
800 E. 8th St.
New Albany, IN 47150
(812) 945-0211

Thermalloy
P.O. Box 34829
Dallas, TX 75234
(214) 243-4321

MAXIM
Power Operational Amplifier

General Description

The Maxim LH0101 Power Operational Amplifier delivers up to 5 Amp peak output current. Packaged in a rugged TO-3 case, the LH0101 combines the ease of use and performance of a FET input op amp with the power handling capabilities of a 5 Amp output stage. The output short circuit protection makes this device ideal for driving AC and DC motors, large capacitive loads, and electromagnetic actuators. The output stage virtually eliminates crossover distortion while using little quiescent power.

The LH0101 is a wideband amplifier, with a full power bandwidth of 300kHz and a gain bandwidth of 5MHz. To simplify connection to the LH0101, the output of Maxim's LH0101 is connected to both the case and to pin 4.

Features

- **Pin for Pin 2nd Source!**
- **5 Amp Peak, 2 Amp Continuous Output Current**
- **Virtually No Crossover Distortion**
- **300 kHz Power Bandwidth**
- **300 pA Input Bias Current**
- **10 V/μs Slew Rate**
- **5 MHz Gain Bandwidth**
- **2 μs Settling Time to 0.01%**
- **Adjustable Current Limit**

Applications

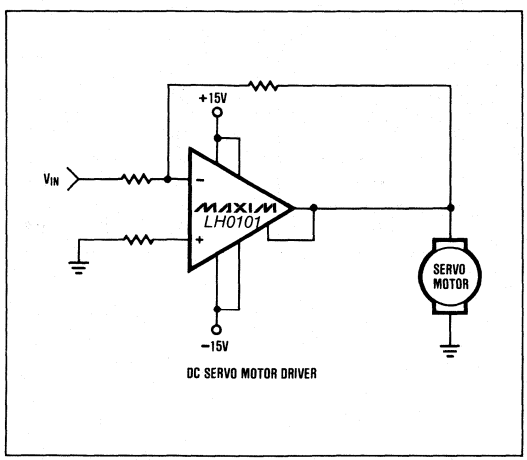
The LH0101 is well suited for applications requiring both standard op amp performance and high current output capability:

DC Motors
AC Motors
Actuators
Coaxial Cable Drivers
Programmable Power Supplies

Ordering Information

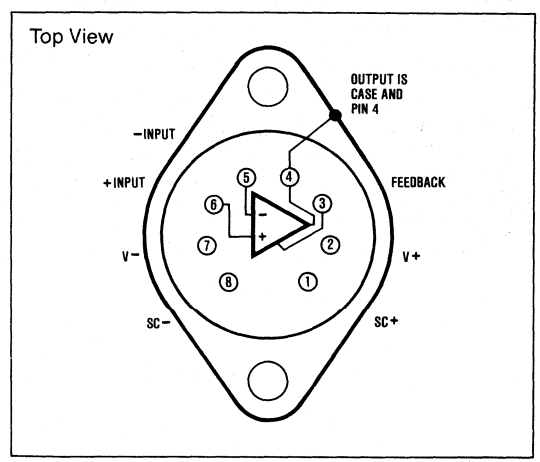
PART	TEMP. RANGE	PACKAGE
LH0101CK	-25°C to +85°C	8 Lead TO-3
LH0101K	-55°C to +125°C	8 Lead TO-3
LH0101ACK	-25°C to +85°C	8 Lead TO-3
LH0101AK	-55°C to +125°C	8 Lead TO-3

Typical Operating Circuit



DC SERVO MOTOR DRIVER

Pin Configuration



Power Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S ..... ±22V
Power Dissipation at T_A = 25°C 5W
  Derate linearly at 25°C/W to zero at 150°C
Power Dissipation at T_C = 25°C 62W
  Derate linearly at 2°C/W to zero at 150°C
Differential Input Voltage, V_{IN} ..... ±40V but < $\pm V_S$
Input Voltage Range, V_{CM} ..... ±20V but < $\pm V_S$
Peak Output Current (50ms pulse) 5A
Output Short Circuit Duration (within rated power dissipation, R_{SC} = 0.35Ω, T_A = 25°C) ..... Continuous
Operating Temperature Range
  LH0101AC, LH0101C ..... -25°C to +85°C
  LH0101A, LH0101 ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Maximum Junction Temperature ..... 150°C
Lead Temperature (Soldering, < 10 seconds) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 25°C unless otherwise noted, see Note 1)

PARAMETER	SYMBOL	CONDITIONS		LH0101AC, LH0101A			LH0101C, LH0101			UNITS
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	T_A = 25°C			1	3		5	10	mV
		$T_{MIN} \le T_A \le T_{MAX}$ (Note 4)				7			15	mV
Change in Input Offset Voltage with dissipated power	$\frac{\Delta V_{OS}}{\Delta P_D}$	(Note 2)			150			300		μV/W
Change in Input Offset Voltage with temperature	$\frac{\Delta V_{OS}}{\Delta T}$	V_{CM} = 0			10			10		μV/°C
Input Bias Current	I_B	T_A = 25°C				300			1000	pA
		$T_A \le T_{MAX}$ (Note 4)	LH0101C/AC			60			60	nA
			LH0101/A			300			1000	nA
Input Offset Current	I_{OS}	T_A = 25°C				75			250	pA
		$T_A \le T_{MAX}$ (Note 4)	LH0101C/AC			15			15	nA
			LH0101/A			75			250	nA
Large Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 10Ω		50	200		50	200		V/mV
Output Voltage Swing	V_O	R_{SC} = 0Ω	R_L = 100Ω	±11.7	±12.5		±11.7	±12.5		V
		A_V = +1 (Note 3)	R_L = 10Ω	±11	±11.6		±11	±11.6		V
			R_L = 5Ω	±10.5	±11		±10.5	±11		V
Common Mode Rejection Ratio	CMRR	ΔV_{IN} = ±10V		85	100		85	100		dB
Power Supply Rejection Ratio	PSRR	ΔV_S = ±5V to ±15V		85	100		85	100		dB
Quiescent Supply Current	I_S				28	35		28	35	mA

AC ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 25°C, see Note 1)

PARAMETER	SYMBOL	CONDITIONS		LH0101AC, LH0101A			LH0101C, LH0101			UNITS
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Equivalent Input Noise Voltage	e_n	f = 1kHz			25			25		nV/√Hz
Input Capacitance	C_{IN}	f = 1MHz			3.0			3.0		pF
Power Bandwidth, -3dB		R_L = 10Ω	A_V = +1		300			300		kHz
Slew Rate (Note 4)	SR			7.5	10			10		V/μs
Small Signal Rise or Fall Time	t_r, t_f				200			200		ns
Small Signal Overshoot					10			10		%
Gain-Bandwidth Product (Note 4)	GBW	R_L = ∞		4.0	5.0			5.0		MHz
Large Signal Settling Time to 0.01%	t_s				2.0			2.0		μs
Total Harmonic Distortion	THD	P_O = 0.5W, f = 1kHz R_L = 10Ω			0.008			0.008		%

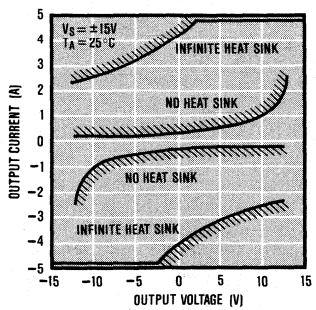
Note 1: Specification is at T_J = 25°C. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, V_{OS} may change 0.5mV and I_B and I_{OS} will change significantly during warmup. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Temperature tests are made only at extremes.

Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

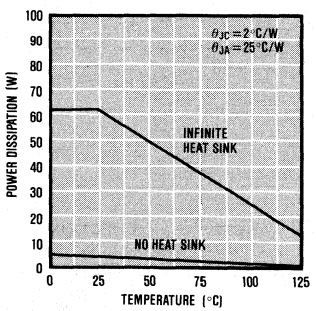
Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

Note 4: These parameters are sample tested to 10% LTPD.

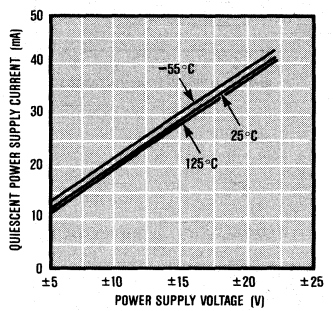
SAFE OPERATING AREA



MAXIMUM POWER DISSIPATION

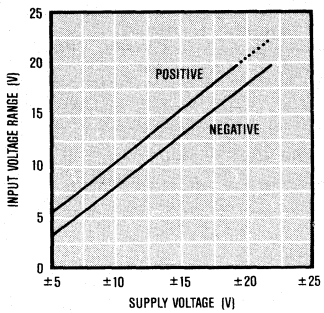


QUIESCENT POWER SUPPLY CURRENT

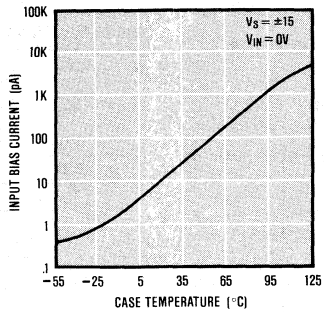


Power Operational Amplifier

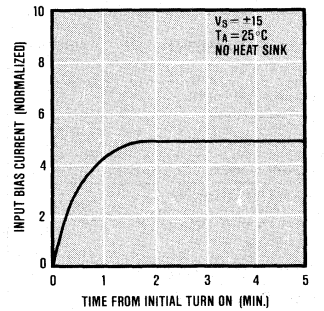
INPUT COMMON-MODE VOLTAGE RANGE



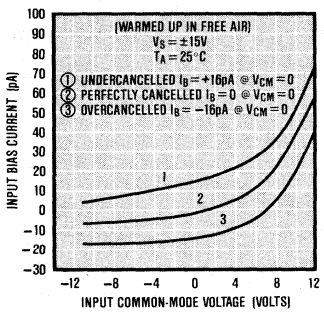
INPUT BIAS CURRENT



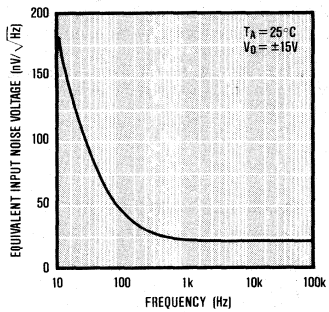
INPUT BIAS CURRENT AFTER WARM-UP



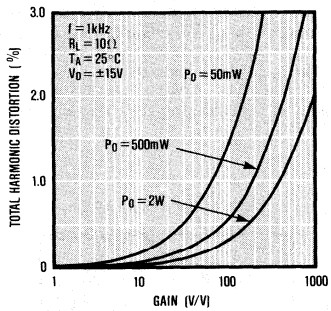
INPUT BIAS CURRENT VS. COMMON-MODE VOLTAGE



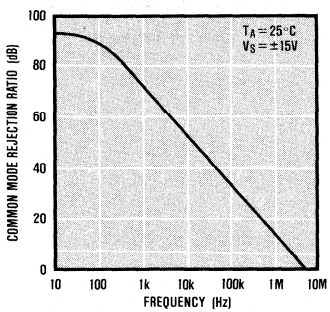
EQUIVALENT INPUT NOISE VOLTAGE



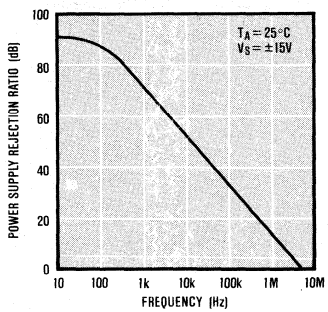
TOTAL HARMONIC DISTORTION VS. GAIN



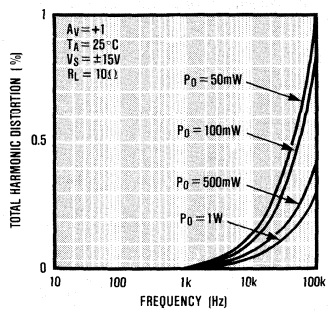
COMMON-MODE REJECTION RATIO VS. FREQUENCY



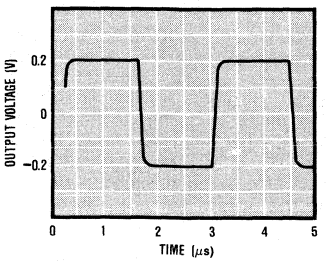
POWER SUPPLY REJECTION RATIO VS. FREQUENCY



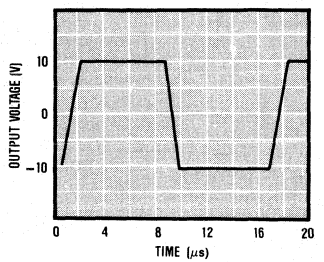
TOTAL HARMONIC DISTORTION VS. FREQUENCY



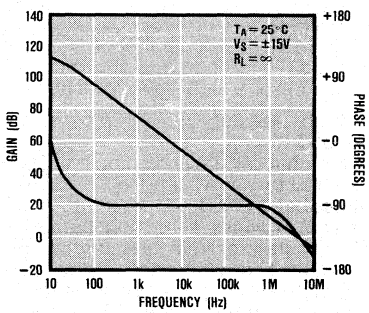
SMALL SIGNAL PULSE RESPONSE (NO LOAD)



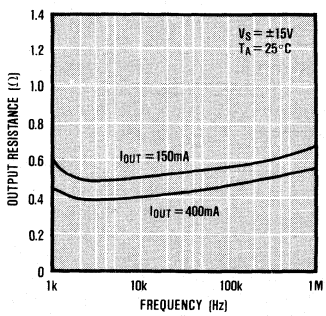
LARGE SIGNAL PULSE RESPONSE (R_L = 10Ω)



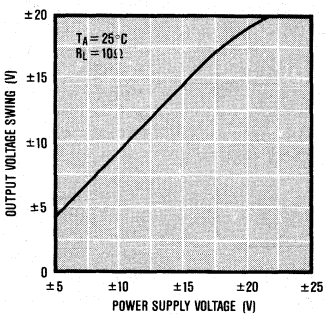
SMALL SIGNAL FREQUENCY RESPONSE (OPEN LOOP)



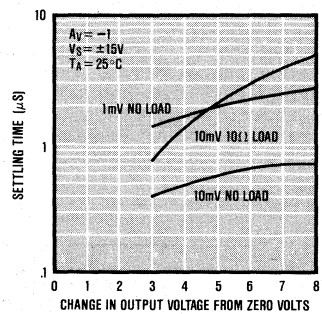
OPEN-LOOP OUTPUT RESISTANCE VS. FREQUENCY



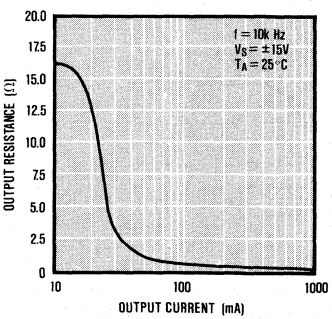
OUTPUT VOLTAGE SWING WITH SWING ENHANCEMENT



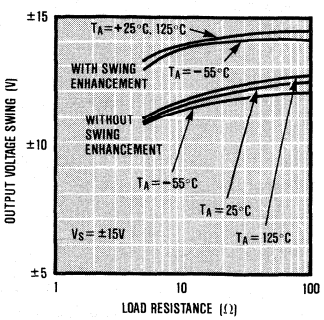
SETTING TIME



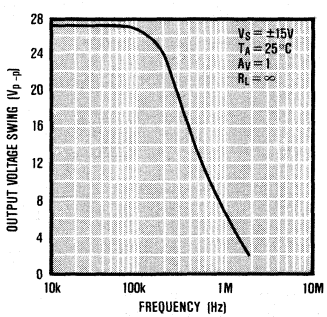
OPEN-LOOP OUTPUT RESISTANCE



OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



OUTPUT VOLTAGE SWING VS. FREQUENCY



5

Power Operational Amplifier

Detailed Description

The LH0101 consists of three stages: an operational amplifier, a buffer, and a power output stage, (see Figure 1). The operational amplifier is similar to the LF156. This operational amplifier was chosen for its low bias current, high slew rate, and fast settling time.

The buffer stage, made up of transistors Q3, Q5, Q10, and Q11, is a unity gain current amplifier. The buffer stage bandwidth is greater than 50MHz, and is current limited to 50mA output by the JFETs Q8 and Q7. If the Feedback pin is connected to the Output, the buffer stage provides all output current up to 25mA. The buffer stage current flows through the 50Ω resistors, R3 and R4. The voltage across these resistors turns on the high power output stage when the buffer stage output current is approximately 25mA. The buffer stage continues to supply current up to its 50mA current limit during the turn-on delay of the output stage. Only in driving low resistance or high capacitance loads at high frequencies will there be any noticeable distortion during the period when the output stage is turning on.

The high power output stage consists of the power darlingtons, Q1 and Q2, and the current limit protection circuit. The power darlington transistors are die attached directly to the case, minimizing thermal resistance. This electrically connects the collectors of Q1 and Q2 to the case, therefore the case is the LH0101 Output connection. The output of the Maxim LH0101 is also connected to pin 4. This additional output connection enables users to make all connections directly via a socket or printed circuit board, without having to make the output connection through heatsink mounting hardware.

Transistors Q6 and Q9 provide current limit protection. The current limit threshold is programmed by sense resistors connected between the supplies and the short circuit protection pins, SC^+ and SC^-. A voltage of about 0.6V across the sense resistors turns on either Q6 (source current limit) or Q9 (sink current limit). These transistors then turn on Q12 or Q4, which divert excess base current drive away from the darlington output transistors, preventing the output current from rising beyond the preset limit.

Application Hints

Output Swing Enhancement

When the Feedback terminal is directly connected to the Output, the buffer stage clips and limits the output voltage swing before the output stage saturates. The output swing is 11V to 12.5V with the Feedback terminal connected to the Output. The output swing can be increased by using the circuit of Figure 2. In this circuit the output stage operates with a gain of 1.5 and the output stage saturation voltage of approximately 1V limits the output voltage swing. The 0.01μF compensation capacitor is required for loop stability in unity gain non-inverting buffer applications using output swing enhancement, but is not needed in circuits with a closed loop gain greater than 1.5.

Capacitive Loads

Capacitive loads create an additional pole with the associated phase shift, which may cause oscillations. The LH0101 typically has 60° of phase margin as a unity gain buffer with no capacitive load. A 1000pF load will reduce this phase margin to 40° and 0.01μF will reduce it to only 22°. A phase margin of only 22° is generally considered unacceptably low and the LH0101 should

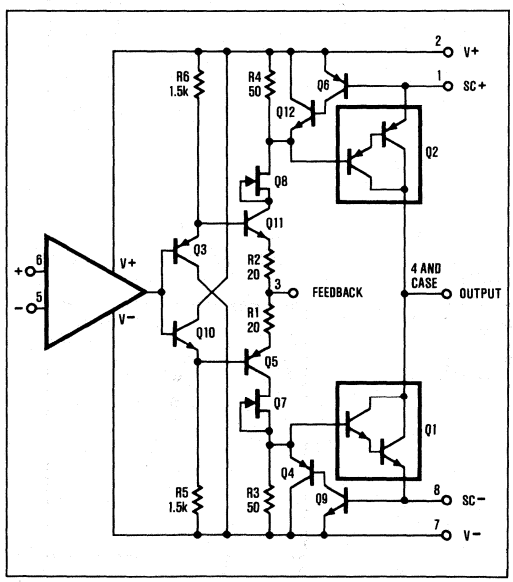


Figure. 1. Maxim LH0101 Schematic.

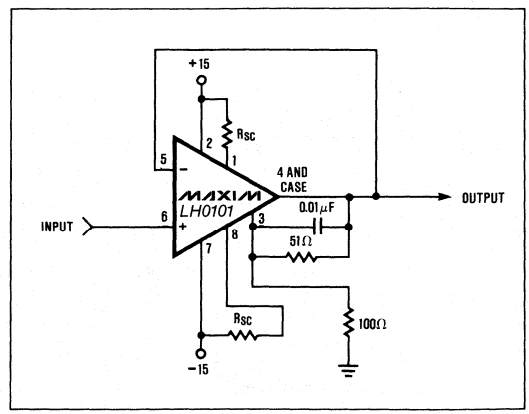


Figure 2. High Power Voltage Follower with Swing Enhancement.

be compensated as shown in Figure 3 when driving capacitive loads in the 0.01 μF range. Figure 4 shows an alternative method of compensation which can easily be used with the output swing enhancement circuit discussed below.

As with most amplifiers, there is a value of load capacitance above which oscillation will not occur. For the LH0101 this value is approximately 0.1 μF. The pole formed by the LH0101 output impedance and capacitive loads greater than 0.1 μF becomes the dominant pole and oscillation will not occur. In summary, if the load capacitance is less than 1000pF or greater than 0.1 μF the circuit should be stable, otherwise use the compensation techniques of Figure 3 or 4.

Inductive Loads

Inductive loads present three potential problems: inductive kickback or back EMF, stability, and safe operating area (SOA) violations. The LH0101 is suitable for driving inductive loads such as voice coil actuators and motors, but many circuits will require protection from the harmful effects of the energy stored in the inductor. The inductive kickback problem occurs when the power to the circuit is removed while high current is still flowing through the inductor. The back EMF or inductive kickback may have enough energy to destroy the LH0101 as current flows from the inductive load, through the output stage, back into the internal circuitry of the LH0101. The clamp diodes shown in Figure 5 will steer the inductive kickback currents directly to the power supplies, thus protecting the LH0101.

Some inductive loads, particularly those with high Q, may cause spurious oscillations. The damping circuit shown in Figure 6, a series combination of 10Ω and 0.01 μF or 0.1 μF, usually cures this type of problem.

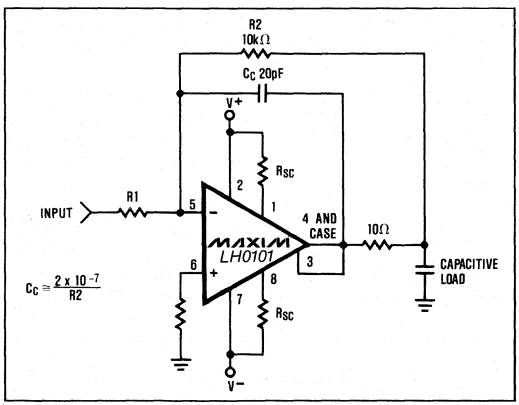


Figure 3. Compensation for Capacitive Load.

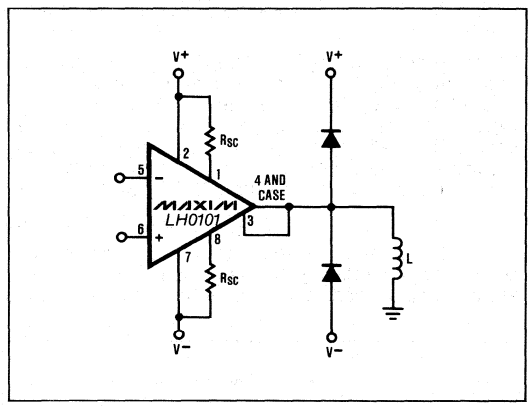


Figure 5. Back EMF Suppression.

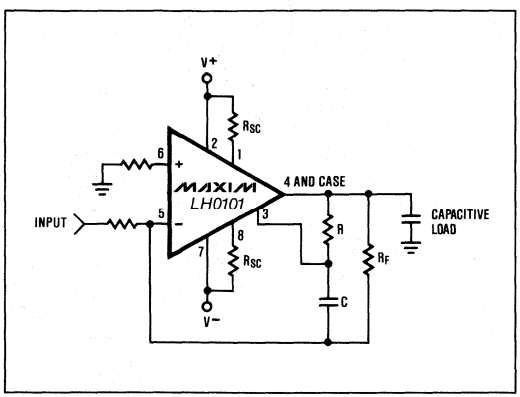


Figure 4. Alternate Compensation for Capacitive Load.

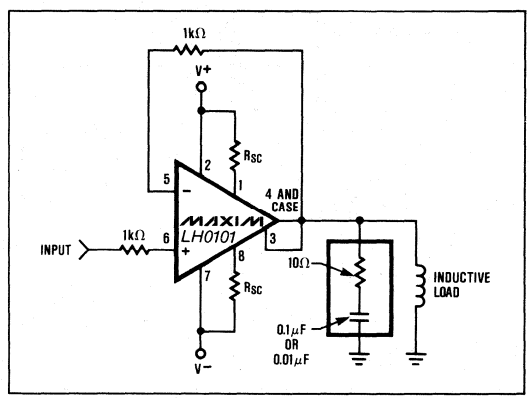


Figure 6. Damping of High Q Inductive Load.

Power Operational Amplifier

Printed Circuit Board Layout and Kelvin Connections or Remote Sensing

Printed circuit board traces which carry high currents must be carefully designed. High current traces must of course be wide enough to handle the current without excessive heating. A 0.030" wide trace on 2oz./ft^2 copper clad board will have a 10°C rise when carrying 3 Amp. Even when the printed circuit board traces are large enough to carry the current, the voltage drops may cause errors in the output. For example, a 0.030" wide trace on a 2oz. copper clad board will have a resistance of 10mΩ per inch of length and will have a voltage drop of 20mV/inch when carrying 2 Amp. Errors due to voltage drops can be avoided by using one trace or conductor for high current output connections and a second trace or conductor for the low current feedback sensing connection. Figure 7 shows the proper configuration of supply and feedback connections. The 470Ω resistor completes the feedback path if the remote sense connection is inadvertently disconnected.

In some cases signal ground and the power ground are connected together elsewhere and cannot be connected as shown in Figure 7. In this case the circuit of Figure 8 can be used. If $R_{SG}/R_{PG} = R_I/R_F$, voltage drops across R_G are turned into a common mode voltage at the input of the LH0101 and are rejected by the 100dB common mode rejection ratio (CMRR) of the LH0101.

Supply Bypassing

The LH0101 must be adequately bypassed to avoid oscillation and stability problems caused by the power supply impedance. The higher currents and lower impedance levels associated with the LH0101 require more bypassing than is normally required for lower power op amps. A 0.1μF ceramic capacitor in parallel with at least 47μF is recommended. The minimum acceptable bypassing is 0.01μF in parallel with 4.7μF between ground and each power supply.

Common Mode Voltage Range

While the common mode rejection ratio (CMRR) is guaranteed only over the ±10V input voltage range, the actual input common mode voltage range (CMVR) is typically -12V to +15.1V with ±15V power supplies.

Exceeding the negative common mode limit on either input will cause a phase reversal: if the inverting input exceeds the negative common mode limit the output will be forced low; if the non-inverting input exceeds the negative common mode limit the output will be forced high.

Exceeding the positive common mode limit on only one input will not cause a phase reversal. Exceeding either the positive or the negative common mode limit with both inputs will force the output high.

The LH0101 does not latch-up when the inputs exceed the common mode voltage range provided the absolute maximum ratings are not exceeded; normal operation resumes when the inputs return to within the common mode voltage range limits.

Input Protection

While the very low input bias current specification of the LH0101 might appear to eliminate the need for a bias compensation resistor at the non-inverting input,

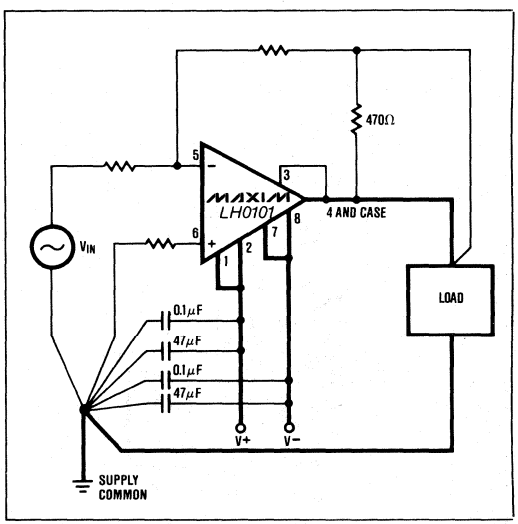


Figure 7. Power Supply Connections.

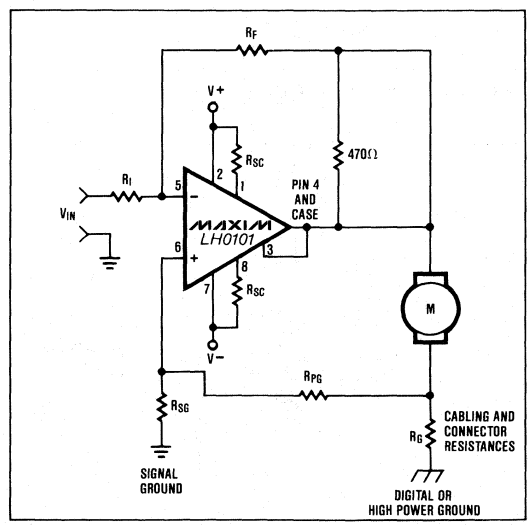


Figure 8. Correcting for Voltage Difference between Signal and Power Grounds.

the bias compensation resistor also protects this input. Direct connection of the inputs to ground should be avoided since excessive fault currents might flow if one of the power supplies were to be interrupted. A 1kΩ or greater resistor in series with the inputs will avoid this potential problem.

Heatsinks and Power Dissipation Limits

The maximum junction temperature of the LH0101 is 150°C. This is the basic limitation that, in conjunction with the thermal resistance, sets the maximum allowable power dissipation for the LH0101. Specifically,

$$P_{DISS(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where

$T_{J(MAX)}$ is the maximum allowable junction temperature of the LH0101, 150°C.

T_A is the ambient temperature.

θ_{JC} is the LH0101 junction to case thermal resistance, 2°C/W.

θ_{CS} is the thermal resistance between the LH0101 case and the heatsink in °C/W.

θ_{SA} is the thermal resistance from the heatsink to ambient.

The θ_{JC} of the LH0101 is typically 2°C/W; a conservative design should use a value of 2.5°C/W to allow for device-to-device variations in θ_{JC}. The actual power dissipation in a given application is the sum of the quiescent power dissipation (850mW typical with ±15V power supplies) and the power dissipation in the output transistors. The dissipation in the output transistors is the time average of the instantaneous product of the output current times the voltage difference between the output and the supply voltage.

Short Circuit Current Limiting

The source and sink current limits are individually set by the current sense resistors connected between the power supplies and the short circuit current limit pins, SC^+ and SC^-. Calculate the resistor values from the formula:

$$I_{SHORT\ CIRCUIT} = \frac{0.6V}{R_{SC}}$$

This equation is only an approximation, and it is not unusual for the actual current limit to vary as much as 25% from the expected value. The 0.6V in the above formula is the V_{BE} of Q6 and Q9, which may vary as much as 10% from device to device. This V_{BE} also has a temperature coefficient of about −2mV/°C. A second error source is the exact value of R_{SC}. Remember that R_{SC} includes all resistance between the power supply and the SC terminal, including printed circuit board trace resistance, solder joints, and if a socket is used, the socket contact resistance. Since R_{SC} may be as low as 0.12Ω, these extra resistances can be a significant fraction of the total R_{SC}. The power dissipation of the current limit resistor is:

$$P_{DISS} = \frac{(0.6V)^2}{R_{SC}\ (\text{in}\ \Omega)} = \frac{0.36}{R_{SC}}\ \text{Watts}$$

When the LH0101 is used without a heatsink, set the current limit to 250mA with 2.7Ω resistors for R_{SC}.

Safe Operating Area

The Safe Operating Area curve shown in the typical characteristics section must not be exceeded. This curve is for a case temperature of 25°C, and must be further derated for operation at elevated case temperatures.

There are two basic limits that must be observed; the maximum current limit and the maximum power dissipation limit. The SOA curve does not have any limits set by secondary breakdown in the output transistors, the power dissipation limit is reached before the transistors approach their secondary breakdown limits.

Table 1. HEATSINKS FOR LH0101

Manufacturer	Part #
Thermalloy	6002-19
IERC	LAIC3B4CB HPI-TO3-33CB

Table 2. SOCKETS FOR LH0101

Manufacturer	Part #	Comments
Robinson Nugent Inc.	0002011	Chassis or heatsink mounted socket
Midland-Ross	450-3716-01-03-00	Low cost socket pins for PCB mounting. 8 socket pins are required to mount one LH0101
Hypertronics	YSK0102-004	

Hypertronics
16 Brent Dr.
Hudson, MA 01749
(617) 568-0451

IERC
135 W. Magnolia Bl.
Burbank, CA 91502
(818) 786-1182

Midland-Ross
Cambion Div.
445 Concord Ave.
Cambridge, MA 02238
(617) 491-5400

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150
(812) 945-0211

Thermalloy
P.O. Box 34829
Dallas, TX 75234
(214) 243-4321

Power Operational Amplifier

Typical Applications

DC Servomotor Amplifiers

Figure 10 shows a voltage feedback DC servomotor amplifier. This type of control loop is normally used when the speed control is achieved by controlling the motor voltage. With the resistor values shown, the voltage at the motor will be -5 x V_{IN}. The output voltage is sensed at the motor, therefore voltage drops in the cable between the LH0101 and the motor will not affect the voltage applied to the motor. The 10Ω resistor and 0.01μF capacitor may be required to prevent oscillations.

Figure 11 shows a current feedback DC servomotor amplifier. This type of control loop is normally used to develop a torque approximately proportional to the input voltage. Like Figure 9 this circuit delivers a constant current that is proportional to the input voltage.

Figure 12 combines both current and voltage feedback to achieve better open loop speed regulation than can be achieved by either Figure 10 or 11. The specific values of R_S, R_{FI} and R_{GI} are chosen to best approximate the Speed/Current/Torque characteristic of the motor. Capacitor C_C may be required for stability if the

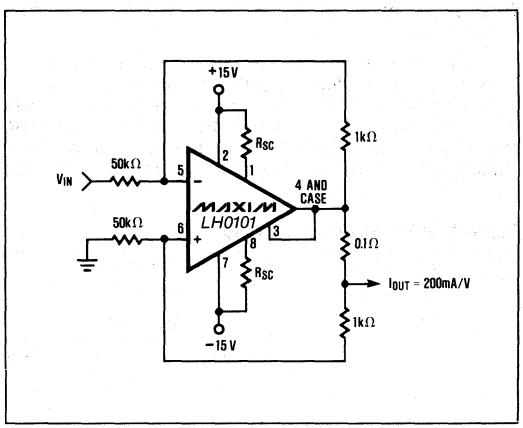


Figure 9. High Current Source/Sink.

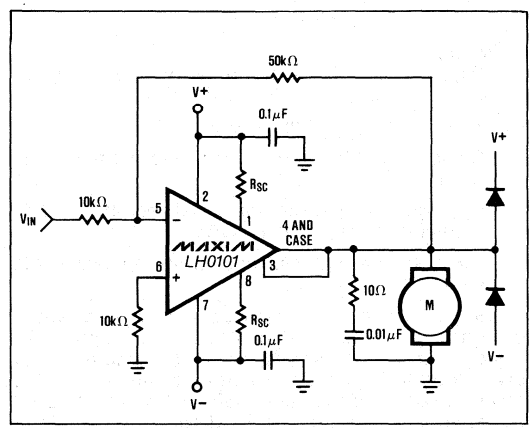


Figure 10. Servo Motor Amplifier.

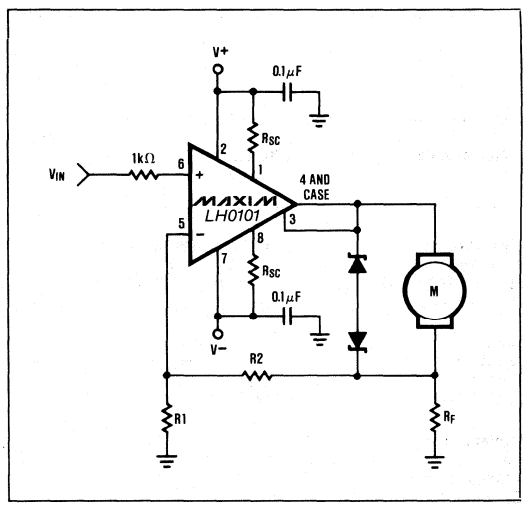


Figure 11. Torque Feedback Servo Motor Amplifier.

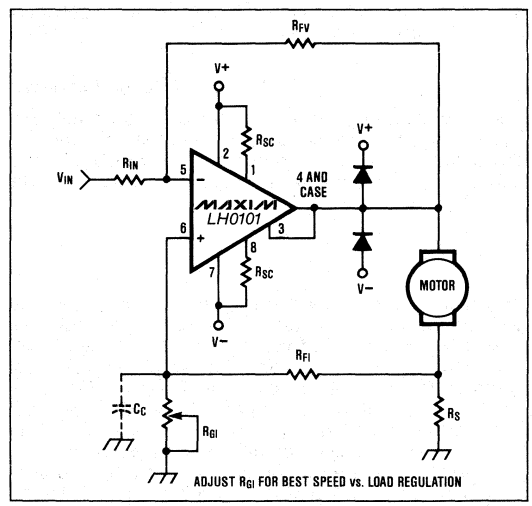


Figure 12. Constant Speed Motor Driver.

positive feedback is such that the motor speed increases with increased torque load.

These circuits will either source or sink current, depending on the polarity of the input voltage, and can drive DC motors in both directions.

Low Distortion Audio Amplifier

The hermetically packaged LH0101 is well suited for use as an audio amplifier for severe environments. Figure 13 shows two LH0101s used in a bridge audio power amplifier. The bridge configuration doubles the voltage that can be delivered to the load, in this case delivering 50V peak-peak to an 8Ω speaker. This means that a 40 Watts RMS can be delivered to the 8Ω speaker while using only ±18V power supplies. The harmonic distortion is a respectable 0.1%, which should suffice for all but the most demanding applications.

CRT Yoke Driver Circuit

The 300kHz power bandwidth and 5 Amp peak output current capability of the LH0101 make it well suited for CRT yoke driver circuits such as Figure 14. This circuit is basically a constant current source/sink with a transconductance of 435 mA/V (reciprocal of the 2.3Ω current sense resistor). The resistor R_{DAMP} lowers the Q of the inductive yoke; the value of R_{DAMP} is chosen empirically for the least distortion at the operating frequency. At low frequencies R_{DAMP} is not required.

DC Servomotor Phase Locked Loop

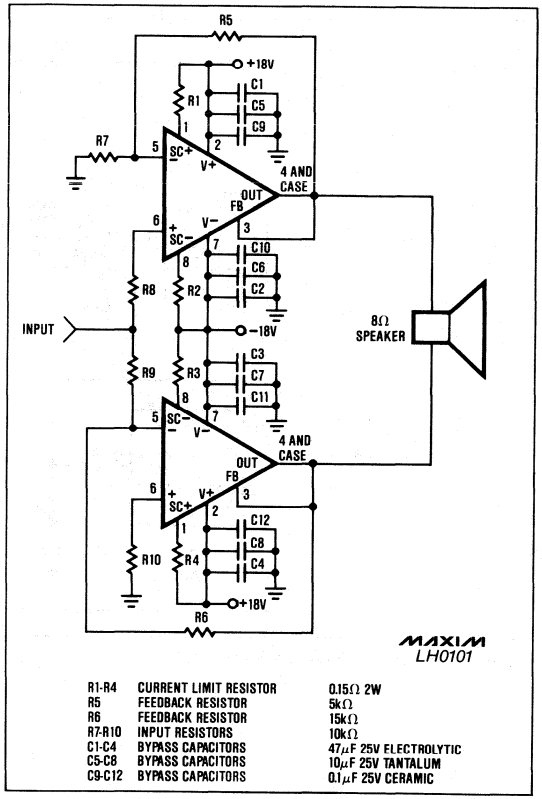
In the circuit of Figure 15, the shaft encoder produces 600 pulses per revolution. These pulses are compared to a reference frequency by the digital phase comparator of the CD4046. The output of the phase comparator passes through a low pass filter and drives the input of the LH0101. The LH0101 amplifies this signal and drives the DC servomotor. The phase-frequency comparator of the CD4046 increases or decreases the input voltage to the LH0101 until the shaft encoder output is the same frequency as the reference input.

$$\text{Motor Speed (in RPM)} = \frac{F_{IN} \times 60}{N}$$

Where F_{IN} is the frequency of the reference input and N is the number of shaft encoder pulses per revolution.

A single-pulse-per-revolution speed pickup can be used in place of the shaft encoder, but the PLL low pass filter time constant must be greatly increased.

Note that this circuit is similar to a standard phase locked loop except that the LH0101, the motor, and the shaft encoder replace the internal VCO of the CD4046. Unlike the VCO of the CD4046, the motor adds another pole to the system response and loop stability must be carefully analyzed, particularly if the motor and its load has significant inertia. As with most feedback systems, the loop will be stable when there is only one dominant pole. The loop filter time constant should preferably be at least 1 decade higher or lower than the constant of the motor and its load.



R1-R4	CURRENT LIMIT RESISTOR	0.15Ω 2W
R5	FEEDBACK RESISTOR	5kΩ
R6	FEEDBACK RESISTOR	15kΩ
R7-R10	INPUT RESISTORS	10kΩ
C1-C4	BYPASS CAPACITORS	47μF 25V ELECTROLYTIC
C5-C8	BYPASS CAPACITORS	10μF 25V TANTALUM
C9-C12	BYPASS CAPACITORS	0.1μF 25V CERAMIC

Figure 13. LH0101 Bridge Audio Power Amplifier.

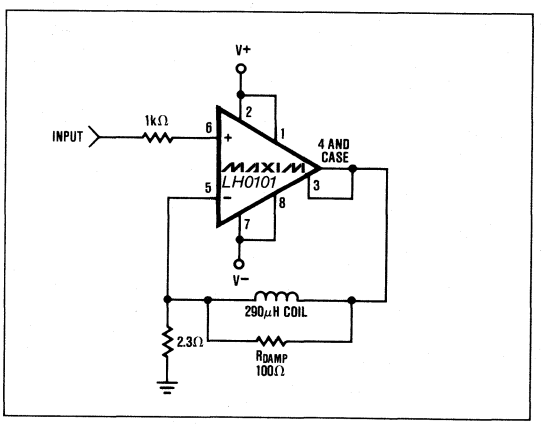


Figure 14. CRT Yoke Driver Circuit.

Power Operational Amplifier

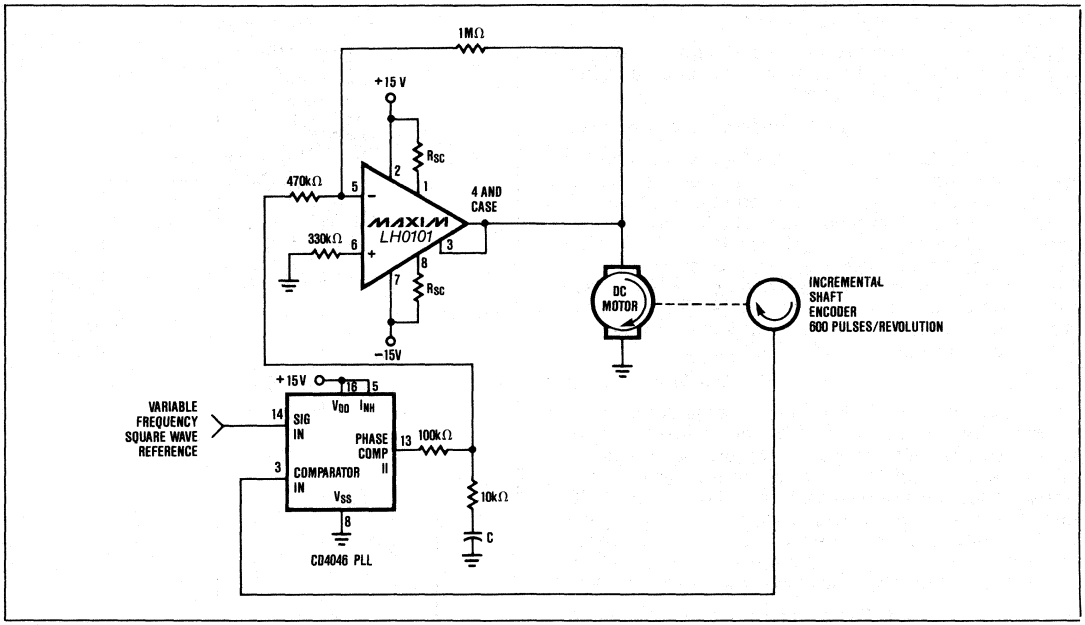


Figure 15. Servomotor Phase Locked Loop.

MAXIM

Precision Operational Amplifier

General Description

The LT1001 offers significant specification improvements over earlier precision operational amplifiers. Particular attention has been paid to the optimization of key parameters such as input offset voltage, common-mode rejection, and power supply rejection. In addition, the high-performance LT1001C commercial temperature device provides considerable cost savings when compared to equivalent grades of competing precision amplifiers.

The input offset voltage of all units is less than 60μV, allowing the premium Military device, the LT1001AM, to be specified at 15μV max. Power dissipation is close to half that of the industry-standard OP-07 precision op amp without sacrificing noise or speed performance. A useful by-product of lower dissipation is decreased warm-up drift.

Applications

Thermocouple Amplifiers

Low-Level Signal Processing

Strain Gauge Amplifiers

High-Accuracy Data Acquisition

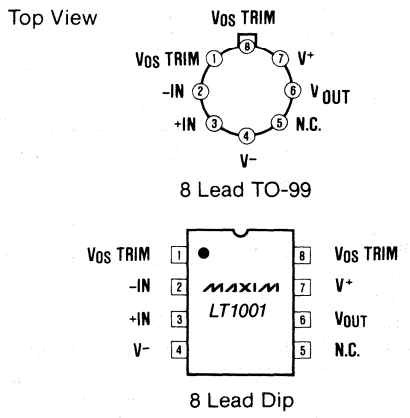
Features

- **Guaranteed Low Offset Voltage**
  - LT1001AM ..... 15μV max
  - LT1001C ..... 60μV max
- **Guaranteed Low Drift**
  - LT1001AM ..... 0.6μV/°C max
  - LT1001C ..... 1.0μV/°C max
- **Guaranteed Low Bias Current**
  - LT1001AM ..... 2nA max
  - LT1001C ..... 4nA max
- **Guaranteed CMRR**
  - LT1001AM ..... 114dB min
  - LT1001C ..... 110dB min
- **Guaranteed PSRR**
  - LT1001AM ..... 110dB min
  - LT1001C ..... 106dB min
- **Low Power Dissipation**
  - LT1001AM ..... 75mW max
  - LT1001C ..... 80mW max
- **Low Noise: 0.3μV_{p-p}**

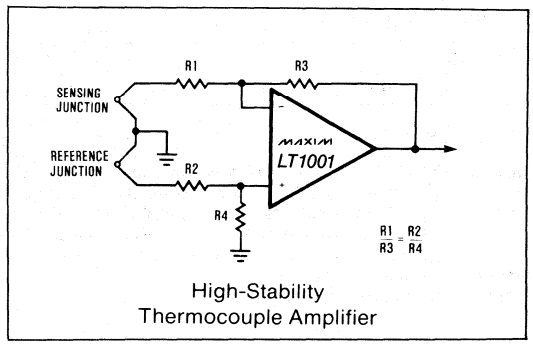
Ordering Information

PART	TEMP. RANGE	PACKAGE*
LT1001AMH	-55°C to +125°C	8 Lead TO-99
LT1001MH	-55°C to +125°C	8 Lead TO-99
LT1001ACH	0°C to +70°C	8 Lead TO-99
LT1001CH	0°C to +70°C	8 Lead TO-99
LT1001ACN8	0°C to +70°C	8 Lead Plastic Dip
LT1001CN8	0°C to +70°C	8 Lead Plastic Dip
LT1001AMJ8	-55°C to +125°C	8 Lead Hermetic Dip
LT1001MJ8	-55°C to +125°C	8 Lead Hermetic Dip
LT1001ACJ8	0°C to +70°C	8 Lead Hermetic Dip
LT1001CJ8	0°C to +70°C	8 Lead Hermetic Dip
LT1001ACS8	0°C to +70°C	8 Lead Small Outline
LT1001CS8	0°C to +70°C	8 Lead Small Outline

Pin Configuration



Typical Operating Circuit



Precision Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... ±22V
Internal Power Dissipation 500mW
TO-99(H) — derate at 7.1mW/°C above +80°C
Hermetic Dip(J) — derate at 6.7mW/°C above +75°C
Plastic Dip(P) — derate at 5.6mW/°C above +36°C
Small Outline(S) — derate at 5mW/°C above +55°C
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
LT1001AMH, LT1001AMJ8,
LT1001MH, and LT1001MJ8 ..... -55°C to +125°C
All Other Parts ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Duration of Output Short Circuit ..... Indefinite
Junction Temperature (T_J) ..... -65°C to +160°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1001AM LT1001AC			LT1001M LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 2) LT1001AM LT1001AC		7 10	15 25		18	60	μV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 3)		0.2	1.0		0.3	1.5	μV/ Month
Input Offset Current	I_{OS}			0.3	2.0		0.4	3.8	nA
Input Bias Current	I_B			±0.5	±2.0		±0.7	±4.0	nA
Input Noise Voltage	$e_{N\ P-P}$	0.1Hz to 10Hz (Note 4)		0.3	0.6		0.3	0.6	μV_{p-p}
Input Noise Voltage Density	e_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.0 9.8	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Resistance Differential-Mode	R_{IN}	(Note 5)	30	100		15	80		MΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	114	126		110	126		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	110	123		106	123		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±12V $R_L \geq 1k\Omega$, V_O = ±10V	450 300	800 500		400 250	800 500		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13.0 ±12.0	±14.0 ±13.5		±13.0 ±12.0	±14.0 ±13.5		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/μS
Closed-Loop Bandwidth	BW	A_{VCL} = +1V (Note 4)	0.4	0.8		0.4	0.8		MHz
Power Consumption	P_D	V_S = ±15V, No Load V_S = ±3V, No Load		46 4	75 6		48 4	80 8	mW

Note 2: LT1001A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.

Note 3: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV. Parameter is sample tested.

Note 4: Sample tested.

Note 5: Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1001AM			LT1001M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 6)		30	60		45	160	µV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}			0.2	0.6		0.3	1.0	µV/°C
Input Offset Current	I_{OS}			0.8	4.0		1.2	7.6	nA
Input Bias Current	I_B			±1.0	±4.0		±1.5	±8.0	nA
Input Voltage Range	IVR		±13	±14		±13	14		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	122		106	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	104	117		100	117		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	300	700		200	700		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.5	±13.5		±12.5	±13.5		V
Power Dissipation	P_D	No Load		55	90		60	100	mW

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	LT1001AC			LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 6)		20	60		30	110	µV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}			0.2	0.6		0.3	1.0	µV/°C
Input Offset Current	I_{OS}			0.5	3.5		0.6	5.3	nA
Input Bias Current	I_B			±0.7	±3.5		±1.0	±5.5	nA
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	124		106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	106	120		103	120		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	350	750		250	750		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.5	±13.8		±12.5	±13.8		V
Power Dissipation	P_D	No Load		50	85		55	90	mW

Note 6: LT1001A grade Offset Voltage is measured one minute after application of power. For all other grades V_{OS} is measured 0.5 seconds after power on.

Precision Operational Amplifier

Applications Information

The LT1001 series devices are pin-compatible with the OP-07, OP-05, 725, 108A or 101A amplifiers. The LT1001 amplifiers can be used to upgrade older designs using these devices with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided the nulling circuitry is removed.

The LT1001 is specified over a wide supply voltage range from ±3V to ±18V. Operation with lower supplies is possible down to ±1.2V (two Ni-Cad batteries), however, at this level the device is stable only in closed-loop gains of +2 and above (or inverting gain of one or higher). Unless proper care is exercised, thermocouple effects, caused by temperature gradients across dissimilar metals at the input terminals connections, can exceed the inherent offset voltage drift of the amplifier. Air currents over the device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Offset Voltage Adjustment

The input offset voltage of the LT1001, and its temperature drift, are minimized by zener-zap trimming at the wafer level. If further nulling of V_{OS} is required, this can be performed using a 10k or 20k potentiometer with no degradation of V_{OS} drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300)\mu V/°C$, e.g. if V_{OS} is adjusted to 300uV, the change in drift will be 1uV/°C. The adjustment range with a 10k or 20k potentiometer is approximately ±2.5mV. If less adjustment range is needed, the sensitivity and resolution of the offset nulling can be improved by using a potentiometer of lower ohmic value in conjunction with fixed resistors.

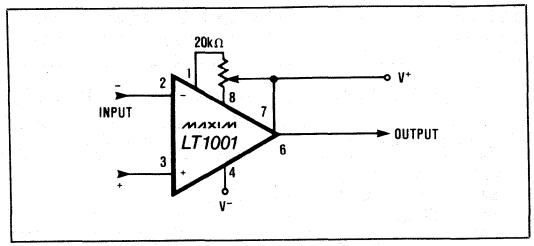
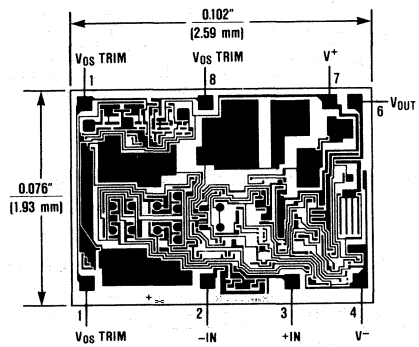


Figure 1. Optional Offset Nulling Circuit.

Chip Topography



Note: Substrate is connected to V-.

MAXIM

Super Low Offset Voltage Operational Amplifier

General Description

The OP07 is a precision operational amplifier with very low input offset voltage (10μV typ., 25μV max. for the OP07A), input offset drift of 0.2μV/°C and low input bias current of 0.7nA. The wide input common mode range of ±14V combined with high CMRR of 110dB minimum (OP07A), plus high input impedance and high open-loop gain make these devices particularly useful for high-gain instrumentation applications.

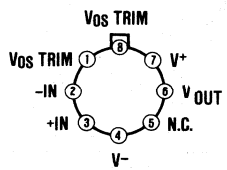
The excellent linearity and gain accuracy are maintained at high open-loop gains, over both time and temperature. The OP07 has become an industry standard and Maxim's reliability and quality are added advantages.

Applications

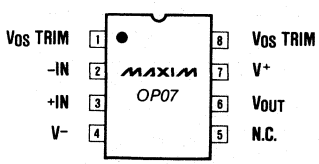
Precision Amplifiers
Thermocouple Amplifiers
Low Level Signal Processing
Medical Instrumentation
Strain Gauge Amplifiers
High Accuracy Data Acquisition

Pin Configuration

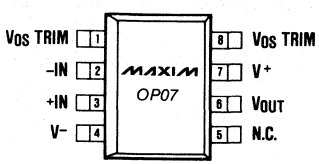
Top View



8 Lead TO-99



8 Lead Dip



8 Lead Small Outline

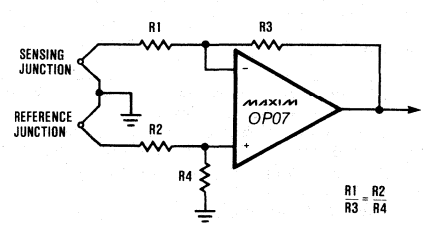
Features

- **Ultra Low Offset Voltage: 10μV**
- **Ultra Low Offset Voltage Drift: 0.2μV/°C**
- **Ultra Stable vs. Time: 0.2μV/Month**
- **Ultra Low Noise: 0.35μV_{p-p}**
- **Wide Supply Voltage: ±3V to ±18V**
- **High Common Mode Input: ±14V**
- **No External Components Required**
- **Fits AD510, 725, 108A/308A, 741 Sockets**

Ordering Information

PART	TEMP. RANGE	PACKAGE
OP07AJ	-55°C to +125°C	TO-99
OP07J	-55°C to +125°C	TO-99
OP07EJ	0°C to +70°C	TO-99
OP07CJ	0°C to +70°C	TO-99
OP07DJ	0°C to +70°C	TO-99
OP07EP	0°C to +70°C	8 Lead Plastic Dip
OP07CP	0°C to +70°C	8 Lead Plastic Dip
OP07DP	0°C to +70°C	8 Lead Plastic Dip
OP07AZ	-55°C to +125°C	8 Lead Hermetic Dip
OP07Z	-55°C to +125°C	8 Lead Hermetic Dip
OP07EZ	0°C to +70°C	8 Lead Hermetic Dip
OP07CZ	0°C to +70°C	8 Lead Hermetic Dip
OP07ECSA	0°C to +70°C	8 Lead Small Outline
OP07CCSA	0°C to +70°C	8 Lead Small Outline
OP07DCSA	0°C to +70°C	8 Lead Small Outline
OP07D/D	0°C to +70°C	Dice

Typical Operating Circuit



High-Stability
Thermocouple Amplifier

Super Low Offset Voltage Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... ±22V
Internal Power Dissipation 500mW
- TO-99(J) — derate at 7.1mW/°C above +80°C
- Hermetic Dip(Z) — derate at 6.7mW/°C above +75°C
- Plastic Dip(P) — derate at 5.6mW/°C above +36°C
- Small Outline — derate at 5mW/°C above +55°C

Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
- OP07AJ, OP07AZ, OP07J and OP07Z ..... -55°C to +125°C
- All Other Parts ..... 0°C to +70°C

Lead Temperature (Soldering, 10 sec) ..... +300°C
Duration of Output Short Circuit ..... Indefinite
Junction Temperature (T_J) ..... -65°C to +160°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 2)		10	25		30	75	µV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 3)		0.2	1.0		0.2	1.0	µV/ Month
Input Offset Current	I_{OS}			0.3	2.0		0.4	2.8	nA
Input Bias Current	I_B			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage	$e_{N\,P-P}$	0.1Hz to 10Hz (Note 4)		0.35	0.6		0.35	0.6	μV_{P-P}
Input Noise Voltage Density	e_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	$I_{N\,P-P}$	0.1Hz to 10Hz (Note 4)		14	30		14	30	pA_{P-P}
Input Noise Current Density	I_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance Differential-Mode	R_{IN}	(Note 5)	30	80		20	60		MΩ
Input Resistance Common-Mode	R_{INCM}			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	126		110	126		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		4	10		4	10	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 5)	300 150	500 400		200 150	500 400		V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V

Note 2: OP07A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
Note 3: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV. Parameter is sample tested.
Note 4: Sample tested.
Note 5: Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 6)	0.1	0.3		0.1	0.3		V/μS
Closed-Loop Bandwidth	BW	A_{VCL} = +1V (Note 6)	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0V, I_O = 0		60			60		Ω
Power Consumption	P_D	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		75 4	120 6	mW
Offset Adjustment Range		R_P = 20kΩ		±4			±4		mV

Note 6: Sample tested.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 7)		25	60		60	200	μV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}	(Note 8)		0.2	0.6		0.3	1.3	μV/°C
Input Offset Current	I_{OS}			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 8)		5	25		8	50	pA/°C
Input Bias Current	I_B			±1.0	±4.0		±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 8)		8	25		13	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	106	123		106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		5	20		5	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	200	400		150	400		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6		±12.0	±12.6		V

Note 7: OP07A grade Offset Voltage is measured one minute after application of power. For all other grades V_{OS} is measured 0.5 seconds after power on.

Note 8: Sample tested.

Super Low Offset Voltage Operational Amplifier

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07E			OP07C			OP07D			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	(Note 1)		30	75		60	150		60	150	µV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 2)		0.3	1.5		0.4	2.0		0.5	3.0	µV/ Month
Input Offset Current	I_{OS}			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current	I_B			±1.2	±4.0		±1.8	±7.0		±2.0	±12.0	nA
Input Noise Voltage	$e_{N\ P-P}$	0.1Hz to 10Hz (Note 3)		0.35	0.6		0.38	0.65		0.38	0.65	μV_{P-P}
Input Noise Voltage Density	e_N	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5		10.5 10.3 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
Input Noise Current	$I_{N\ P-P}$	0.1Hz to 10Hz (Note 3)		14	30		15	35		15	35	pA_{P-P}
Input Noise Current Density	I_N	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
Input Resistance Differential-Mode	R_{IN}	(Note 4)	15	50		8	33		7	31		MΩ
Input Resistance Common-Mode	R_{INCM}			160			120			120		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		5	20		7	32		7	32	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 5)	200 150	500 400		120 100	400 400		120	400 400		V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5	±13.0 ±12.8 ±12.0		V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3		0.1	0.3		0.1	0.3		V/µS
Closed-Loop Bandwidth	BW	A_{VCL} = +1V (Note 3)	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0V, I_O = 0		60			60			60		Ω
Power Consumption	Pd	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		80 4	150 8		80 4	150 8	mW
Offset Adjustment Range		R_P = 20kΩ		±4			±4			±4		mV

Note 1: Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Note 2. Long-Term Input Offset Stability refers to the average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation.

Note 3. Sample tested.

Note 4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07E			OP07C			OP07D			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	(Note 5)		45	130		85	250		85	250	μV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}	(Note 6)		0.3	1.3		0.4	1.8		0.7	2.5	μV/°C
Input Offset Current	I_{OS}			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 6)		8	35		12	50		12	50	pA/°C
Input Bias Current	I_B			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 6)		13	35		18	50		18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		7	32		10	51		10	51	μV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	180	400		100	400		100	400		V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±12.6		±11.0	±12.6		±11.0	±12.6		V

Note 5: Input Offset Voltage is measured 0.5 seconds after application of power.
Note 6: Sample tested.

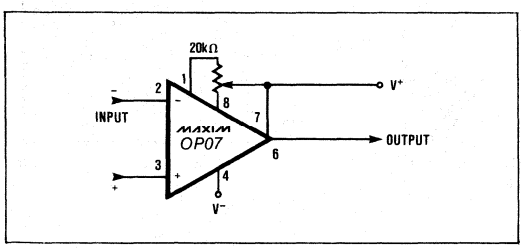


Figure 1. Optional Offset Nulling Circuit.

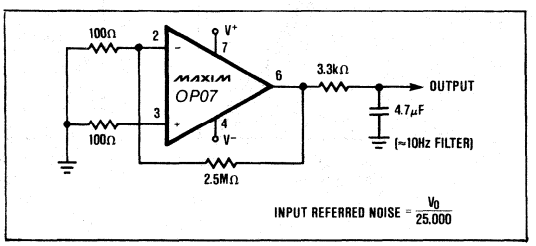
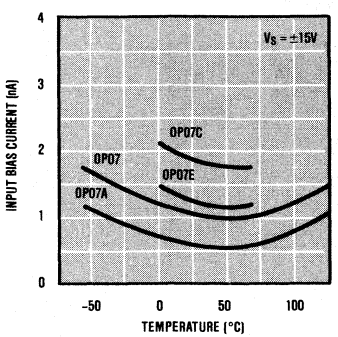
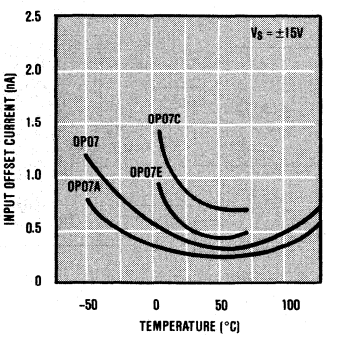


Figure 2. Low Frequency Noise Test Circuit.

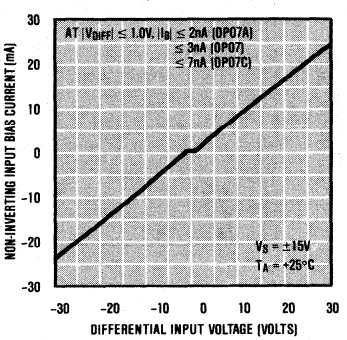
INPUT BIAS CURRENT vs. TEMPERATURE



INPUT OFFSET CURRENT vs. TEMPERATURE

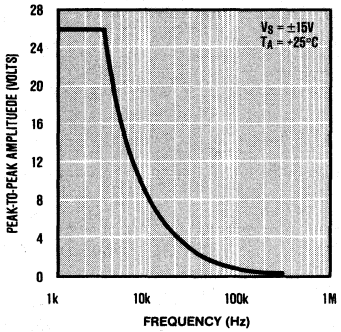


INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE

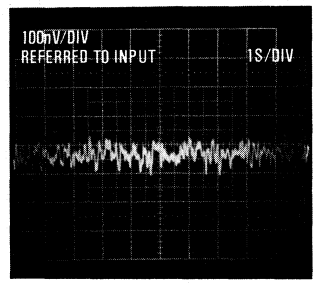


Super Low Offset Voltage Operational Amplifier

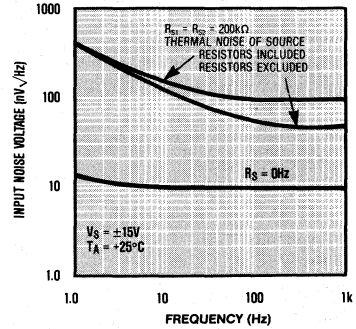
MAXIMUM OUTPUT SWING vs. FREQUENCY



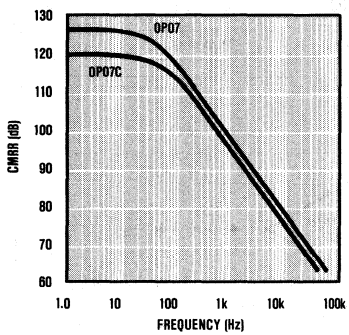
LOW FREQUENCY NOISE



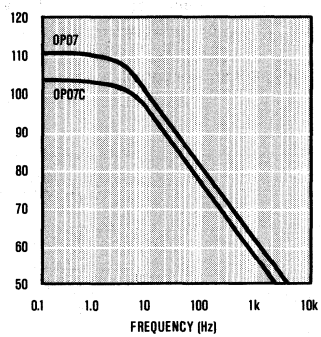
TOTAL INPUT NOISE VOLTAGE vs. FREQUENCY



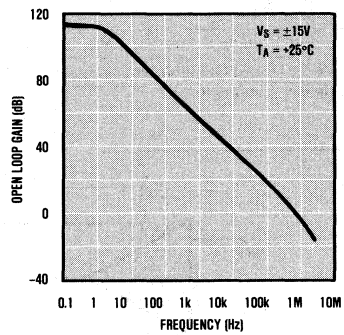
CMRR vs. FREQUENCY



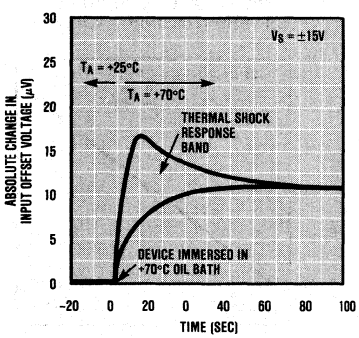
PSRR vs. FREQUENCY



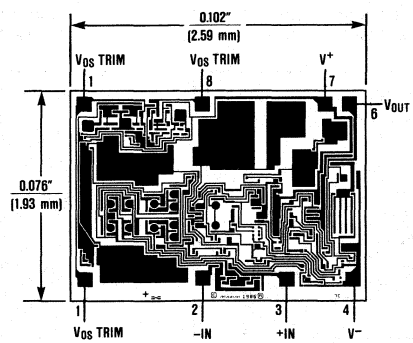
OPEN LOOP FREQUENCY RESPONSE



OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



Chip Topography



MAXIM

Programmable Gain Amplifier

General Description

The PGA100 is a precision, digitally-programmable gain amplifier (PGA) combined with an 8 channel ±35V protected input multiplexer. The user can select any one of eight analog input channels to be amplified by one of the eight noninverting binarily weighted gain steps from 1 to 128. The digital gain and channel select are internally latched for easy microprocessor interface. The fast 5μsec settling time allows the PGA100 to be used in rapid channel scanning data acquisition systems.

Applications

Data Acquisition Amplifier

Software Error Correction

Digitally-Controlled Autoranging

Test Equipment

Remote Instrumentation System

System Dynamic Range and Resolution Improvement

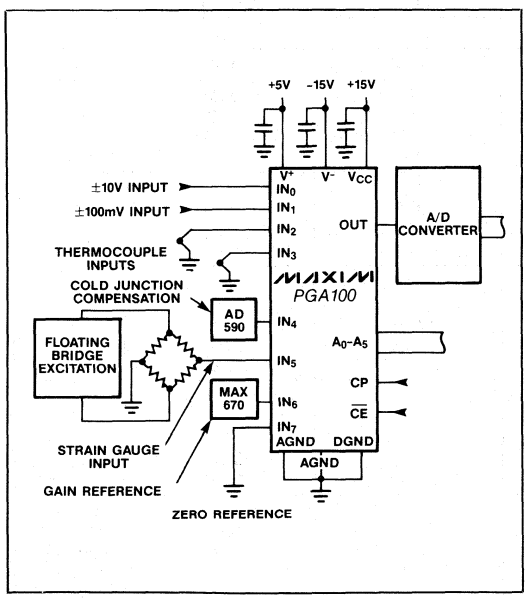
Features

- **High Gain Accuracy ±0.02% max (B Grade)**
- **Input protection, ±20V above ±15V supplies**
- **High Input Impedance: $10^{11}\Omega$**
- **Fast Settling, 5μsec to 0.01%**
- **Low Channel to Channel Crosstalk, -90dB**
- **Low nonlinearity ±0.005% max (B Grade)**
- **8 analog input channels**
- **8 Selectable Gains, 1, 2, 4, 8, 16, 32, 64, 128 V/V**
- **Fully microprocessor-compatible**

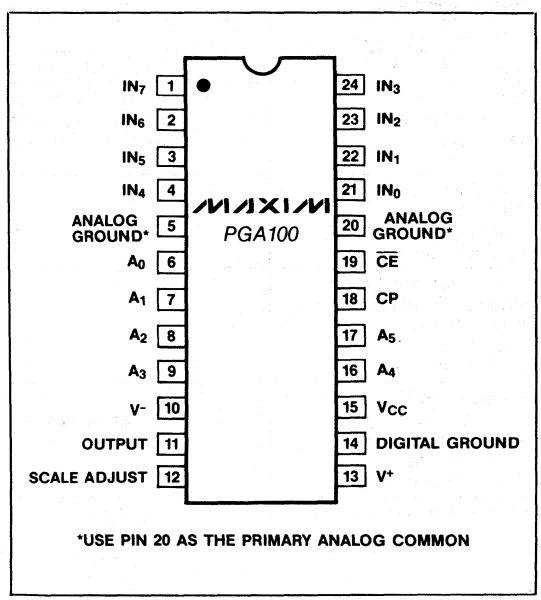
Ordering Information

PART	TEMP. RANGE	PACKAGE
PGA100AG	-25°C to +85°C	24 Pin Ceramic Side Braze
PGA100BG	-25°C to +85°C	24 Pin Ceramic Side Braze

Typical Operating Circuit



Pin Configuration



*USE PIN 20 AS THE PRIMARY ANALOG COMMON

Programmable Gain Amplifier

ABSOLUTE MAXIMUM RATINGS

Analog Supply (V^+, V^-) ..... ±18V
Digital Supply (V_{CC}) ..... +7V
Input Voltage Range Analog ..... V^--20V≤V_{IN}≤V^++20V
Input Voltage Range Digital ..... -0.3≤V_{IN}≤+7V
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering 10 seconds) ..... 300°C
Output Short-Circuit Duration .... Continuous to Ground
Junction Temperature ..... 175°C
Power Dissipation 1W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V^+ = +15V, V^- = -15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	PGA100AG			PGA100BG			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain Accuracy (Note 1) vs Temperature (Note 2) vs Time		G = 1 to 128, I_O = 1mA -25°C ≤ T_A ≤ +85°C		±.01 ±5 ±.001	±.05 ±10		±.005 ±5 ±.001	±.02 ±10	% ppm/°C %/1000 Hrs.
Nonlinearity (Note 3) vs Temperature (Note 2) vs Time		G = 1 to 128, I_O = 1mA -25°C ≤ T_A ≤ +85°C		±.004 ±2 ±.001	±.01 ±5		±.002 ±2 ±.001	±.005 ±5	% of FS ppm/°C %/1000 Hrs.
Rated Output Voltage		I_{OUT} = ±2mA	±10			±10			V
Rated Output Current		V_{OUT} = ±10V	±2			±2			mA
Output Resistance		Gain ≤ 128		0.05			0.05		Ω
Short Circuit Current				±15			±15		mA
Capacitive Load		Phase margin ≥ 25°		1000			1000		pF
Offset Voltage vs Temperature vs Supply vs Time		T_A = 25°C -25°C ≤ T_A ≤ +85°C 8V ≤ |V| ≤ 18V		±0.1 ±6 ±10 ±15	±1 ±80		±.05 ±6 ±10 ±15	±.5 ±80	mV µV/°C µV/V µV/month
Input Bias Current "Off" Channel "On" Channel vs Temperature				 ±10 ±0.1 Note 4			 ±10 ±0.1 Note 4	 1	 pA nA
Input Difference Current, between Channels: "Off" Channel "On" Channel vs Temperature				 ±20 ±0.2 Note 4			 ±20 ±0.2 Note 4	 ±2	 pA nA
Analog Input Characteristics: Input Voltage Range Input Impedance "Off" Channel "On" Channel		Linear Operation		 ±10 10^{12}||15 10^{11}||25			 ±10 10^{12}||15 10^{11}||25		 V Ω||pF Ω||pF
Input Voltage Noise Density		f_O = 1Hz f_O = 10Hz f_O = 100Hz f_O = 1kHz f_O = 10kHz f_O = 100kHz		200 60 25 18 18 18			200 60 25 18 18 18		nV/√Hz nV/√Hz nV/√Hz nV/√Hz nV/√Hz nV/√Hz

ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5V, V^+ = +15V, V^- = -15V, T_A = +25°C, unless otherwise noted.)

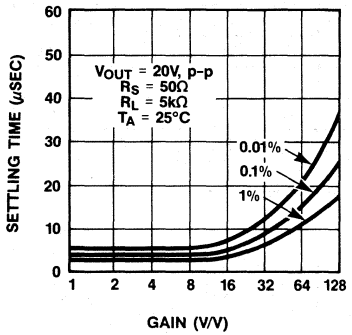
PARAMETER	SYMBOL	CONDITIONS	PGA100AG			PGA100BG			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Noise		f_{BW} = 0.1Hz to 10Hz		2.6			2.6		μV_{p-p}
Current Noise Density		f_O = 0.1Hz thru 8kHz		6			6		$fA/\sqrt{Hz}$
Current Noise		f_{BW} = 0.1Hz to 10Hz		115			115		fA_{p-p}
Gain Bandwidth Product				5			5		MHz
Full Power Bandwidth		G=1, V_O=20V_{p-p}, R_L=5kΩ		220		80	220		kHz
Slew Rate		G=1, V_O=±10V, R_L=5kΩ		14		5	14		V/μsec
Settling Time (Note 5) to 1% to 0.1% to 0.01%		G=1, V_O=±10V, R_L=5kΩ		 2.5 3 5			 2.5 3 5		 μsec μsec μsec
Rise Time		10% to 90%, 100mV		70			70		nsec
Phase Margin		G = 1, R_L = 5kΩ		60			60		°
Overload Recovery (Note 6)		G = 1, 50% overdrive		2			2		μsec
Crosstalk, RTI (Note 5, 7)		20V_{p-p}, 1kHz sine, R_S = 1kΩ on all OFF channels		±0.003			±0.003		%
Digital Inputs (Note 8): Input "LOW" Threshold					0.8			0.8	V
Input "HIGH" Threshold			2.0			2.0			V
Clock Pulse Width (low)	t_{WL}		20			20			nsec
Setup Time (CP to data)	t_{S1}		20			20			nsec
Hold Time (CP to data)	t_{H1}		5			5			nsec
Setup Time ($\overline{CE}$ to CP)	t_{S2}		25			25			nsec
Hold Time ($\overline{CE}$ to CP)	t_{H2}		5			5			nsec
V^+/V^- Range		Derated performance	±8		±18	±8		±18	V
V^+ Current				20	27		15	20	mA
V^- Current				10	16		7.5	12	mA
V_{CC} Range		Full performance	4.75		5.25	4.75		5.25	V
V_{CC} Current		V_{CC} = +5.25V		15	27		15	27	mA

Note 1: Inaccuracy is the percent error between the actual and ideal gain selected measured after temperature stabilization. It may be externally adjusted to zero.
Note 2: Parameter is untested and is not guaranteed.
Note 3: Nonlinearity is the maximum peak deviation from a "best straight line" (curve fitting on input-output graph) expressed as a percent of the full scale peak-to-peak output. Gain constant, V_{OUT} ranges from -10V to +10V.
Note 4: Doubles approximately every 10°C.
Note 5: See Typical Performance Curves.
Note 6: Time required for the output to return from saturation to linear operation following the removal of an input overdrive signal.
Note 7: Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is express as a percent of the signal applied to all OFF channels.
Note 8: All digital inputs are one 74LSTTL load. Timing specifications not tested; guaranteed by design.

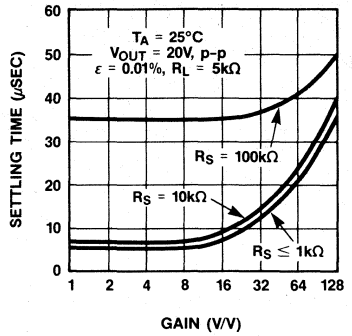
Programmable Gain Amplifier

Typical Performance Curves

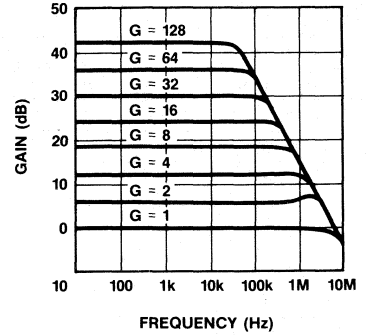
SETTLING TIME vs GAIN



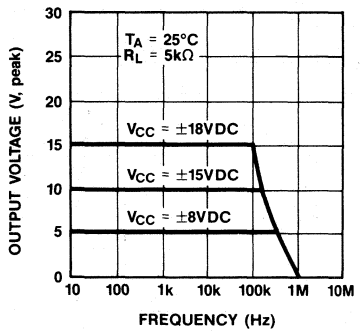
SETTLING TIME vs GAIN AND SOURCE RESISTANCE



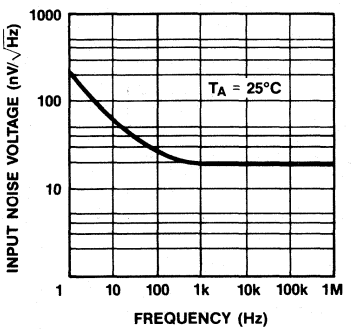
SMALL SIGNAL FREQUENCY RESPONSE



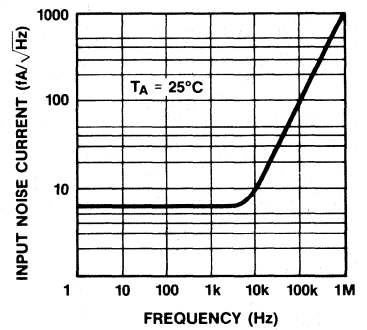
LARGE SIGNAL OUTPUT VOLTAGE vs FREQUENCY



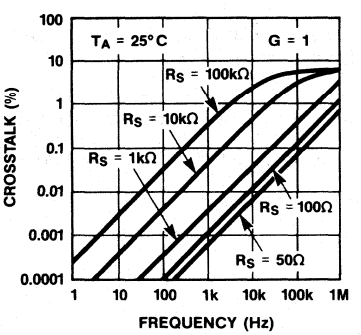
INPUT NOISE VOLTAGE vs FREQUENCY



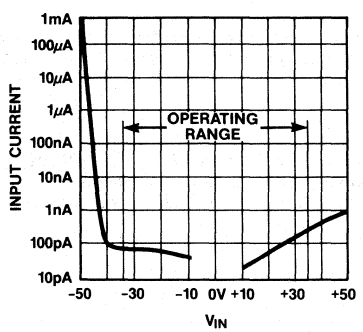
INPUT NOISE CURRENT vs FREQUENCY



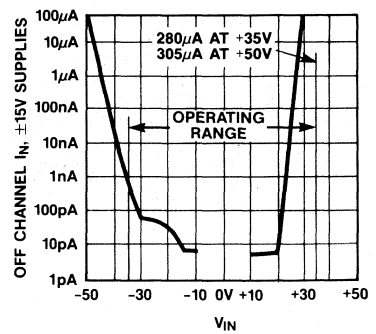
CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY



OFF CHANNEL LEAKAGE CURRENT vs INPUT VOLTAGE WITH ±15V SUPPLIES



INPUT LEAKAGE vs INPUT VOLTAGE WITH $V^+ = V^- = 0V$



Description

The PGA100 consists of an 8 channel ±35V protected input multiplexer followed by a non-inverting operational amplifier whose gain may be set using another multiplexer selecting outputs on a resistive feedback network (see Figure 1). Both multiplexers are fed from a TTL 6 bit latch similar to a 74LS378. The digital inputs are latched by the positive transition of the clock pulse, pin 18, when the clock enable, pin 19, is low. The relative set up and hold times specified in the Electrical Specifications are shown in Figure 3.

Layout Considerations

The PGA100 has dual analog ground pins and a separate digital ground. These must be connected at some single point in the system. The resistance seen by the analog ground is critical and must be kept below 5 milliohms to meet the accuracy specifications. Pin 20 is the primary analog ground, so should be used as the system reference point.

Input Overvoltage Protection

The PGA100 can withstand input overvoltage of up to ±35V, or 20V greater than ±15V analog supply voltages. In normal operation, this allows inputs up to plus and minus 35V. Even with the analog supplies powered down, the inputs may still be stimulated up to plus and minus 20V without damage. This degree of protection is achieved with a Maxim proprietary circuit/process as used in the MAX358 multiplexer. Note that overdriven inputs go to a relatively high impedance state that minimizes input loading and power dissipation.

Optional Gain Scale/Adjust

Ordinarily, no connection is made to pin 12 and this results in the standard gains specified in Table 1. A slight adjustment in the gains other than unity may be made by connecting a resistor or potentiometer between pin 12 and the output and/or ground. This will allow any one gain to be adjusted exactly, but at the expense of the others. The pin 12 connection has no effect on the unity gain accuracy.

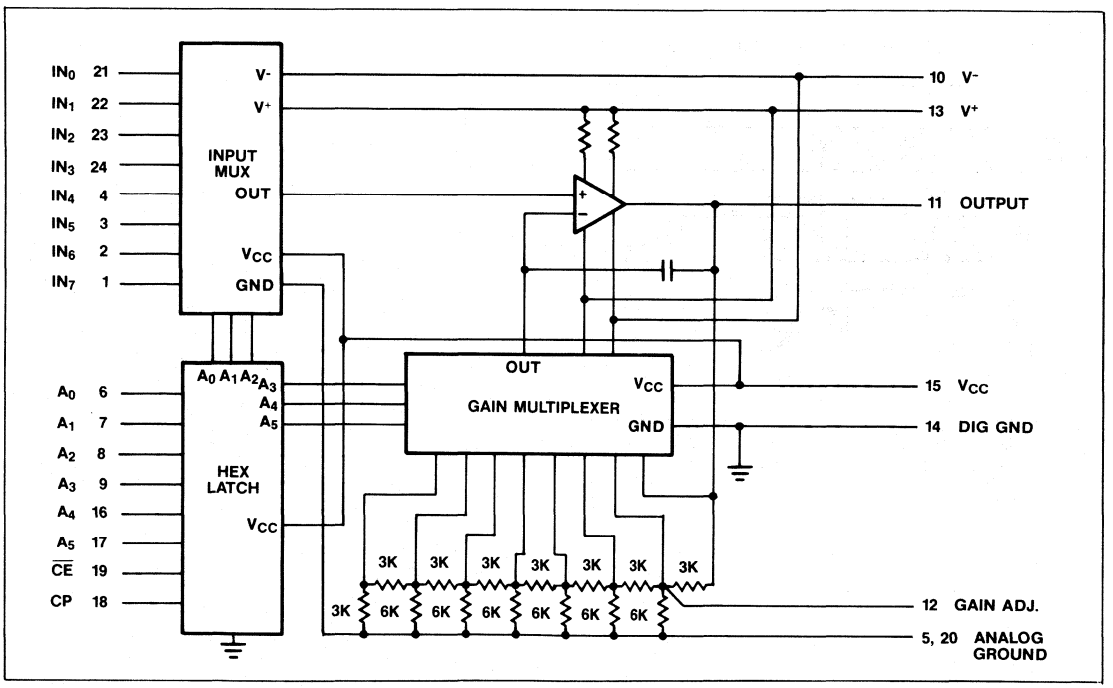


Figure 1. Equivalent Internal Schematic

Programmable Gain Amplifier

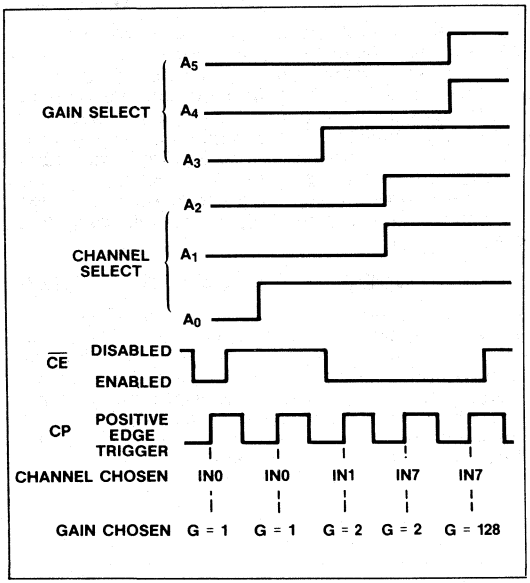


Figure 2. Timing Diagram for Selected Addresses

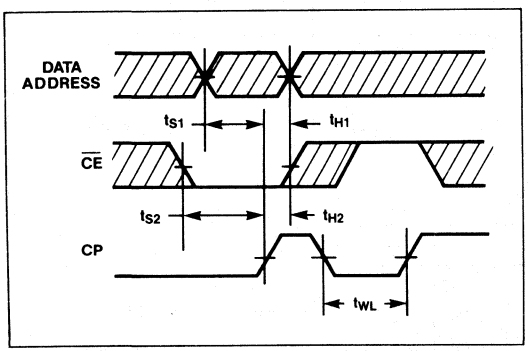


Figure 3. Data Address and Clock Enable Setup and Hold Times

Table 1: Gain and Channel Select Truth Table

Channel A0	A1	A2	Gain A3	A4	A5	
0	0	0				Channel 0
1	0	0				Channel 1
0	1	0				Channel 2
1	1	0				Channel 3
0	0	1				Channel 4
1	0	1				Channel 5
0	1	1				Channel 6
1	1	1				Channel 7
			0	0	0	Gain = 1
			1	0	0	Gain = 2
			0	1	0	Gain = 4
			1	1	0	Gain = 8
			0	0	1	Gain = 16
			1	0	1	Gain = 32
			0	1	1	Gain = 64
			1	1	1	Gain = 128

0 = Low
1 = High

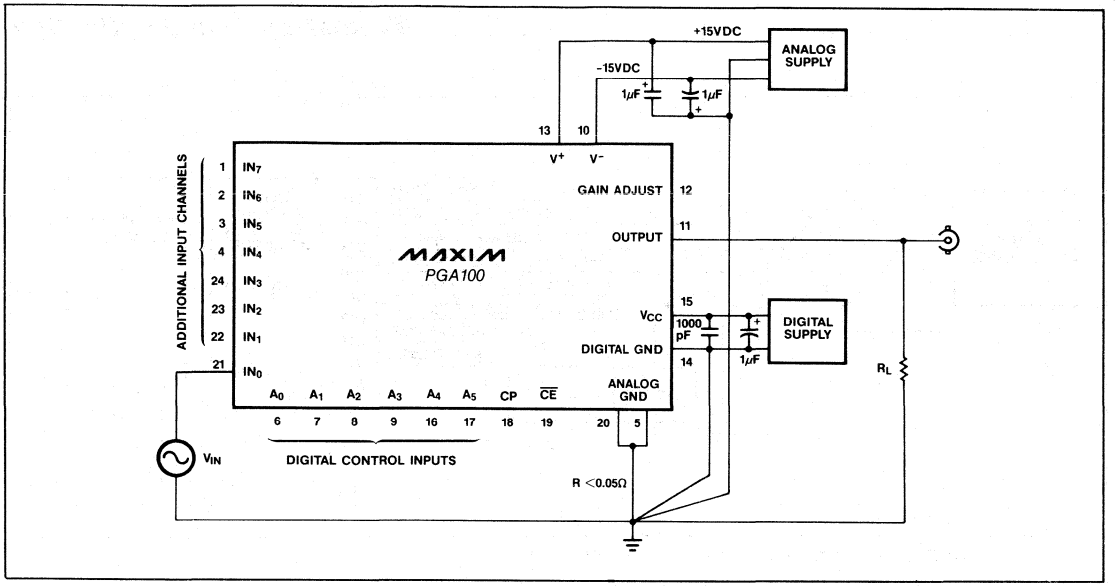


Figure 4. Basic Power Supply, Ground, and Signal Connections.

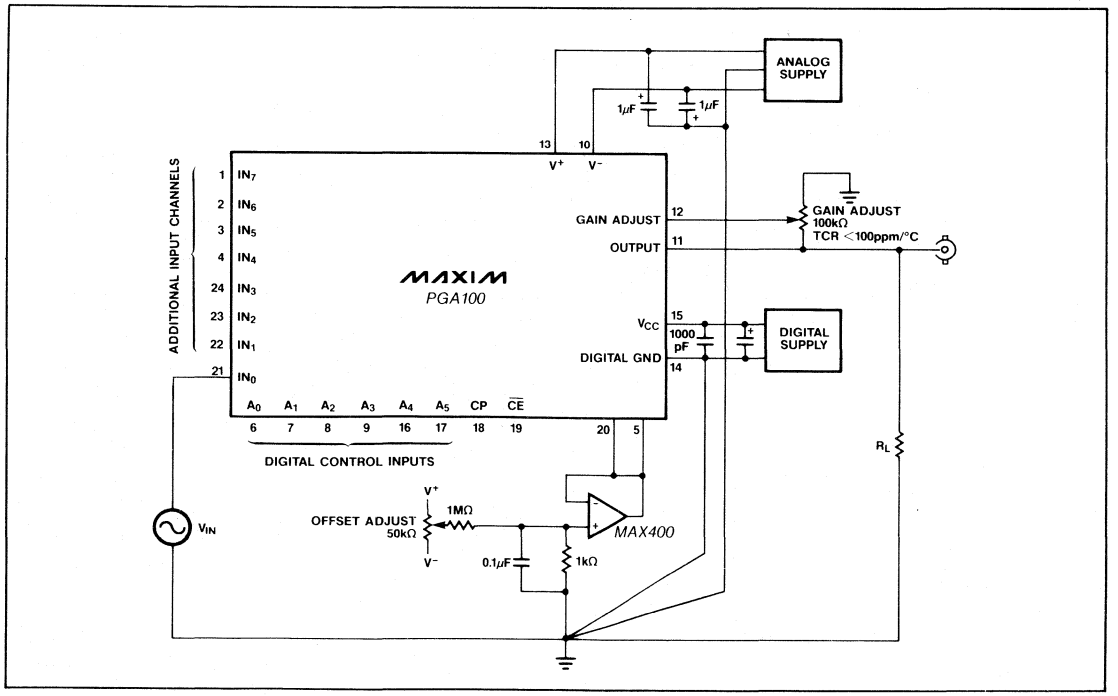


Figure 5. External Gain and Offset Adjustment

Programmable Gain Amplifier

Typical System Application

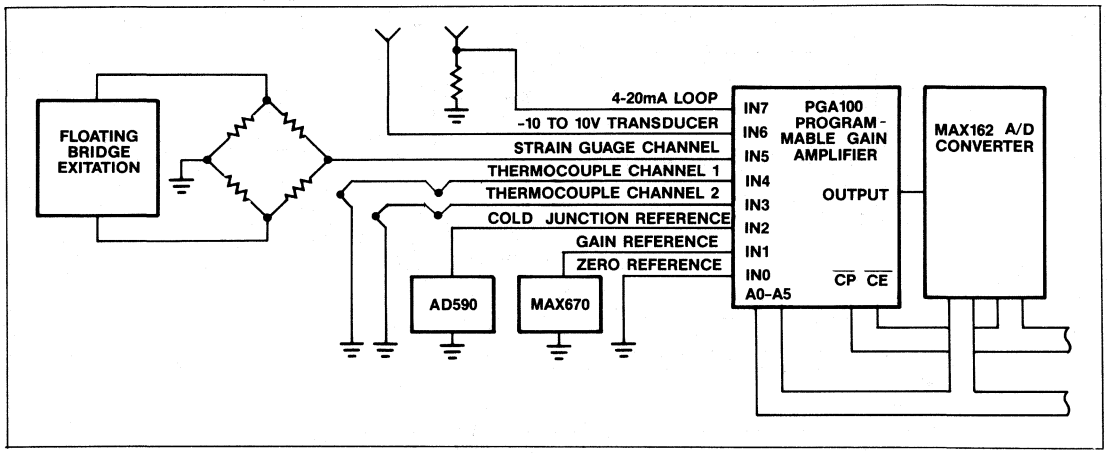


Figure 6. Multiple Channel, Variable Gain Data Acquisition System.

MAXIM

Power Supply Circuits

Voltage Regulators & Converters

Linear Voltage Regulators

Part Number	Output Voltage	Input Voltage	Quiescent Current (Typ/Max)	Output Voltage Accuracy	Features	Page No.
AC-DC Regulators						
MAX600	Fixed 5V or 1.3V to 9V	110/220VAC	70µA/150µA	±4%	Full wave bridge	6-1
MAX601	Fixed 5V	110/220VAC	70µA/150µA	±4%	Half wave bridge	6-1
MAX602	Fixed 5V or 1.3V to 8V	6 to 9VAC	70µA/150µA	±4%	For use with isolation transformer	6-1
MAX610	Fixed 5V or 1.3V to 9V	110/220VAC	70µA/150µA	±4%	Full wave bridge	6-5
MAX611	Fixed 5V	110/220VAC	70µA/150µA	±4%	Half wave bridge	6-5
MAX612	Fixed 5V or 1.3V to 8V	6 to 9VAC	70µA/150µA	±4%	For use with isolation transformer	6-5
DC Linear Regulators						
MAX663	Fixed 5V or 1.3V to 15V	2V to 16.5V	6µA/12µA	±5%	+5V or programmable output	6-73
MAX664	Fixed -5V or -1.3V to -15V	-2V to -16.5V	6µA/12µA	±5%	-5V or programmable output	6-73
MAX666	Fixed 5V or 1.3V to 15V	2V to 16.5V	6µA/12µA	±5%	Fixed +5V or programmable output voltage Low Battery Detector	6-73
ICL7663	1.3V to 15V	1.5V to 16V	4µA/10µA	±8%		
ICL7663A	1.3V to 15V	2.0V to 16V	4µA/10µA	±1%	Accurate output voltage	6-125
ICL7663B	1.3V to 10V	1.5V to 10V	4µA/10µA	±8%		
ICL7664	-1.3V to -15V	-2V to -16V	3.5µA/10µA	±8%		
ICL7664A	-1.3V to -15V	-2V to -16V	3.5µA/10µA	±1%	Accurate output voltage	6-133

DC-DC Converters

Part Number	Description	Input Voltage	Output Voltage	Comments	Page No.
Boost Converters					
MAX630/4193	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4193 2nd source	6-17
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components	6-29
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components	6-29
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components	6-29
Inverting Converters					
MAX634/4391	DC-DC Voltage Inverter	2V to 16.5V	up to -20V	Improved RC4391 2nd source	6-37
MAX635	DC-DC Voltage Inverter	2V to 16.5V	-5V	Only 3 external components	6-49
MAX636	DC-DC Voltage Inverter	2V to 16.5V	-12V	Only 3 external components	6-49
MAX637	DC-DC Voltage Inverter	2V to 16.5V	-15V	Only 3 external components	6-49
Step Down Converter					
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components	6-57
Boost Converters					
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET	6-65
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET	6-65
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET	6-65
Charge Pump Converters					
MAX680	± Output Charge Pump	2.0V to 6.0V	±10V ($5V_{IN}$)	4 external capacitors	6-81
ICL7660	Negative Charge Pump	1.5V to 10V	$-V_{IN}$	Not regulated	6-117

Supervisory Power Supply Circuits

uP Reset, Power Fail Detector, Battery Switchover, and Watchdog Timer

Part Number	Pins	Reset Level (Volts)	Supply Current (mA)	Reset Delay (ms)	Battery Switch	RAM Protect	Low Line In	Low Line Out	Page No.
MAX690	8	4.65	4	50	Yes	No	No	No	6-87
MAX691	16	4.65	4	50*	Yes	Yes	No	Yes	6-87
MAX692	8	4.40	4	50	Yes	No	No	No	6-87
MAX693	16	4.40	4	50*	Yes	Yes	No	Yes	6-87
MAX694	8	4.65	4	200	Yes	No	No	No	6-87
MAX695	16	4.65	4	200*	Yes	Yes	No	Yes	6-87
MAX696	16	Adj.	4	50*	Yes	No	Yes	Yes	6-101
MAX697	16	Adj.	.06	50*	No	Yes	Yes	Yes	6-101

* default; also adjustable

Voltage Detectors

Part Number	Description	Supply Voltage Range	Supply Current (typ/max)	Threshold Accuracy	Page No.
MAX8211	Single Channel, Non-inverting voltage detector	2.0V to 16.5V	5µA/15µA	±3.5%	6-113
MAX8212	Single Channel, Inverting voltage detector	2.0V to 16.5V	5µA/15µA	±3.5%	6-113
ICL7665	Two Channels: one inverting, one non-inverting	1.6V to 16.0V	2.5µA/10µA	±7.5%	6-139
ICL7665A	Two Channels: one inverting, one non-inverting	2.0V to 16.0V	2.5µA/10µA	±2%	6-139

6

AC To DC Regulator (110/220VAC To 5.0VDC)

General Description

The MAX600 family of AC to DC Power Converters minimizes the cost, simplifies the design, and reduces the component count, size, and weight of ½ watt power supplies. With an 8 VRMS input voltage the MAX600 needs only a single filter capacitor to make a complete 5V, 100mA power supply. With the addition of a current limiting resistor and a current limiting capacitor, the MAX600 connects directly to the 100 VAC or 220 VAC power line to make a minimum component count 110/220VAC to 5VDC power supply.

The three members of the MAX600 family differ in three respects: full or half wave rectification, 12V or 18V zener voltage, and the assignment of pin 4 to the function of setting the output voltage or setting the time delay. The MAX600 has a full wave rectifier, a 12V zener, and the output voltage is either the internally preset +5V or user adjustable from 1.3 to 9V. The MAX601 has a half wave rectifier, a 12V zener, a fixed 5V output, and pin 4 controls the time delay of the reset output. The MAX602 has a full wave rectifier, an 18V zener, and the output voltage is either the internally preset +5V or user adjustable in the range of +1.3V to +15V.

For more detailed application information on AC to DC Regulators, refer to the MAX610/11/12 data sheet.

Applications

Minimum Component Count Power Supplies
Uninterruptable 5V Power Supplies
Precision Battery Chargers
Line Powered Appliances
Industrial Controls
Off Line Instruments
Triac Output Power Controllers

Typical Operating Circuit

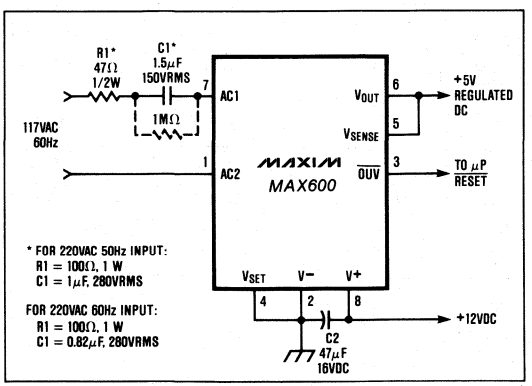


Figure 1. Simple Line-Powered 5V Supply.

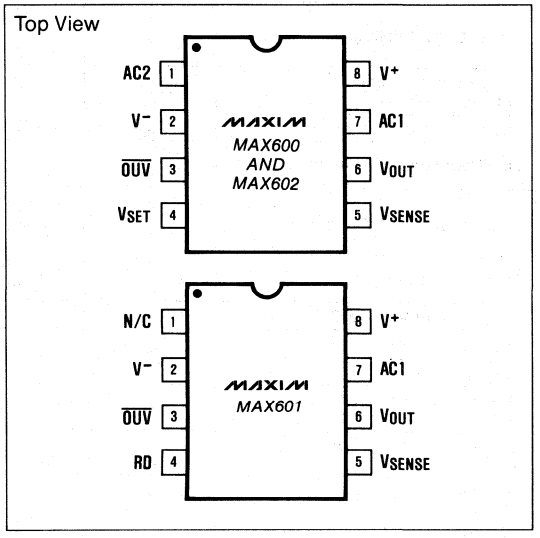
Features

- ◆ **Direct 110/220VAC to 5VDC Conversion**
- ◆ **Minimum External Component Count**
- ◆ **Output Voltage Preset to 5V ±4%**
- ◆ **70μA Typical Quiescent Current**
- ◆ **Over/Undervoltage Detection**
- ◆ **Power-up Reset Circuit with Programmable Delay**
- ◆ **Programmable Current Limiting**
- ◆ **Programmable Output Voltage: 1.3V to 15V**
- ◆ **Low Cost, Limited Temperature Range Alternative to MAX610/11/12**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX600LPA2	0°C to +50°C	8 Lead Plastic Dip
MAX601LPA2	0°C to +50°C	8 Lead Plastic DIP
MAX602LPA2	0°C to +50°C	8 Lead Plastic Dip

Pin Configurations



AC To DC Regulator (110/220VAC To 5.0VDC)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... 0°C to +50°C
Maximum Junction Temperature ..... +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Power Dissipation @ 25°C 750mW
derate 8mW/C above 25°C.
Input Current
MAX601
AC1, V^-; 250μs non-repetitive pulse 5A
AC1, V^-; continuous ..... 180mA RMS
V^+ 150mA
MAX600, MAX602
AC1, AC2; 250μs non-repetitive pulse 5A
AC1, AC2; continuous ..... 120mA RMS
V^+ 150mA
All other terminals 10mA

Input Voltage
MAX600, MAX601 (Note 1)
AC1, AC2 ..... 11.5V
V^+ 10.8V
MAX602
AC1, AC2 ..... 17V
V^+ 16.2V
All other terminals ..... (V^- - 0.3V) to (V^+ + 0.3V)
Output Current
V^+, V_{OUT} 150mA
$\overline{OUV}$ 10mA

Note 1: The maximum input voltage may be exceeded if the maximum input current and power dissipation specifications are observed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is no implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V^+ = 10V, R_{SENSE} = 0Ω, V_{SET} connected to V^- unless noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage	V_F	I_F = 1mA I_F = 50mA		0.62 1.1	 2.0	V
Zener Voltage	V_Z	I_Z = 50mA, Measure at V^+ MAX600, MAX601, MAX602		 12.4 18.6		V
Zener Dynamic Resistance	R_Z	I_Z = 50mA MAX600, MAX601, MAX602		 6 9		Ω
Preset Output Voltage	V_{OUT}	0.5mA ≤ I_{OUT} ≤ 50mA T_A = 25°C 0°C ≤ T_A ≤ +50°C	 4.80 4.75	 5.00 5.00	 5.20 5.25	V
Temperature Coefficient of Output Voltage	$\frac{\Delta V_{OUT}}{\Delta T}$	0°C ≤ T_A ≤ +50°C		±100		ppm/°C
Internal Voltage Reference	V_{SET}	MAX600, MAX602		1.3		V
Line Regulation (DC Input)	$\frac{\Delta V_{OUT}}{\Delta V^+}$	8V ≤ V^+ ≤ V_Z		0.25		%/V
Line Regulation (AC Input)	$\frac{\Delta V_{OUT}}{\Delta V_{AC}}$	I_{OUT} = 10mA $70V_{RMS}$ < V_{IN} < $140V_{RMS}$ or $140V_{RMS}$ < V_{IN} < $280V_{RMS}$		 0.001 0.001		%/V
Output Impedance	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	I_{OUT} Changing from 1mA to 51mA		0.6	2.0	Ω
Input-Output Voltage Differential	$V^+ - V_{OUT}$	I_{OUT} = 25mA		1.1	2.0	V
V_{SET} Input Current	I_{SET}			0.01	100	nA
Supply Current Total	I^+			70	150	μA
Overvoltage Detection Voltage	V_{OUVH}	Measured at V_{SENSE}		5.4	5.65	V
Undervoltage Detection Voltage	V_{OUVL}	Measured at V_{SENSE}	4.35	4.65		V
$\overline{OUV}$ Output Leakage	I_{OUV}	V_{SENSE} = 5V, $\overline{OUV}$ = 5V		0.001	10	μA
$\overline{OUV}$ Output Voltage	V_{OUV}	V_{SENSE} ≥ 5.65V or V_{SENSE} ≤ 4.35V, I_{OUV} = 1mA			0.4	V
Reset Time Delay	t_{DELAY}	MAX601, C3 = 0.01μF		30		ms
Reset Pin Threshold	V_{TH}	MAX601, V^+ = V_Z		8.0		V

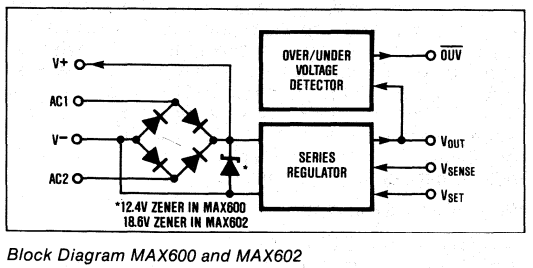
AC To DC Regulator (110/220VAC To 5.0VDC)

Pin Descriptions

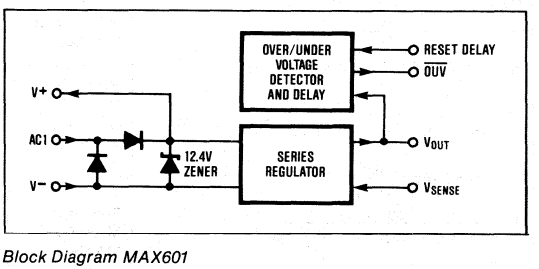
PIN	PIN #	DESCRIPTION
AC1	7	AC input to the internal diode rectifier.
AC2	1 (MAX600/02)	Second AC input to the full wave bridge rectifier.
N/C	1 (MAX601)	This pin is not connected on the MAX601.
V^-	2	Negative output terminal. This terminal is also an AC input for the half wave rectifier of MAX601.
V_{OUT}	6	Positive regulated DC output.
V_{SENSE}	5	Current limit input. The output short circuit current limit is 0.6V/R_{SENSE}, where R_{SENSE} is a current sensing resistor connected between V_{OUT} and V_{SENSE}.
$\overline{OUV}$	3	This open drain pin goes low during undervoltage and overvoltage conditions. The undervoltage and overvoltage thresholds are fixed at 4.65V (undervoltage) and 5.4V (overvoltage) and do not change, even if the output voltage is changed via the V_{SET} terminal.

PIN	PIN #	DESCRIPTION
V^+	8	Positive unregulated or raw DC output of the rectifier. The raw DC filter capacitor connects to this terminal.
RD	4 (MAX601)	An external capacitor connected to the Reset Delay pin determines the Reset Delay period. The reset time delay is directly proportional to the capacitance connected to this pin; each 0.01μF of capacitance results in 30 milliseconds of delay. This delay period must elapse before the Reset/OUV pin goes high after an overvoltage or undervoltage condition.
V_{SET}	4 (MAX600/02)	If the V_{SET} terminal is grounded, the MAX600 and MAX602 output voltage will be the preset 5V ±4%. Alternatively, the V_{SET} input can be used to set the output voltage to any voltage from 1.3V to 15V (MAX602) or 1.3V to 10V (MAX600 and MAX601), using a simple resistive voltage divider.

Block Diagrams



Block Diagram MAX600 and MAX602



Block Diagram MAX601

Typical Applications

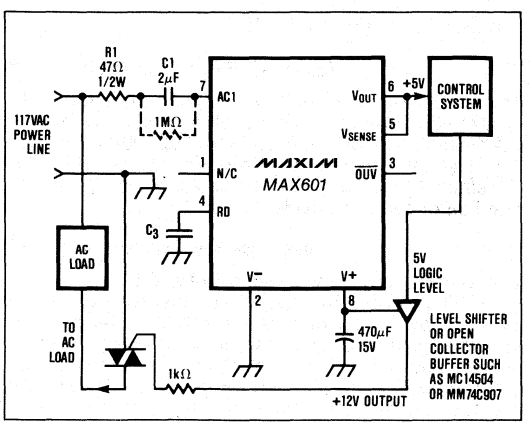


Figure 2. Driving Triacs With +12V Supply.

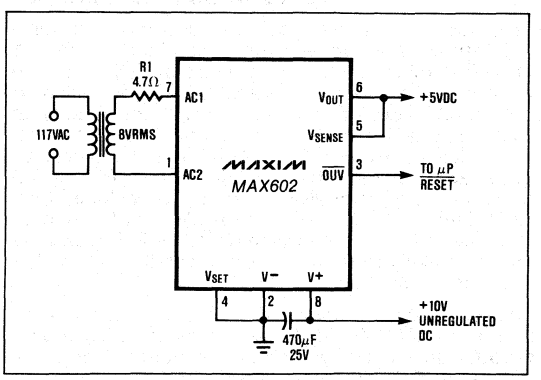


Figure 3. Transformer Isolated 5V Power Supply.

AC To DC Regulator (110/220VAC To 5.0VDC)

Cautions and Component Selection

1) Unless driven by a transformer, the 5V output of the MAX600/01/02 is **NOT ISOLATED** from the power line and all circuitry connected to the MAX600/01/02 should be treated as if it were directly connected to the power line. The MAX600/01/02, its circuitry, and all components driven by the 5V output present a shock hazard and should be in a protective enclosure to prevent accidental contact.

2) Use an isolation transformer or ground fault interrupter (GFI) when breadboarding, testing, or troubleshooting a MAX600 family based line-power supply or any circuitry powered by the MAX600 family. If the MAX600/01/02 is connected directly to the power line, do **NOT** connect the ground of an oscilloscope to the circuit — this will severely damage the oscilloscope and destroy the MAX600/01/02.

Table 1. DESIGN FORMULAE

FORMULA	EXAMPLE in FIGURE	COMMENTS
V_{OUT} = 5V ± 4%. V_{SET} Grounded	1	
$V_{OUT} = 1.3V\ (1 + \frac{R2}{R3})$	4	MAX600 and MAX602
$I_{OUT(MAX)} = C1 \times 4\sqrt{2} \times V_{RMS} \times F_{IN}$	1	Full wave — MAX600, MAX602
$I_{OUT(MAX)} = C1 \times 2\sqrt{2} \times V_{RMS} \times F_{IN}$	2	Half wave — MAX601
$I_{CURRENT\ LIMIT} = \frac{0.6V}{R_{SENSE}}$	4	
$C1 = \frac{I_{OUT(MAX)}}{(V_{RMS} - V_{OUT}) \times 4\sqrt{2} \times F_{IN}}$	1	Full wave — MAX600, MAX602
$C1 = \frac{I_{OUT(MAX)}}{(V_{RMS} - V_{OUT}) \times 2\sqrt{2} \times F_{IN}}$	2	Half wave — MAX601
Time delay = C3 x 3 (in secs) (in μF)	2	MAX601 only

Current Limiting Capacitor, C1

This capacitor is the most critical component for a 110/220VAC input power supply based on the MAX601 family. It must continuously withstand the full line voltage so it should be rated for AC operation. A conservative designer will use a capacitor rated for at least 150VRMS working voltage for 110VAC circuits, and at least 280VRMS for 220VAC or 240VAC circuits. This capacitor must be a NON-POLARIZED capacitor such as polyester (Mylar™) or polypropylene metallized film. Metallized film capacitors are preferred over metal foil capacitors since metal foil capacitors are more likely to fail as a short circuit than are metallized film capacitors.

The value of C1 determines both the power dissipation of the MAX600/01/02 and the maximum available output current. The value of C1 should be the smallest value that will deliver the desired output current

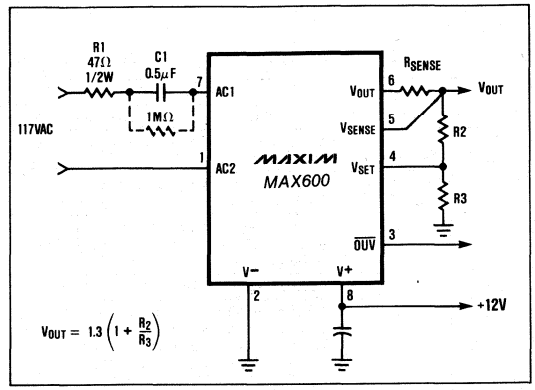


Figure 4. Adjustable Output Voltage.

at minimum line voltage, since the power dissipated by the MAX600/01/02 increases with increasing values of C1. Table 1 gives the formula for calculating C1 as a function of the desired output current.

Current Limiting Resistor, R1

R1 limits the maximum peak current that occurs when power is first applied to the MAX600 just as the power line voltage is at its maximum. The instantaneous peak current must be limited to 5 Amps. For 110VAC input voltage R1 must be 33Ω or greater; for 220VAC input voltage R1 must be 68Ω or greater. The recommended values are 47Ω for 110VAC and 100Ω for 220VAC. The power dissipation in R1 is constant, independent of the load current.

With 110VAC 60Hz input

$$Pd(R1)\ (\text{in mW}) = 1.6 \times C1^2\ (\text{in } \mu F) \times R1\ (\text{in } \Omega)$$

With 220VAC 50Hz input

$$Pd(R1)\ (\text{in mW}) = 2.7 \times C1^2\ (\text{in } \mu F) \times R1\ (\text{in } \Omega)$$

Raw DC Filter Capacitor, C2

This capacitor is normally an aluminum or tantalum electrolytic capacitor. C2 is ordinarily 47μF when the MAX600/02 are driven from the 110/220VAC power line. The half wave MAX601 requires larger values for C2 since the output current is supplied by C2 for one-half of each line cycle.

Adjustable Output Voltage

The MAX601 output voltage is fixed at 5V ± 4%. The MAX600 and MAX602 output voltages can be set to 5V ± 4% by simply connecting the V_{SET} terminal to V−; other output voltages can be selected by connecting an external resistive voltage divider between the output and V_{SET} as shown in Figure 4. Calculate the resistor values for other voltages using the formula in Table 1.

AC To DC Regulator (110/220 VAC To 5.0V DC)

General Description

The MAX610 family of AC to DC Power Converters minimizes the cost, simplifies the design, and reduces the component count, size, and weight of 1/2 watt power supplies. With an 8 VRMS input voltage the MAX610 needs only a single filter capacitor to make a complete 5V, 100mA power supply. With the addition of a current limiting resistor and a current limiting capacitor, the MAX610 connects directly to the 110VAC or 220VAC power line to make a minimum component count 110/220VAC to 5VDC power supply.

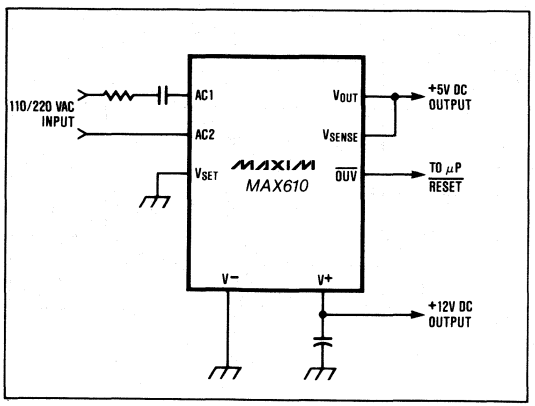
The three members of the MAX610 family differ in three respects: full or half wave rectification, 12V or 18V zener voltage, and the assignment of pin 4 to the function of setting the output voltage or setting the time delay. The MAX610 has a full wave rectifier, a 12V zener, and the output voltage is either the internally preset +5V or user adjustable from 1.3 to 9V. The MAX611 has a half wave rectifier, a 12V zener, a fixed 5V output, and pin 4 controls the time delay of the reset output. The MAX612 has a full wave rectifier, an 18V zener, and the output voltage is either the internally preset +5V or user adjustable in the range of +1.3V to +15V.

Applications

The MAX610 family is ideal for applications where size, weight, component count, and cost of 1/2 watt power supplies must be reduced. The reliable powerup reset and over/undervoltage detection makes the MAX610 family well suited for microprocessor based controllers.

Minimum Component Count Power Supplies
Uninterruptable 5V Power Supplies
Precision Battery Chargers
Line Powered Appliances
Industrial Controls
Off Line Instruments
Triac Output Power Controllers

Typical Operating Circuit



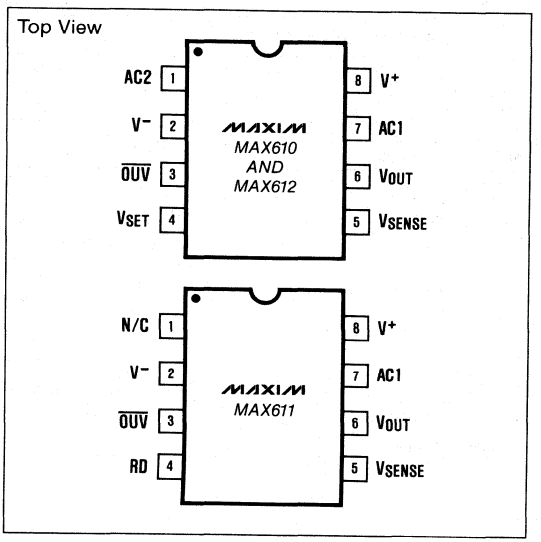
Features

- **Direct 110/220VAC to 5V DC Conversion**
- **Minimum External Component Count**
- **Output Voltage Preset to 5V ±4%**
- **70μA Typical Quiescent Current**
- **Over/Undervoltage Detection**
- **Power-up Reset Circuit with Programmable Delay**
- **Programmable Current Limiting**
- **Programmable Output Voltage: 1.3V to 15V.**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX610CPA	0°C to +70°C	8 Lead Plastic DIP
MAX611CPA	0°C to +70°C	8 Lead Plastic DIP
MAX612CPA	0°C to +70°C	8 Lead Plastic DIP

Pin Configurations



AC To DC Regulator (110/220 VAC To 5.0V DC)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... 0°C to +70°C
Maximum Junction Temperature ..... +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Power Dissipation @ 25°C 750mW
derate 8mW/C above 25°C.
Input Current
MAX611
AC1, V^-; 250μs non-repetitive pulse 5A
AC1, V^-; continuous ..... 180mA RMS
V^+ 150mA
MAX610, MAX612
AC1, AC2; 250μs non-repetitive pulse 5A
AC1, AC2; continuous ..... 120mA RMS
V^+ 150mA
All other terminals 10mA

Input Voltage
MAX610, MAX 611 (Note 1)
AC1, AC2 ..... 11.5V
V^+ 10.8V
MAX612
AC1, AC2 ..... 17V
V^+ 16.2V
$\overline{OUV}$ ..... (V^- - 0.3) to +16V
All other terminals ..... (V^- - 0.3V) to (V^+ + 0.3V)
Output Current
V^+, V_{OUT} 150mA
$\overline{OUV}$ 10mA

Note 1: The maximum input voltage may be exceeded if the maximum input current and power dissipation specifications are observed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is no implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V^+ = 10V, R_{SENSE} = 0Ω, V_{SET} connected to V^- unless noted)

INPUT RECTIFIER AND ZENER

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage	V_F	I_F = 1mA I_F = 50mA		0.62 1.1	 2.0	V V
Zener Voltage	V_Z	I_Z = 50mA, Measure at V^+ MAX610, MAX611, MAX612		 12.4 18.6		 V V
Zener Dynamic Resistance	R_Z	I_Z = 50mA MAX610, MAX611, MAX612		 6 9		 Ω Ω

SERIES VOLTAGE REGULATOR

Preset Output Voltage	V_{OUT}	0.5mA ≤ I_{OUT} ≤ 50mA T_A = 25°C 0°C ≤ T_A ≤ +70°C	 4.80 4.75	 5.00 5.00	 5.20 5.25	 V V
Temperature Coefficient of Output Voltage	$\frac{\Delta V_{OUT}}{\Delta T}$	0°C ≤ T_A ≤ +70°C		±100		ppm/°C
Internal Voltage Reference	V_{SET}	MAX610, MAX612,		1.3		V
Line Regulation (DC Input)	$\frac{\Delta V_{OUT}}{\Delta V^+}$	8V ≤ V^+ ≤ V_Z, Figure 7		0.25		%/V
Line Regulation (AC Input)	$\frac{\Delta V_{OUT}}{\Delta V_{AC}}$	I_{OUT} = 10mA $70V_{RMS} < V_{IN} < 140V_{RMS}$ or $140V_{RMS} < V_{IN} < 280V_{RMS}$ Figure 3, 4		 0.001 0.001		 %/V %/V
Output Impedance	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	I_{OUT} changing from 1mA to 51mA		0.6	2.0	Ω
Input-Output Voltage Differential	$V^+ - V_{OUT}$	I_{OUT} = 25mA		1.1	2.0	V
V_{SET} Input Current	I_{SET}			0.01	100	nA
Supply Current	I^+			70	150	μA

ELECTRICAL CHARACTERISTICS (Continued)

(T_A = 25°C, V^+ = 10V, R_{SENSE} = 0Ω, V_{SET} connected to V^- unless noted)

OVER VOLTAGE DETECTOR

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Detection Voltage	V_{OUVH}	Measured at V_{SENSE}		5.4	5.65	V
Undervoltage Detection Voltage	V_{OUVL}	Measured at V_{SENSE}	4.35	4.65		V
$\overline{OUV}$ Output Leakage	I_{OUV}	V_{SENSE} = 5V, $\overline{OUV}$ = 5V		0.001	10	µA
$\overline{OUV}$ Output Voltage	V_{OUV}	$V_{SENSE} \geq 5.65V$ or $V_{SENSE} \leq 4.35V$, I_{OUV} = 1mA			0.4	V
Reset Time Delay	t_{DELAY}	Figure 10A, MAX611 Only C3 = 0.01µF		30		ms
Reset Pin Threshold	V_{TH}	MAX611 Only $V^+ = V_Z$		8.0		V

Pin Descriptions

PIN	PIN #	DESCRIPTION
AC1	7	AC input to the internal diode rectifier.
AC2	1 (MAX610/12)	Second AC input to the full wave bridge rectifier.
N/C	1 (MAX611)	This pin is not connected on the MAX611.
V^-	2	Negative output terminal. This terminal is also an AC input for the half wave rectifier of MAX611.
V_{OUT}	6	Positive regulated DC output.
V_{SENSE}	5	Current limit input. The output short circuit current limit is 0.6V/R_{SENSE}, where R_{SENSE} is a current sensing resistor connected between V_{OUT} and V_{SENSE}.
$\overline{OUV}$	3	This open drain pin goes low during undervoltage and overvoltage conditions. The undervoltage and overvoltage thresholds are fixed at 4.65V (undervoltage) and 5.4V (overvoltage) and do not change, even if the output voltage is changed via the V_{SET} terminal.

PIN	PIN #	DESCRIPTION
V^+	8	Positive unregulated or raw DC output of the rectifier. The raw DC filter capacitor connects to this terminal.
RD	4 (MAX611)	An external capacitor connected to the Reset Delay pin determines the Reset Delay period. The reset time delay is directly proportional to the capacitance connected to this pin; each 0.01µF of capacitance results in 30 milliseconds of delay. This delay period must elapse before the Reset/$\overline{OUV}$ pin goes high after an overvoltage or undervoltage condition — see Figure 10.
V_{SET}	4 (MAX610/12)	If the V_{SET} terminal is grounded, the MAX610 and MAX612 output voltage will be the preset 5V ±4%. Alternatively, the V_{SET} input can be used to set the output voltage to any voltage from 1.3V to 15V (MAX612) or 1.3V to 10V (MAX610 and MAX611), using a simple resistive voltage divider — see Figure 8.

Block Diagrams

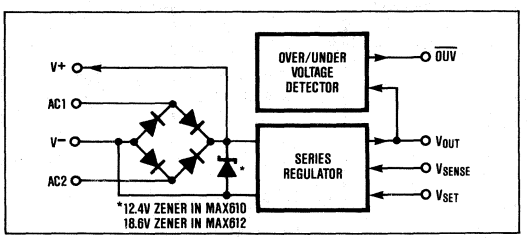


Figure 1. Block Diagram MAX610 and MAX612.

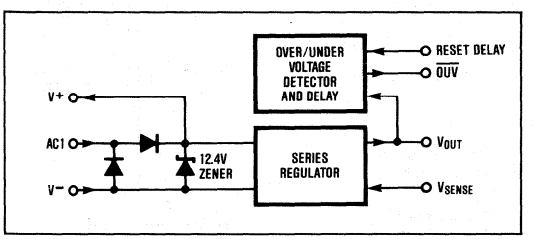


Figure 2. Block Diagram MAX611.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Typical Applications

Simple Line-Powered 5V Supply

Figure 3 shows a 50mA, 5V power supply using the full wave MAX610. Typical component values for both 110VAC and 220VAC 50/60Hz operation are shown. The output of this power supply is **NOT ISOLATED** from the power line: **the MAX610 and any equipment powered by the MAX610 must be enclosed to avoid shock hazards.** To avoid a second potential shock hazard, include the optional 1MΩ resistor shown in dotted lines. This resistor will discharge the voltage left on C1 when the 110/220VAC is disconnected.

110/220VAC to 5V, Half Wave Rectification

Figure 4 shows a 50mA 5V power supply using the half wave MAX611. The circuit differs from Figure 3 in that the 5V output is referenced to one side of the 110VAC power line. This circuit is generally preferred for systems that control triacs, where it is desired to have V^- connected to the power line. Note that for a given amount of output current, the value of C1 must be twice the value used in the full wave circuit of Figure 3. As with all MAX610 family circuits that do not use a transformer to isolate the circuit, this circuit is **NOT ISOLATED** from the power line.

Minimum Component Count 5V, 10mA Power Supply

For output currents of less than 10mA capacitor C1 of Figure 3 can be omitted, resulting in the circuit shown in Figure 5. The available output current is determined by the value of R1. For example, with R1 = 8.2kΩ, the available output current is 10mA, while the power dissipation in R1 is 1.3W. Double both the resistance value and the wattage rating of R1 for use with 220VAC input.

Transformer Isolated 5V Power Supply

If isolation from the power line is required, use the MAX612 in the circuit of Figure 6. The MAX612 must have an input voltage of at least 8V peak to maintain a regulated 5V output, but the peak transformer output voltage must not exceed 17V unless the current is limited as shown in Figures 3 and 4. The AC input line voltage can range from 80VRMS to 160VRMS with the 8VRMS nominal transformer voltage shown.

The MAX612 power dissipation is approximately $(V_{IN(peak)} - V_{OUT}) \times I_{LOAD}$. With the 8VRMS transformer shown, the power dissipated in the MAX612 limits the maximum output current to 100mA at 25°C ambient and 30mA at 70°C. If the 8V transformer is replaced by a 6.3V transformer, the maximum output current increases to 150mA at 25°C, but the minimum input line voltage to maintain output voltage regulation is increased to 100VRMS. When using a 6.3VRMS transformer, the filter capacitor connected to V^+ must be increased to 2200μF to ensure that the minimum voltage at V^+ is greater than 6V throughout each line cycle.

Resistor R1 limits the peak input current, but is not needed if the transformer impedance limits the peak current to a suitable value. As a rule of thumb, R1 can be omitted if the short circuit output current of the transformer is less than 2 Amps.

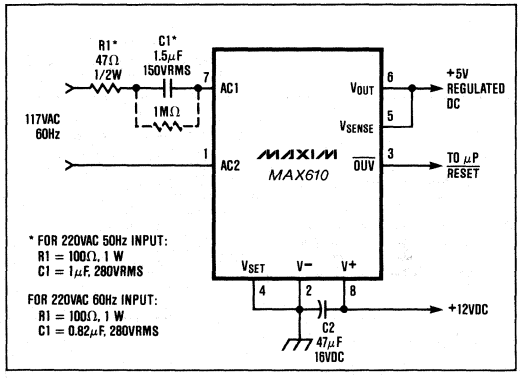


Figure 3. Simple Line-Powered 5V Supply.

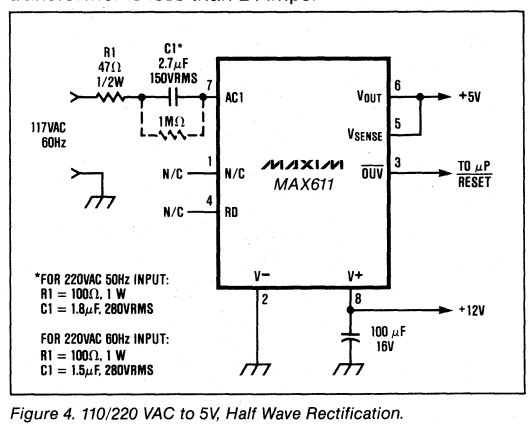


Figure 4. 110/220 VAC to 5V, Half Wave Rectification.

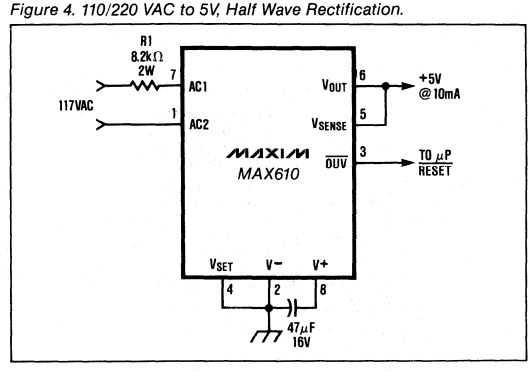


Figure 5. Minimum Component Count 5V, 10mA Supply.

AC To DC Regulator (110/220 VAC To 5.0V DC)

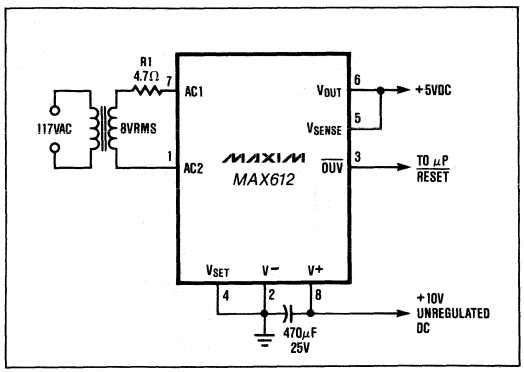


Figure 6. Transformer Isolated 5V Power Supply.

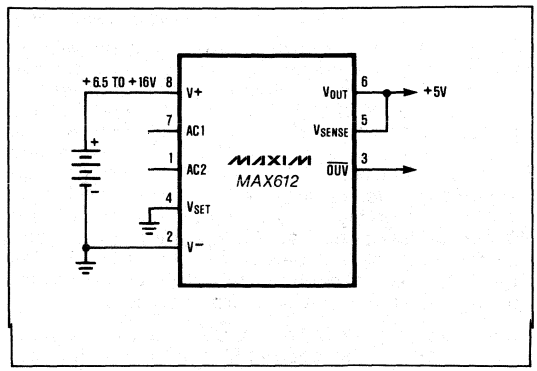


Figure 7. DC Input 5V Output Power Supply.

DC Input 5V Power Supply

The MAX610 family can also be powered by a DC input at the V^+ pin, as shown in Figure 7. The MAX610/11/12 typically use only 70μA of quiescent current, and can supply up to 150mA at 5V. The power dissipation in this mode of operation is simply calculated as

$$Pd = (V_{IN} - V_{OUT}) \times I_{OUT}.$$

The MAX610 family has a very low minimum $V_{IN} - V_{OUT}$ or dropout voltage; they need only 6.5V input to deliver 150mA at 5V.

The MAX612 can be used with input voltages up to 16V. The MAX610 and MAX611 are suitable for use with input voltages up to 10V.

Adjustable Output Voltage

The MAX611 output voltage is fixed at 5V ± 4%. The MAX610 and MAX612 output voltages can be set to 5V ± 4% by simply connecting the V_{SET} terminal to V^-; other output voltages can be selected by connecting an external resistive voltage divider between the output and V_{SET} as shown in Figure 8. Calculate the resistor values for other voltages using the formula

$$V_{OUT} = 1.3V \times \left(1 + \frac{R2}{R3}\right).$$

The maximum input voltage to the MAX612 is limited to 16V, enabling the MAX612 to supply any voltage from 1.3V to 15V. The maximum input voltage to the MAX610 is 10V, and the MAX610 can supply any output voltage from 1.3V to 9V.

The output voltage of the standard MAX610 is set to 5V ± 4% with an undervoltage trip point of 4.65V and an overvoltage trip point of 5.4V. Other output voltages are available through fusible link programming. The

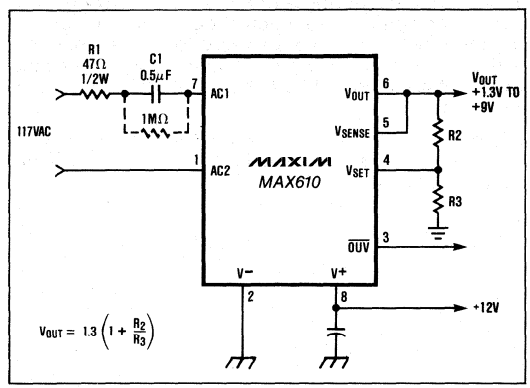


Figure 8. Adjustable Output Voltage.

overvoltage and undervoltage trip points are fixed at 107% and 93% of the pretrimmed output voltage. Consult factory regarding availability and minimum order requirements for preset voltages other than 5V.

Output Circuit Current Limiting

Figure 9 shows how a resistor, R_{SENSE}, can be added to any of the above circuits to provide short circuit current limit protection. A voltage difference between V_{SENSE} and V_{OUT} greater than a base-emitter voltage (approximately 0.6V) activates the MAX610/11/12 output current limit protection circuitry.

$$I_{CURRENT\ LIMIT} = \frac{0.6V}{R_{SENSE}}$$

When current limiting occurs, the voltage at V_{SENSE} will fall below 4.65V, causing the $\overline{OUV}$ output to go low.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Powerup Reset Delay

The MAX611 differs from the MAX610/12 in that MAX611 pin 4 controls a reset delay period, whereas the MAX610/12 pin 4 is used to adjust the output voltage. Both the MAX610/12 $\overline{OUV}$ pin and the MAX611 $\overline{OUV}$ pin go low immediately after the output voltage goes below the undervoltage or above the overvoltage threshold. The MAX610/12 $\overline{OUV}$ pin will go high immediately after the output returns to 5V. The MAX611 $\overline{OUV}$ pin will go high only after the output has been at 5V for a delay period determined by the value of a capacitor connected between V^- and pin 4 of the MAX611. This makes the $\overline{OUV}$ output well suited for driving the reset input of microprocessors.

Upon power-up the MAX611 $\overline{OUV}$ output will stay low until the output has been at 5V for the length of the delay period. This provides a reliable power-up reset to the microprocessor. Whenever the MAX611 output falls below 4.65V (as during a brownout), the $\overline{OUV}$ pin will go low, resetting the microprocessor. The output voltage must remain above 4.65V for the entire delay period before the $\overline{OUV}$ pin will go high: each time the voltage falls below 4.65V the reset delay period is restarted.

The delay period is approximately 30 milliseconds for each 0.01µF of capacitance. Leave pin 4 floating if this additional delay is not desired.

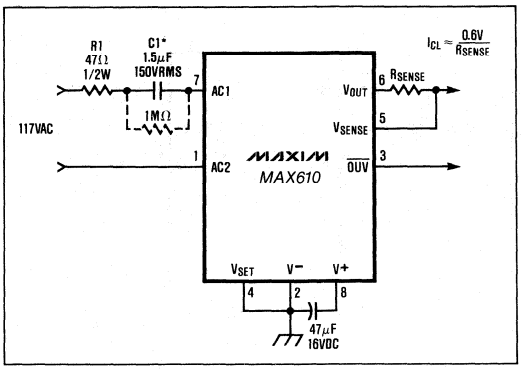


Figure 9. Short Circuit Current Limiting.

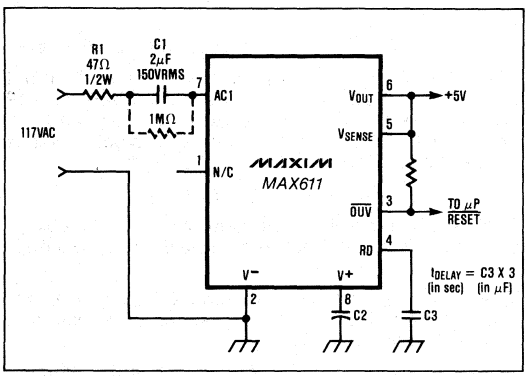


Figure 10A. Power-Up Reset Delay.

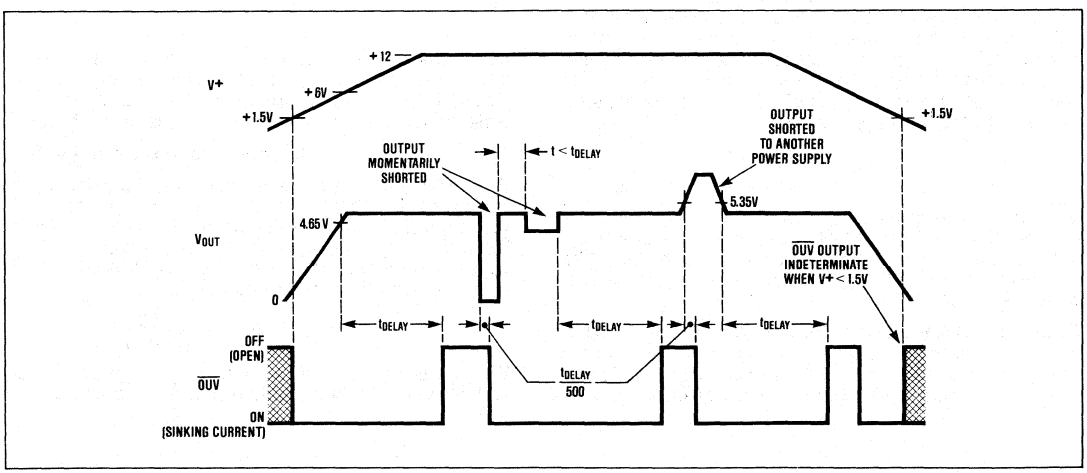


Figure 10B. Power-Up Reset Delay.

AC To DC Regulator (110/220 VAC To 5.0V DC)

+12V Output for Driving Triacs, Relays and MOSFETs

In some circuits a voltage higher than 5V is needed to drive relays, triacs, or power MOSFET gates. The DC output voltage at V^+ is +12V (+18V for MAX612) and can be used to trigger triacs as shown in Figure 11. The V^+ voltage is equal to the MAX610/11 zener voltage until the load current (total current drawn from the +12V and the +5V) approaches the maximum available output current (40mA for each μF of C1 capacitance with 110VAC 60Hz input, 70mA/μF with 220VAC 50Hz input). The ripple on the +12V is relatively low. With the components shown in Figure 11 the ripple voltage is about 5mV peak-peak at 10mA load current and 20mV at 40mA load current.

Increasing Output Current

The maximum allowable value for C1, and therefore the output current available from the MAX610 family, is limited by the power dissipated in the internal zener under no load conditions. By dissipating some of this power in an external zener, the output current capability can be increased.

The MAX611 can deliver up to 150mA at 5V when an external 7.5V zener is connected as shown in Figure 12. Note that capacitor C1 has been increased to 10μF, and that the 7.5V zener must be capable of dissipating approximately 2 watts under no load conditions.

Figure 13, the equivalent circuit using the MAX610, can supply 120mA at 5V. Since the MAX610 has a full wave rectifier, the value of C1 need only be half the value needed in the half wave circuit of Figure 12. The zeners each dissipate approximately 1 watt under no load conditions, with the zener power dissipation decreasing with increased output load current.

The method of increasing the available output current of the MAX610 shown in Figure 14 uses only one zener. The power dissipation of the MAX610 is slightly higher in this circuit than in that of Figure 13, since the zener current passes through the bridge rectifier of the MAX610. The values shown are suitable for up to 100mA output current.

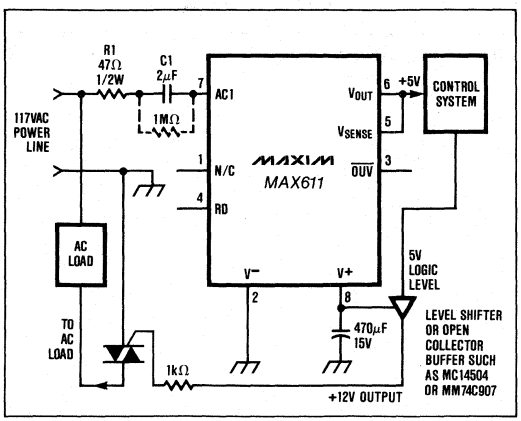


Figure 11. Driving Triacs With +12V Supply.

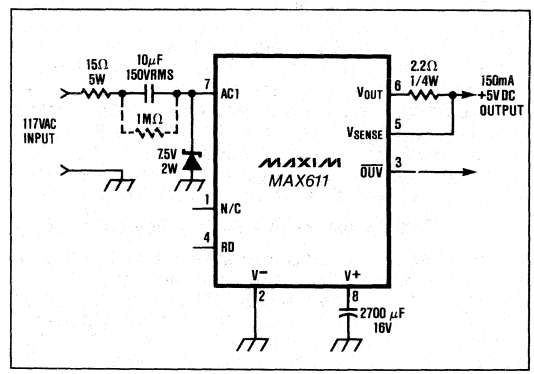


Figure 12. Increasing Maximum Allowable MAX611 Output Current.

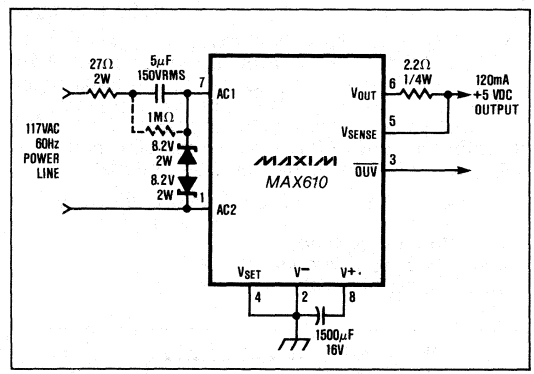


Figure 13. Increasing MAX610 Output Current.

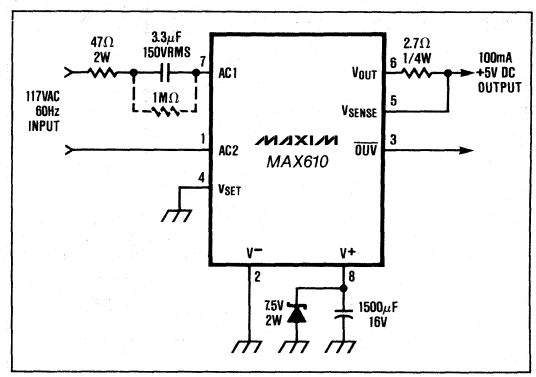


Figure 14. Increasing MAX610 Output Current, Alternative Method.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Uninterruptable 5V Power Supply

Figure 15 shows a simple way to combine a MAX610 with a battery to form an uninterruptable 5V power supply. When the 110VAC line voltage is present resistor R2 trickle charges the 7.2V NiCad battery. When the 110VAC is removed the NiCad battery will supply current through diode D1, and the MAX610 output will remain a constant 5V. The MAX610 will continue to deliver 5V out until V^+ is approximately 5.8V and the battery voltage is approximately 6.5V. Alkaline 9V or NiCad 8.4V batteries are also suitable; R2 should not be used with the non-rechargeable 9V alkaline battery. If isolation from the power line is required, drive AC1 and AC2 with a transformer as shown in Figure 6.

Polarity Insensitive Battery Powered Supply

Figure 16 shows a +5V power supply which will work even if the battery is installed backwards: the full wave bridge rectifier of the MAX612 will correct the battery polarity. The MAX612 is well suited for battery powered circuits since its quiescent current is only 70μA. The MAX610 can also be used if the battery voltage is less than 10V.

Battery Charger

The +6.7V open circuit or float voltage of Figure 17 is set by R2 and R3; the maximum charging current of 60mA is set by the value of C1. Since, unlike transformer driven battery chargers, C1 conducts current throughout most of each line cycle, the ratio of the RMS charging current to the average charging current is only about 1.2:1, and capacitor C2 is optional.

$I_{AVG(MAX)} = V_{IN} \times 5.56\ F_{IN} \times C$ (maximum charging current)

F_{IN} = Input Frequency
$I_{RMS} = 1.2\ I_{AVG}$; without C2
$I_{RMS} = I_{AVG}$; with C2.

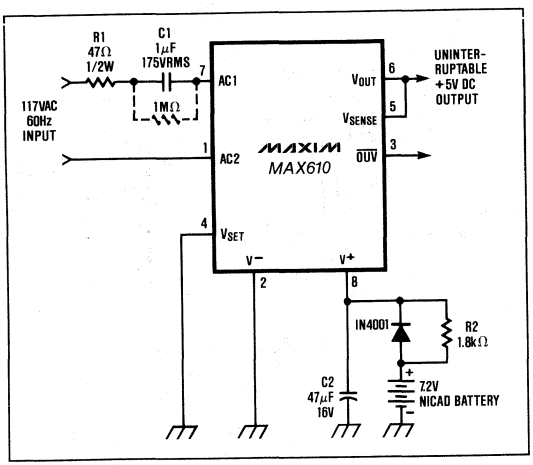


Figure 15. Uninterruptable 5V Power Supply.

The half wave MAX611 can also be used in this circuit, but the value of C1 must be doubled and the ratio of RMS current to average current increases to about 1.7:1.

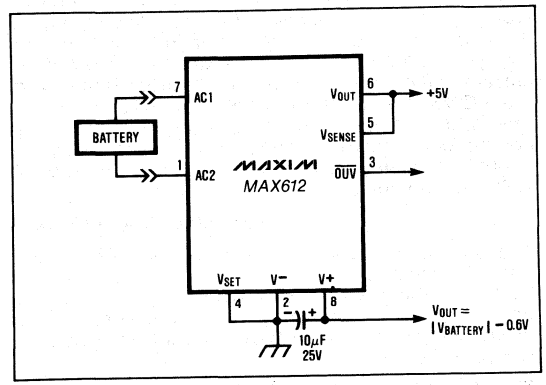


Figure 16. Polarity Insensitive Battery-Powered Supply.

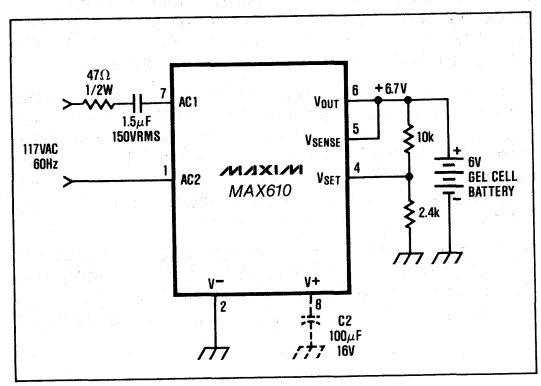


Figure 17. Simple Battery Charger.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Component Selection

The component values shown in the Typical Applications above are suitable for most applications. This section gives the reasons for the particular component values chosen, explains the effect of using other values, and discusses the component specifications.

Current Limiting Capacitor, C1

This capacitor is the most critical component for a 110/220VAC input power supply based on the MAX610 family. It must continuously withstand the full line voltage so it should be rated for AC operation. A conservative designer will use a capacitor rated for at least 150VRMS working voltage for 110VAC circuits, and at least 280VRMS for 220VAC or 240VAC circuits. This capacitor must be a NON-POLARIZED capacitor such as polyester (Mylar™) or polypropylene metallized film. Metallized film capacitors are preferred over metal foil capacitors since metal foil capacitors are more likely to fail as a short circuit than are metallized film capacitors.

The value of C1 determines both the power dissipation of the MAX610/11/12 and the maximum available output current. The value of C1 should be the smallest value that will deliver the desired output current at minimum line voltage, since the power dissipated by the MAX610/11/12 increases with increasing values of C1. Table 1 gives the formula for calculating C1 as a function of the desired output current. Table 2 shows some typical component suppliers and part numbers.

Current Limiting Resistor, R1

R1 limits the maximum peak current that occurs when power is first applied to the MAX610 just as the power line voltage is at its maximum. The instantaneous peak current must be limited to 5 Amps. For 110VAC input voltage R1 must be 33Ω or greater; for 220VAC input voltage R1 must be 68Ω or greater. The recommended values are 47Ω for 110VAC and 100Ω for 220VAC. The power dissipation in R1 is constant, independent of the load current.

With 110VAC 60Hz input

$$\underset{(\text{in mW})}{Pd(R1)} = 1.6 \times \underset{(\text{in } \mu F)}{C1^2} \times \underset{(\text{in } \Omega)}{R1}$$

With 220VAC 50Hz input

$$\underset{(\text{in mW})}{Pd(R1)} = 2.7 \times \underset{(\text{in } \mu F)}{C1^2} \times \underset{(\text{in } \Omega)}{R1}$$

Raw DC Filter Capacitor, C2

This capacitor is normally an aluminum or tantalum electrolytic capacitor. C2 is ordinarily 47μF when the MAX610/12 are driven from the 110/220VAC power line. The half wave MAX611 requires larger values for C2 since the output current is supplied by C2 for one-half of each line cycle.

Reset Delay Capacitor

This capacitor, labeled C3 in Figure 10, is non-critical and is usually a low cost ceramic capacitor.

Table 1. DESIGN FORMULAE

FORMULA	EXAMPLE in FIGURE	COMMENTS
$V_{OUT} = 5V \pm 4\%$. V_{SET} Grounded	3	
$V_{OUT} = 1.3V\ (1 + \frac{R2}{R3})$	8	MAX610 and MAX612
$I_{OUT(MAX)} = C1 \times 4\ \sqrt{2} \times V_{RMS} \times F_{IN}$	3	Full wave — MAX610, MAX612
$I_{OUT(MAX)} = C1 \times 2\ \sqrt{2} \times V_{RMS} \times F_{IN}$	4	Half wave — MAX611
$I_{CURRENT\ LIMIT} = \frac{0.6V}{R_{SENSE}}$	9	
$C1 = \frac{I_{OUT(MAX)}}{(V_{RMS} - V_{OUT}) \times 4\ \sqrt{2} \times F_{IN}}$	3	Full wave — MAX610, MAX612
$C1 = \frac{I_{OUT(MAX)}}{(V_{RMS} - V_{OUT}) \times 2\ \sqrt{2} \times F_{IN}}$	4	Half wave — MAX611
Time delay (in secs) = C3 (in μF) × 3	10	MAX611 only

Table 2. COMPONENT MANUFACTURERS

MFG	PART #	DESCRIPTION
Sprague	730P105X9250	1μF, 175V_{RMS} metallized polypropylene capacitor
	730P205X9250	2μF, 175V_{RMS} metallized polypropylene capacitor
	730P105X9400	1μF, 275V_{RMS} metallized polypropylene capacitor
	730P205X9400	2μF, 275V_{RMS} metallized polypropylene capacitor
TRW	TRW-40 1.0 20% 330VAC	1μF, 330VAC metallized polyester capacitor
	TRW-40 2.0 20% 330VAC	2μF, 330VAC metallized polyester capacitor
Aavid	5801B	Slip on heatsink for 8 pin Plastic DIP

Sprague Electric Co.
481 Marshall St.
North Adams, MA
(413) 664-4481

TRW Capacitor Division
301 W. O St.
Ogallala, NE 69153
(308) 284-3611

Aavid Engineering, Inc.
30 Cook Court, Box 400
Laconia, NH 03247
(603) 524-4443

The above table is included to assist you in obtaining components for use with the MAX610 family. This list is by no means inclusive and does not constitute an endorsement by Maxim Integrated Products.

AC To DC Regulator (110/220 VAC To 5.0V ADC)

Cautions and Application Hints

1) Unless driven by a transformer, the 5V output of the MAX610/11/12 is **NOT ISOLATED** from the power line, and all circuitry connected to the MAX610/11/12 should be treated as if it were directly connected to the power line. The MAX610/11/12, its circuitry, and all components driven by the 5V output present a shock hazard and should be in a protective enclosure to prevent accidental contact.

2) Use an isolation transformer or ground fault interrupter (GFI) when breadboarding, testing, or troubleshooting a MAX610 family based line-power supply or any circuitry powered by the MAX610 family. If the MAX610/11/12 is connected directly to the power line, do **NOT** connect the ground of an oscilloscope to the circuit — this will severely damage the oscilloscope and destroy the MAX610/11/12.

3) When the 110/220VAC input is disconnected from a MAX610 family based power supply, the input capacitor, C1, may be left charged to the peak input line voltage, creating a shock hazard on the input terminals. The optional 1MΩ resistor shown in Figure 3 is recommended for use in any of the circuits when the input to the power supply may be disconnected or where the input capacitor must be discharged to prevent shock hazards to maintenance or service personnel.

4) C1 must be able to withstand the peak AC input voltage. The power source should be properly fused.

5) Observe the power dissipation limit. Excessive power dissipation will cause the junction temperature to rise above the absolute maximum rating and will degrade the reliability.

6.) Use the minimum value of C1 that will deliver the desired output current. Minimizing the value of C1 minimizes the dissipation of the MAX610/11/12, thus increasing the reliability of the power supply.

7) The over/undervoltage detection circuit is setup for 5V operation. Even if the V_{SET} terminal is used to set another output voltage, the over/undervoltage detection is left set at 4.65V and 5.4V.

8) If the value of C2, the raw DC filter capacitor, is above 750μF, limit the maximum output current by inserting a resistor between V_{OUT} and V_{SENSE}. This prevents damage to the MAX610/11/12 which might occur if the energy stored in a large valued C2 were discharged into a short circuit. If C2 is below 750μF this protection is not necessary.

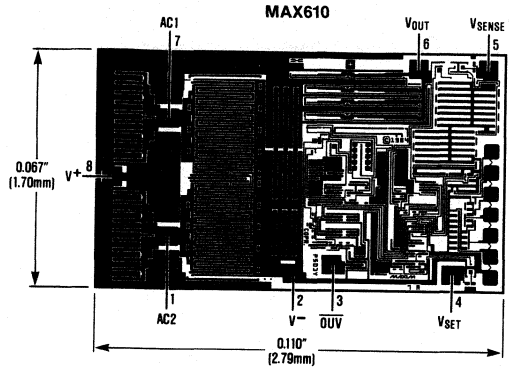
9) While the MAX610 family is stable without an output filter capacitor, it is good engineering practice to have power supply bypass capacitors on the output to compensate for the increased output impedance of the MAX610/11/12 at high frequency. A 47μF in parallel with a 0.1μF will keep the effective output impedance low from DC to greater than 1MHz.

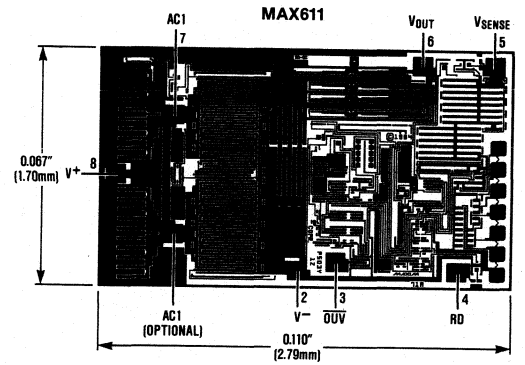
10) When powering the MAX610 or MAX612 through the V^+ terminal and using only the DC linear regulator, connect both AC1 and AC2 terminals to V^-.

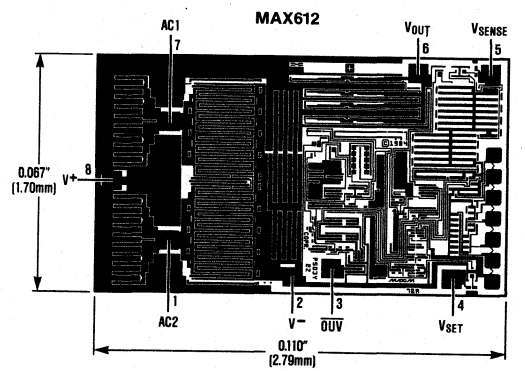
When using only the DC linear regulator portion of the MAX611 the AC1 terminal should be connected to V^-.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Chip Topography







6

MAXIM

CMOS Micropower Step-Up Switching Regulator

General Description

Maxim's MAX630 and MAX4193 CMOS DC-DC regulators are designed for simple, efficient, minimum size DC-DC converter circuits in the 5 milliwatt to 5 watt range. The MAX630 and MAX4193 provide all control and power handling functions in a compact 8 pin package: a 1.31V bandgap reference, an oscillator, a voltage comparator, and a 375mA N-channel output MOSFET. A comparator is also provided for low battery detection.

Operating current is only 70μA and is nearly independent of output switch current or duty cycle. A logic level input shuts down the regulator to less than 1μA quiescent current. Low current operation ensures high efficiency even in low power battery operated systems. The MAX630 and MAX4193 are compatible with most battery voltages, operating from 2.0V to 16.5V.

The devices are pin compatible with the Raytheon bipolar circuits, RC4191/2/3, while providing significantly improved efficiency and low voltage operation. Maxim also manufactures the MAX631, MAX632, and MAX633 DC-DC converters which reduce the external component count in fixed output 5V, 12V, and 15V circuits. See Table 2 on the last page of this data sheet for a summary of other Maxim DC-DC converters.

Applications

+5V to +15V DC-DC Converters

High Efficiency Battery Powered DC-DC Converters

+3V to +5V DC-DC Converters

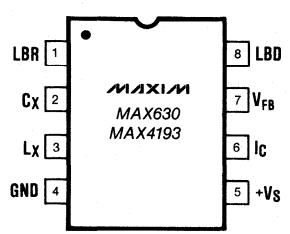
9V Battery Life Extension

Uninterruptible 5V Power Supplies

5mW to 5 Watt Switch-mode Power Supplies

Pin Configuration

Top View



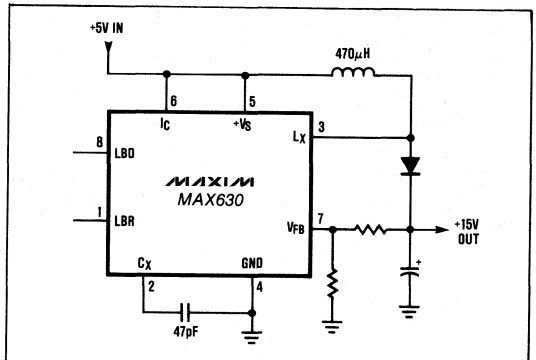
Features

- ♦ High Efficiency—85% Typical
- ♦ 70μA Typical Operating Current
- ♦ 1μA Maximum Quiescent Current
- ♦ 2.0 to 16.5V Operation
- ♦ 525mA (Peak) Onboard Drive Capability
- ♦ ±1.5% Output Voltage Accuracy (MAX630)
- ♦ Low Battery Detector
- ♦ Compact 8 Pin Mini-DIP and SO Packages
- ♦ Pin Compatible With RC4191/2/3

Ordering Information

PART	TEMP. RANGE	8 Lead PACKAGE
MAX630CPA	0°C to +70°C	8 Lead Plastic DIP
MAX630CSA	0°C to +70°C	8 Lead Small Outline
MAX630CJA	0°C to +70°C	8 Lead CERDIP
MAX630EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX630ESA	-40°C to +85°C	8 Lead Small Outline
MAX630EJA	-40°C to +85°C	8 Lead CERDIP
MAX630MJA	-55°C to +125°C	8 Lead CERDIP
MAX4193C/D	0°C to +70°C	Dice
MAX4193CPA	0°C to +70°C	8 Lead Plastic DIP
MAX4193CSA	0°C to +70°C	8 Lead Small Outline
MAX4193CJA	0°C to +70°C	8 Lead CERDIP
MAX4193EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX4193ESA	-40°C to +85°C	8 Lead Small Outline
MAX4193EJA	-40°C to +85°C	8 Lead CERDIP
MAX4193MJA	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



+5V to +15V Converter

CMOS Micropower Step-Up Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Operating Temperature Range
MAX630C, MAX4193C ..... 0°C to +70°C
MAX630E, MAX4193E ..... -40°C to +85°C
MAX630M, MAX4193M ..... -55°C to +125°C

Power Dissipation
Plastic DIP (derate 6.25mW/°C above 50°C) 468mW
Small Outline (derate 5.88mW/°C above 50°C) 441mW
CERDIP (derate 8.33mW/°C above 50°C) 833mW
Input Voltage (Pins 1, 2, 6, 7) ..... -0.3V to $+V_S$ +0.3V
Output Voltage, L_X and LBD 18V
L_X Output Current ..... 525mA Peak
LBD Output Current 50mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is no implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +6.0V, T_A = +25°C, I_C = 5.0μA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX630			MAX4193			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage	$+V_S$	Operating Start-up	2.0 1.8		16.5	2.4		16.5	V
Internal Reference Voltage	V_{REF}		1.29	1.31	1.33	1.24	1.31	1.38	V
Switch Current	I_{SW}	V_3 = 400mV	75	150		75	150		mA
Supply Current (at Pin 5)	I_S	I_3 = 0mA		70	125		90	200	μA
Efficiency				85			85		%
Line Regulation (Note 1)		$0.5V_0 < V_S < V_0$		0.08	0.2		0.08	0.5	% V_{OUT}
Load Regulation (Note 1)		V_S = +5V, P_{LOAD} = 0 to 150mW		0.2	0.5		0.2	0.5	% V_{OUT}
Operating Frequency Range (Note 2)	F_O		0.1	40	75	0.1	25	75	kHz
Reference Set Internal Pulldown Resistance	R_{IC}	$V_6 = V_S$	0.5	1.5	10	0.5	1.5	10	MΩ
Reference Set Input Voltage Threshold	V_{IC}		0.2	0.8	1.3	0.2	0.8	1.3	V
Switch Current	I_{SW}	V_3 = 1.0V	100			100			mA
Switch Leakage Current	I_{CO}	V_3 = 16.5V		0.01	1.0		0.01	5.0	μA
Supply Current (Shut Down)	I_{SO}	$I_C < 0.01\mu A$		0.01	1.0		0.01	5.0	μA
Low Battery Bias Current	I_{LBR}			0.01	10		0.01	10	nA
Capacitor Charging Current	I_{CX}			30			30		μA
C_X + Threshold Voltage				$+V_S$ - 0.1			$+V_S$ - 0.1		V
C_X - Threshold Voltage				0.1			0.1		V
V_{FB} Input Bias Current	I_{FB}			0.01	10		0.01	10	nA
Low Battery Detector Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	250	600		250	600		μA
Low Battery Detector Output Leakage	I_{LBDO}	V_8 = 16.5V, V_1 = 1.4V		0.01	5.0		0.01	5.0	μA

Note 1: Guaranteed by correlation with DC pulse measurements.
Note 2: The operating frequency range is guaranteed by design and verified with sample testing.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +6.0V, T_A = Full Operating Temperature Range, I_C = 5.0μA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX630			MAX4193			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage	$+V_S$		2.2		16.5	3.5		16.5	V
Internal Reference Voltage	V_{REF}		1.25	1.31	1.37	1.20	1.31	1.42	V
Supply Current (Pin 5)	I_S	I_3 = 0mA		70	200		90	300	μA
Line Regulation (Note 1)		$0.5V_{OUT} < V_S < V_{OUT}$		0.2	0.5		0.5	1.0	% V_{OUT}
Load Regulation (Note 1)		V_S = $+0.5V_0$, P_L = 0 to 150mW		0.5	1.0		0.5	1.0	% V_{OUT}
Reference Set Internal Pulldown Resistance	R_{IC}	$V_6 = V_S$ 0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C	 0.45 0.4 0.3	 1.5 1.5 1.5	 10 10 10	 0.45 0.4 0.3	 1.5 1.5 1.5	 10 10 10	MΩ
Reference Set Input Voltage Threshold	V_{IC}		0.2	0.8	1.3	0.2	0.8	1.3	V
Switch Leakage Current	I_{C0}	V_3 = 16.5V		0.1	30		0.1	30	μA
Supply Current (Shut Down)	I_{S0}	$I_C < 0.01μA$		0.01	10		0.01	30	μA
Low Battery Detector Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	250	600		250	600		μA

Note 1: Guaranteed by correlation with DC pulse measurements.

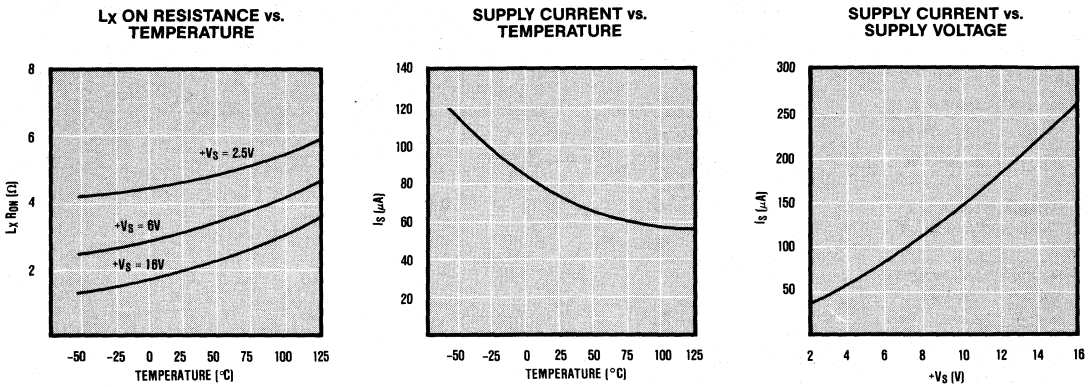
Pin Description

PIN	NAME	FUNCTION
1	LBR	Low Battery Detection Comparator input.The LBD output, pin 8, sinks current when ever this pin is below the low battery detector threshold, typically 1.31V.
2	C_X	An external capacitor connected between this terminal and ground sets the oscillator frequency. 47pF = 40KHz.
3	L_X	This pin drives the external inductor. The internal N-channel MOSFET which drives L_X has an output resistance of 4 ohms and a peak current rating of 525mA.
4	GND	Ground.
5	$+V_S$	The positive supply voltage, from 2.0V to 16.5V (MAX630).

PIN	NAME	FUNCTION
6	I_C	The MAX630/MAX4193 shuts down when this pin is left floating or is driven below 0.2V. For normal operation connect I_C directly to $+V_S$ or drive it high with either a CMOS gate or pull-up resistor connected to $+V_S$. The supply current is typically 10nA in the shutdown mode.
7	V_{FB}	The output voltage is set by an external resistive divider connected from the converter output to V_{FB} and Ground. The MAX630/MAX4193 will pulse the L_X output whenever the voltage at this terminal is less than 1.31V.
8	LBD	The Low Battery Detector output is an open drain N-channel MOSFET which sinks up to 600 μA (typ) whenever the LBR input, pin 1, is below 1.31V.

CMOS Micropower Step-Up Switching Regulator

Typical Operating Characteristics



Detailed Description

The operation of the MAX630 can best be understood by examining the voltage regulating loop of Figure 1. R1 and R2 divide the output voltage, which is compared with the 1.3V internal reference by comparator COMP1. When the output voltage is lower than desired, the comparator output goes high and the oscillator output pulses are passed through the NOR gate latch, turning on the output N-channel MOSFET at pin 3, L_X. As long as the output voltage is less than the desired voltage, pin 3 drives the inductor with a series of pulses at the oscillator frequency.

Each time the output N-channel MOSFET is turned on, the current through the external coil, L1, increases, storing energy in the coil. Each time the output turns off, the voltage across the coil reverses sign and the voltage at L_X rises until the catch diode, D1, is forward biased, delivering power to the output.

When the output voltage reaches the desired level, 1.31V x (1 + R1/R2), the comparator output goes low and the inductor is no longer pulsed. Current is then supplied by the filter capacitor, C1, until the output voltage drops below the threshold, and once again L_X is switched on, repeating the cycle. The average duty cycle at L_X is directly proportional to the output current.

Output Driver (L_X Pin)

The MAX630/MAX4193 output device is a large N-channel MOSFET with an ON resistance of 4 ohms and a peak current rating of 525mA. One well known advantage that MOSFETs have over bipolar transistors in switching applications is higher speed, which reduces switching losses and allows the use of smaller, lighter, less costly magnetic components. Also important is that MOSFETs, unlike bipolar transistors, do not require base current which, in low power DC-DC converters, often accounts for a major portion of input power.

The operating current of the MAX630 and MAX4193 increases by approximately 1μA/kHz at maximum power output due to the charging current required by the gate capacitance of the L_X output driver (e.g. 40μA increase at a 40kHz operating frequency). In comparison, equivalent bipolar circuits typically drive their NPN L_X output device with 2mA of base drive, causing the bipolar circuit's operating current to increase by a factor of 10 between no load and full load.

Oscillator

The oscillator frequency is set by a single external, low cost ceramic capacitor connected to pin 2, C_X. 47pF sets the oscillator to 40kHz, a reasonable compromise between lower switching losses at low frequencies and reduced inductor size at higher frequencies.

Low Battery Detector

The low battery detector compares the voltage on LBR with the internal 1.31V reference. The output, LBD, is an open drain N-channel MOSFET. In addition to detecting and warning of a low battery voltage, the comparator can also perform other voltage monitoring operations such as power failure detection.

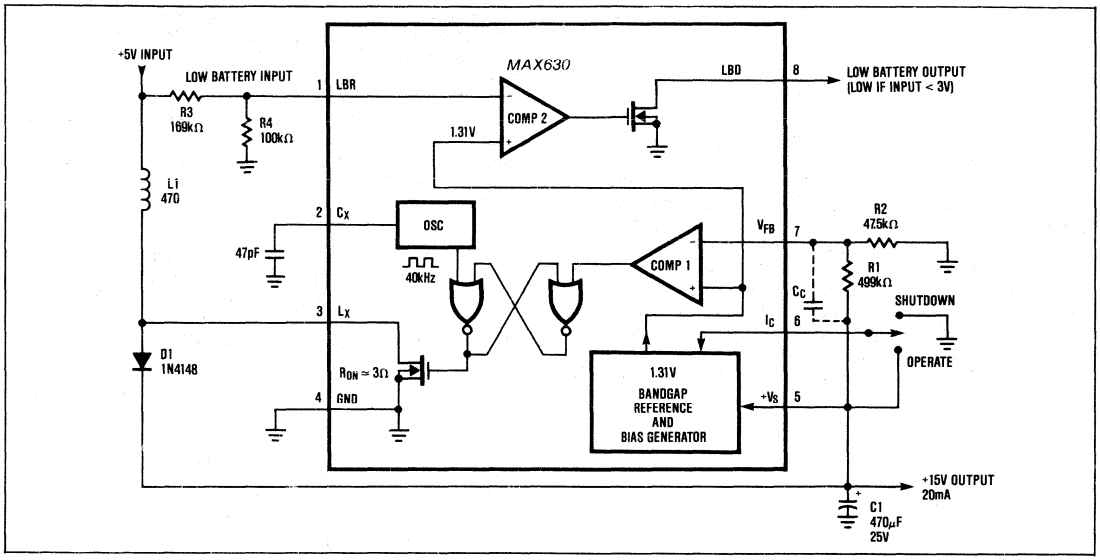


Figure 1. +5V to +15V Converter and Block Diagram

Another use of the low battery detector is to lower the oscillator frequency when the input voltage goes below a specified level. Lowering the oscillator frequency increases the available output power, compensating for the decrease in available power caused by reduced input voltage (See Figure 5).

Logic Level Shutdown Input

The shutdown mode is entered whenever I_C (pin 6) is driven below 0.2V or left floating. When shut down, the MAX630's analog circuitry, oscillator, L_X and LBD outputs are turned off. The device's quiescent current during shutdown is typically 10nA (1μA max).

Bootstrapped Operation

In most circuits, the preferred source of $+V_S$ voltage for the MAX630 and MAX4193 is the boosted output voltage. This is often referred to as a "bootstrapped" operation since the circuit figuratively "lifts" itself up.

The ON resistance of the N-channel L_X output decreases with an increase in $+V_S$, however, the device operating current goes up with $+V_S$ (see typical operating graph, I_S vs. $+V_S$). In circuits with very low output current and input voltages greater than 3V it may be more efficient to connect $+V_S$ directly to the input voltage rather than bootstrap.

External Components

Resistors

Since the LBR and V_{FB} input bias currents are specified as 10nA maximum, the current in the dividers R1/R2 and R3/R4 (figure 1) may be as low as 1μA without significantly affecting accuracy. Normally R2 and R4 are between 10k ohms and 1M ohm, which sets the current in the voltage dividers in the 1.3μA to 130μA range. R1 and R3 can then be calculated as follows:

$$10k\Omega \le R2 \le 1M\Omega \qquad R1 = R2 \times \frac{V_{OUT} - 1.31V}{1.31V}$$

$$10k\Omega \le R4 \le 1M\Omega \qquad R3 = R4 \times \frac{V_{LB} - 1.31V}{1.31V}$$

Where V_{OUT} is the desired output voltage and V_{LB} is the desired low battery warning threshold.

If the I_C (shutdown) input is pulled up through a resistor rather than connected directly to $+V_S$, the current through the pullup resistor should be a minimum of 4μA with I_C at the input-high threshold of 1.3V:

$$R_{IC} \le \frac{+V_S - 1.3V}{4\mu A}$$

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CMOS Micropower Step-Up Switching Regulator

Inductor Value

The available output current from a DC-DC voltage boost converter is a function of the input voltage, external inductor value, output voltage and the operating frequency.

The inductor must 1) have the correct inductance, 2) be able to handle the required peak currents, and 3) have acceptable series resistance and core losses. If the inductance is too high, the MAX630 will not be able to deliver the desired output power, even with the L_X output on for every oscillator cycle. The available output power can be increased by either decreasing the inductance or the frequency. Reducing the frequency increases the on-period of the L_X output, thereby increasing the peak inductor current. The available output power is increased since it is proportional to the square of the peak inductor current (I_{pk}).

$$L_{MAX} = \frac{(V_{IN}\, T_{ON})^2 f}{2\, P_{OUT}}$$

$$\text{since: } P_{OUT} = \frac{L I_{pk}^2 f}{2}$$

$$\text{and: } I_{pk} = \frac{V_{IN}\, T_{ON}}{L}$$

Where P_{OUT} includes the power dissipated in the catch diode (D1) as well as that in the load. If the inductance is too low, the current at L_X may exceed the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = \frac{V_{IN}\, T_{ON}}{I_{MAX}}$$

Where I_{MAX} = 525mA (peak L_X current) and T_{ON} is the on-time of the L_X output.

The most common MAX630 circuit is a boost mode converter (Figure 1). When the N-channel output device is on, the current linearly rises since:

$$\frac{di}{dt} = \frac{V}{L}$$

At the end of the on-time (14μs for 40kHz, 55% duty cycle oscillator) the current is:

$$I_{pk} = \frac{V\, T_{ON}}{L} = \frac{5V \times 14\mu s}{470\mu H} = 150mA.$$

The energy in the coil is:

$$E = \frac{L I_{pk}^2}{2} = 5.25\mu J$$

At maximum load this cycle is repeated 40,000 times per second, and the power tranferred through the coil is 40,000x5.25 = 210mW. Since the coil only supplies the voltage above the input voltage, at 15V, the DC-DC converter can supply 210mW/(15V-5V) = 21mA. The coil provides 210mW and the battery directly supplies another 105mW, for a total of 315mW of output power. If the load draws less than 21mA, the MAX630 turns on its output only often enough to keep the output voltage at a constant 15V.

Reducing the inductor value increases the available output current: lower L increases the peak current, thereby increasing the available power. The external inductor required by the MAX630 is readily obtained from a variety of suppliers. (See Table 1). Standard coils are suitable for most applications.

Types of Inductors

Molded Inductors

These are cylindrically wound coils which look similar to 1 watt resistors. They have the advantages of low cost and ease of handling, but have higher resistance, higher losses, and lower power handling capability than other types.

Potted Toroidal Inductors

A typical 1mH, 0.82 ohm potted toroidal inductor (Dale TE-3Q4TA) is 0.685" in diameter by 0.385" high and mounts directly onto a printed circuit board by its leads. Such devices offer high efficiency and mounting ease, but at a somewhat higher cost than molded inductors.

Ferrite Cores (Pot Cores)

Pot cores are very popular as switch-mode inductors since they offer high performance and ease of design. The coils are generally wound on a plastic bobbin, which is then placed between two pot core sections. A simple clip to hold the core sections together completes the inductor. Smaller pot cores mount directly onto printed circuit boards via the bobbin terminals. Cores come in a wide variety of sizes, often with the center posts ground down to provide an air gap. The gap prevents saturation while accurately defining the inductance per turn squared.

Pot cores are suitable for all DC-DC converters, but are usually used in the higher power applications. They are also useful for experimentation since it is easy to wind coils onto the plastic bobbins.

Toroidal Cores

In volume production the toroidal core offers high performance, low size and weight, and low cost. They are, however, slightly more difficult for prototyping, in that manually winding turns onto a toroid is more tedious than on the plastic bobbins used

with pot cores. Toroids are more efficient for a given size since the flux is more evenly distributed than in a pot core, where the effective core area differs between the post, side, top and bottom.

Since it is difficult to gap a toroid, manufacturers produce toroids using a mixture of ferromagnetic powder (typically iron or Mo-Permalloy powder) and a binder. The permeability is controlled by varying the amount of binder, which changes the effective gap between the ferromagnetic particles. Mo-Permalloy powder (MPP) cores have lower losses and are recommended for the highest efficiency, while iron powder cores are lower cost.

Table 1. Coil and Core Manufacturers

MANUFACTURER	TYPICAL PART #	DESCRIPTION
MOLDED INDUCTORS		
Dale	IHA-104	500μH, 0.5 ohms
Nytronics	WEE-470	470μH, 10 ohms
TRW	LL-500	500μH, 0.75 ohms
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 ohms
TRW	MH-1	600μH, 1.9 ohms
Torotel Prod.	PT 53-18	500μH, 5 ohms,
FERRITE CORES AND TOROIDS		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T²
Magnetics	555130	Tor. Core, 53nH/T²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T²

Note: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Diodes

In most MAX630 circuits, the inductor current returns to zero before L_X turns on for the next output pulse. This allows the use of slow turn-off diodes. On the other hand, the diode current abrubtly goes from zero to full peak current each time L_X switches off (figure 1, D1). To avoid excessive losses, the diode must therefore have a fast turn-on time.

For low power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well.

For higher current circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Filter Capacitor

The output voltage ripple has two components, with approximately 90° phase difference between them. One component is created by the change in the capacitor's stored charge with each output pulse. The other ripple component is the product of the capacitor's charge/discharge current and its ESR (effective series resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is generally larger than that caused by the change in charge.

$$V_{ESR} = I_{pk} \times ESR = \left(\frac{V_{IN}}{2Lf}\right) \times ESR \text{ (Volts p-p)}$$

Where V_{IN} is the coil input voltage, L is its inductance, f is the oscillator frequency, and ESR is the equivalent series resistance of the filter capacitor.

The output ripple resulting from the change in charge on the filter capacitor is:

$$V_{dQ} = \frac{Q}{C} \text{ where, } Q = t_{DIS} \times \frac{I_{peak}}{2}$$

$$\text{and, } I_{peak} = t_{CHG} \times \frac{V_{IN}}{L}$$

$$V_{dQ} = \frac{V_{IN}(t_{CHG})(t_{DIS})}{2LC}$$

Where t_{CHG} and t_{DIS} are the charge and discharge times for the inductor (1/2f can be used for nominal calculations).

Oscillator Capacitor, C_X

The oscillator capacitor, C_X, is a non-critical ceramic or silver mica capacitor. C_X can also be calculated by:

$$C_X = \frac{2.14 \times 10^{-6}}{f} - C_{INT} \; (C_{INT} \approx 5pF, \text{ see text})$$

Where f is the desired operating frequency in Hertz, and C_{INT} is the sum of the stray capacitance on the C_X pin and the internal capacitance of the package. The internal capacitance is typicaly 1pF for the plastic package and 3pF for the CERDIP package. Typical stray capacitances are about 3pF for normal printed circuit board layouts, but will be significantly higher if a socket is used.

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Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents can flow through the ground connection of the MAX630/4193. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and supply bypassing should be used for the device.

When large values (>50kΩ) are used for the voltage setting resistors, R1 and R2 of Figure 1, stray capacitance at the V_{FB} input can add a lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100pF to 10nF in parallel with R1 in Figure 1.

DC-DC Converter Configurations

DC-DC converters come in three basic topologies: buck, boost, and buck-boost (figure 2). The MAX630 is usually operated in the positive voltage boost circuit, where the output voltage is greater than the input.

The boost circuit is used where the input voltage is always less than the desired output and the buck circuit is used where the input is greater than the output. The buck-boost circuit inverts, and can be used with input voltages which are either greater or less than the output.

DC-DC converters can also be classified by the control method. The two most common are pulse width modulation (PWM) and pulse frequency modulation (PFM). PWM switch-mode power supply ICs (of which current mode control is one variant) are well established in high power off-line switchers. Both PWM and PFM circuits control the output voltage by varying duty cycle. In the PWM circuit the frequency is held constant and the width of each pulse is varied. In the PFM circuit, the pulse width is held constant and duty cycle is controlled by changing the pulse repetition rate.

The MAX630 refines the basic PFM by employing a constant frequency oscillator. Its output MOSFET is switched on when the oscillator is high and the output voltage is lower than desired. If the output voltage is higher than desired, the MOSFET output is disabled for that oscillator cycle. This "pulse skipping" varies the average duty cycle, and thereby controls the output voltage.

Note that, unlike the PWM ICs which use an op-amp as the control element, the MAX630 uses a comparator to compare the output voltage to an onboard reference. This reduces the number of external components, and operating current.

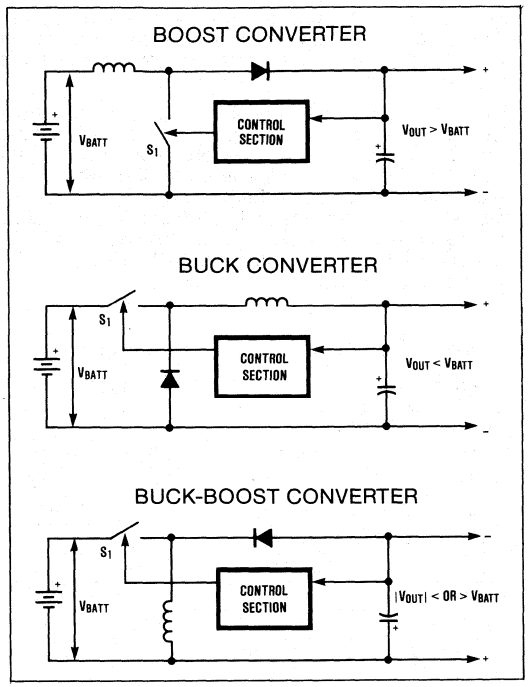

Figure 2. DC-DC Converter Configurations

Typical Applications

+5V to +15V DC-DC Converter

Figure 1 shows a simple circuit which generates +15V at approximately 20mA from a +5V input. The MAX630 has a ±1.5% reference accuracy, so the output voltage has an untrimmed accuracy of ±3.5% if R1 and R2 are 1% resistors. Other output voltages can also be selected by changing the feedback resistors. Capacitor C_X sets the oscillator frequency (47pF=40kHz), while C1 limits output ripple to about 50mV.

With a low cost molded inductor, the circuit's efficiency is about 75%, but an inductor with lower series resistance such as the Dale TE3Q4TA increases efficiency to around 85%. A key to high efficiency is that the MAX630 itself is powered from the +15V output. This provides the onboard N-channel output device with 15V gate drive, lowering its ON resistance to about 4 ohms. When +5V power is first applied, current flows through L1 and D1, supplying the MAX630 with 4.4V for startup.

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+5V to ±15V DC-DC Converter

The circuit in Figure 3 is similar to that of Figure 1 except that two more windings are added to the inductor. The 1408 (14mm x 8mm) pot core specified is an IEC standard size available from many manufacturers (see Table 1). The -15V output is semi-regulated, typically varying from -13.6V to -14.4V as the +15V load current changes from no load to 20mA.

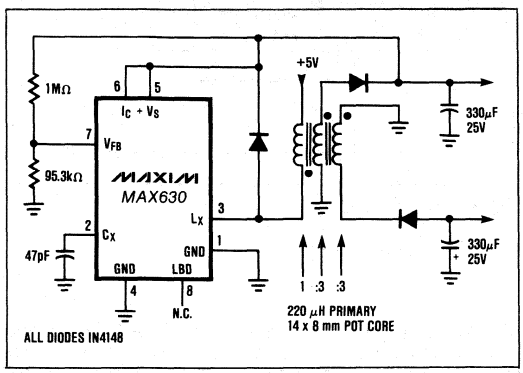


Figure 3. +5V to ±15V Converter

2½ Watt 3V to 5V DC-DC Converter

Some systems, although battery powered, need high currents for short periods, and then shutdown to a low power state. The extra circuitry of Figure 4 is designed to meet these high current needs. Operating in the buck-boost or flyback mode, the circuit converts -3V to +5V. The left side of the figure is similar to Figure 1, and supplies 15V for the gate drive of the external power MOSFET. This 15V gate drive ensures that the external device is completely turned on and has low ON resistance.

The right side of Figure 4 is a -3V to +5V buck-boost converter. This circuit has the advantage that when the MAX630 is turned off the output voltage falls to 0V, unlike the standard boost circuit where the output voltage is V_{BATT}-0.6V when the converter is shutdown. When shutdown, this circuit uses less than 10uA, with most of the current being the leakage current of the power MOSFET.

The inductor and output filter capacitor values have been selected to accomodate the increased power levels. With the values indicated, this circuit can supply up to 500mA at 5V, with an efficiency of 85%. Since the left side of the circuit powers only the right hand MAX630, the circuit will start up with battery voltages as low as 1.5V, independent of the loading on the +5V output.

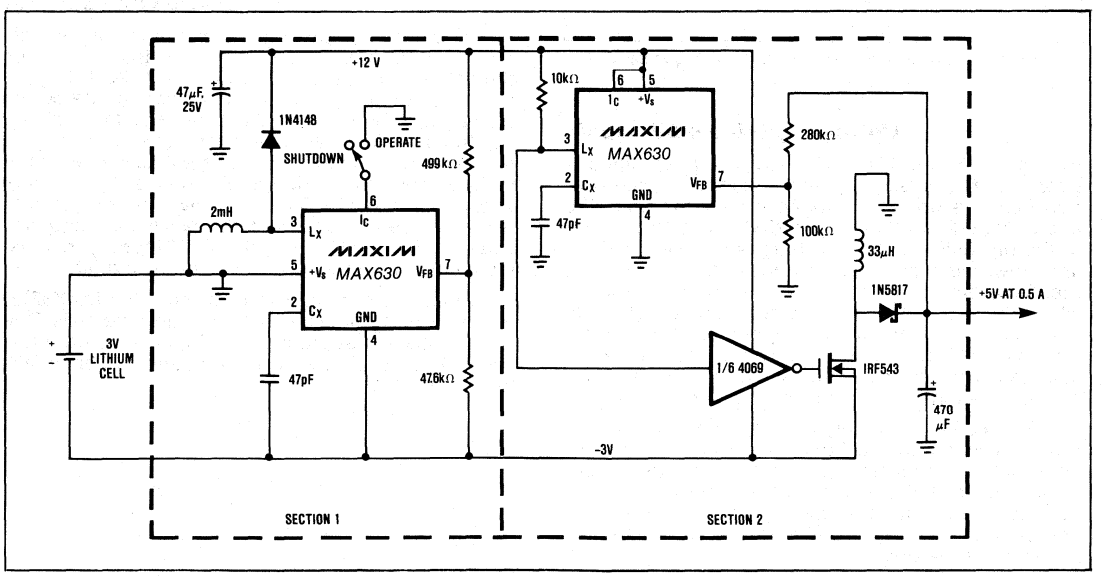


Figure 4. High Power 3V to 5V Converter with Shutdown

CMOS Micropower Step-Up Switching Regulator

+3V Battery to +5V DC-DC Converter

A common power supply requirement involves conversion of a 2.4 or 3V battery voltage to a 5V logic supply. The circuit in figure 5 converts 3V to 5V at 40mA with 85% efficiency. When I_C (pin 6) is driven low, the output voltage will be the battery voltage minus the drop across diode D1.

The optional circuitry using C1, R3, and R4 lowers the oscillator frequency when the battery voltage falls to 2.0V. This lower frequency maintains the output power capability of the circuit by increasing the peak inductor current, compensating for the reduced battery voltage.

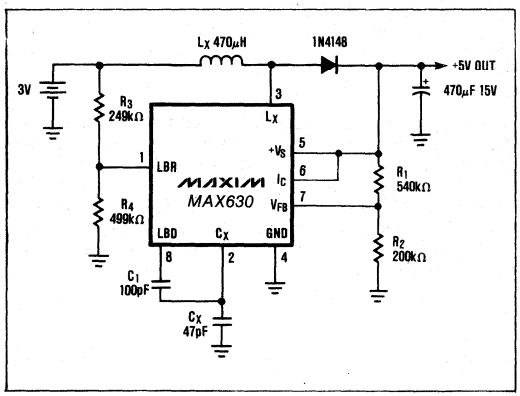


Figure 5. 3V to 5V Converter with Low-Battery Frequency Shift

Uninterruptable +5V Supply

In Figure 6 the MAX630 provides a continuous supply of regulated +5V, with automatic switch-over between line power and battery backup. When the line powered input voltage is at +5V, it provides 4.4V to the MAX630 and trickle charges the battery. If the line powered input falls below the battery voltage, the 3.6V battery supplies power to the MAX630, which boosts the battery voltage up to +5V, thus maintaining a continuous supply to the uninterruptable +5V bus. Since the +5V output is always supplied through the MAX630, there are no power spikes or glitches during power transfer.

The MAX630's low battery detector monitors the line powered +5V, and the LBD output can be used to shut down unnecessary sections of the system during power failures. Alternatively, the low battery detector could monitor the Nicad battery voltage and provide warning of power loss when the battery is nearly discharged.

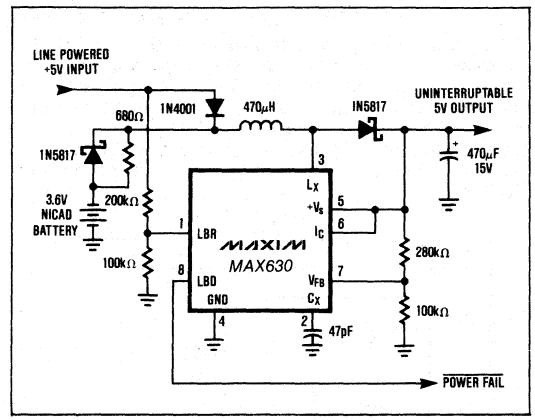


Figure 6. Uninterruptable +5V Supply

Unlike battery backup systems that use 9V batteries, this circuit does not need +12 or +15V to recharge the battery. Consequently, it can be used to provide +5V backup on modules or circuit cards which only have 5V available.

9V Battery Life Extender

Figure 7's circuit provides a minimum of 7V until the 9V battery voltage falls to less than 2V. When the battery voltage is above 7V the MAX630's I_C pin is low, putting it into the shutdown mode which draws only 10nA. When the battery voltage falls to 7V, the MAX8212 Voltage Detector's output goes high, enabling the MAX630. The MAX630 then maintains the output voltage at 7V even as the battery voltage falls below 7V. The low battery detector (LBD) is used to decrease the oscillator frequency when the battery voltage falls to 3V, thereby increasing the output current capability of the circuit.

Note that this circuit (with or without the MAX8212) can be used to provide 5V from 4 alkaline cells. The initial voltage is approximately 6V, and the output is maintained at 5V even when the battery voltage falls to less than 2V.

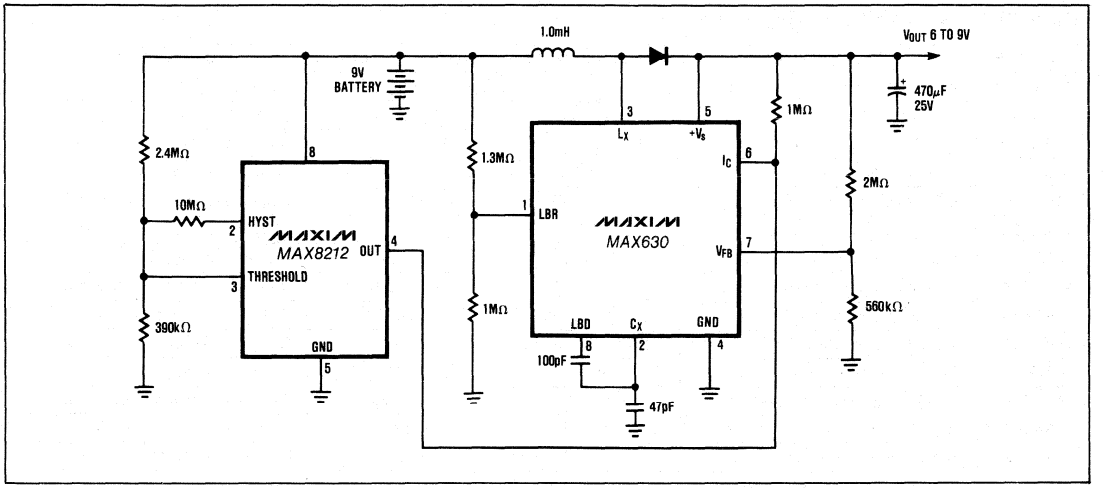


Figure 7. Battery Life Extension Down To 3V In

Dual Tracking Regulator

A MAX634 Inverting Regulator is combined with a MAX630 in Figure 8 to provide a dual tracking ±15V output from a 9V battery. The reference for the -15V output is derived from the positive output via R3 and R4. Both regulators are set to maximize output power at low battery voltage by reducing the oscillator frequency, via LBR, when V_{BATT} falls to 7.2V.

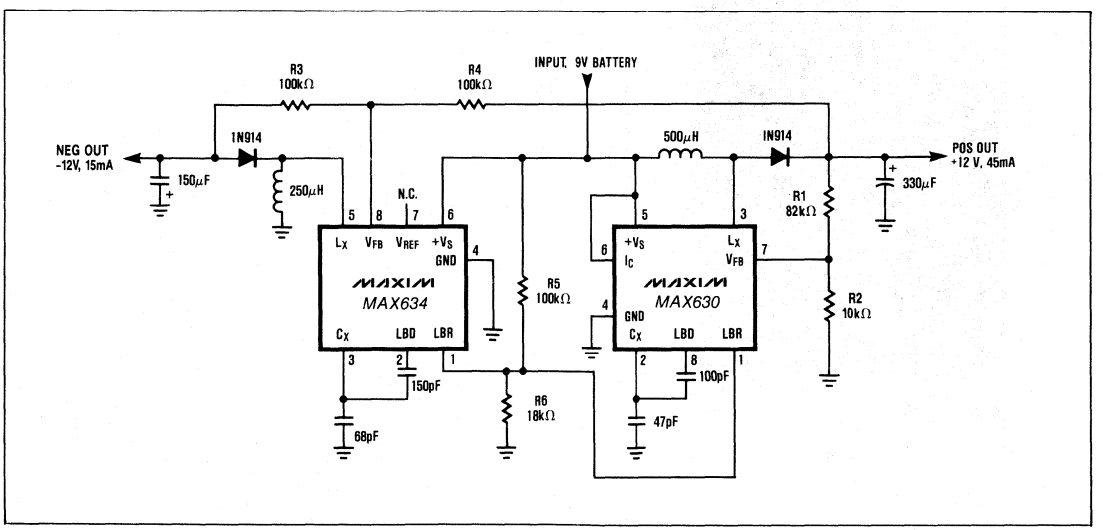


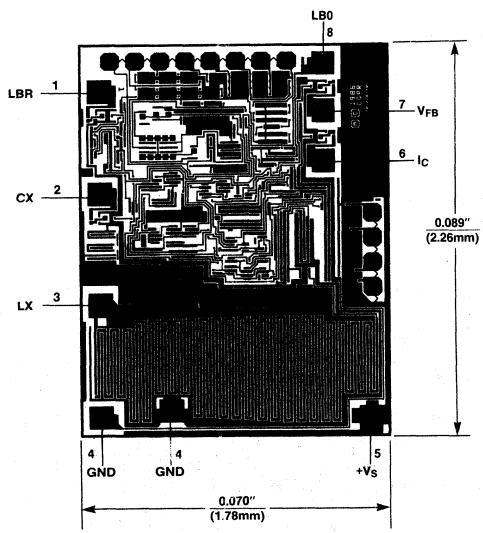
Figure 8. ±12V Dual Tracking Regulator

CMOS Micropower Step-Up Switching Regulator

Table 2. Maxim DC-DC Converters

DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

Chip Topography



MAXIM

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

General Description

Maxim's MAX631, MAX632, and MAX633 are +5V, +12V, and +15V fixed output, step-up DC-DC converters for use in low power, high efficiency switching regulator applications. All control and power switching functions are included in a compact 8-pin package: a bandgap reference, oscillator, voltage comparator, catch diode, and a 325mA (peak) N-channel MOSFET. The only external components required are an output filter capacitor and a low cost inductor. Also included on-chip are low battery detection circuitry and a charge pump output for generating a negative voltage in dual supply applications.

Though most simply used as fixed output regulators, the MAX631/32/33 can also be set for other output voltages by adding an external voltage divider. Maxim's proprietary Dual Mode™ circuitry allows both fixed and adjustable output operation in one device.

Maxim also manufactures fixed -5V, -12V, and -15V output, inverting DC-DC converters, as well as both positive and negative DC-DC converters with additional features such as external MOSFET drive for higher power, adjustable oscillator frequency, and logic level shutdown. See Table 3 on the last page of this data sheet for a summary of other DC-DC converter products.

Applications

Minimum Component, High Efficiency DC-DC Converters

Portable Instruments

Rechargeable and Primary Battery Power Conversion

Uninterruptable On-Board Power Supplies

Card Level Multiple Power Conversion

Features

- ♦ **High Efficiency — 80% Typical**
- ♦ **Only 2 External Components**
- ♦ **Fixed +5V, +12V, +15V Output Voltages**
- ♦ **Adjustable Output with Two Resistors**
- ♦ **Charge Pump for Negative Output**
- ♦ **Internal 450mA (peak) Power MOSFET**
- ♦ **Low Operating Current — 135μA Typical**
- ♦ **Compact 8-Pin Mini-DIP and Small Outline Packages**

Ordering Information

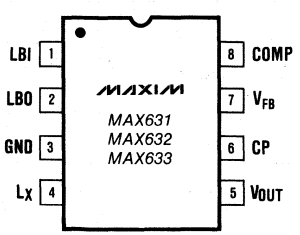
PART*	TEMP. RANGE	PACKAGE
MAX631XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX631XCSA	0°C to +70°C	8 Lead Small Outline
MAX631XC/D	0°C to +70°C	Dice
MAX631XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX631XESA	-40°C to +85°C	8 Lead Small Outline
MAX631XEJA	-40°C to +85°C	8 Lead CERDIP
MAX631XMJA	-55°C to +125°C	8 Lead CERDIP
MAX632XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX632XCSA	0°C to +70°C	8 Lead Small Outline
MAX632XC/D	0°C to +70°C	Dice
MAX632XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX632XESA	-40°C to +85°C	8 Lead Small Outline
MAX632XEJA	-40°C to +85°C	8 Lead CERDIP
MAX632XMJA	-55°C to +125°C	8 Lead CERDIP

*X = A for 5% Output Accuracy. X = B for 10% Accuracy.

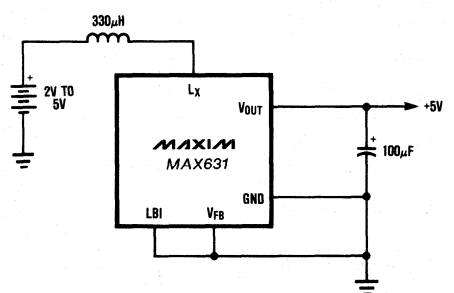
(Ordering Information continued on last page.)

Pin Configuration

Top View



Typical Operating Circuit



+5V Output DC-DC Converter

Dual Mode is a trademark of Maxim Integrated Products.

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{OUT} ..... +18V
Output Voltage, L_X and LBO ..... +18V
Input Voltage, Pins 1 and 7 ..... -0.3V to (V_{OUT} + 0.3V)
L_X Output Current ..... 450mA Peak
LBO Output Current 50mA
Operating Temperature Range
MAX63XXC ..... 0°C to +70°C
MAX63XXE ..... -40°C to +85°C
MAX63XXM ..... -55°C to +125°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage Range		Voltage at V_{OUT} Over Temperature (C, E) Over Temperature (M)	 2.0 2.4		 16.5 16.5	V
Startup Voltage		Voltage at V_{OUT} T_A = +25°C Over Temperature (C, E) Over Temperature (M)	 1.5 1.8 2.0	 1.3		V
Supply Current	I_S	L_X off, Over Temperature V_{OUT} = +5V V_{OUT} = +12V V_{OUT} = +15V		 0.135 0.5 0.75	 0.4 2.0 2.5	mA
Reference Voltage (Internal)		T_A = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
V_{OUT} Voltage		No Load, V_{FB} = GND Over Temperature MAX631A, MAX632A, MAX633A } 5% Output Accuracy MAX631B, MAX632B, MAX633B } 10% Output Accuracy	 4.75 11.4 14.25 4.5 10.8 13.5	 5.0 12.0 15.0 5.0 12.0 15.0	 5.25 12.6 15.75 5.5 13.2 16.5	V
Efficiency				80		%
Line Regulation (Note 1)		+0.5V_{OUT} < +V_S < V_{OUT}		0.08		% V_{OUT}
Load Regulation (Note 1)		V_S = +0.5V_{OUT}, P_{OUT} = 0 to 150mW		0.2		% V_{OUT}
Oscillator Frequency	f_O	V_{OUT} = +2V = +5V = +12V, +15V		35 45 50		kHz
Oscillator Duty Cycle				50		%
L_X ON Resistance	R_{ON}	I_X = 100mA, V_{OUT} = +5V = +15V		6 3.5	12 7	Ω
L_X Leakage Current	I_{XL}	V_4 = +16.5V T_A = +25°C Over Temperature (C, E) Over Temperature (M)		0.01	 1.0 30 100	μA
Diode Forward Voltage	V_F	I_F = 100mA,			1.0	V
CP ON Resistance		V_{OUT} = +5V, I_{OUT} = ±10mA V_{OUT} = +15V, I_{OUT} = ±30mA		70 30	140	Ω

Note 1: Guaranteed by correlation with DC pulse measurements.

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{FB} Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Input Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V_2 = +0.4V, V_1 = +1.1V T_A = 25°C Over Temperature	0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V_2 = +16.5V, V_1 = +1.4V		0.01	3.0	µA

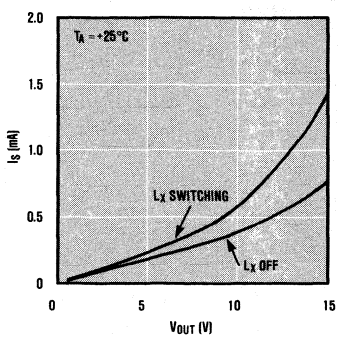
Pin Description

PIN	NAME	FUNCTION
1	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the Low Battery Detector threshold (1.31V), LBO (Pin 2) sinks current.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when the LBI (Pin 1) is below 1.31V.
3	Ground	Ground
4	L_X	This pin drives the external inductor with an internal N-channel power MOSFET. L_X has an output resistance of typically 6Ω and a peak current rating of 450mA.
5	V_{OUT}	The regulated DC-DC converter output.

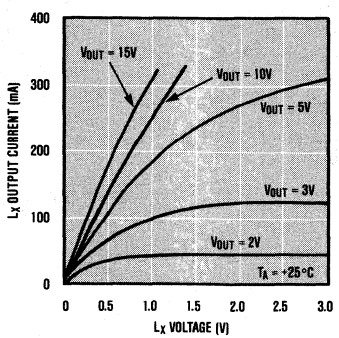
PIN	NAME	FUNCTION
6	CP	The Charge Pump output is a low impedance buffer which swings from GROUND to V_{OUT} at the oscillator frequency. Two external capacitors and diodes can be connected to generate a negative output voltage (See Figure 3).
7	V_{FB}	When V_{FB} is grounded, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected from the V_{OUT} to V_{FB} and GROUND, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between V_{OUT} and COMP reduces low frequency ripple and improves transient response.

Typical Operating Characteristics

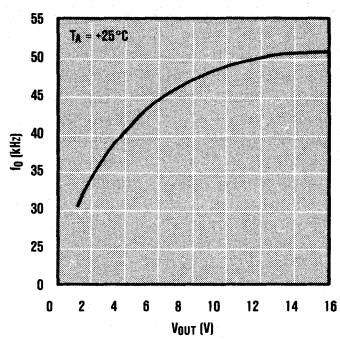
SUPPLY CURRENT vs. OUTPUT VOLTAGE



LX OUTPUT CURRENT vs. VOUT



OSCILLATOR FREQUENCY vs. OUTPUT VOLTAGE



CMOS Fixed/Adjustable Output Step-up Switching Regulators

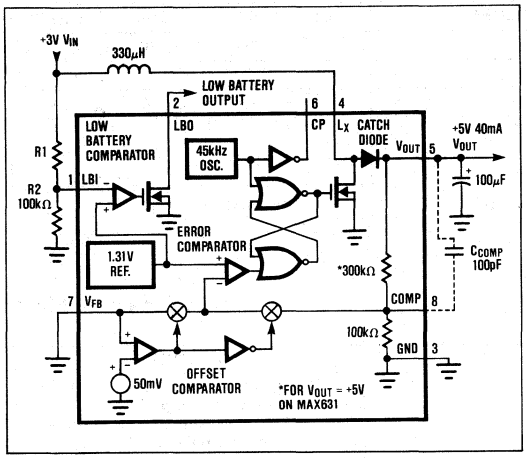


Figure 1. +3V to +5V Converter and Block Diagram

Detailed Description

The operation of the MAX631/32/33 can best be understood by examining the regulating loop of Figure 1. When the output voltage drops below the preset (or externally set) value, the Error Comparator switches high and connects the internal 45kHz Oscillator to the gate of the L_X output driver. The output device is a large N-channel MOSFET with a typical ON resistance of 6Ω and a current rating of 150mA (450mA peak). The following equation, which approximately determines the required peak current for a given application, provides a good rule of thumb to see if the MAX631/32/33's output device is suitable:

$$\frac{8\,(V_{OUT} - V_{IN})\,I_{OUT}}{V_{IN}} \leq 450mA$$

When activated, L_X turns on and off at the internal clock frequency. During each ON half cycle, the current through the inductor rises linearly, storing energy in the coil. When L_X switches off, the coil's magnetic field collapses, and voltage across the inductor reverses sign. The voltage at L_X then rises until the internal diode is forward biased, delivering power to the output. When the output voltage reaches the desired level, the Error Comparator inhibits L_X until the load discharges the output filter capacitor to less than the desired output level. See the Maxim MAX630 data sheet for further discussion on different types of DC-DC converters.

V_{IN}, Bootstrapped Operation

The MAX631/32/33 does not have a V_{IN} pin. Input power to start the DC-DC converter is supplied via the external inductor to the V_{OUT} pin. Once the converter has started, it is then powered from its own output. This "bootstrap" design ensures that the output MOSFET at L_X will have maximum gate drive and hence a minimum R_{ON}. It also allows the converter to start at lower input voltages.

V_{IN}, Greater Than V_{OUT}

If the regulator's input voltage is more than one forward diode drop greater than the desired output voltage, the L_X output will not turn on. Current will still be supplied to the load directly through the inductor and the internal diode, but without regulation. As long as the input is more than 0.6V above the desired output, the actual output voltage will be equal to the input voltage minus 0.6V.

Fixed or Adjustable Output

For operation at one of the preset output voltages (+5V for the MAX631, +12V for MAX632, and +15V for MAX633), V_{FB} is connected to GROUND. No external resistors are required.

For adjustable operation, other output voltages are selected by connecting an external voltage divider to V_{FB} as shown in Figure 2. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ

$$R3 = R4\left(\frac{V_{OUT}}{1.31V} - 1\right)$$

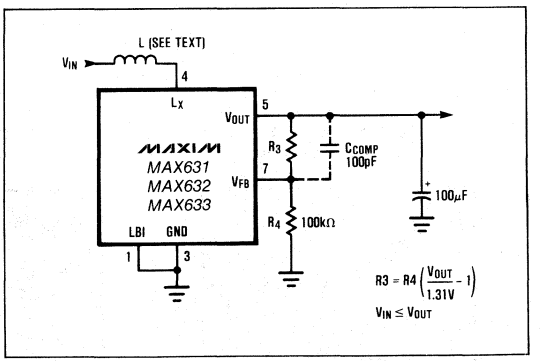


Figure 2. Connections for adjustable output

CMOS Fixed/Adjustable Output Step-up Switching Regulators

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input (LBI, Pin 1) with the internal 1.31V bandgap reference. The Low Battery Detector Output (LBO, Pin 2) goes low whenever the input voltage at LBI is less than 1.31V. The Low Battery detection voltage is set by resistors R1 and R2 (Figure 1).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ

$$R1 = R2\left(\frac{V_{LB}}{1.31V} - 1\right)$$ (V_{LB} is the desired Low Battery detection voltage)

Negative Output Voltage

The Charge Pump (CP) output, pin 6, is a low impedance buffer which swings from Ground to V_{OUT} at the oscillator frequency. Two external capacitors and diodes can be connected as shown in Figure 3, to generate a negative output voltage of $-(V_{OUT} - 1.2V)$ or a positive output of $2(V_{OUT} - 1.2V)$. 1.2V is the forward drop of two silicon diodes. Both circuits can be used at once if desired. With 10μF capacitors, the output impedance of V_{CP} is about 30 ohms. If space is critical, the capacitors can be reduced, but with a slight increase in output impedance and V_{CP} output ripple. See also Typical Applications, Figure 4 and 5.

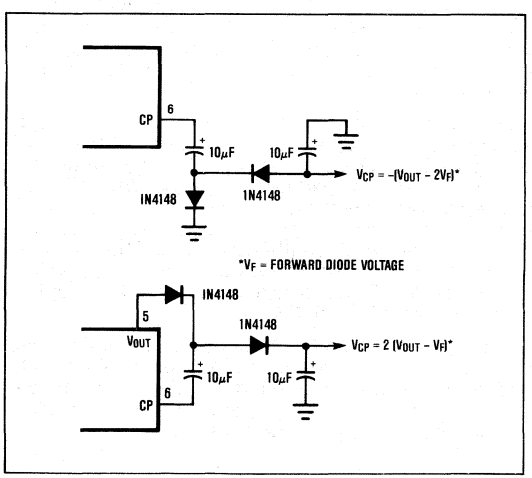


Figure 3. Using the Charge Pump (CP) output as a voltage inverter and/or doubler. Both circuits can be used together.

External Components

Inductor Selection

The available output current from a DC-DC voltage boost converter is a function of the input voltage, external inductor value, output voltage and the operating frequency. For most MAX631/32/33 applications the inductor is the only design variable since the operating frequency is fixed, and the input and output voltages are set by the application. The proper inductor must 1) have the correct inductance, 2) be able to handle the required peak currents, and 3) have acceptable series resistance and core losses.

When the MAX631/32/33's N-channel output device turns on, the coil current linearly rises since:

$$\frac{di}{dt} = \frac{V}{L}$$ where L is inductance in the coil.

At the end of the on-time, t_{ON}, the peak current, I_{pk}, is:

$$I_{pk} = \frac{V\,t_{ON}}{L} \quad \text{where: } t_{ON} = \frac{1}{2f_O}$$

The energy in the coil is:

$$E_L = \frac{L\,I_{pk}^2}{2}$$

At maximum load this cycle is repeated f_O (typically 45kHz) times per second, and the power transferred through the coil, $P_L = f_O \times E_L$. Since the coil only supplies the voltage above the input voltage:

$$I_{OUT} = \frac{P_L}{V_{OUT} - V_{IN}}$$

The DC-DC converter's output current is provided both by the inductor and directly from the battery. If the load draws less than the maximum current, L_X turns on only often enough to keep the output voltage at the desired level.

If the selected inductor has too high a value, the MAX631/32/33 will not be able to deliver the desired output power, even with the L_X output turned on for every oscillator cycle. The available output power can be increased by either raising the input voltage or lowering the inductance. This causes the current to rise at a faster rate, and results in a higher peak current at the end of each cycle. The available output power increases since it is proportional to the square of the peak inductor current. The maximum inductance therefore is:

$$L_{MAX} = \frac{V_{IN}^2}{8f_O\,P_L}$$

since: $P_L = \frac{L\,I_{pk}^2\,f_O}{2}$ and: $I_{pk} = \frac{V_{IN}}{2f_O\,L}$

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CMOS Fixed/Adjustable Output Step-up Switching Regulators

Remember that the required output power must include what is dissipated in the forward drop of the catch diode (V_F) as well:

$$P_{OUT} = I_{OUT}(V_{OUT} + V_F) = P_L + V_{IN}\ I_{OUT}$$

If the coil's inductance is too low, the current at L_X may rise above the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = \frac{V_{IN}}{2f_O\ I_{MAX}}\ (I_{MAX} = 450mA)$$

Table 2 shows nominal inductor parameters for a variety of input and output voltages. Values are given for both maximum output and maximum efficiency designs. In low power circuits where efficiency is not critical, a low cost molded inductor will suffice. For higher power circuits, or when high efficiency is required, pot cores and toroids should be used. See Tables 1 and 2 for typical part numbers and manufacturers. Refer to the Maxim MAX630 data sheet for additional information on inductor selection.

Table 1. Coil and Core Manufacturers

MANUFACTURER	TYPICAL PART #	DESCRIPTION
MOLDED INDUCTORS		
Dale	IHA-104	500μH, 0.5 ohms
Caddell-Burns	7070-29	220μH, 0.55 ohms
Gowanda	1B253	250μH, 0.44 ohms
TRW	LL-500	500μH, 0.75 ohms
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 ohms
TRW	MH-1	600μH, 1.9 ohms
Gowanda	050AT1003	100μH, 0.05 ohms
FERRITE CORES AND TOROIDS (Note 2)		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T²
Magnetics	555130	Tor. Core, 53nH/T²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T²

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 2: Permag Corp. is a distributor for many of the listed core and toroid manufacturers. (516) 822-3311.

Output Filter Capacitor

The MAX631/32/33's output ripple has two components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each L_X pulse. The other is the product of the capacitor's charge-discharge current and its ESR (equivalent series resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100 to 500μF range, in parallel with a 0.1μF ceramic capacitor. See the MAX630 data sheet for more information on output filter capacitors.

Catch Diode

The MAX631 series regulators contain an internal "catch" diode and therefore require no external diode for most applications. If desired however, an external diode can be connected in parallel with the internal diode at the L_X and V_{OUT} pins. A Schottky diode for example, with a low forward voltage drop, will provide some improvement in efficiency.

Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents flow through the ground connection to the MAX631/32/33. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and power supply bypassing should be used.

When large values (>50kΩ) are used for the voltage setting resistors (adjustable output mode), R3 and R4 of Figure 2, stray capacitance at the V_{FB} input can add a "lag" to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the V_{FB} node. It can also be remedied by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

The COMP input, pin 8, allows access to the internal voltage divider so that compensation can also be added when fixed output operation is used. A capacitor connected between V_{OUT} and COMP again adds a "lead" to the regulator's response.

Typical Applications

Basic Step-Up Circuits

Figure 1 shows the basic boost or step-up circuit for the MAX631, MAX632, and MAX633. The circuit is the same for Table 2 which shows values for typical input voltages and output currents.

Table 2. Inductor Selection for Common Designs

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	Eff. (%)	INDUCTOR P.N. (Note 1)	μH	Ω
2	5	5	78	CB 6860-21	470	0.4
2	5	10	74	G 1B253	250	0.44
2	5	15	61	G 1B103	100	0.25
3	5	25	82	CB 6860-21	470	0.4
3	5	40	75	CB 7070-29	220	0.55
3	12	5	79	CB 6860-19	330	0.35
3	12	10	79	CB 7070-28	180	0.48
5	12	12	88	CB 6860-21	470	0.4
5	12	25	87	CB 6860-19	330	0.35
3	15	5	73	CB 7070-29	220	0.55
3	15	8	71	CB 7070-27	150	0.43
5	15	10	85	CB 6860-21	470	0.4
5	15	15	85	CB 6860-19	330	0.35
8	15	35	90	G 1B503	500	0.56

Note 1: CB = Cadell-Burns, NY, (516)-746-2310
G = Gowanda Electronics Corp., NY, (716)-532-2234
Other Manufacturers Listed In Table 1

Plus and Minus Output Voltages

Both positive and negative output voltages can be generated with only one inductor when the charge pump (CP) output is connected as shown in Figure 4. The circuit provides approximately ±10mA with V_{OUT} = +15V, (MAX633), and ±15mA if V_{OUT} = +12V (MAX632). The negative output is about 3V less than V_{OUT} due to the forward voltage drop of the 1N4148 diodes and the output impedance of CP. Using Schottky diodes (IN5817) will increase the negative output by about 1V. The performance of the CP output is shown in Figure 5.

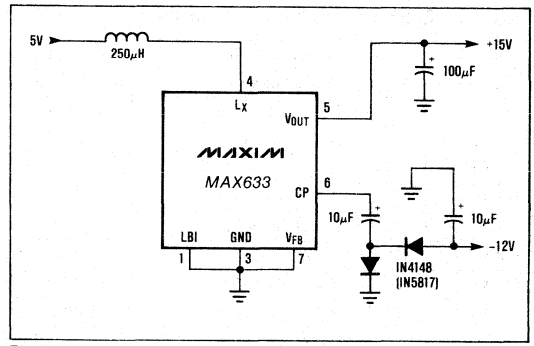

Figure 4. +5V to +15V/-12V Converter

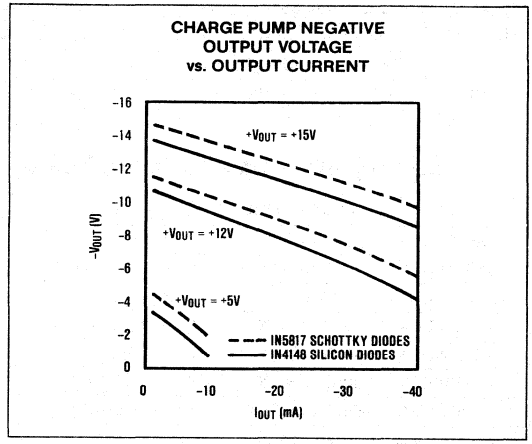

Figure 5. Charge Pump Negative Output Voltage vs. Current

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CMOS Fixed/Adjustable Output Step-up Switching Regulators

Table 3. Maxim DC-DC Converters

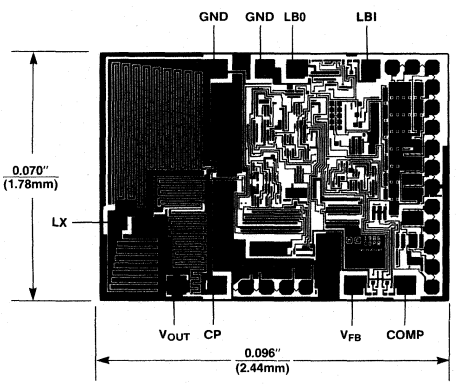
DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

Ordering Information (continued)

PART*	TEMP. RANGE	PACKAGE
MAX633XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX633XCSA	0°C to +70°C	8 Lead Small Outline
MAX633XC/D	0°C to +70°C	Dice
MAX633XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX633XESA	-40°C to +85°C	8 Lead Small Outline
MAX633XEJA	-40°C to +85°C	8 Lead CERDIP
MAX633XMJA	-55°C to +125°C	8 Lead CERDIP

**X = A for 5% Output Accuracy. X = B for 10% Accuracy.*

Chip Topography



MAXIM

CMOS Micropower Inverting Switching Regulator

General Description

Maxim's MAX634 and MAX4391 CMOS DC-DC regulators are designed for simple, efficient, inverting DC-DC converter circuits. The MAX634 and MAX4391 switching regulators provide all control and power handling functions in a compact 8 pin package: a 1.25V bandgap reference, an oscillator, a comparator for output voltage regulation, and a 525mA P-channel output MOSFET. A second comparator is also provided for convenient low battery detection.

The operating current is typically 100μA and is nearly independent of output switch current and duty cycle, thus ensuring high efficiency even in low power battery operated systems. Operating in the inverting configuration, the MAX634 and MAX4391 can convert a positive input voltage in the range of +3V to 16.5V to any negative output voltage up to -20V.

These devices are pin compatible enhancements of the Raytheon bipolar circuit, RC4391. Improvements include significantly higher efficiency, extended low voltage operation and improved output voltage accuracy (MAX634).

Maxim manufactures a broad line of DC-DC converters, including the MAX635, MAX636, and MAX637; which reduce the external component count in fixed -5V, -12V, and -15V output DC-DC converter circuits. See Table 2 on the last page of this data sheet for a summary of other Maxim DC-DC converters.

Applications

High Efficiency Battery Powered DC-DC Converters

Board Level, Local Power Supply Generation

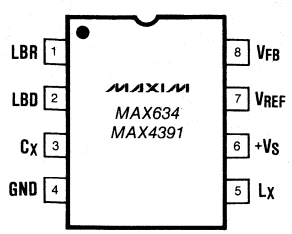
Regulated Negative Output Power Supplies

+5V to ±12V or ±15V Power Conversion

Regulated Voltage Inverters

Pin Configuration

Top View



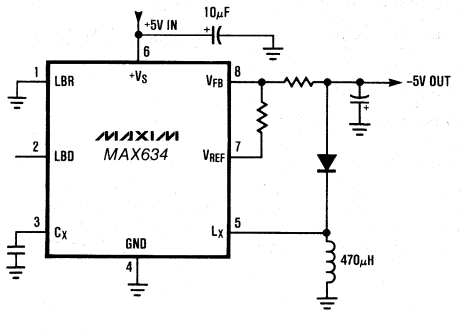
Features

- ◆ **Converts Positive Voltage to Negative Voltage**
- ◆ **Low Operating Current—100μA**
- ◆ **Compact 8 Pin MiniDIP and SO Packages**
- ◆ **High Efficiency—85% Typical**
- ◆ **Low Battery Detector**
- ◆ **4% Output Voltage Accuracy (MAX634)**
- ◆ **+3V to +16.5V Input Voltage Range**
- ◆ **Adjustable Output Voltage**
  - **—Up to -20V with Simple Coil**
  - **—Virtually Unlimited Voltage with Transformer**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX634C/D	0°C to +70°C	Dice
MAX634CPA	0°C to +70°C	8 Lead Plastic DIP
MAX634CSA	0°C to +70°C	8 Lead Small Outline
MAX634EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX634ESA	-40°C to +85°C	8 Lead Small Outline
MAX634EJA	-40°C to +85°C	8 Lead CERDIP
MAX634MJA	-55°C to +125°C	8 Lead CERDIP
MAX4391C/D	0°C to +70°C	Dice
MAX4391CPA	0°C to +70°C	8 Lead Plastic DIP
MAX4391CSA	0°C to +70°C	8 Lead Small Outline
MAX4391EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX4391ESA	-40°C to +85°C	8 Lead Small Outline
MAX4391EJA	-40°C to +85°C	8 Lead CERDIP
MAX4391MJA	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



+5V to -5V Converter

CMOS Micropower Inverting Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) ..... +18V
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Operating Temperature Range
MAX634C, MAX4391C ..... 0°C to +70°C
MAX634E, MAX4391E ..... -40°C to +85°C
MAX634M, MAX4391M ..... -55°C to +125°C

Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW
Input Voltage, Pins 1, 3, 8 (Note 2) ..... -0.3V to $+V_S$ +0.3V
L_X Output Current ..... 525mA Peak
LBD Output Current 50mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +6.0V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX634 MIN.	MAX634 TYP.	MAX634 MAX.	MAX4391 MIN.	MAX4391 TYP.	MAX4391 MAX.	UNITS
Supply Voltage (Note 1)	$+V_S$		2.3		16.5	4.0		16.5	V
Supply Current	I_{IN}	No External Loads $+V_S$ = 4.0V $+V_S$ = 16.5V		70 150	150 500		90 170	250 500	µA
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V $V_{OUT\ nom}$ = -15.0V	-5.20 -15.70		-4.80 -14.30	-5.35 -15.85		-4.65 -14.15	V
Line Regulation (Note 4)		$V_{OUT\ nom}$ = -5.0V V_{IN} = 5.0V to 15V			2.0			3.0	$\%V_{OUT}$
Load Regulation (Note 4)		$V_{OUT\ nom}$ = -5.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW $V_{OUT\ nom}$ = -15.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW			0.4 0.14			0.4 0.14	$\%V_{OUT}$
Reference Voltage			1.22	1.25	1.28	1.18	1.25	1.32	V
Switch Current	I_{SW}	Pin 5 = 5.0V	75	150		75	150		mA
Switch Leakage Current	I_{CO}	Pin 5 = -18V, $+V_S$ = 6V		0.01	1.0		0.01	5.0	µA
Capacitor Charging Current	I_{CX}			30			30		µA
C_X + Threshold Voltage				$+V_S$ - 0.1			$+V_S$ - 0.1		V
C_X - Threshold Voltage				0.1			0.1		V
Operating Frequency Range (Note 3)	F_O		0.1		75	0.1		75	kHz
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1000		250	600		µA
Low Battery Output Leakage	I_{LBDO}	V_8 = 16.5V, V_1 = 1.4V		0.01	3.0		0.01	5.0	µA
Low Battery Input Threshold	V_{LBR}			1.25			1.25		V
Low Battery Input Bias Current	I_{LBR}			0.01	10		0.01	10	nA
Feedback Input Bias Current	I_{FB}			0.01	10		0.01	10	nA
Efficiency		Figure 2		80			80		%

Note 1: In addition to the Absolute Maximum rating of +18V, the input voltage also must not exceed 24 - $|-V_{OUT}|$.
Note 2: The input voltage limit may be exceeded provided input current is limited to less than 1mA.
Note 3: The operating frequency range is guaranteed by design and verified with sample testing.
Note 4: Guaranteed by correlation with DC pulse measurements.

ELECTRICAL CHARACTERISTICS

(+V_S = +6.0V, full operating temperature range unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX634 MIN.	MAX634 TYP.	MAX634 MAX.	MAX4391 MIN.	MAX4391 TYP.	MAX4391 MAX.	UNITS
Supply Voltage (Note 5)	$+V_S$		2.6		16.5	4.0		16.5	V
Supply Current	I_{IN}	No External Loads $+V_S$ = 4.0V $+V_S$ = 16.5V			150 500			250 500	µA
Reference Voltage	V_{REF}		1.18	1.25	1.32	1.13	1.25	1.36	V
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V $V_{OUT\ nom}$ = -15.0V	-5.25 -16.0		-4.75 -14.0	-5.5 -16.5		-4.5 -13.5	V
Line Regulation		$V_{OUT\ nom}$ = -5.0V $+V_S$ = 5.0V to 15V			3.0			4.0	$\%V_{OUT}$
Load Regulation		$V_{OUT\ nom}$ = -5.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW $V_{OUT\ nom}$ = -15.0V $+V_S$ = 4.5V, C_X = 350pF P_{LOAD} = 0mW to 75mW			0.5 0.3			0.5 0.3	$\%V_{OUT}$
Switch Leakage Current	I_{CO}	Pin 5 = -18V, $+V_S$ = 6V		0.01	20			30	µA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500			250			µA
Low Battery Output Leakage	I_{LBDO}	V_8 = 16.5V, V_1 = 1.4V			3			5	µA

Note 5: In addition to the Absolute Maximum rating of +18V, the input voltage also must not exceed 24 - | $-V_{OUT}$|.

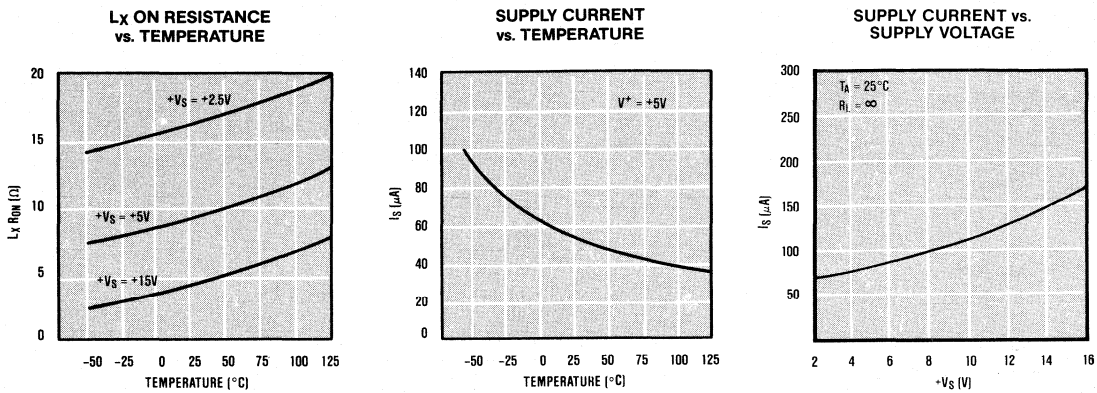
Pin Description

PIN	NAME	FUNCTION
1	LBR	Low Battery Detection comparator input. The LBD output, pin 2, sinks current when this pin is below the low battery detector threshold of 1.25V.
2	LBD	The Low Battery Detector output is an open drain N-channel MOSFET which sinks current when the LBR input, pin 1, is below 1.25V.
3	C_X	An external capacitor connected between this terminal and ground sets the oscillator frequency. 47pF = 40kHz
4	GND	Ground.
5	L_X	External Inductor output driver. The internal P-channel MOSFET which drives this pin has an output resistance of 8Ω and a peak current rating of 525mA.

PIN	NAME	FUNCTION
6	$+V_S$	The positive supply voltage, from +3V to +16.5V (MAX634). The total voltage difference between the negative output voltage and the positive input voltage must be less than 24V.
7	V_{REF}	The Voltage REFerence output is 1.25V, generated by an on-chip bandgap reference.
8	V_{FB}	The output voltage is set by an external resistive divider connected to the Voltage Feedback input, pin 8. The MAX634/MAX4391 will pulse the L_X ouput whenever the voltage at this terminal is above Ground.

CMOS Micropower Inverting Switching Regulator

Typical Operating Characteristics



Detailed Description

Principle of Operation

Figure 1 shows a simplified buck-boost voltage inverter, sometimes called an inverting or flyback converter. When the switch is closed a charging current flows through the inductor, creating a magnetic field. When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. Since the switch is now open, the current must flow through the diode, thereby charging the capacitor with a negative voltage. The current linearly decays to zero and the magnetic field collapses as the energy stored in the inductor is transferred to the output filter capacitor.

The MAX634 controls the magnitude of the negative output voltage by turning the switch on and off only when the output voltage has fallen below the desired value.

Basic Circuit Operation

Figure 2 shows the standard circuit for converting a positive input voltage into a negative voltage. When the feedback voltage at pin 8 is above ground, the P-channel MOSFET at pin 5 turns on during the next low-going period of the oscillator. The P-channel MOSFET delivers current to the external inductor, storing energy in its magnetic field. When the oscillator output goes high, the P-channel MOSFET turns off, and the "kickback" of the inductor pulls current through diode D1, negatively charging the output filter capacitor, C1. This cycle repeats until the output voltage pulls the feedback input, pin 8, below ground.

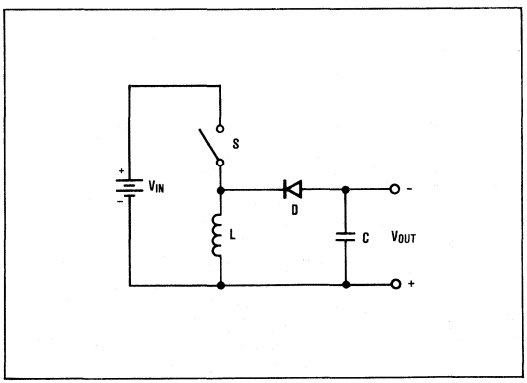


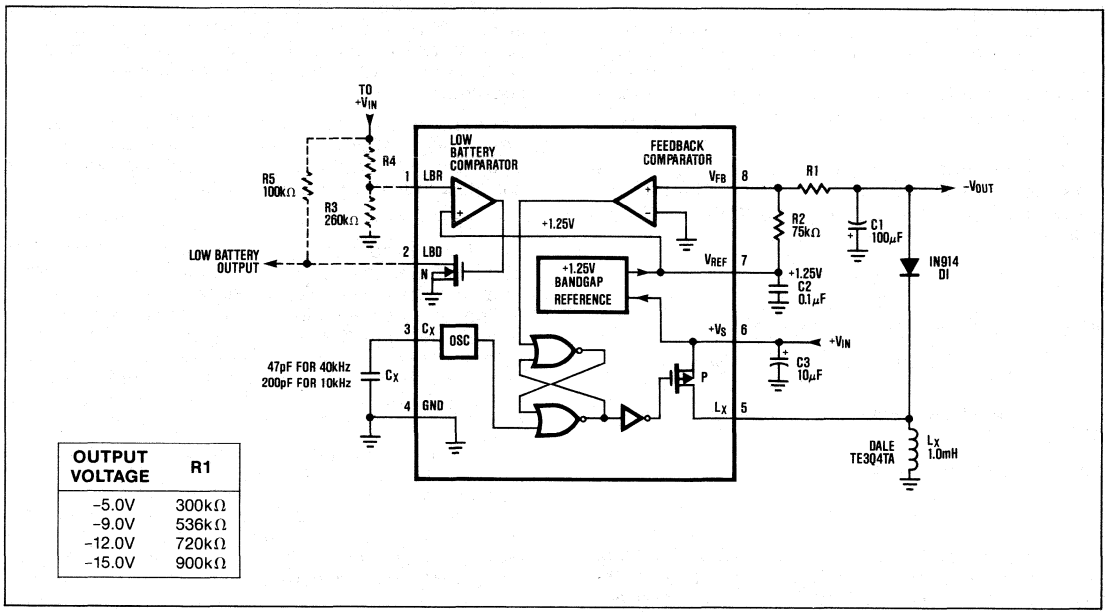
Figure 1. Simplified Voltage Inverter

The NOR gate latch prevents high frequency oscillations by not allowing L_X to switch repeatedly during an oscillator cycle.

The output voltage is determined by the internal 1.25V reference and the ratio of the resistors R1 and R2.

$$V_{OUT} = 1.25V \times \frac{R1}{R2}$$

Capacitor C1 is the output filter capacitor. The capacitance and ESR (equivalent series resistance) of C1 determine the output ripple. C2 and C3 are bypass capacitors; while C_X sets the oscillator frequency.



OUTPUT VOLTAGE	R1
-5.0V	300kΩ
-9.0V	536kΩ
-12.0V	720kΩ
-15.0V	900kΩ

Figure 2. Standard Application Circuit

Oscillator

The MAX634/MAX4391 oscillator uses only one external component, a capacitor C_X connected between pin 3 and Ground. A value of 47pF sets the oscillator frequency to approximately 40kHz.

The oscillator can also be externally driven with a CMOS gate which swings from ground to $+V_S$. The L_X output is always off when the C_X pin is externally driven high.

Low Battery Detector

The Low Battery Detector (LBD) Output (pin 2, Figure 2) sinks current whenever the input voltage at Low Battery Resistor (pin 1) is less than +1.25V. The LBR input is a high impedance CMOS input, with less than 10nA leakage current. The LBD output is an open drain N-channel MOSFET with about 500Ω of output resistance. The operating voltage of the low battery detector can be adjusted using an external voltage divider as shown in Figure 2. If hysteresis is desired, add a resistor between pins 1 and 2.

$$V_{LOBATT} = 1.25V \times (1 + \frac{R4}{R3}) \text{ or,}$$

$$R4 = R3 \times (\frac{V_{LOBATT}}{1.25V} - 1)$$

where V_{LOBATT} is the operating voltage of the low battery detector, and R3 is usually between 10kΩ and 10MΩ, with a typical value being 470kΩ.

External Component Selection

Inductor Value

The available output current from an inverting DC-DC voltage converter is determined by the value of the external inductor, the output voltage, the input voltage, and the operating frequency. The inductor must 1) have the correct inductance, 2) be able to handle the peak currents, and 3) have acceptable series resistance and core losses.

$$L_{MAX} = \frac{(V_{IN}\, T_{ON})^2\, f}{2\, P_{OUT}}$$

$$L_{MIN} = \frac{V_{IN}\, T_{ON}}{I_{MAX}}$$

where I_{MAX} is the maximum allowable peak L_X current (525mA).

Contrary to what most people would expect at first glance, reducing the inductor value increases the available output current: lower L increases the peak current, thereby increasing the available power. If the inductance is too high, the MAX634/MAX4391 will not be able to deliver the desired output power,

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even with the L_X output turned on with each oscillator cycle. The available output power can be increased by either decreasing the inductance or by decreasing the frequency. Decreasing the frequency increases the on period of the L_X output, thereby increasing the peak inductor current, which in turn increases the available output power since the output power is proportional to the square of the peak inductor current.

The most common MAX634 circuit is the buck-boost voltage inverter (Figure 2). When the P-channel output device is on, the current in the inductor linearly rises since:

$$\frac{di}{dt} = \frac{V}{L}$$

At the end of the on period the current is

$$I_{pk} = \frac{V_{IN}\ T_{on}}{L} = \frac{5V \times 50\mu s}{1mH} = 250mA$$

assuming a 10kHz, 50% duty cycle oscillator and $+V_S = 5V$

The energy in the coil is:

$$E = \frac{1}{2} L\ I_{pk}^2 = 31.2\mu J$$

At maximum load this cycle is repeated 10,000 times per second, and the power transferred through the coil is 10,000 x 31.2μJ = 312mW. If the output voltage is -5V, then 312/5 = 62.5mA of output current is available, ignoring losses and component tolerances. In a practical circuit, 50mA of output current is available at -5V.

The external inductor required by the MAX634/MAX4391 is readily obtained from a variety of suppliers. (See Table 1.)

Types of Inductors

Molded Inductors

These are cylindrically wound coils which look similar to 1 watt resistors. They have the advantages of low cost and ease of handling, but have higher resistance, higher losses, and lower power handling capability than other types.

Potted Toroidal Inductors

A typical 1mH, 0.82 ohm potted toroidal inductor (Dale TE-3Q4TA) is 0.685" in diameter by 0.385" high and mounts directly onto a printed circuit board by its leads. Such devices offer high efficiency and mounting ease, but at a somewhat higher cost than molded inductors.

Ferrite Cores (Pot Cores)

Pot cores are very popular as switch-mode inductors since they offer high performance and ease of design. The coils are generally wound on a plastic bobbin, which is then placed between two pot core sections. A simple clip to hold the core sections together completes the inductor. Smaller pot cores mount directly onto printed circuit boards via the bobbin terminals. Cores come in a wide variety of sizes, often with the center posts ground down to provide an air gap. The gap prevents saturation while accurately defining the inductance per turn squared.

Pot cores are suitable for all DC-DC converters, but are usually used in the higher power applications. They are also useful for experimentation since it is easy to wind coils onto the plastic bobbins.

Toroidal Cores

In volume production the toroidal core offers high performance, low size and weight, and low cost. They are, however, slightly more difficult for prototyping, in that manually winding turns onto a toroid is more tedious than on the plastic bobbins used with pot cores. Toroids are more efficient for a given size since the flux is more evenly distributed than in a pot core, where the effective cross sectional area differs between the post, side, top and bottom.

Since it is difficult to gap a toroid, manufacturers produce toroids using a mixture of ferromagnetic powder (typically iron or Mo-Permalloy powder) and a binder. The permeability is controlled by varying the amount of binder, which changes the effective gap between the ferromagnetic particles. Mo-Permalloy powder (MPP) cores have lower losses and are recommended for the highest efficiency, while iron powder cores are lower cost.

Table 1. Coil and Core Manufacturers

MANUFACTURER	TYPICAL PART #	DESCRIPTION
MOLDED INDUCTORS		
Dale	IHA-104	500μH, 0.5 ohms
Caddell-Burns	6860-19	330μH, 0.33 ohms
TRW	LL-500	500μH, 0.75 ohms
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 ohms
TRW	MH-1	600μH, 1.9 ohms
Torotel Prod.	PT 53-18	500μH, 5 ohms
FERRITE CORES AND TOROIDS		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T²
Magnetics	555130	Tor. Core, 53nH/T²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T²

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

External Diode

In most MAX634 circuits the inductor current returns to zero before L_X turns on for the next output pulse. This allows the use of slow turn-off diodes. On the other hand, the diode current abruptly goes from zero to full peak current each time L_X switches off (Figure 2, D1). To avoid excessive losses during turn-on, the diode must have a fast turn-on time.

The 1N914 or 1N4148 is suitable for low power applications. The 1N5817 series of Schottky diodes or their equivalent are suitable for higher power applications. Rectifier diodes such as the 1N4001 series are unacceptable since their slow turn-on results in excessive losses.

Filter Capacitor

The output filter capacitor (C1 in Figure 2) stores the energy delivered by the inductor, and delivers current to the load. The output voltage ripple is directly affected by the capacitance and the equivalent series resistance (ESR) of the output filter capacitor.

The output voltage ripple has two components, with approximately 90° phase difference. One ripple component is created by the change in stored charge in the capacitor with each output pulse. The other ripple component is the product of the capacitor charge/discharge current times the ESR (effective series resistance) of the capacitor. With low cost aluminum electrolytic capacitors, the ESR produced ripple is generally larger than the ripple from the change in charge.

$$V_{ESR} = I_{pk} \times ESR \text{ (Volts P-P)}$$

$$= \left(\frac{V_{IN}}{2LF}\right) \times ESR \text{ (Volts P-P)}$$

where V_{IN} is the input voltage to the coil, L is the inductance of the coil, f is the oscillator frequency, and ESR is the equivalent series resistance of the output filter capacitor.

The output ripple resulting from the change in charge on the filter capacitor is:

$$V_{dQ} = \frac{Q}{C} \text{ where: } Q = t_{DIS} \times \frac{I_{peak}}{2}$$

$$\text{and: } I_{peak} = t_{CHG} \times \frac{V_{IN}}{L}$$

$$V_{dQ} = \frac{V_{IN}(t_{CHG})(t_{DIS})}{2LC}$$

where t_{CHG} and t_{DIS} are the charge and discharge times for the inductor (1/(2f) can be used for norminal calculations).

Oscillator Capacitor, C_X

The oscillator capacitor can be a low cost ceramic capacitor. If the circuit will be operated over a wide temperature range, an capacitor with a low temperature coefficient of capacitance should be used.

The value of C_X can be calculated using the formula:

$$C_X = \frac{2.14 \times 10^{-6}}{f} - C_{INT}$$

where f is the desired operating frequency in Hertz, and C_{INT} is the sum of the stray capacitance on the C_X pin and the internal capacitance of the package. The internal capacitance is about 1pF for the plastic package and 3pF for the CERDIP package. Typical stray capacitance is about 3pF for normal printed circuit board layouts, but will be significantly higher if a socket is used.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that the peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external current boosting transistors. Inductor saturation leads to very high current levels through the external boost transistors, causing excessive power dissipation, poor efficiency, and possible damage to the inductor and the external transistor.

Test for saturation by applying the maximum load, the maximum input voltage, and (for a safety margin) lowering the clock frequency by 25%. Monitor the inductor current using a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates. It is this rapid current increase and the resultant high peak currents that can damage the inductor and the external boost transistor.

Bypassing and Compensation

The high operating current pulses in the L_X output and the external inductor can cause erratic operation unless the MAX4391/MAX634 is properly bypassed. Connect a 10µF bypass capacitor directly across the MAX4391 between pin 6 ($+V_S$) and pin 4 (Ground) to minimize the inductance and high frequency impedance of the power source. Make sure that the high current ground return path of the inductor does not cause a voltage drop in the MAX4391 ground line.

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The reference voltage output, pin 7, should also be bypassed to ground to avoid coupling to the high current path that includes the L_X output, the inductor, and its ground return.

With light loads, coupling from the high power circuit into the control circuitry may cause the output pulses to occur in bursts, thereby increasing low frequency ripple and degrading the line and load regulation. Normal operation with evenly distributed output pulses can be restored by adding a 100pF to 10nF compensation capacitor across the feedback resistor, R1. Minimizing the stray capacitance on the V_{FB} terminal will often eliminate the need for this compensation capacitor.

Typical Applications

-5V Output Regulated Voltage Inverter

The standard circuit in Figure 2 will deliver 50mA at -5V. Efficiency is 85% when using a low loss pot core or toroidal inductor such as the Dale TE3Q4TA series. Using a low cost molded inductor with several ohms series resistance reduces the efficiency to 70%.

-12V and -15V Output DC-DC Inverters

The circuit of Figure 2 can also be used for -12V or -15V outputs by simply changing the value of R1 in the feedback network using the formula

$$R1 = \frac{V_{OUT}\ R2}{1.25V}$$

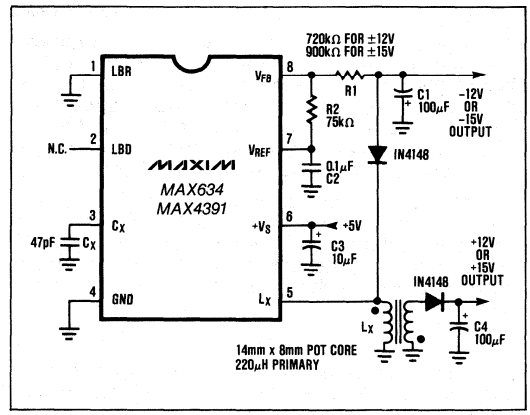

Figure 3. Dual Output, ±12V or ±18V DC-DC Converter

Dual Output, ±12V or ±15V DC-DC Converters

The buck-boost configuration of the MAX634 is well suited for dual output DC-DC converters. As shown in Figure 3, all that is needed is a second winding on the inductor. Typically, this second winding is bifilar (primary and secondary are wound simultaneously using two wires in parallel). The inductor core is usually a toroid or a pot core, see Table 1.

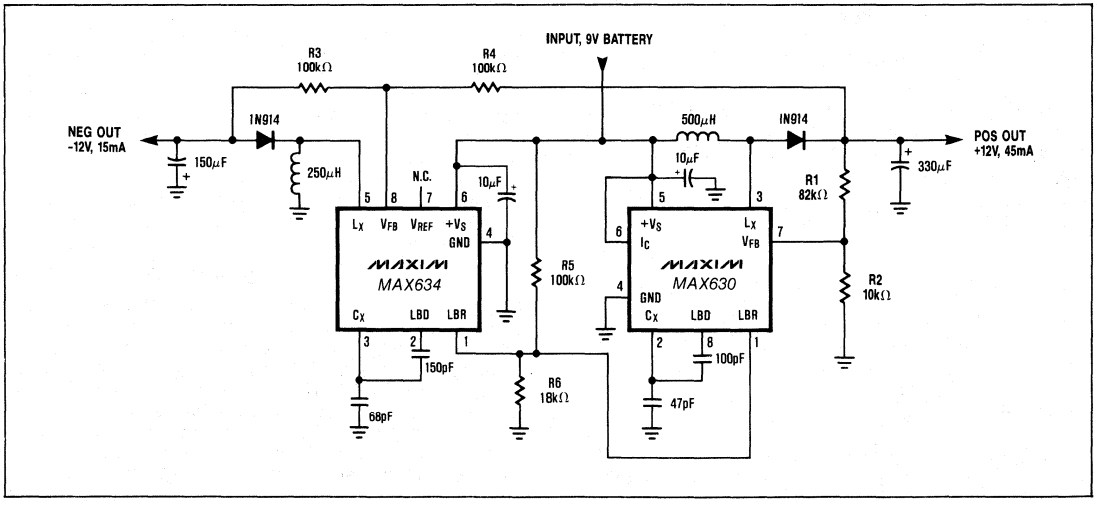

Figure 4. ±12V Dual Tracking Regulator

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The negative output voltage is fully regulated by the MAX634. The positive voltage is semi-regulated, and will vary slightly with load changes on either the positive or negative outputs. See the MAX630 data sheet for a similar circuit with a fully regulated positive output and a semi-regulated negative output. If both outputs must be fully regulated use both a MAX634 and a MAX630, as shown in Figure 4.

Voltage Inverter

In Figure 5, the negative output voltage tracks the positive input voltage. This circuit performs the same function as Maxim's ICL7660, but with better output regulation and higher output current capability. With the circuit components shown, Figure 5 will deliver approximately 50mA at -9V when the input is +9V, and about 30mA at -5V when the input is +5V.

Input voltage tracking is achieved by using the positive input voltage as the reference instead of the onboard bandgap reference.

The output voltage is set by the input voltage, R1, and R2 as follows:

$$V_{OUT} = -\frac{R2}{R1} \times +V_S$$

Low Power Shutdown

Unlike the MAX630, the MAX634 and MAX4391 do not have a logic level shutdown pin, but a low power mode can easily be implemented as shown in Figure 6. Since the operating current is only 250μA maximum, the GND pin can be driven directly by a CMOS gate or N-channel FET. Drive GND low for normal operation; let it float or drive it high to enter the low power shutdown mode. In low power shutdown the MAX634 circuit draws only the leakage current of the L_X output.

The Ground pin should be well bypassed and any voltage drop across the CMOS gate adds to the reference voltage, slightly increasing the regulated output voltage.

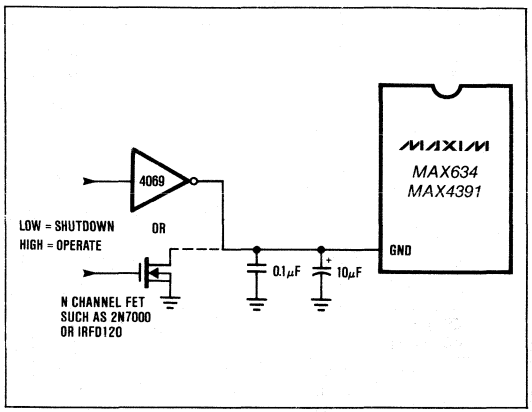


Figure 6. Low Power Shutdown

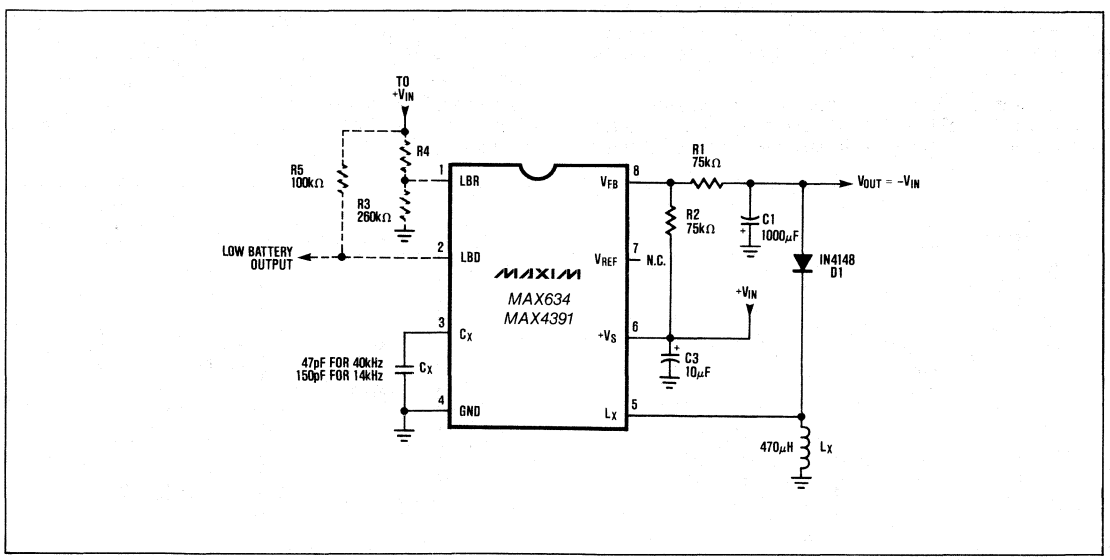
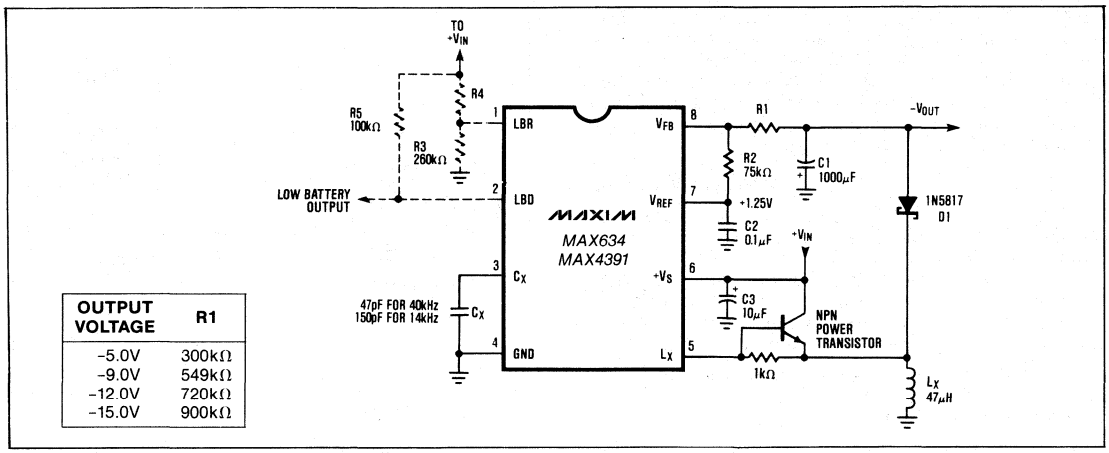


Figure 5. Regulated Voltage Inverter

CMOS Micropower Inverting Switching Regulator



OUTPUT VOLTAGE	R1
-5.0V	300kΩ
-9.0V	549kΩ
-12.0V	720kΩ
-15.0V	900kΩ

Figure 7. Boosting Output Power With External NPN Power Transistor

Boosting Output Power With External Power Devices

The MAX634 and MAX4391 are limited to a maximum switch current of 525mA. If higher current, or output resistance less than the 6 ohms of the MAX634 is required, the circuits of Figures 7, 8, or 9 can be used.

The circuit of Figure 7 uses an NPN bipolar transistor to boost the output current. All of the NPN transistor base current is used to drive the inductor, but the voltage drop across the transistor will be approxmately 0.7V.

The circuit of Figure 8 uses a low resistance N-channel MOSFET in a transformer coupled voltage inverter circuit. This circuit has the advantage that a positive output voltage can also be obtained by simply adding a diode and an output filter capacitor. The -15V output is fully regulated for both line and load variations; the +20V output voltage will varies with changes in load on either the +20V or -15V output, as well as changes in the +5V input. This variation is normally less than 10%.

High Output Voltage

The circuit in Figure 9 converts any positive voltage from +3V to +16V to any desired output voltage, as long as the voltage breakdown of the external P-Channel MOSFET is not exceeded. This circuit is also useful for generating a high power, high efficiency -12V or -15V output using a simple one winding coil.

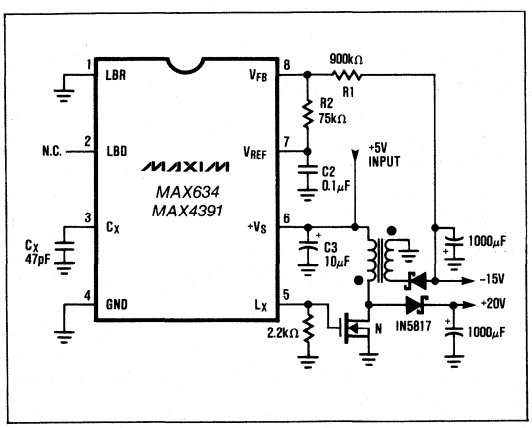


Figure 8. High Power +5V to -15V DC-DC Converter

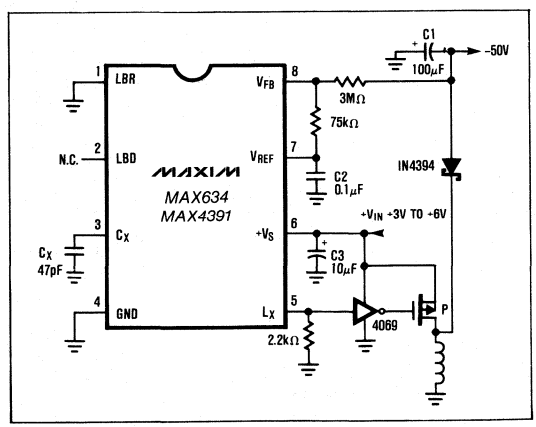


Figure 9. Boosting Voltage External P-Channel MOSFET

Operating with Wide Input Voltage Range

The available output power varies as the square of the input voltage. The Low Battery Detector can compensate for a reduction in input voltage by lowering the oscillator frequency, as shown in Figure 10. With the values shown, the oscillator frequency is 40kHz when the input voltage is above 6V. When the input falls below 6V, the Low Battery Detector (LBD) output goes low, placing the 100pF capacitor in parallel with C_X, reducing the oscillator frequency to 14kHz. This increases the available output power by a factor of 3.

This circuit can be used with any of the other application circuits in this data sheet.

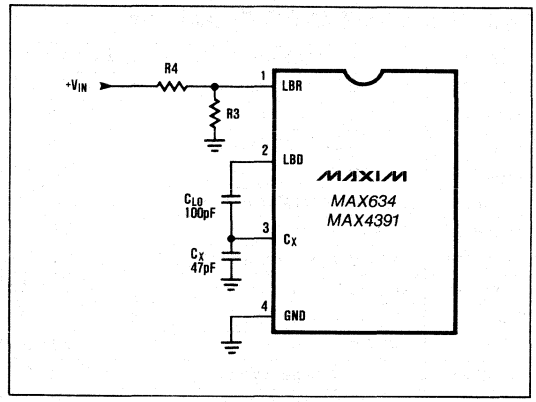
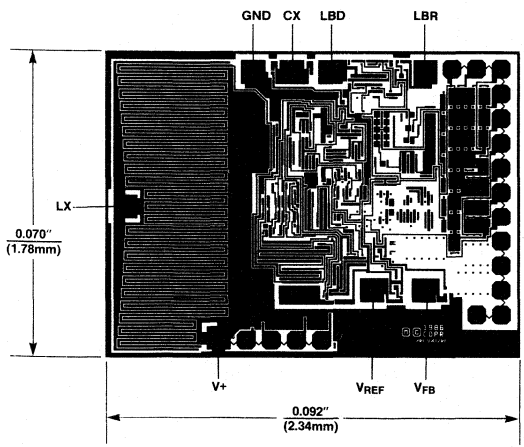


Figure 10. Wide Input Voltage Range Operation with Variable Frequency Oscilator.

Chip Topography



CMOS Micropower Inverting Switching Regulator

Table 2. Maxim DC-DC Converters

DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

MAXIM

Fixed Output CMOS Inverting Switching Regulators

General Description

Maxim's MAX635, MAX636, and MAX637 are -5V, -12V, and -15V fixed output, inverting DC-DC converters for use in low power, high efficiency switching regulator applications. All control and power switching functions are included in a compact 8-pin package: a bandgap reference, oscillator, feedback voltage comparator, and 525mA (peak) P-channel MOSFET. The only external components required are a diode, output filter capacitor, and low cost inductor. Convenient low battery detection circuitry is also included on-chip.

Though most simply used as fixed output regulators, the MAX635/36/37 can also be set for other output voltages by adding an external voltage divider. Maxim's proprietary Dual Mode™ circuitry allows both fixed and adjustable output operation in one device.

Maxim also manufactures a series of +5V, +12V, and +15V DC-DC converters, as well as both positive and negative output switching regulators with additional features such as external MOSFET drive for higher power, adjustable oscillator frequency, and logic level shutdown. See Table 3 on the last page of this data sheet for a summary of other DC-DC Converter Products.

Applications

Minimum Component, High Efficiency DC-DC Converters

+5V to -5V, +12V to -12V or -15V Conversion

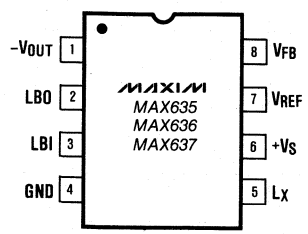
Portable Instruments

Rechargeable and Primary Battery Power Conversion

Board Level Low Power DC to DC Conversion

Pin Configuration

Top View



Features

- ◆ **High Efficiency — 85% Typical**
- ◆ **Only 3 External Components**
- ◆ **Fixed -5V, -12V, -15V Output Voltages**
- ◆ **Adjustable Output with Two Resistors**
- ◆ **Internal 525mA (peak) Power MOSFET**
- ◆ **Low Operating Current — 80μA Typical**
- ◆ **Compact 8-Pin Mini-DIP and Small Outline Packages**
- ◆ **Low Battery Detector**

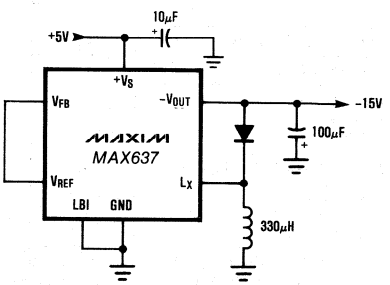
Ordering Information

PART*	TEMP. RANGE	PACKAGE
MAX635XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX635XCSA	0°C to +70°C	8 Lead Small Outline
MAX635XC/D	0°C to +70°C	Dice
MAX635XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX635XESA	-40°C to +85°C	8 Lead Small Outline
MAX635XEJA	-40°C to +85°C	8 Lead CERDIP
MAX635XMJA	-55°C to +125°C	8 Lead CERDIP
MAX636XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX636XCSA	0°C to +70°C	8 Lead Small Outline
MAX636XC/D	0°C to +70°C	Dice
MAX636XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX636XESA	-40°C to +85°C	8 Lead Small Outline
MAX636XEJA	-40°C to +85°C	8 Lead CERDIP
MAX636XMJA	-55°C to +125°C	8 Lead CERDIP

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy

(Ordering information continued on last page.)

Typical Operating Circuit



+5V to -15V Converter

Fixed Output CMOS Inverting Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ (Note 1) ..... +18V
Input Voltage, Pins 2, 3, 8 ..... -0.3V to ($+V_S$ + 0.3V)
L_X Output Current ..... 525mA Peak
LBO Output Current 50mA
Operating Temperature Range
MAX63XXC ..... 0°C to +70°C
MAX63XXE ..... -40°C to +85°C
MAX63XXM ..... -55°C to +125°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Note 1)	$+V_S$	T_A = +25°C Over Temperature	2.3 2.6		16.5 16.5	V
Supply Current	I_S	No Load, L_X off, Over Temperature $+V_S$ = +5V $+V_S$ = +15V		 80 260	 150 500	µA
Reference Voltage	V_{REF}	T_A = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
V_{OUT} Voltage (Note 2)		No Load, V_{FB} = V_{REF}, Over Temperature MAX635A, MAX636A, MAX637A (5% Output Accuracy) MAX635B, MAX636B, MAX637B (10% Output Accuracy)	 -4.75 -11.4 -14.25 -4.5 -10.8 -13.5	 -5.0 -12.0 -15.0 -5.0 -12.0 -15.0	 -5.25 -12.6 -15.75 -5.5 -13.2 -16.5	V
Efficiency				85		%
Line Regulation (Note 2)		+5V < $+V_S$ < +15V		0.5		% V_{OUT}
Load Regulation (Note 2)		P_{OUT} = 0mW to 150mW		0.2		% V_{OUT}
Oscillator Frequency	f_O	$+V_S$ = +5V $+V_S$ = +15V		50 70		kHz
Oscillator Duty Cycle				50		%
L_X ON Resistance	R_{ON}	I_X = 100mA, $+V_S$ = +5V $+V_S$ = +15V		9 4	16 8	Ω
L_X Leakage Current	I_{XL}	$+V_S$ = +16.5V T_A = +25°C Over Temperature		0.01	1.0 30	µA
V_{FB} Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V_2 = +0.4V, V_3 = +1.1V T_A = +25°C Over Temperature	 0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V_2 = +16.5V, V_3 = +1.4V		0.01	3.0	µA

Note 1: In addition to the Absolute Maximum rating of +18V, the input voltage also must not exceed 24V - $|-V_{OUT}|$.
Note 2: Guaranteed by correlation with DC pulse measurements.

Fixed Output CMOS Inverting Switching Regulators

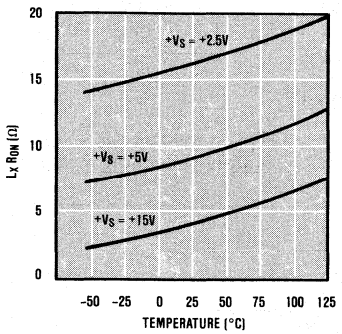
Pin Description

PIN	NAME	FUNCTION
1	$-V_{OUT}$	The sense INPUT for fixed output operation. Although it is connected to output of the DC-DC converter (Figure 2), V_{OUT} does not supply current. It is internally connected to the on-chip voltage divider.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when the LBI (Pin 3) is below +1.31V.
3	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the Low Battery Detector threshold (+1.31V), LBO (Pin 2) sinks current.
4	GND	Ground.

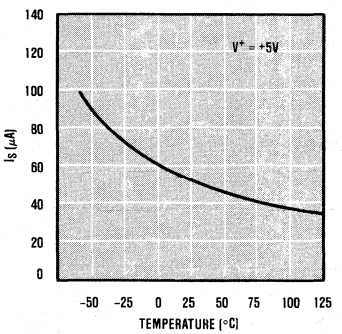
PIN	NAME	FUNCTION
5	L_X	This pin drives the external inductor with an internal P-channel power MOSFET. L_X has an output resistance of typically 6Ω and a peak current rating of 525mA.
6	$+V_S$	The positive Supply Voltage, from +2V to +16.5V. The total difference between the negative output voltage and the positive input must be less than 24V.
7	V_{REF}	The Voltage Reference output is +1.31V, generated by an on-chip bandgap reference.
8	V_{FB}	When V_{FB} is tied to V_{REF}, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected from the $-V_{OUT}$ to V_{FB} and V_{REF}, this pin becomes the feedback input for adjustable output operation.

Typical Operating Characteristics

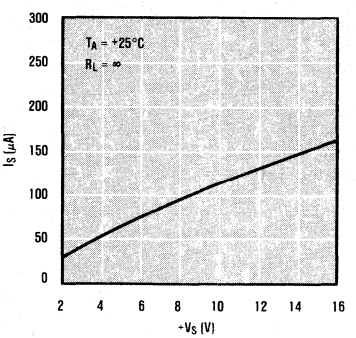
L_X ON RESISTANCE vs. TEMPERATURE



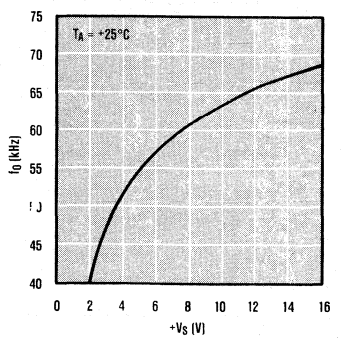
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



6

Fixed Output CMOS Inverting Switching Regulator

Detailed Description

Principle of Operation

Figure 1 shows a simplified buck-boost voltage inverter, sometimes called an inverting or flyback converter. When the switch is closed a charging current flows through the inductor, creating a magnetic field. When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. Since the switch is now open, the current must flow through the diode, thereby charging the capacitor with a negative voltage. The current linearly decays to zero and the magnetic field collapses as the energy stored in the inductor is transferred to the output filter capacitor.

The MAX635/36/37 controls the magnitude of the negative output voltage by turning the switch on and off only when the output voltage has fallen below the desired value.

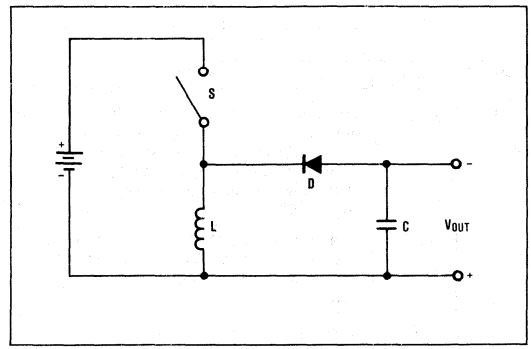


Figure 1. Simplified Inverting Converter

Basic Circuit Operation

Figure 2 shows the standard circuit for converting a positive input voltage into a negative voltage. When the voltage at V_{OUT} is higher than the desired level, the MOSFET at L_X (Pin 5) turns on during the next low-going period of the oscillator. L_X delivers current to the external inductor, storing energy in its magnetic field. When the oscillator output goes high, the MOSFET turns off, but current continues to flow in the inductor and diode D1, negatively charging the output filter capacitor, C1. This cycle repeats until the output voltage reaches the desired negative value. The NOR gate latch prevents high frequency oscillations by not allowing L_X to switch repeatedly during an oscillator cycle.

Low Battery Detector

The Low Battery Output, LBO (Pin 2), sinks current whenever the input voltage at Low Battery Input, LBI (Pin 3), is less than +1.31V. LBI is a high impedance CMOS input, with less than 10nA leakage current. LBO is an open drain N-channel MOSFET with about 500Ω of output resistance. The operating voltage of the Low Battery Detector can be adjusted using an external voltage divider as shown in Figure 2. If hysteresis is desired, add a resistor between pins 2 and 3.

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$R1 = R2\left(\frac{V_{LB}}{1.31V} - 1\right)$$

(V_{LB} is the desired Low Battery detection voltage)

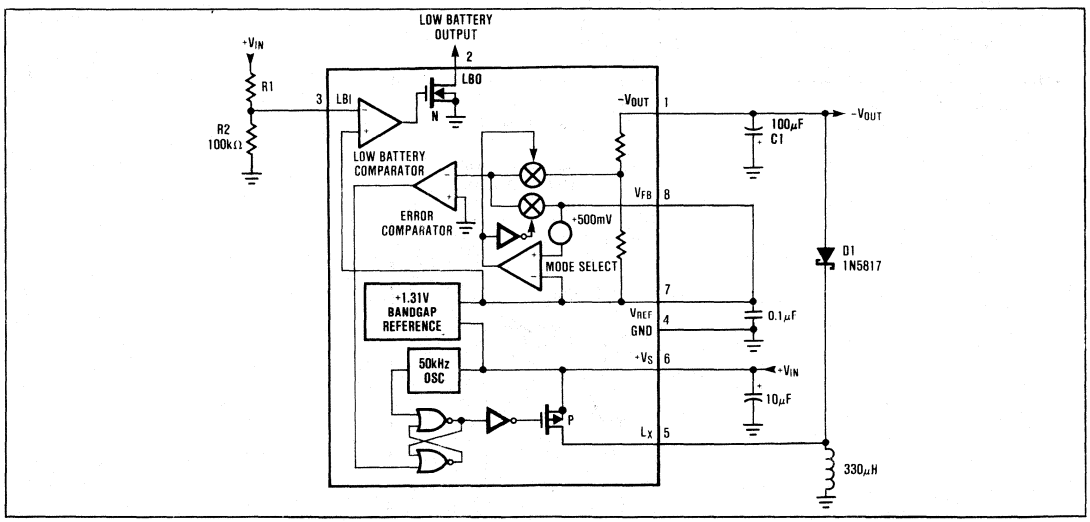


Figure 2. MAX635/36/37 Block Diagram and Typical Circuit

Fixed or Adjustable Output

For operation at one of the preset output voltages (-5V for the MAX635, -12V for MAX636, and -15V for MAX637), V_{FB} is connected to V_{REF}. No external resistors are required.

For adjustable operation, other output voltages are selected by connecting an external voltage divider to V_{FB} as shown in Figure 3. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$V_{OUT} = -1.31V \times \frac{R3}{R4}$$

External Components

Inductor Selection

The available output current from an inverting DC-DC voltage converter is a function of the input voltage, external inductor value, output voltage and the operating frequency. For most MAX635/36/37 applications the inductor is the only design variable since the operating frequency is fixed, and the input and output voltages are set by the application. The proper inductor must 1) have the correct inductance, 2) be able to handle the required peak currents, and 3) have acceptable series resistance and core losses.

When L_X's P-channel output device turns on, the coil current linearly rises since:

$$\frac{di}{dt} = \frac{V_{IN}}{L}$$ where L is inductance of the coil.

At the end of the on-time, t_{ON}, the peak current, I_{pk}, is:

$$I_{pk} = \frac{V_{IN}\, t_{ON}}{L} \quad \text{where: } t_{ON} = \frac{1}{2f_O}$$

The energy in the coil is:

$$E_L = \frac{L\, I_{pk}^2}{2}$$

At maximum load this cycle is repeated f_O (typically 50kHz) times per second, and the power transferred through the coil is $P_L = f_O \times E_L$. The output current, ignoring losses:

$$I_{OUT} = \frac{P_L}{V_{OUT}} = \frac{V_{IN}^2}{8F_O V_{OUT} L}$$

If the load draws less than the maximum current, L_X turns on only often enough to keep the output voltage at the desired level.

If the selected inductor has too high a value, the MAX635/36/37 will not be able to deliver the desired output power, even with the L_X output turned on for every oscillator cycle. The available output power can be increased by either raising the input voltage or lowering the inductance value. This causes the current to rise at a faster rate, and results in a higher peak current at the end of each cycle. The available output power increases since it is proportional to the square of the peak inductor current. The maximum inductance therefore is:

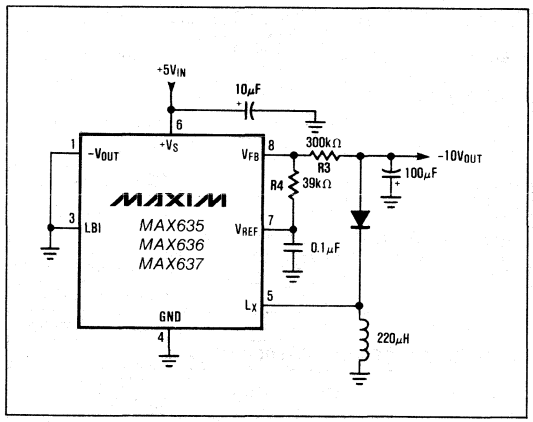


Figure 3. Adjustable Output Operation

$$L_{MAX} = \frac{V_{IN}^2}{8f_O P_L}$$

since: $P_L = \frac{L\, I_{pk}^2 f_O}{2}$ and: $I_{pk} = \frac{V_{IN}}{2f_O L}$

If the coil's inductance is too low, the current at L_X may rise above the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = \frac{V_{IN}}{2f_O I_{MAX}} \quad \text{where } I_{MAX} = 525mA$$

Table 1 lists some coil manufacturers and typical part numbers. Table 2 shows nominal inductor parameters for a variety of input and output voltages using the basic circuit of figure 2. In low power circuits where efficiency is not critical, a low cost molded inductor will suffice. For high power circuits, or when high efficiency is required, pot cores or toroids should be used. Refer to the MAX630 data sheet for additional information on types of inductors.

Fixed Output CMOS Inverting Switching Regulator

Table 1. Coil and Core Manufacturers

MANUFACTURER	TYPICAL PART #	DESCRIPTION
MOLDED INDUCTORS		
Dale	IHA-104	500μH, 0.5 ohms
Caddell-Burns	7070-29	220μH, 0.55 ohms
Gowanda	1B253	250μH, 0.44 ohms
TRW	LL-500	500μH, 0.75 ohms
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 ohms
TRW	MH-1	600μH, 1.9 ohms
Gowanda	050AT1003	100μH, 0.05 ohms
FERRITE CORES AND TOROIDS (Note 2)		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T²
Magnetics	555130	Tor. Core, 53nH/T²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T²

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 2: Permag Corp. is a distributor for many of the listed core and toroid manufacturers. (516) 822-3311

Table 2. Inductor Selection for Common Designs

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	Eff. (%)	INDUCTOR P.N. (Note 1)	μH	Ω
+3	-5	5	60	6860-19	330	0.35
+5	-5	25	76	6860-19	330	0.35
+9	-5	40	79	6860-19	330	0.35
+12	-5	45	85	6860-21	470	0.40
+15	-5	50	90	6860-23	680	0.55
+5	-12	12	74	6860-19	330	0.35
+9	-12	30	84	6860-19	330	0.35
+12	-12	40	89	6860-21	470	0.40
+3	-15	2	65	6860-21	470	0.40
+5	-15	8	77	6860-19	330	0.35
+9	-15	25	85	6860-19	330	0.35

Note 1: Caddell-Burns N.Y. (516) 746-2310

External Diode

In most DC-DC converter circuits the current in the "catch" diode abruptly goes from zero to its peak value each time L_X switches off (Figure 2, D1). To avoid excessive losses the diode must have a fast turn-on time. For low power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher current circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Output Filter Capacitor

The MAX635/36/37's output ripple has two components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each L_X pulse. The other is the product of the capacitor's charge-discharge current and its ESR (equivalent series resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100 to 500μF range, in parallel with a 0.1μF ceramic capacitor. See the MAX630 data sheet for more information on output filter capacitors.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boosting transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

Fixed Output CMOS Inverting Switching Regulator

Bypassing and Compensation

The high current pulses in the L_X output and the external inductor can cause erratic operation unless the MAX635/36/37 is properly bypassed. Connect a 10μF bypass capacitor directly across the device between $+V_S$ (Pin 6) and Ground (Pin 4) to minimize the inductance and high frequency impedance of the power source. Also make sure that the high current ground return path of the inductor does not cause a voltage drop in the regulator's ground line.

The reference voltage output, V_{REF} (Pin 7), should be bypassed to ground with 0.1μF, again avoiding coupling to the high current path that includes the L_X output, the inductor, and its ground return.

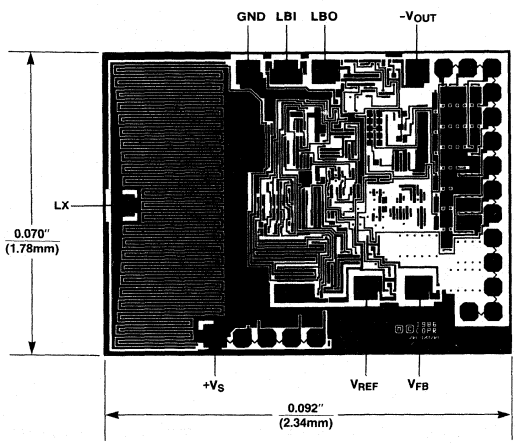
When large values (>50kΩ) are used for the voltage setting resistors (R3 and R4 of Figure 3) in the adjustable output mode, stray capacitance at the V_{FB} input can add a "lag" to the feedback response, destabilizing the regulator and causing output pulses to occur in bursts. This increases low frequency ripple and lowers efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the V_{FB} node. Normal operation with evenly distributed output pulses can be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

Typical Applications

Basic Inverting DC-DC Converters

Figure 2 shows the basic voltage inverting circuit for the MAX635, MAX636, and MAX637. The circuit is the same for Table 2 which shows inductor values for typical input and output voltages. Note that there is no restriction on the relationship between the input and output voltage as is the case with step-up and step-down DC-DC converters. $+V_S$ can be greater or less than $|-V_{OUT}|$.

Chip Topography



Low Power Shutdown

A low power shutdown mode can easily be implemented with the MAX635/36/37 as shown in Figure 4. Since the Ground pin current is only 500μA max., Ground can be driven directly by a CMOS gate or N-channel FET. Ground is driven low for normal operation, and driven high or allowed to float for shutdown mode. When shut down, the inverter draws only the leakage current of the L_X output.

Note that any voltage drop across the CMOS gate adds to the MAX635/36/37's reference and therefore slightly increases the regulated output voltage. Also, the Ground pin (Pin 4) should be bypassed to true circuit ground with 10μF to minimize noise.

See the MAX634/MAX4391 data sheet for other applications of inverting DC-DC converters.

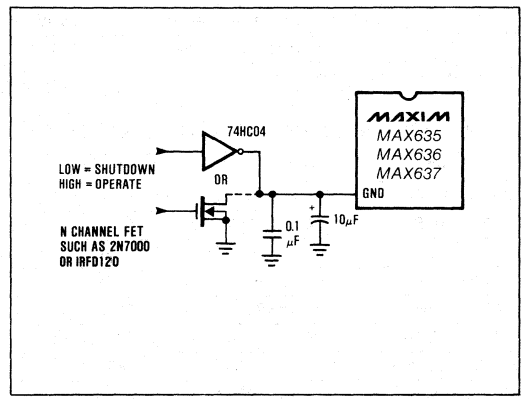


Figure 4. Low Power Shutdown

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Fixed Output CMOS Inverting Switching Regulator

Table 3. Maxim DC-DC Converters

DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

Ordering Information (continued)

PART*	TEMP. RANGE	PACKAGE
MAX637XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX637XCSA	0°C to +70°C	8 Lead Small Outline
MAX637XCJA	0°C to +70°C	8 Lead CERDIP
MAX637XC/D	0°C to +70°C	8 Lead Dice
MAX637XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX637XESA	-40°C to +85°C	8 Lead Small Outline
MAX637XEJA	-40°C to +85°C	8 Lead CERDIP
MAX637XMJA	-55°C to +125°C	8 Lead CERDIP

**X = A for 5% Output Accuracy, X = B for 10% Output Accuracy*

Fixed +5V CMOS Step-Down Switching Regulator

General Description

Maxim's MAX638 step-down switching regulator is designed for efficient, low power, minimum component count DC-DC converter circuits. It provides an alternative to conventional linear voltage regulators when efficiency and power consumption are most important. All control and power switching functions are contained in a compact 8-pin package: a bandgap reference, oscillator, feedback voltage comparator, and a 525mA (peak) P-channel power MOSFET. A small, low cost inductor, output filter capacitor, and catch diode are the only external components required. Convenient low battery detection circuitry is also included.

The MAX638 is most simply used as a fixed +5V output regulator but can be set for other voltages by adding an external voltage divider. Maxim's proprietary Dual Mode™ circuitry allows both fixed and adjustable output operation from one device. Also, with a simple external buffering circuit, the input voltage can be increased to the breakdown voltage of an external power MOSFET.

Maxim also manufactures a broad line of step-up and inverting DC-DC converters. Included are positive and negative output switching regulators with additional features such as logic level shutdown, adjustable oscillator, and charge-pump output. See Table 2 on the last page of this data sheet for a summary of other DC-DC Converter Products.

Applications

Efficient DC-DC Step-Down Regulation

Linear Voltage Regulator Replacement

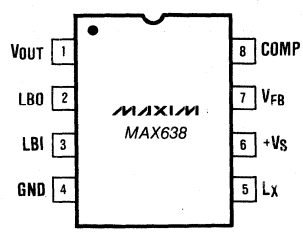
+12V to +5V Conversion

Battery Life Extension

Portable Instruments

Pin Configuration

Top View



Features

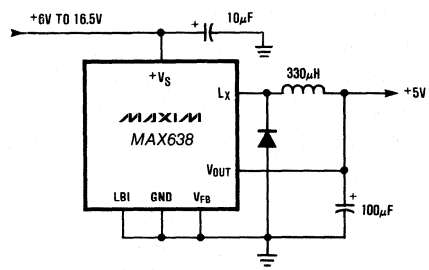
- ◆ **Fixed +5V Output**
- ◆ **Adjustable Output with Two Resistors**
- ◆ **Internal 525mA (peak) Power MOSFET**
- ◆ **Low Operating Current**
- ◆ **High Efficiency — 85% Typical**
- ◆ **Compact 8-Pin Mini-DIP and Small Outline Packages**
- ◆ **Only 3 External Components**
- ◆ **Low Battery Detector**

Ordering Information

PART*	TEMP. RANGE	PACKAGE
MAX638XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX638XCSA	0°C to +70°C	8 Lead Small Outline
MAX638XC/D	0°C to +70°C	Dice
MAX638XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX638XESA	-40°C to +85°C	8 Lead Small Outline
MAX638XEJA	-40°C to +85°C	8 Lead CERDIP
MAX638XXMJA	-55°C to +125°C	8 Lead CERDIP

X = A for 5% Output Accuracy, X = B
For X = B for 10% Output Accuracy

Typical Operating Circuit



+5V Output Step-Down Regulator

Fixed +5V CMOS Step-Down Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ ..... +18V
Output Voltage, L_X and LBO ..... +18V
Input Voltage, Pins 2, 3, 7, 8 ..... -0.3V to ($+V_S$ + 0.3V)
L_X Output Current ..... 525mA Peak
LBO Output Current 50mA
Operating Temperature
MAX638C ..... 0°C to +70°C
MAX638E ..... -40°C to +85°C
MAX638M ..... -55°C to +125°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($+V_S$ = +12V, T_A = +25°C unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	$+V_S$	Over Temperature V_{OUT} = +5V Adjustable mode	 5 2.6		 16.5 16.5	V
Supply Current	I_S	T_A = +25°C Over Temperature		135 180	 600	µA
Reference Voltage (Internal)		T_A = +25°C Over Temperature	1.28 1.24	1.31	1.34 1.38	V
V_{OUT} Voltage (Note 1)		No Load, V_{FB} = GND, 638A Over Temperature 638B	4.75 4.5	5.0 5.0	5.25 5.5	V
Efficiency				85		%
Line Regulation (Note 1)		+10V < $+V_S$ < +15V		0.2		% V_{OUT}
Load Regulation (Note 1)		P_{OUT} = 0mW to 150mW		0.2		% V_{OUT}
Oscillator Frequency	f_O			65		kHz
Oscillator Duty Cycle				50		%
L_X ON Resistance	R_{ON}	I_X = 100mA		6	12	Ω
L_X Leakage Current	I_{XL}	V_5 = 0V T_A = +25°C Over Temperature		0.01	1.0 30	µA
V_{FB} Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Input Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V_2 = +0.4V, V_3 = +1.1V T_A = +25°C Over Temperature	 0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V_2 = +16.5V, V_3 = +1.4V		0.01	3.0	µA

Note 1: Guaranteed by correlation with DC pulse measurements

Fixed +5V CMOS Step-Down Switching Regulator

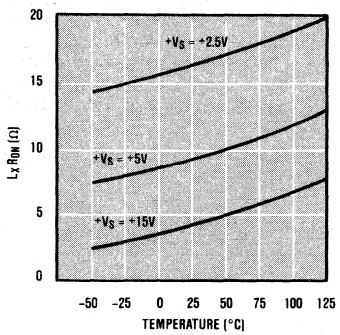
Pin Description

PIN	NAME	FUNCTION
1	V_{OUT}	The sense INPUT for fixed +5V output operation. Though it is connected to the output of the DC-DC converter (Figure 2), the V_{OUT} pin does not supply current. It is internally connected to the on-chip voltage divider.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when the LBI (Pin 1) is below +1.31V.
3	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the Low Battery Detector threshold (+1.31V), LBO (Pin 2) sinks current.
4	GND	Ground

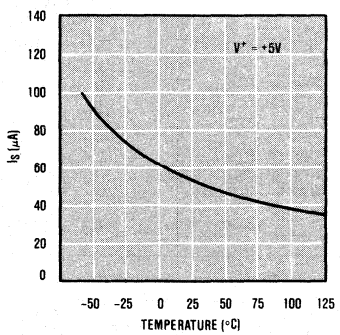
PIN	NAME	FUNCTION
5	L_X	This pin drives the external inductor with an internal P-channel power MOSFET. L_X has an output resistance of typically 6Ω and a peak current rating of 525mA.
6	V_S	The input voltage, from V_{OUT} to +16.5V.
7	V_{FB}	When V_{FB} is grounded, the DC-DC converter output will be +5V. When an external voltage divider is connected from the V_{OUT} to V_{FB} and GROUND, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. It is normally left unconnected. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between V_{OUT} and COMP reduces low frequency ripple and improves transient response.

Typical Operating Characteristics

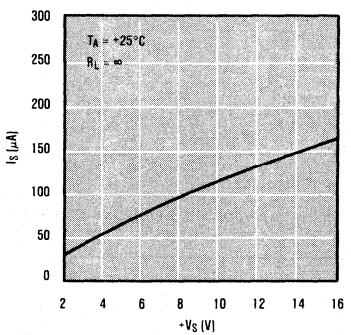
L_X ON RESISTANCE vs. TEMPERATURE



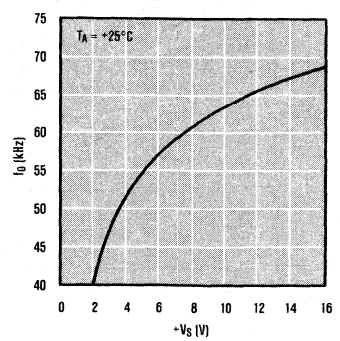
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



Fixed +5V CMOS Step-Down Switching Regulator

Detailed Description

Basic Operation

Figure 1 shows a simplified step-down DC-DC converter. When the switch is closed a charging current flows through the inductor, creating a magnetic field. This same current flows into the filter capacitor and load as well. When the switch opens, the current continues to flow through the inductor in the same direction as the charging current, but since the switch is now open, the current must flow through the diode. When the switch is open, the inductor alone supplies current to the load. This current linearly decays to zero as the magnetic field collapses and the stored energy is transferred to the filter capacitor and load.

Figure 2 shows a block diagram of the MAX638 and a typical connection in which a +9V input is converted to a +5V output with 85% efficiency. When the output drops below +5V, the Error Comparator switches high and connects the internal 65kHz oscillator to the gate of the L_X output driver. L_X turns on and off at the clock frequency, charging and discharging the inductor and supplying current to the output as described above. When the output voltage reaches +5V, the comparator output goes low and the inductor is no longer pulsed.

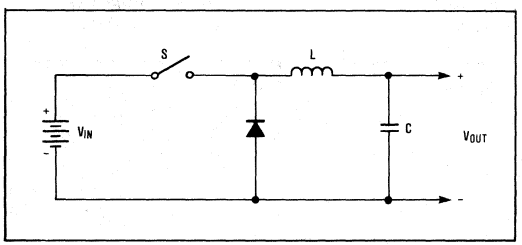


Figure 1. Simplified Step-Down Converter

Output Driver (L_X Pin)

A large P-channel MOSFET with an on-resistance of approximately 6Ω is used to charge the inductor. It is internally connected between $+V_S$ and L_X and has a peak current rating of 525mA. The available output current for most applications will be somewhat less than the peak current rating. A good rule of thumb for MAX638 maximum output current is:

$$4\ I_{OUT} < 525mA, \text{ assuming } V_{IN} \simeq 2\ V_{OUT}$$

Fixed or Adjustable Output

For operation at the preset +5V output voltage, V_{FB} is connected to GROUND and no external resistors are required. For adjustable operation, other output voltages are selected by connecting an external voltage divider to V_{FB} as shown in Figure 3. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$R3 = R4\ (\frac{V_{OUT}}{1.31V} - 1)$$

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input (LBI, Pin 1) with the internal +1.31V bandgap reference. The Low Battery Detector Output (LBO, Pin 2) goes low whenever the input voltage at LBI is less than +1.31V. The Low Battery detection voltage is set by resistors R1 and R2 (Figure 1).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$R1 = R2\ (\frac{V_{LB}}{1.31V} - 1)$$

(V_{LB} is the desired Low Battery detection voltage)

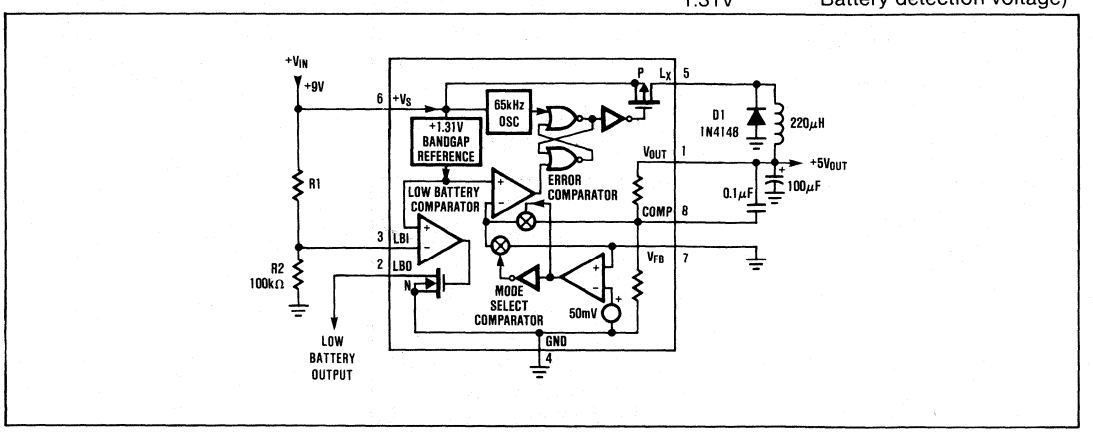


Figure 2. MAX638 Block Diagram and Typical Circuit

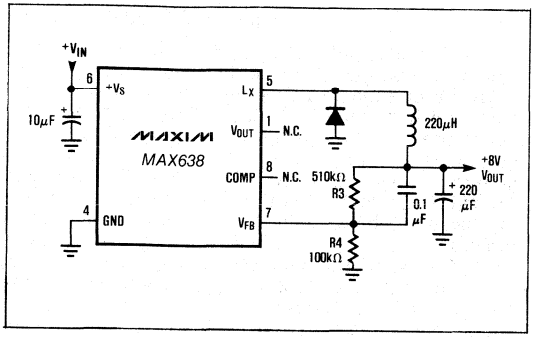


Figure 3. Adjustable Output Operation

External Components

Inductor Selection

The available output current from a DC-DC voltage step-down converter is a function of the input voltage, external inductor value, output voltage and the operating frequency. For most MAX638 applications the inductor is the only design variable since the operating frequency is fixed, and the input and output voltages are set by the application. The proper inductor must 1) have the correct inductance, 2) be able to handle the required peak currents, and 3) have acceptable series resistance and core losses.

When the MAX638's P-channel output device turns on, the coil current linearly rises since:

$$\frac{di}{dt} = \frac{V_{IN}}{L}$$ where L is inductance of the coil.

At the end of the on-time (t_{ON}), the peak current (I_{pk}), is:

$$I_{pk} = \frac{(V_{IN} - V_{OUT})\, t_{ON}}{L} \quad \text{where: } t_{ON} = \frac{1}{2f_O}$$

The energy in the coil is:

$$E_L = \frac{L\, I_{pk}^2}{2}$$

At maximum load, this cycle is repeated f_O (typically 65kHz) times per second, and the power transferred through the coil is $P_L = f_O \times E_L$. The coil supplies power to the load during each half cycle. During the other half cycle, V_{IN} supplies current, while also charging the coil. Therefore:

$$I_{OUT} = \frac{P_L}{V_{OUT}} + \frac{I_{pk}}{4}$$

where $I_{pk}/4$ is the average current supplied to the load while the coil is charging. If the load draws less than the maximum current, L_X turns on only often enough to keep the output voltage at the desired level.

If the selected inductor has too high a value, the MAX638 will not be able to deliver the desired output power, even with the L_X output turned on for every oscillator cycle. The available output power can be increased by either raising the input voltage or lowering the inductance. This causes the current to rise at a faster rate, and results in a higher peak current at the end of each cycle. The available output power increases since it is proportional to the square of the peak inductor current. The maximum inductor value therefore is:

$$L_{MAX} = \frac{(V_{IN} - V_{OUT})^2}{8f_O\, P_L}$$

$$\text{since } P_L = \frac{L\, I_{pk}^2\, f_O}{2} \quad \text{and } I_{pk} = \frac{V_{IN} - V_{OUT}}{2f_O\, L}$$

where P_L is the power supplied by the coil. The total output power (P_{OUT}) is partly supplied by V_{IN} as well as the coil, but also includes the power dissipated in the forward drop of the catch diode (V_f):

$$P_{OUT} = P_L + (V_{IN} - V_{OUT})\frac{I_{pk}}{4}$$

$$= I_{OUT}V_{OUT} + \frac{P_L V_F}{(V_{OUT} + V_F)}$$

where $I_{pk}/4$ approximates the average charging current of the inductor as a function of its peak value.

If the coil's inductance is too low, the peak current at L_X will exceed the maximum rating of the MAX638. The minimum allowed inductor value is determined by:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{2f_O\, I_{MAX}} \quad \text{where } I_{MAX} = 525\text{mA}$$

Fixed +5V CMOS Step-Down Switching Regulator

Table 1. Coil and Core Manufacturers

MANUFACTURER	TYPICAL PART #	DESCRIPTION
MOLDED INDUCTORS		
Dale	IHA-104	500μH, 0.5 ohms
Caddell-Burns	7070-29	220μH, 0.55 ohms
Gowanda	1B253	250μH, 0.44 ohms
UTC	LL-500	500μH, 0.75 ohms
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 ohms
UTC	MH-1	600μH, 1.9 ohms
Gowanda	050AT1003	100μH, 0.05 ohms
FERRITE CORES AND TOROIDS (Note 2)		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T²
Magnetics	555130	Tor. Core, 53nH/T²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T²

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 2: Permag Corp. is a distributor for many of the listed core and toroid manufacturers. (516) 822-3311.

Reducing the inductor value increases the available output current: lower L increases the available output power. The external inductor required by the MAX638 is readily obtained from a variety of suppliers (see Table 1). Standard coils are suitable for most applications, however toroids and pot cores will often provide improved performance at high power levels or where maximum efficiency is needed. See the MAX630 data sheet for additional information on different types of inductors.

Output Filter Capacitor

The MAX638's output ripple has two components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each L_X pulse. The other is the product of the capacitor's charge-discharge current and its ESR (equivalent series resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100μF to 500μF range, in parallel with a 0.1μF ceramic capacitor. See the MAX630 data sheet for more information on output filter capacitors.

External Diode

In most MAX638 circuits the current in the external diode abruptly goes from zero to its peak value each time L_X switches off (figure 2, D1). To avoid excessive losses the diode must have a fast turn-on time. For low power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher current circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boost transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

Bypassing and Compensation

Since the inductor charge and discharge currents can be relatively large, high currents may flow in ground connections near the MAX638. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and power supply bypassing should be used. A 10μF aluminum electrolytic placed at the device pins is recommended.

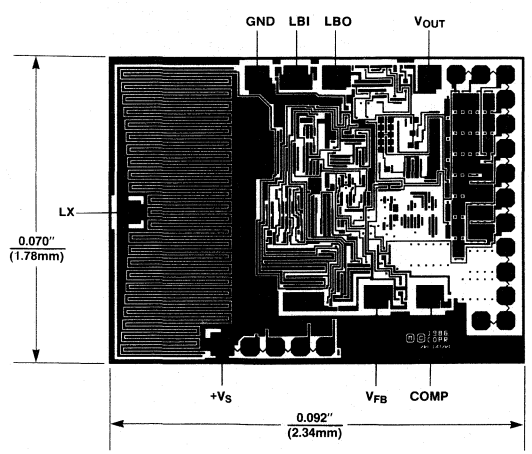
When large values (>50kΩ) are used for the voltage setting resistors (adjustable output mode), R3 and R4 of Figure 3, stray capacitance at the V_{FB} input can add a "lag" to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the V_{FB} node. It can also be remedied by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

Typical Applications

Basic Step-Down Circuits

Figure 2 shows the basic voltage inverting circuit for the MAX638. The output also can be adjusted to voltages other than +5V by adding two resistors as shown in Figure 3.

Chip Topography



Low Power Shutdown

A low power shutdown mode can easily be implemented with the MAX638 as shown in Figure 4. Since the Ground pin current is only 600μA, Ground can be driven directly by a CMOS gate or N-channel FET. Ground is driven low for normal operation, and driven high or allowed to float for shutdown mode. When shut down, the MAX638 draws only the leakage current of the L_X output.

Note that any voltage drop across the CMOS gate adds to the MAX638's reference and therefore slightly increases the regulated output voltage. Also, the Ground pin (Pin 4) should be bypassed to true circuit ground with 10μF to minimize noise.

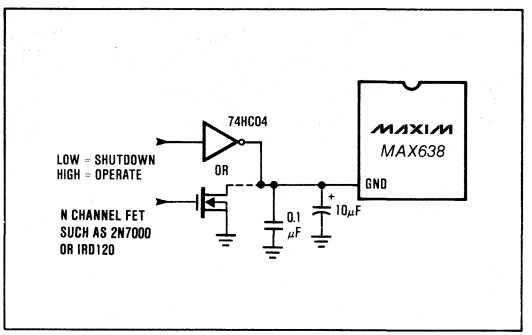


Figure 4. Low Power Shutdown

Fixed +5V CMOS Step-Down Switching Regulator

Table 2. Maxim DC-DC Converters

DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

MAXIM

Fixed Output 10 Watt CMOS Step-Up Switching Regulators

General Description

Maxim's MAX641, MAX642, and MAX643 are fixed +5V, +12V, and +15V output step-up switching regulators designed for simple, minimum component count DC-DC converter circuits in the 5 milliwatt to 10 Watt range. All control functions are contained in a compact 8-pin package: a bandgap reference, oscillator, voltage comparator, catch diode, and a driver output for an external power MOSFET or bipolar transistor. An on-chip N-channel power MOSFET is also included for low power applications. When using the internal MOSFET, only an output filter capacitor and a small low cost inductor are required. Low battery detection circuitry is also included on-chip.

If output voltages other than +5V, +12V, or +15V are required, the regulators can also be programmed for other voltages with two external resistors. Maxim's proprietary Dual Mode™ circuitry allows both fixed and adjustable output operation in one device.

Maxim also manufactures a series of -5V, -12V, and -15V DC-DC converters, as well as both positive and negative output switching regulators with additional features such as logic level shutdown, adjustable oscillator and charge-pump output. See Table 1 on the last page of this data sheet for a summary of other DC-DC converter products.

Applications

Simple, High Efficiency DC-DC Converters

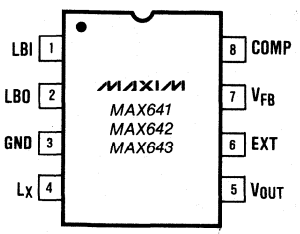
Uninterruptible Board-Level Power Supplies

Power Conditioning for Battery Systems

Portable Instruments and Communications

Pin Configuration

Top View



Features

- ◆ **Fixed +5V, +12V, +15V Output Voltages**
- ◆ **Adjustable Output with Two Resistors**
- ◆ **On-Chip Driver for High Power External MOSFET**
- ◆ **Internal 450mA (peak) Power MOSFET**
- ◆ **Low Operating Current — 135μA Typical**
- ◆ **High Efficiency — 80% Typical**
- ◆ **Compact 8-Pin Mini-DIP and Small Outline Packages**

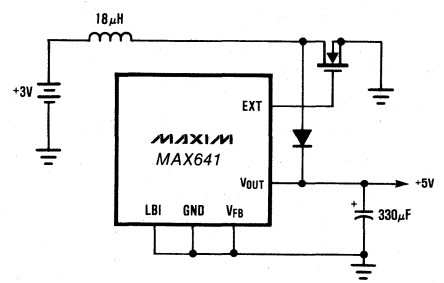
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX641XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX641XCSA	0°C to +70°C	8 Lead Small Outline
MAX641XC/D	0°C to +70°C	Dice
MAX641XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX641XESA	-40°C to +85°C	8 Lead Small Outline
MAX641XEJA	-40°C to +85°C	8 Lead CERDIP
MAX641XMJA	-55°C to +125°C	8 Lead CERDIP
MAX642XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX642XCSA	0°C to +70°C	8 Lead Small Outline
MAX642XC/D	0°C to +70°C	Dice
MAX642XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX642XESA	-40°C to +85°C	8 Lead Small Outline
MAX642XEJA	-40°C to +85°C	8 Lead CERDIP
MAX642XMJA	-55°C to +125°C	8 Lead CERDIP

X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.

(Ordering information continued on last page.)

Typical Operating Circuit



+5V Output DC-DC Converter

Fixed Output 10 Watt CMOS Step-Up Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{OUT} ..... +18V
Output Voltage, L_X and LBO ..... +18V
Input Voltage, Pins 1, 2, 7, 8 ..... -0.3V to ($+V_{OUT}$ + 0.3V)
L_X Output Current ..... 450mA Peak
LBO Output Current 50mA
Operating Temperature
MAX64XXC ..... 0°C to +70°C
MAX64XXE ..... -40°C to +85°C
MAX64XXM ..... -55°C to +125°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	$+V_S$	Voltage at V_{OUT} Over Temperature	2.0		16.5	V
Startup Voltage	$+V_S$	Voltage at V_{OUT} T_A = +25°C Over Temperature	1.5 1.8	1.3		V
Supply Current	I_S	L_X off, Over Temperature V_{OUT} = +5V V_{OUT} = +12V V_{OUT} = +15V		0.135 0.5 0.75	0.4 2.0 2.5	mA
Reference Voltage (Internal)	V_{REF}	T_A = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
V_{OUT} Voltage (Note 1)		No Load, V_{FB} = GND, Over Temperature MAX641A, MAX642A, MAX643A (5% Output Accuracy) MAX641B, MAX642B, MAX643B (10% Output Accuracy)	 4.75 11.4 14.25 4.5 10.8 13.5	 5.0 12.0 15.0 5.0 12.0 15.0	 5.25 12.6 15.75 5.5 13.2 16.5	V
Efficiency		With External MOSFET		80		%
Line Regulation (Note 1)		$0.5V_{OUT} < +V_S < V_{OUT}$		0.08		% V_{OUT}
Load Regulation (Note 1)		$+V_S = 0.5V_{OUT}$, P_{OUT} = 0mW to 150mW		0.2		% V_{OUT}
Oscillator Frequency	f_O	V_{OUT} = +2V = +5V = +12V, +15V		35 45 50		kHz
Oscillator Duty Cycle				50		%
EXT Output Resistance		V_{OUT} = +5V, I_{OUT} = ±10mA V_{OUT} = +15V, I_{OUT} = ±30mA		140 90		Ω
EXT Switching Time	t_{ON}, t_{OFF}	C_L = 330pF V_{OUT} = +5V V_{OUT} = +15V		160 125		ns
L_X ON Resistance	R_{ON}	I_X = 100mA, V_{OUT} = +5V V_{OUT} = +15V		6 3.5	12 7	Ω
L_X Leakage Current	I_{XL}	V_4 = +16.5V T_A = +25°C Over Temperature (C, E) Over Temperature (M)		0.01	1.0 30 100	μA

Note 1: Guaranteed by correlation with DC pulse measurements.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Diode Forward Voltage	V_F	I_F = 100mA			1.0	V
V_{FB} Input Bias Current	I_{FB}			0.01	10	nA
Low Battery Threshold	V_{LBI}			1.31		V
Low Battery Input Bias Current	I_{LBI}			0.01	10	nA
Low Battery Output Current	I_{LBO}	V_2 = +0.4V, V_1 = +1.1V T_A = +25°C Over Temperature	 0.5	1.0		mA
Low Battery Output Leakage Current	I_{LBOL}	V_2 = +16.5V, V_1 = +1.4V		0.01	3.0	µA

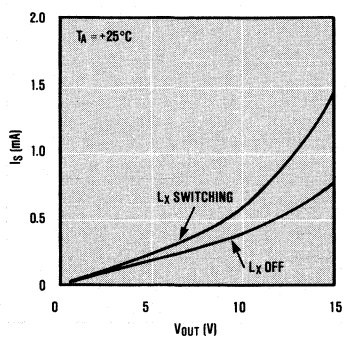
Pin Description

PIN	NAME	FUNCTION
1	LBI	Low Battery Input. When the voltage at LBI is lower than the Low Battery Detector threshold (+1.31V), LBO (Pin 2) sinks current.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when the LBI (Pin 1) is below +1.31V.
3	GND	Ground
4	L_X	In low power applications L_X drives the external inductor with an internal N-channel power MOSFET. L_X has a typical output resistance of 6Ω and a peak current rating of 450mA.
5	V_{OUT}	The regulated DC-DC converter output when the internal MOSFET and catch diode are used. When an external diode is used, this pin becomes the supply voltage input pin, and is usually connected to the cathode of the external diode.

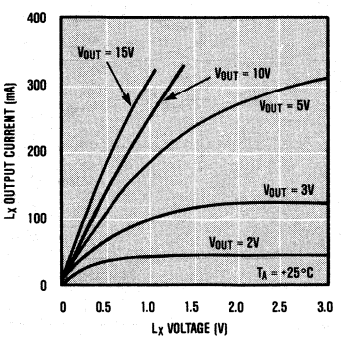
PIN	NAME	FUNCTION
6	EXT	The drive output for an external power MOSFET or bipolar transistor. EXT swings from GND to V_{OUT} and has a 10Ω sink/source impedance. EXT is low when L_X is open-circuit and is high when L_X is on.
7	V_{FB}	When V_{FB} is grounded, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected from the V_{OUT} to V_{FB} and GROUND, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between V_{OUT} and COMP reduces low frequency ripple and improves transient response. Ground comp when using an External Voltage divider on V_{FB}.

Typical Operating Characteristics

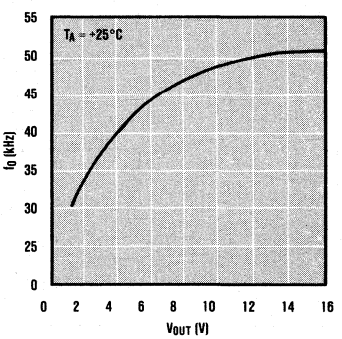
SUPPLY CURRENT vs. OUTPUT VOLTAGE



L_X OUTPUT CURRENT vs. V_{OUT}



OSCILLATOR FREQUENCY vs. OUTPUT VOLTAGE



Fixed Output 10 Watt CMOS Step-Up Switching Regulators

Detailed Description

Basic Operation

The operation of the MAX641 series can best be understood by examining the regulating loop of Figure 1. When the output voltage drops below the preset (or externally set) value, the Error Comparator switches high and connects the internal 45kHz Oscillator to the L_X and EXT outputs. EXT is typically connected to the gate of an external N-channel power MOSFET. When EXT is activated, the MOSFET turns on and off at the internal clock frequency.

When EXT is high, the MOSFET switches on and the inductor current increases linearly, storing energy in the coil. When EXT switches the MOSFET off, the coil's magnetic field collapses, and the voltage across the inductor reverses sign. The voltage at the anode of the catch diode then rises until the diode is forward biased, delivering power to the output. As the output voltage reaches the desired level, the Error Comparator inhibits EXT until the load discharges the output filter capacitor to less than the desired output level. See the Maxim MAX630 data sheet for further discussion on different types of DC-DC converters.

Though designed to power an external MOSFET or bipolar transistor, the MAX641 series will also work well in low power applications (<250mW) with its own internal MOSFET and catch diode. In these applications the L_X output does the current switching and an external capacitor and inductor are all that is needed.

V_{IN}, Bootstrapped Operation

The MAX641/42/43 does not have a V_{IN} pin. Input power to start the DC-DC converter is supplied via the external inductor, and diode if used, to the V_{OUT} pin. If an external catch diode is used, its cathode should be connected to V_{OUT} as well. Once the converter has started, it is then powered from its own output. This design ensures that the output MOSFET will have maximum gate drive and hence a minimum R_{ON}. It also allows the converter to start at lower input voltages.

V_{IN} Greater Than V_{OUT}

If the regulator's input voltage is more than one forward diode drop greater than the desired output voltage, the EXT and L_X outputs will not turn on. Despite this, current will still be supplied to the load directly through the catch diode, but without regulation. The output will equal the input voltage less the forward drop of the catch diode (about 0.6V) as long as the input is more than 0.6V above the desired output.

Fixed or Adjustable Output

For operation at one of the preset output voltages (+5V for the MAX641, +12V for MAX642, and +15V for MAX643), V_{FB} is connected to GROUND. No external resistors are required.

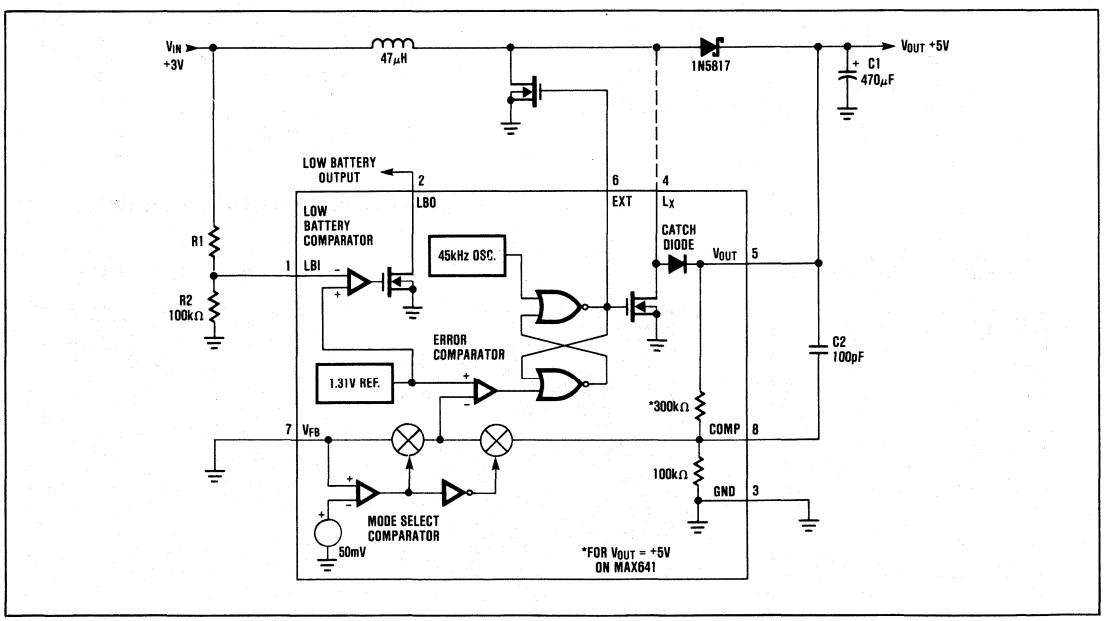


Figure 1. +3V to +5V Converter and Block Diagram

For adjustable output operation, other voltages are selected by connecting an external voltage divider to V_{FB} as shown in Figure 2. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$R3 = R4 \left(\frac{V_{OUT}}{1.31V} - 1\right)$$

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input (LBI), pin 1, with the internal +1.31V bandgap reference. The Low Battery Detector Output (LBO), pin 2, goes low whenever the input voltage at LBI is less than +1.31V. The Low Battery threshold is set by resistors R1 and R2 (Figure 1).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$R1 = R2 \left(\frac{V_{LB}}{1.31V} - 1\right)$$ (V_{LB} is the desired Low Battery detection voltage)

External Components

Inductor Selection

The available output current from a DC-DC voltage boost converter is a function of the input voltage, external inductor value, output voltage and the operating frequency. For most MAX641/42/43 applications the inductor is the only design variable since the operating frequency is fixed, and the input and output voltages are set by the application. The proper inductor must 1) have the correct inductance, 2) be able to handle the required peak currents, and 3) have acceptable series resistance and core losses.

When the inductor driver turns on:

$$\frac{di}{dt} = \frac{V_{IN}}{L}$$ where L is inductance of the coil.

At the end of the on-time, t_{ON}, the peak current, I_{pk}, is:

$$I_{pk} = \frac{V_{IN}\, t_{ON}}{L} \quad \text{where: } t_{ON} = \frac{1}{2f_O}$$

The energy in the coil is:

$$E_L = \frac{L\, I_{pk}^2}{2}$$

At maximum load this cycle is repeated f_O (typically 45kHz) times per second, and the power transferred through the coil is $P_L = f_O \times E_L$. Since the coil supplies the voltage above the input voltage:

$$I_{OUT} = \frac{P_L}{V_{OUT} - V_{IN}}$$

The DC-DC converter's output current is provided both by the inductor and directly from the battery. If the load draws less than the maximum current, EXT (or L_X) turns on only often enough to keep the output voltage at the desired level.

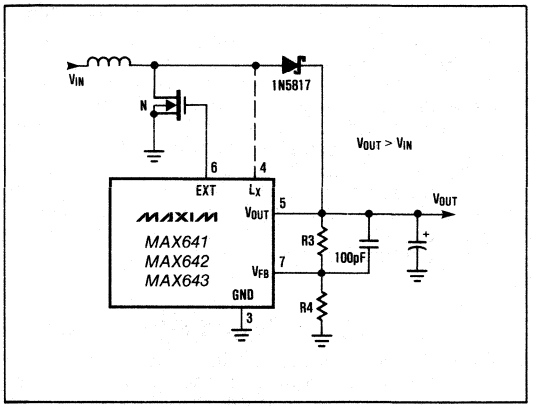


Figure 2. Connections for Adjustable Output Operation.

If the selected inductor has too high a value, the MAX641/42/43 will not be able to deliver the desired output power, even with the output turned on for every oscillator cycle. The available output power can be increased by either raising the input voltage or lowering the inductance. This causes the current to rise at a faster rate, and results in a higher peak current at the end of each cycle. The available output power increases since it is proportional to the square of the peak inductor current. The maximum inductance therefore is:

$$L_{MAX} = \frac{V_{IN}^2}{8f_O\, P_L}$$

$$\text{since: } P_L = \frac{L\, I_{pk}^2\, f_O}{2} \quad \text{and: } I_{pk} = \frac{V_{IN}}{2f_O\, L}$$

Remember that the required output power must include what is dissipated in the forward drop of the catch diode (V_F) as well:

$$P_{OUT} = P_L = I_{OUT}(V_{OUT} + V_F) = P_L + V_{IN}\, I_{OUT}$$

If the coil's inductance is too low, the current at L_X may rise above the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = \frac{V_{IN}}{2f_O\, I_{MAX}}$$

I_{MAX} depends on the current rating of the inductor and external MOSFET or transistor, if used. For the internal MOSFET (L_X output), I_{MAX} is 450mA.

Refer to the MAX631 data sheet for more details on inductor selection and operation using the internal MOSFET output (L_X).

Fixed Output 10 Watt CMOS Step-Up Switching Regulators

External MOSFET

An external MOSFET or transistor can be used to drive the inductor in high power applications. The current handling specifications of the external device must match the peak current which flows in the inductor (see Inductor Selection). The only restriction on the size of the external driver is that the EXT output must be able to drive the external device's gate (or base) capacitance at the internal clock rate (45kHz). The external driver may also be used to increase operating voltage range of the MAX641/42/43 (see Typical Applications).

Output Filter Capacitor

The MAX641/42/43's output ripple has two components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each L_X pulse. The other is the product of the capacitor's charge-discharge current and its ESR (equivalent series resistance). With low cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100μF to 500μF range, in parallel with a 0.1μF ceramic capacitor. See the MAX630 data sheet for more information on output filter capacitors.

Diodes

When the MAX641/42/43 is used with an external power MOSFET, the internal diode can be used if the peak diode current rating (450mA) and maximum package power dissipation ratings are observed. For higher power circuits an external Schottky diode such as the 1N5817 (1 Amp) or 1N5821 (3 Amp) should be connected between L_X and V_{OUT}, in parallel with the internal diode. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are not recommended because their slow turn-on time results in excessive losses and poor efficiency.

Application Hints

Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents flow through the ground connection near the MAX641/42/43. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and a bypass capacitor (10μF) should be at the V_{OUT} pin, even if large filter capacitors are used elsewhere in the circuit.

When large values (>50kΩ) are used for the voltage setting resistors (R3 and R4 of Figure 2) in the adjustable output mode, stray capacitance at the V_{FB} input can add a "lag" to the feedback response, destabilizing the regulator and causing output pulses to occur in bursts. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the V_{FB} node. Normal operation with evenly distributed pulses can also be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

The COMP input, pin 8, allows access to the internal voltage divider so that compensation can also be added when fixed output operation is used. A capacitor connected between V_{OUT} and COMP again adds a "lead" to the regulator's response.

Inductor Saturation

It is important to be sure that the inductor does not saturate, particularly in high power circuits. Inductor saturation leads to very high current levels through the external boost transistor, causing excessive power dissipation, poor efficiency, and possible damage to the inductor and the external transistor.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

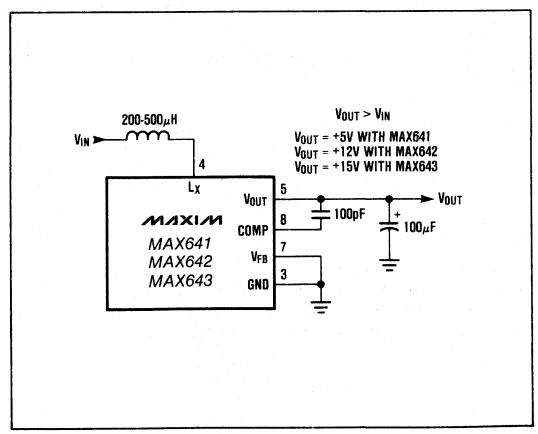


Figure 3. Low Power, Fixed Output Step-Up Converter Using L_X

Fixed Output 10 Watt CMOS Step-Up Switching Regulators

Typical Applications

Basic High Power Hookup

Figure 2 shows the standard circuit configuration for a fixed output step-up DC-DC converter. The output power is determined by the current ratings of the external MOSFET and inductor as well as the switching times of the EXT output into the gate capacitance of the MOSFET. Typical switching times are given in the Electrical Characteristics table.

Step-Up Conversion Using L_X

In low power Applications the L_X output and internal diode may be used instead of an external MOSFET and diode as shown in Figure 3. The power handling capability of this circuit is about 250mW. See the MAX631 data sheet for inductor selection information.

High Voltage Operation

If the external MOSFET or transistor has an adequate voltage rating, then the output voltage range of the MAX641/42/43 can be extended (Figure 4). The adjustable output mode must be used (V_{FB} connected to external resistors) and the V_{OUT} pin must be connected to the circuit's INPUT voltage.

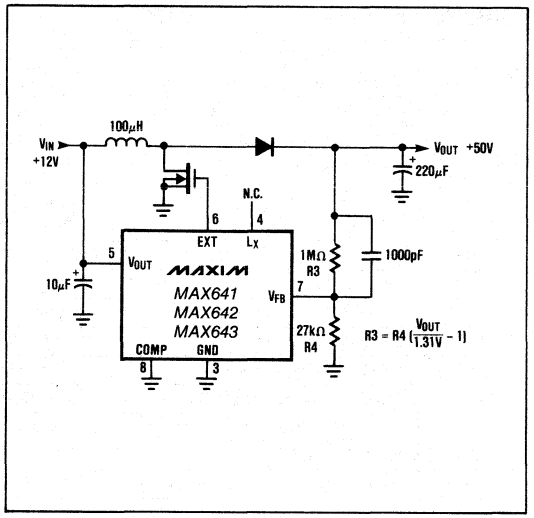


Figure 4. High Voltage Step-Up Converter

6

Fixed Output 10 Watt CMOS Step-Up Switching Regulators

Table 1. Maxim DC-DC Converters

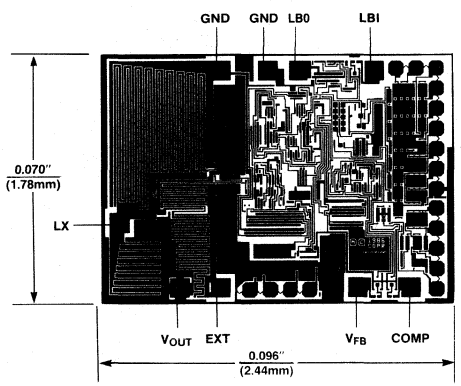
DEVICE	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
ICL7660	Charge Pump Voltage Inverter	1.5V to 10V	$-V_{IN}$	Not regulated
MAX4193	DC-DC Boost Converter	2.4V to 16.5V	$V_{OUT} > V_{IN}$	RC4193 2nd source
MAX630	DC-DC Boost Converter	2.0V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4191 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
MAX4391	DC-DC Voltage Inverter	4V to 16.5V	up to -20V	RC4391 2nd source
MAX634	DC-DC Voltage Inverter	2.3V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2.3V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2.3V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2.3V to 16.5V	-15V	Only 3 external components
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
MAX641	High Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX643XCPA	0°C to +70°C	8 Lead Plastic DIP
MAX643XCSA	0°C to +70°C	8 Lead Small Outline
MAX643XC/D	0°C to +70°C	8 Lead Dice
MAX643XEPA	-40°C to +85°C	8 Lead Plastic DIP
MAX643XESA	-40°C to +85°C	8 Lead Small Outline
MAX643XEJA	-40°C to +85°C	8 Lead CERDIP
MAX643XMJA	-55°C to +125°C	8 Lead CERDIP

**X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.*

Chip Topography



MAXIM

Dual Mode™ 5V/Programmable Micropower Voltage Regulators

General Description

The MAX663/664/666 CMOS voltage regulators have a maximum quiescent current of 12μA. They can be used either as 5 volt, fixed output regulators with no additional components, or can be adjusted from 1.3V to 16V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The MAX66X series, ideally suited for battery powered systems, has an input voltage range of 2 to 16.5V, an output current capability of 40mA, and can operate with low input-output differentials. Other features include current limiting and low power shut down.

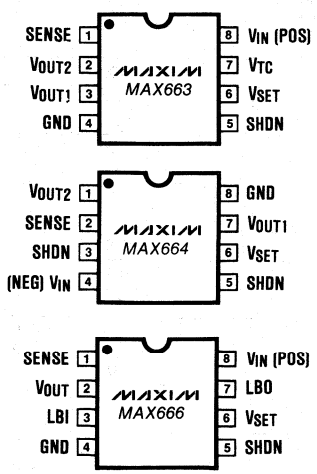
The MAX663 positive regulator and MAX664 negative regulator are both pin and electrically compatible with the ICL7663 and ICL7664 and can plug-in replace these devices, improving performance and eliminating the need for external resistors in 5V applications. The MAX666 has a positive output and includes on-chip low-battery detection circuitry.

Applications

Handheld Instruments
LCD Display Systems
Pagers
Remote Data Acquisition and Telemetry
Radio Controlled Devices
Long-life Battery Powered Systems

Pin Configuration

Top View



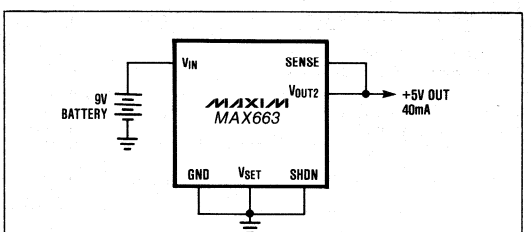
Features

- **Dual Mode Operation: Fixed +5V or Adjustable from +1.3V to +16V**
- **Low Power CMOS: 12μA Max Quiescent Current**
- **40mA Output Current, with Current Limiting**
- **Pin-Compatible Upgrade of ICL7663 and ICL7664**
- **+2V to +16.5V Operating Range**
- **Low Battery Detector (MAX666)**
- **No Output Over-Shoot on Power Up**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX663C/D	0°C to +70°C	Dice
MAX663CPA	0°C to +70°C	8 Lead Plastic DIP
MAX663CSA	0°C to +70°C	8 Lead Small Outline
MAX663EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX663ESA	-40°C to +85°C	8 Lead Small Outline
MAX663EJA	-40°C to +85°C	8 Lead CERDIP
MAX663MJA	-55°C to +125°C	8 Lead CERDIP
MAX664C/D	0°C to +70°C	Dice
MAX664CPA	0°C to +70°C	8 Lead Plastic DIP
MAX664CSA	0°C to +70°C	8 Lead Small Outline
MAX663EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX664ESA	-40°C to +85°C	8 Lead Small Outline
MAX664EJA	-40°C to +85°C	8 Lead CERDIP
MAX664MJA	-55°C to +125°C	8 Lead CERDIP
MAX666C/D	0°C to +70°C	Dice
MAX666CPA	0°C to +70°C	8 Lead Plastic DIP
MAX666CSA	0°C to +70°C	8 Lead Small Outline
MAX666EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX666ESA	-40°C to +85°C	8 Lead Small Outline
MAX666EJA	-40°C to +85°C	8 Lead CERDIP
MAX666MJA	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



Dual Mode 5V/Programmable Micropower Voltage Regulators

ABSOLUTE MAXIMUM RATINGS

MAX663 and MAX666

Input Supply Voltage ..... +18V
Terminal Voltage
Pins 1,3,5,6, MAX663 — Pin 7, and MAX666 — Pin 2, ... GND -0.3V to V_{IN} +0.3V
MAX663 — Pin 2 ..... GND -0.3V to V_{OUT1} +0.3V
MAX666 — Pin 7 ..... GND -0.3V to +16.5V
Output Source Current
MAX663,666 — Pin 2 (V_{OUT2}, V_{OUT}) 50mA
MAX663 — Pin 3 (V_{OUT1}) 25mA
Output Sink Current, Pin 7 ..... -10mA

MAX664

Input Supply Voltage ..... -18V
Terminal Voltage
Pins 1,3,5,6,7 ..... V_{IN} -0.3V to GND +0.3V
Pin 2 ..... V_{IN} -0.3V to V_{OUT1} +0.3V
Output Sink Current, (Pins 1,7) ..... -25mA

ALL DEVICES

Power Dissipation
Plastic DIP (Derate 8.3mW/°C above +50°C) 625mW
Small Outline (Derate 6mW/°C above +50°C) 450mW
CERDIP (Derate 8mW/°C above +50°C) 800mW
Operating Temperature Range
MAX66XC ..... 0°C to +70°C
MAX66XE ..... -40°C to +85°C
MAX66XM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, MAX663 AND MAX666

(V_{IN} = +9V, V_{OUT} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	Over Temperature (C) Over Temperature (E, M)	2.0 2.2		16.5	V
Quiescent Current	I_Q	No Load, V_{IN} = +16.5V T_A = +25°C Over Temperature (C) Over Temperature (E, M)		6	 12 15 20	µA
Output Voltage	V_{OUT}	V_{SET} = GND Over Temperature (C, E) Over Temperature (M)	4.75 4.5	5.0 5.0	5.25 5.5	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	+2V ≤ V_{IN} ≤ +15V, V_{OUT} = V_{REF}		0.03	0.35	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	MAX663: 1mA ≤ I_{OUT2} ≤ 20mA MAX663: 50µA ≤ I_{OUT1} ≤ 5mA MAX666: 1mA ≤ I_{OUT} ≤ 20mA		3.0 1.0 3.0	7.0 5.0 7.0	Ω
Reference Voltage	V_{SET}	V_{OUT} = V_{SET}	1.27		1.33	V
Reference Tempco.	$\Delta V_{SET}/\Delta T$	Over Temperature		±100		ppm/°C
V_{SET} Internal Threshold for Fixed +5V or Adjustable Output	$V_{F/A}$	V_{SET} < $V_{F/A}$ for +5V Out V_{SET} > $V_{F/A}$ for Adjustable Out		50		mV
V_{SET} Input Current	I_{SET}	Over Temperature (C, E) Over Temperature (M)		±0.01	±10 ±25	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN} HI = Output Off V_{SHDN} LO = Output On	1.4		 0.3	V
Shutdown Input Current	I_{SHDN}			±0.01	±10	nA
SENSE Input Threshold	V_{OUT} - V_{SENSE}	Current Limit Threshold		0.5		V
SENSE Input Resistance	R_{SENSE}			3		MΩ
Input-Output Saturation Resistance, MAX663 - V_{OUT1}	R_{SAT}	V_{IN} = +2V, I_{OUT} = 1mA V_{IN} = +9V, I_{OUT} = 2mA V_{IN} = +15V, I_{OUT} = 5mA		200 70 50	500 150 150	Ω
Output Current, V_{OUT2} (V_{OUT} on MAX666)	I_{OUT}	+3V ≤ V_{IN} ≤ +16.5V V_{IN} - V_{OUT} = +1.5V	40			mA
Minimum Load Current	$I_{L(MIN)}$	T_A = +25°C Over Temperature (C, E) Over Temperature (M)			1.0 5.0 10.0	µA

ELECTRICAL CHARACTERISTICS, MAX663 AND MAX666 (continued)

(V_{IN} = +9V, V_{OUT} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LBI Input Threshold	V_{LBI}	MAX666	1.21	1.28	1.37	V
LBI Input Current	I_{LBI}	MAX666		±0.01	±10	nA
LBO Output Saturation Resistance	R_{SAT}	MAX666, I_{SAT} = 2mA		35		Ω
LBO Output Leakage Current		MAX666, LBI = +1.4V		10		nA
V_{TC} Open-Circuit Voltage (Note 1)	V_{TC}	MAX663		0.9		V
V_{TC} Sink Current (Note 1)	I_{TC}	MAX663		8.0	2.0	mA
V_{TC} Temperature Coefficient (Note 1)		MAX663		+2.5		mV/°C

Note 1: This output (MAX663 only) has a positive temperature coefficient. Using it in conjunction with the input of the regulator at V_{SET}, a negative coefficient results in the output voltage. The V_{TC} pin will not source current.

ELECTRICAL CHARACTERISTICS, MAX664

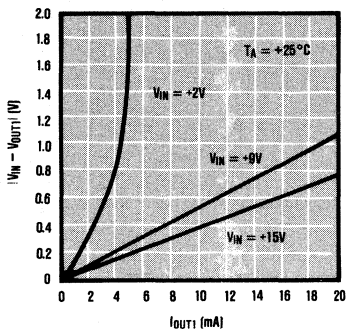
(V_{IN} = -9V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	Over Temperature (C) Over Temperature (E, M)	-2.0 -2.2		-16.5	V
Quiescent Current	I_Q	No Load, V_{IN} = -16.5V T_A = +25°C Over Temperature (C) Over Temperature (E, M)		6	 12 15 20	µA
Output Voltage	V_{OUT}	V_{SET} = GND Over Temperature (C, E) Over Temperature (M)	 -4.75 -4.5	 -5.0 -5.0	 -5.25 -5.5	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$-2V \le V_{IN} \le -15V$, $V_{OUT} = V_{REF}$		0.03	0.35	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{OUT2} connected to V_{OUT1}, $1mA \le I_{OUT} \le 15mA$		2.0	5.0	Ω
Reference Voltage	V_{SET}	$V_{OUT} = V_{SET}$	-1.27		-1.33	V
Reference Tempco.	$\Delta V_{SET}/\Delta T$	Over Temperature		±100		ppm/°C
V_{SET} Internal Threshold for Fixed -5V or Adjustable Output Operation	$V_{F/A}$	$V_{SET} < V_{F/A}$ for -5V Out, $V_{SET} > V_{F/A}$ for Variable Out		-50		mV
V_{SET} Input Current	I_{SET}	Over Temperature (C, E) Over Temperature (M)		±0.01	±10 ±25	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN} HI = Output Off V_{SHDN} LO = Output On	-1.4		 -0.3	
Shutdown Input Current	I_{SHDN}			±0.01	±10	nA
SENSE Input Threshold	$V_{OUT} - V_{SENSE}$	Current Limit Threshold		-0.6		V
SENSE Input Resistance	R_{SENSE}			3		MΩ
Input-Output Saturation Resistance	R_{SAT}	V_{OUT2} connected to V_{OUT1} V_{IN} = -2V, I_{OUT} = -1mA V_{IN} = -9V, I_{OUT} = -2mA V_{IN} = -15V, I_{OUT} = -5mA		 150 40 30	 500 80 60	Ω
Minimum Load Current	$I_{L(MIN)}$	T_A = +25°C Over Temperature (C, E) Over Temperature (M)			-1.0 -5.0 -10.0	µA

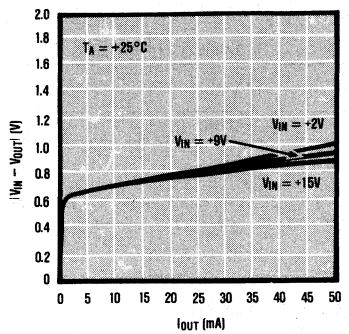
Dual Mode 5V/Programmable Micropower Voltage Regulators

Typical Operating Characteristics

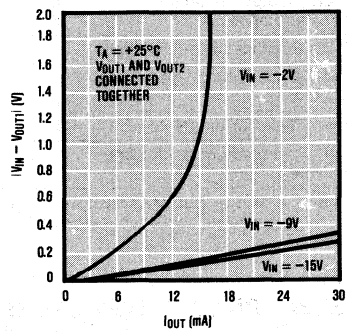
MAX663 V_{OUT1} INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



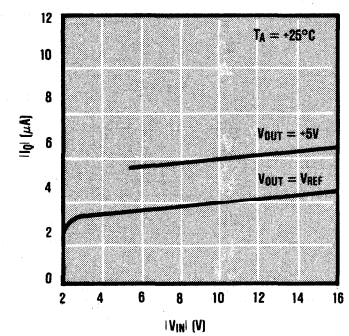
MAX663 V_{OUT2}, MAX666 V_{OUT} INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



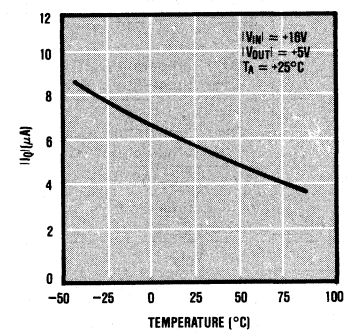
MAX664 INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



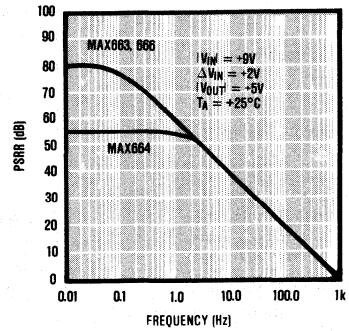
QUIESCENT CURRENT vs. INPUT VOLTAGE



QUIESCENT CURRENT vs. TEMPERATURE



INPUT POWER SUPPLY REJECTION RATIO



Pin Description

NAME	FUNCTION (See text for details)
$V_{OUT(1)(2)}$	Regulator Output(s)
V_{IN}	Regulator Input
SENSE	Current limit sense input
LBI	Low battery detection input
LBO	Low battery detection output
SHUTDOWN	Disables output for minimum power consumption
V_{SET}	Ground this pin for 5V output or Connect to external resistive divider for adjustable output
V_{TC}	Temperature-proportional voltage for negative TC output

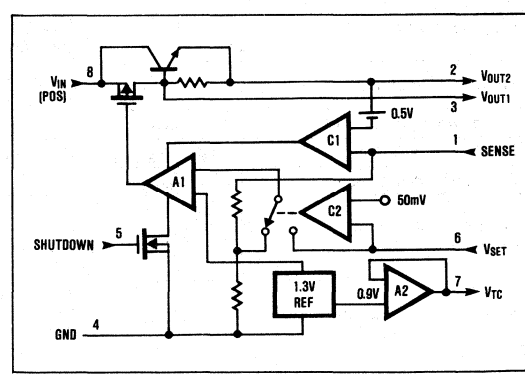


Figure 1. MAX663 Positive Regulator, Block Diagram

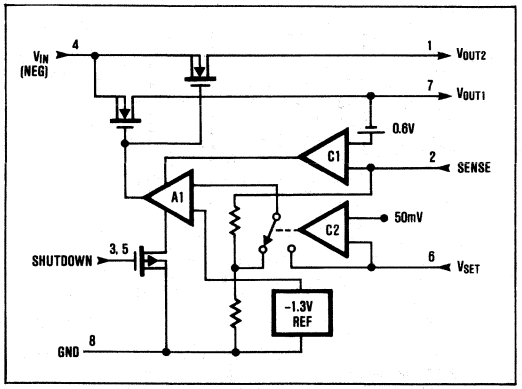


Figure 2. MAX664 Negative Regulator, Block Diagram

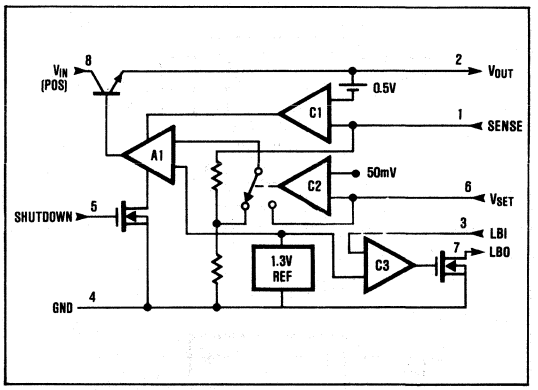


Figure 3. MAX666 Positive Regulator With Low Battery Detector, Block Diagram

Detailed Description

As shown in the block diagrams for each device (Figures 1, 2, and 3), the main elements of the MAX66X family of regulators are a micropower bandgap reference, an error amplifier, and one or two series pass output devices. A P-channel FET and an NPN transistor are used on the MAX663, two N-channel FETs are used in the MAX664 , and one NPN output transistor is used in the MAX666. All regulators also contain two comparators, one for current limiting (C1) and another which selects fixed 5V or adjustable output operation (C2).

The bandgap reference, which is trimmed to 1.30V ±30mV, is internally connected to one input of the error amplifier, A1. The feedback signal from the regulator output is supplied to the A1's other input by either an on-chip voltage divider or by two external resistors. When V_{SET} is grounded the internal divider provides the error amplifier's feedback signal for a fixed 5V output. When V_{SET} is more than 50mV above ground (below ground for the MAX664) the error amplifier's input is switched directly to the V_{SET} pin and external resistors set the output voltage.

Comparator C1 monitors the output current via the SENSE input and shuts down the regulator's output(s) by disabling A1. An external current sense resistor, R_{CL}, sets the limit value. The MAX663 and MAX666 current-limit when the voltage on R_{CL} exceeds 0.5V. The MAX664 current limits at 0.6V.

The MAX663 has an additional amplifier, A2, which provides a temperature-proportional output, V_{TC}. When this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

The MAX666 has a third comparator, C3, which compares the LBI input to the internal 1.30V reference. The Low Battery Output, LBO, is an open drain FET connected to Ground. The Low Battery threshold can also be set with a voltage divider at LBI. In addition, all devices also have a SHUTDOWN input which disables the error amplifier and regulator output(s).

Basic Circuit Operation

Figure 4 shows the connections for fixed 5V output positive and negative regulators. The V_{SET} input is grounded and no external resistors are required. Figure 5 shows adjustable output operation with current limiting. The output voltage is set by R1 and R2 and the current limit threshold is set by R_{CL}. V_{OUT} should be connected to SENSE if current limiting is not used and the SHUTDOWN input should be grounded if not used.

Output Voltage Selection

If V_{SET} is not connected to Ground, the output voltage is set by the equation:

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1}, \text{ where } V_{SET} = 1.30V$$

or, to simplify resistor selection:

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30V} - 1\right)$$

Since the input bias current at V_{SET} has a maximum value of 10nA, relatively large values can be used for R1 and R2 with no loss of accuracy. 1MΩ is a typical value for R1. The tolerance on V_{SET} is guaranteed to be less than ±30mV. This allows the output to be preset without trim pots, using only fixed resistors in most cases.

Dual Mode 5V/Programmable Micropower Voltage Regulators

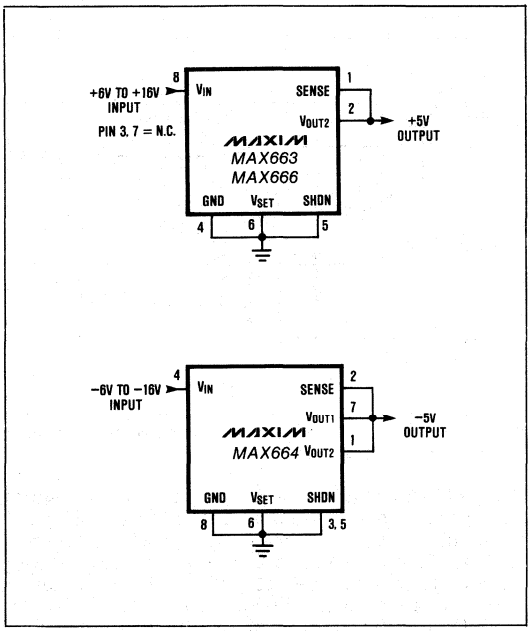


Figure 4. Connections for Fixed 5V Output

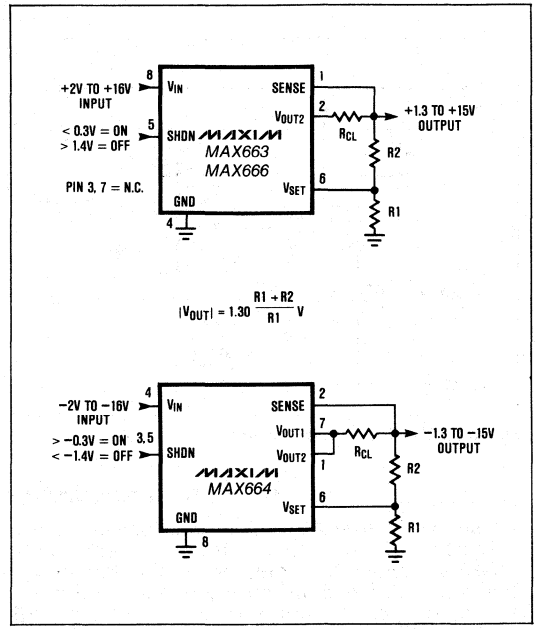


Figure 5. Connections for Adjustable Output

Current Limiting

Internal current limiting is activated on all MAX66X devices when the voltage difference between V_{OUT} and the SENSE input exceeds an internal threshold. The limit value is externally set by R_{CL} using the equation:

$$R_{CL} = \frac{V_{CL}}{I_{CL}}$$

V_{CL} = 0.5V for MAX663 and MAX666
V_{CL} = -0.6V for MAX664
($V_{CL} = V_{OUT} - V_{SENSE}$)

where R_{CL} is the current limit sense resistor and I_{CL} is the maximum current. R_{CL} should be chosen so that neither the 50mA absolute maximum output current specification nor the maximum power dissipation is exceeded.

If current limiting is used, remember that the additional voltage drop across R_{CL} must be considered when determining the regulator's dropout voltage. If current limiting is not used, the SENSE input should be connected to the output(s).

Shutdown Input

The SHUTDOWN input allows the regulator to be turned off with a logic level signal. Since the current drain in shutdown mode is limited to the regulator's quiescent current (12μA Max) this is sometimes desirable in applications where very low power consumption is needed. The SHUTDOWN input should be driven with a CMOS logic level since the input threshold is only 0.3V (-0.3V on the MAX664). In TTL systems, an open-collector driver with a pullup resistor will work with the MAX663/666 if a small collector current is used to keep the output's V_{SAT} below 0.3V. Collector currents as low as 1μA are suitable since the SHUTDOWN pin's input current is less than 10nA. Note that the MAX664's SHUTDOWN input is activated by a negative level. On both positive and negative regulators the SHUTDOWN input should be grounded for normal operation.

Low Battery Detection

The MAX666 contains on-chip circuitry for low battery or low power supply detection. If the voltage at LBI (Low Battery Input, pin 3) falls below the regulator's internal reference (1.30V) then LBO (Low Battery Output, pin 7), an open drain output, goes low. The threshold can be set to any level above the reference voltage by connecting a resistive divider to LBI (Figure 6) based on the equation:

$$R3 = R4 \times \left(\frac{V_{BATT}}{1.30V} - 1\right)$$

where V_{BATT} is the desired threshold of the Low Battery Detector and R3 and R4 are the LBI input divider resistors. Since LBI's input current is no more than 10nA, then R3 and R4 can have high

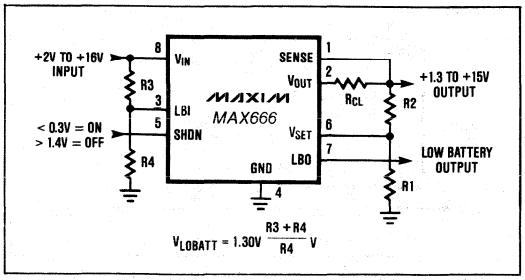


Figure 6. Adjustable Positive Output With Low Battery Detection

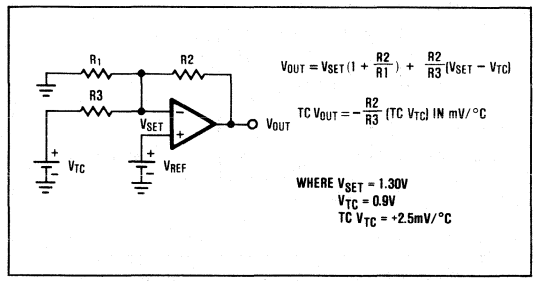


Figure 7. Temperature-Proportional Output Equations, MAX663

values to minimize loading. If, for example, V_{OUT} were 5V, then a 6V low-battery threshold could be set using 10MΩ for R3 and 2.7MΩ for R4. When megohm resistor values are used, special attention should be paid to PC board leakage which can introduce error at the LBI input.

Temperature-Proportional Output

The V_{TC} output (MAX663 only) has a positive temperature coefficient of about +2.5mV/°C. When connected to the summing junction of the error amplifier (V_{SET}) through a resistor, this positive coefficient results in a controllable negative temperature coefficient at the output of the MAX663. At 25°C the voltage at the V_{TC} output is typically 0.9V. Figure 7 shows a simplified diagram of the MAX663 and the equations for setting both the output voltage and the tempco when V_{TC} is used. When not used, V_{TC} should be left unconnected.

Negative output temperature coefficients are most commonly used in multiplexed LCD modules or display systems to compensate for the inherent negative tempco of the LCD threshold. Figure 8 shows a MAX663 generating a temperature compensated V_{DISP} for the Maxim ICM7233 triplexed LCD display driver.

Application Hints

Input-Output (Dropout) Voltage

A regulator's minimum input-output differential, or dropout voltage, determines the lowest usable input voltage. In battery powered systems this will determine the useful end-of-life battery voltage. The MAX663 and MAX666 have a dropout voltage of 1V at full output. This means that as 5V regulators, for example, they will provide a regulated 5V output at 40mA as long as the input voltage is 6V or greater.

For low current applications (I_{OUT} < 5mA) the MAX663 can operate with input-output differentials below 1V when V_{OUT1} is used. The dropout voltage will then depend on the P-channel output FET's saturation resistance multiplied by the load current (see MAX663 Electrical Specifications, R_{SAT}).

The MAX664 (negative output) uses two N-channel FETs as output devices so its dropout voltage is also a function of R_{SAT} times its load current (see Electrical Specifications).

Output Connections

When using V_{OUT1} on the MAX663 for low current, low dropout applications, V_{OUT2} and V_{OUT1} must be connected together since the current limit circuitry is referenced only to V_{OUT2} (Figure 1). V_{OUT2} does not supply load current in this configuration since the base of the NPN output transistor is shorted by the output connection. For high current operation V_{OUT2} should be used alone and V_{OUT1} should be left unconnected. V_{OUT1} is not provided on the MAX666. On the MAX664, V_{OUT1} and V_{OUT2} should always be connected together for proper operation and lowest dropout voltage.

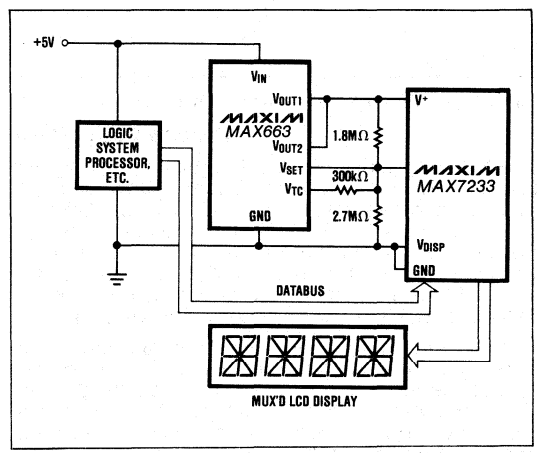


Figure 8. Driving a Multiplexed LCD Display. Consistent operation over more than 40°C temperature span, as opposed to about 10°C with fixed drive voltage, is allowed by negative temperature coefficient drive voltage to the displays. Based on EPSON LDB-728 Display or equivalent.

Dual Mode 5V/Programmable Micropower Voltage Regulators

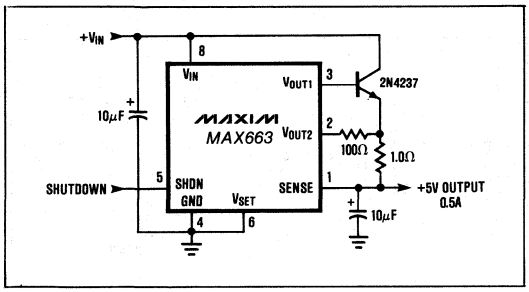


Figure 9. Positive Regulator With Boosted Output, Current Limit, and Low I_Q Shutdown

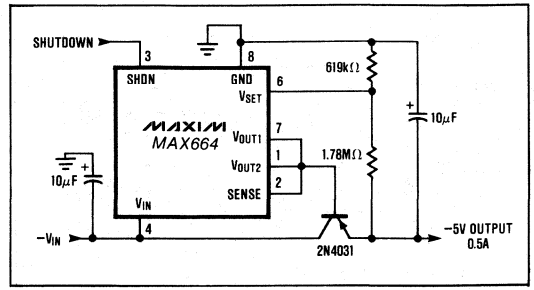


Figure 10. Negative Regulator With Boosted Output and Low I_Q Shutdown

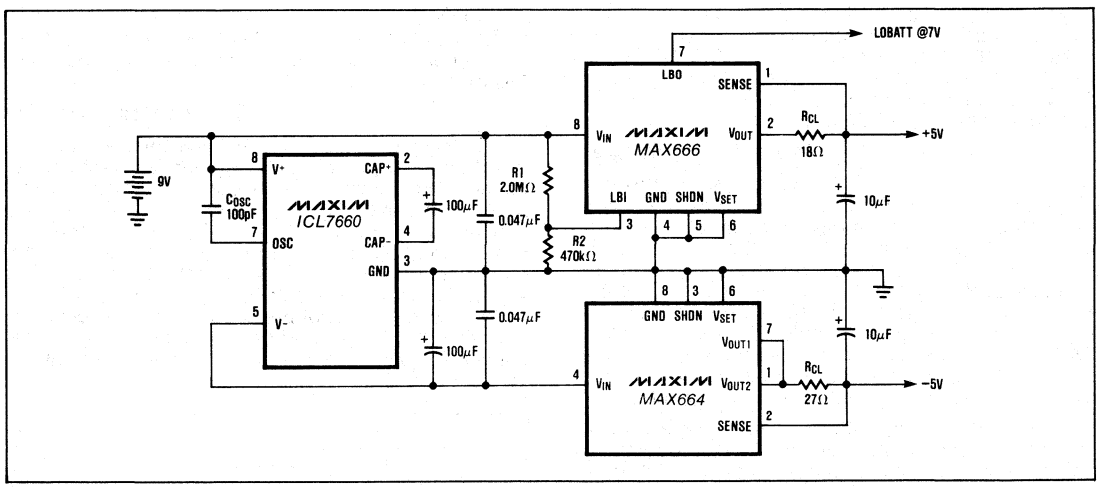


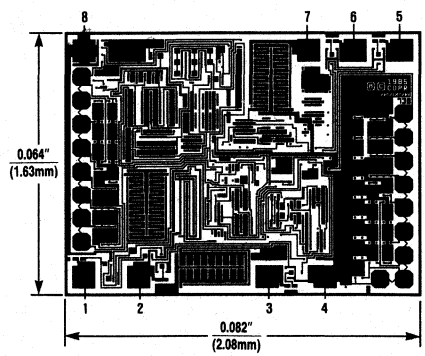
Figure 11. ±5V Power Supply Using One 9V Battery

Bypass Capacitors

The MAX66X series of CMOS regulators is designed primarily for low quiescent current battery powered systems and has limited line and load regulation at frequencies above 10Hz. The high frequency performance is easily improved by adding an output filter capacitor across the load. 10µF is a good typical value. If high frequency performance is not an issue then an output bypass capacitor is not required.

In battery powered systems an input capacitor helps to reduce noise, improve dynamic performance, and reduce the input rate-of-rise at the regulator's input. In extreme cases excessive voltage rate-of-rise at the inputs of CMOS devices can cause SCR latch-up. The low impedance of Ni-Cad and Lead-Acid batteries make this possible when they are switched directly to the regulator input with no current limiting resistance, inductance, or input filtering. The addition of a 0.1µF or greater input capacitor limits the input rate-of-rise to a safe level.

Chip Topography



(See Pin Configurations (front page) for pin functions)

+5V to ±10V Voltage Converter

General Description

The MAX680 is a monolithic CMOS dual charge pump voltage converter that provides ±10V outputs from an input voltage of +5V, using four external capacitors. The MAX680 provides both a positive step-up charge pump to develop +10V from the +5V input and an inverting charge pump to generate the -10V output. The MAX680 includes an on-chip 8kHz oscillator and all the necessary circuitry (except the four capacitors) to produce both positive and negative voltages from a single positive supply.

The output source impedances are typically 150Ω, providing useful output currents up to 10mA. The low quiescent current and high efficiency make this device suitable for a variety of applications that need both positive and negative voltages generated from a single supply.

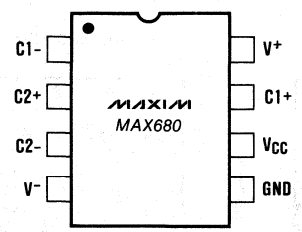
Applications

The MAX680 can be used wherever a single positive supply is available and positive and negative voltages are required. Common applications include the generation of ±6V from a 3V battery and generation of ±10V from the standard +5V logic supply for use with analog circuitry. Typical applications include:

±10V from +5V Logic Supply
±6V from a 3V Lithium Cell
Handheld Instruments
Battery Operated Equipment
Data Acquisition Systems
Panel Meters
Operational Amplifier Power Supplies

Pin Configuration

Top View



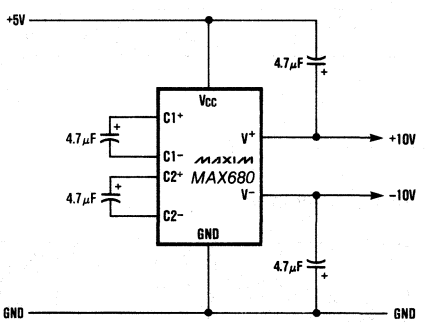
Features

- ◆ 95% Voltage Conversion Efficiency
- ◆ 85% Power Conversion Efficiency
- ◆ Wide Voltage Range: +2.0V to +6.0V
- ◆ Only Four External Capacitors Required
- ◆ 500μA Supply Current
- ◆ Monolithic CMOS Design

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX680C/D	0°C to +70°C	Dice
MAX680CPA	0°C to +70°C	8 Lead Plastic DIP
MAX680CSA	0°C to +70°C	8 Lead Small Outline
MAX680EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX680EJA	-40°C to +85°C	8 Lead CERDIP
MAX680ESA	-40°C to +85°C	8 Lead Small Outline
MAX680MJA	-55°C to +125°C	8 Lead CERDIP

Typical Operating Circuit



+5V to ±10V Converter

+5V to ±10V Voltage Converter

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... +6.2V
V^+ ..... +12V
V^- ..... -12V
V^- Short Circuit Duration ..... Continuous
V^+ Current 75mA
V_{CC} dV/dT 1V/µs

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
Small Outline (derate 6mW/°C above +50°C) 450mW
CERDIP (derate 8mW/°C above +50°C) 800mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

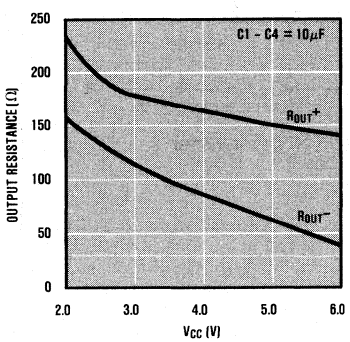
ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = +25°C, test circuit figure 1, unless noted)

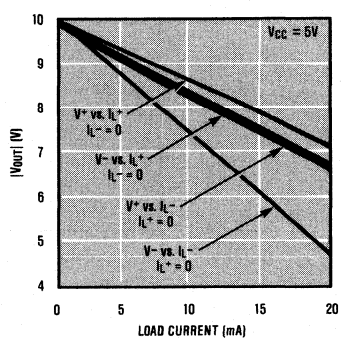
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I_{CC}	V_{CC} = 3V, T_A = +25°C, R_L = ∞ V_{CC} = 5V, T_A = +25°C, R_L = ∞ V_{CC} = 5V, 0°C ≤ T_A ≤ +70°C, R_L = ∞ V_{CC} = 5V, -40°C ≤ T_A ≤ +85°C, R_L = ∞ V_{CC} = 5V, -55°C ≤ T_A ≤ +125°C, R_L = ∞		0.5 1	1 2 2.5 3 3	mA
Supply Voltage Range	V^+	MIN. ≤ T_A ≤ MAX.	2.0	1.5 to 6.0	6.0	V
Positive Charge Pump Output Source Resistance	R_{OUT}^+	I_L^+ = 10mA, I_L^- = 0mA, V_{CC} = 5V, T_A = +25°C I_L^+ = 5mA, I_L^- = 0mA, V_{CC} = 2.8V, T_A = +25°C I_L^+ = 10mA, I_L^- = 0mA, V_{CC} = 5V, 0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		150 180	250 300 325 350 400	Ω
Negative Charge Pump Output Source Resistance	R_{OUT}^-	I_L^+ = 10mA, I_L^- = 0mA, V^+ = 10V, T_A = +25°C I_L^+ = 5mA, I_L^- = 0mA, V^+ = 5.6V, T_A = +25°C I_L^+ = 10mA, I_L^- = 0mA, V^+ = 10V, 0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		90 110	150 175 200 200 250	Ω
Oscillator Frequency	f_{OSC}		4	8		kHz
Power Efficiency	P_{EFF}	R_L = 10kΩ		85		%
Voltage Conversion Efficiency	V_{EFF}	V^+, R_L = ∞ V^-, R_L = ∞	95 90	99 97		%

Typical Operation Characteristics

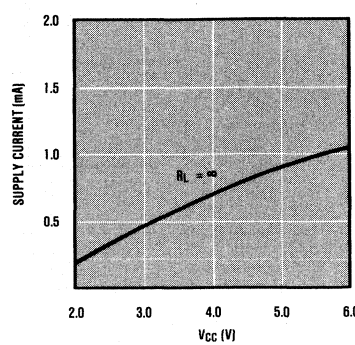
OUTPUT RESISTANCE vs. V_{CC}



V_{OUT} vs. LOAD CURRENT

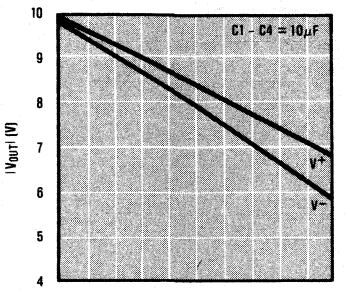


SUPPLY CURRENT vs. V_{CC}

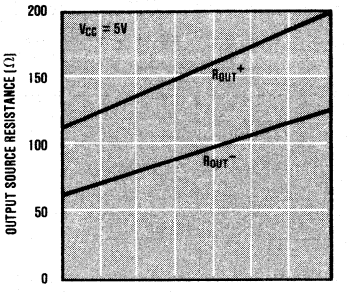


Typical Operation Characteristics

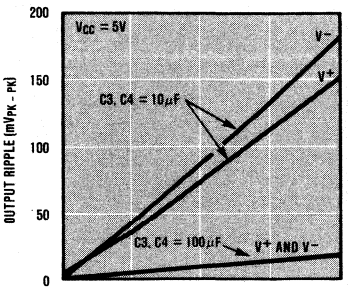
OUTPUT VOLTAGE vs. OUTPUT CURRENT FROM V+ TO V−



OUTPUT SOURCE RESISTANCE vs. TEMPERATURE



OUTPUT RIPPLE vs. OUTPUT CURRENT



Detailed Description

All the circuitry needed to implement a voltage quadrupler is contained in the MAX680. Only four external capacitors are needed. These may be inexpensive polarized electrolytic capacitors with values in the range of 0.1µF to 100µF.

Figure 2A illustrates the idealized operation of the positive voltage converter. The on-chip oscillator generates a 50% duty cycle clock signal. During the first half of the cycle, switches S2 and S4 are open, switches S1 and S3 are closed, and the capacitor C1 is charged to the input voltage V_{CC}. During the second half cycle, switches S1 and S3 are open, S2 and S4 are closed, and the capacitor C1 is translated upward by V_{CC} volts. Assuming ideal switches and no load on C3, charge is transferred onto C3 from C1 such that the voltage on C3 will be $2V_{CC}$, generating the positive supply.

Figure 2B illustrates the negative converter. The switches of the negative converter are out of phase from the positive converter. During the second half of the clock cycle, S6 and S8 are open, S5 and S7 are closed, thus charging C2 from V+ (pumped up to $2V_{CC}$ by the positive charge pump) to GND. In the first half of the clock cycle, S5 and S7 are open, S6 and S8 are closed, and the charge on C2 is transferred to C4, generating the negative supply. The eight switches are CMOS power MOSFETs. Switches S1, S2, S4 and S5 are P-channel devices while switches S3, S6, S7, and S8 are N-channel devices.

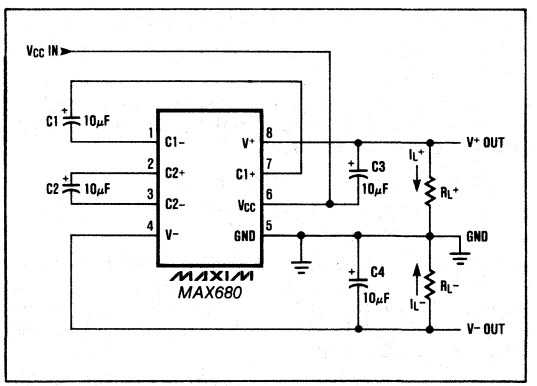


Figure 1. Test Circuit

+5V to ±10V Voltage Converter

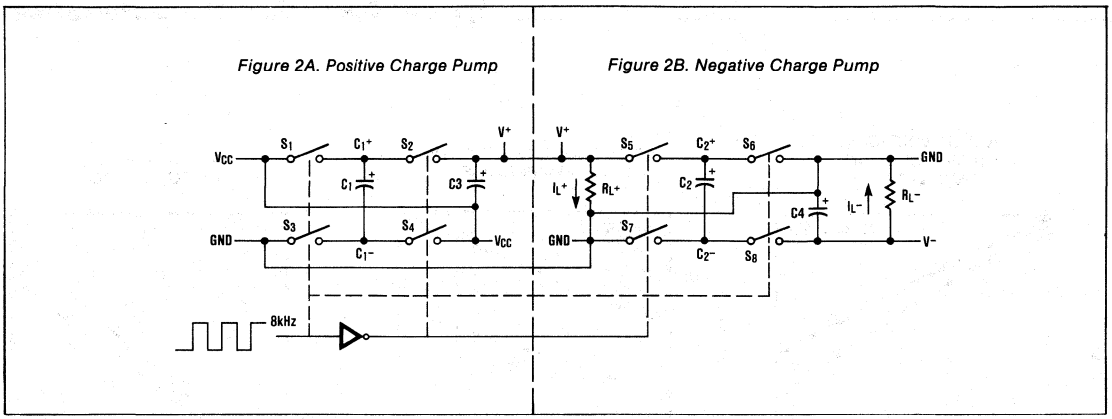


Figure 2. Idealized Voltage Quadrupler

Efficiency Considerations

Theoretically a charge pump voltage multiplier can approach 100% efficiency under the following conditions:

- The charge pump switches have virtually no offset and extremely low on resistance
- Minimal power is consumed by the drive circuitry
- The impedances of the reservoir and pump capacitors are negligible

For the MAX680, the energy loss per clock cycle is the sum of the energy loss in the positive and negative converters as below:

$$Loss_{TOT} = Loss_{POS} + Loss_{NEG}$$

$$= \tfrac{1}{2}C_1[(V^+)^2 - 2(V^+)(V_{CC})] + \tfrac{1}{2}C_2[(V^+)^2 - (V-)^2]$$

There will be a substantial voltage difference between ($V^+ - V_{CC}$) and V_{CC} for the positive pump and between V^+ and V^- if the impedances of the pump capacitors C1 and C2 are high with respect to their respective output loads.

Larger values of reservoir capacitors C3 and C4 will reduce output ripple. Larger values of both pump and reservoir capacitors improve the efficiency.

Maximum Operating Limits

The MAX680 has on-chip zener diodes that clamp V_{CC} to approximately 6.2V, V^+ to 12.4V, and V^- to -12.4V. Never exceed the maximum supply voltage or excessive current may be shunted by these diodes, potentially damaging the chip. The MAX680 will operate over the entire operating temperature range with an input voltage of 2V to 6V.

Applications

Positive and Negative Converter

The most common application of the MAX680 is as a dual charge pump voltage converter which provides positive and negative outputs of two times a positive input voltage. The simple circuit of Figure 3 shows that only four external components are needed, capacitors C1 and C3 for the positive pump and C2 and C4 for the negative pump. In most applications all four capacitors are low-cost 10μF or 22μF polarized electrolytics. For applications where PC board space is at a premium and low currents are being drawn

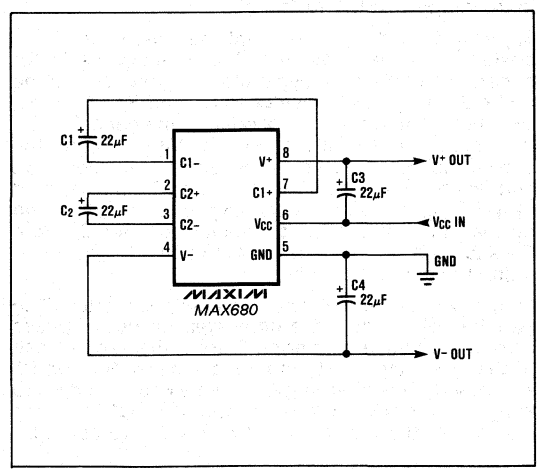


Figure 3. Positive and Negative Converter

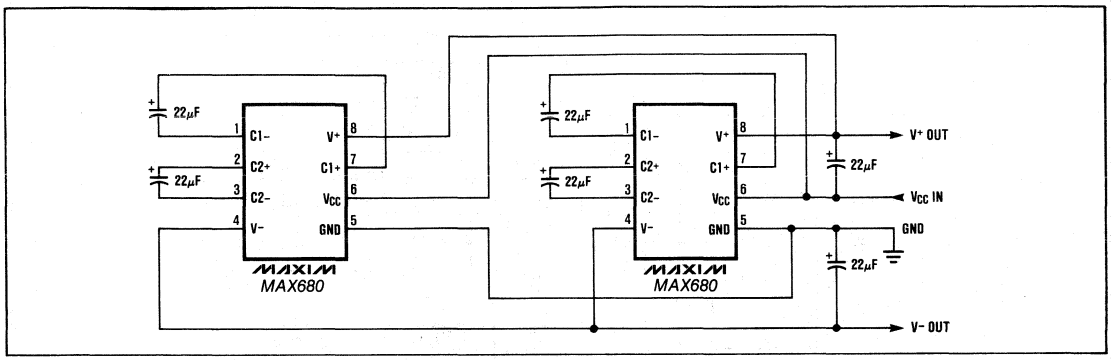


Figure 4. Paralleling MAX680s For Lower Source Resistance

from the MAX680, 1µF reservoir capacitors may be used for the pump capacitors C1 and C2, with 4.7µF reservoir capacitors C3 and C4. Capacitors C1 and C3 must be rated at 6V or greater, and capacitors C2 and C4 must be rated at 12V or greater.

The MAX680 is NOT a voltage regulator; the output source resistance of either charge pump is approximately 150 ohms at room temperature with V_{CC} at 5V. This means that with an input V_{CC} of 5V, under light load V^+ will approach +10V and V^- will be at -10V, but BOTH V^+ and V^- will droop towards GND as the current drawn from EITHER V^+ or V^- increases, since the negative converter draws its power from the output of the positive converter. To predict the output voltages, treat the chip as two separate converters and analyze them separately. First, the droop of the negative supply (V_{DROP}^-) equals the current drawn from V^- - (I_L^-) times the source resistance of the negative converter (RS^-):

$$V_{DROP}^- = I_L^- \times RS^-$$

Likewise, the droop of the positive supply (V_{DROP}^+) equals the current drawn from the positive supply (I_L^+) times the source resistance of the positive converter (RS^+), except that the current drawn from the positive supply is the sum of the current drawn by the load on the positive supply (I_L^+) plus the current drawn by the negative converter (I_L^-):

$$V_{DROP}^+ = I_L^+ \times RS^+ = (I_L^+ + I_L^-) \times RS^+$$

The positive output voltage will be:

$$V^+ = 2V_{CC} - V_{DROP}^+$$

The negative output voltage will be:

$$V^- = -(V^+ - V_{DROP}) = -(2V_{CC} - V_{DROP}^+ - V_{DROP}^-)$$

The positive and negative charge pumps are tested and specified separately to provide the separate values of output source resistance for use in the above formulas. When the positive charge pump is tested, the negative charge pump is unloaded, and when the negative charge pump is tested, the positive supply V^+ is from an external source, isolating the negative charge pump.

The ripple voltage on either output can be calculated by noting that the current drawn from the output is supplied by the reservoir capacitor alone during one half cycle of the clock. This results in a ripple of:

$$V_{RIPPLE} = \frac{1}{2} I_{OUT} (1/f_{PUMP}) (1/CR)$$

For the nominal f_{PUMP} of 8kHz with 10µF reservoir capacitors, the ripple will be 30mV with I_{OUT} at 5mA. Remember that in most applications, the I_{OUT} of the positive charge pump is the load current PLUS the current taken by the negative charge pump.

Paralleling Devices

Paralleling multiple MAX680s reduces the output resistance of both the positive and negative converters. The effective output resistance is the output resistance of a single device divided by the number of devices. As illustrated in Figure 4, each MAX680 requires separate pump capacitors C1 and C2, but all can share a single set of reservoir capacitors.

±5V Regulated Supplies From A Single 3V Battery

Figure 5 shows a complete ±5V power supply using one 3V battery. The MAX680 provides +6V at V^+ which is regulated to +5V by the MAX666 and -6V which is regulated to -5V by the MAX664. The

+5V to ±10V Voltage Converter

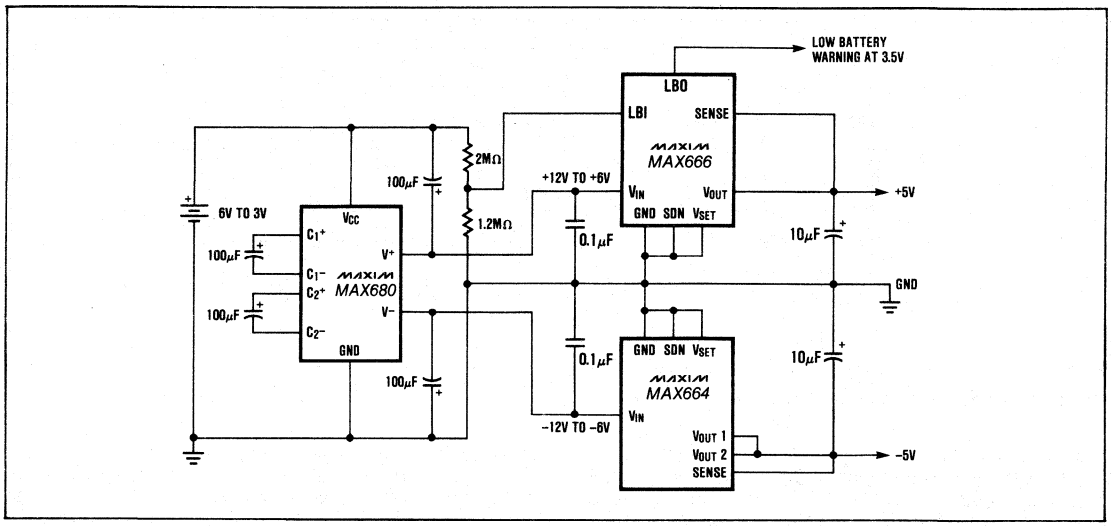
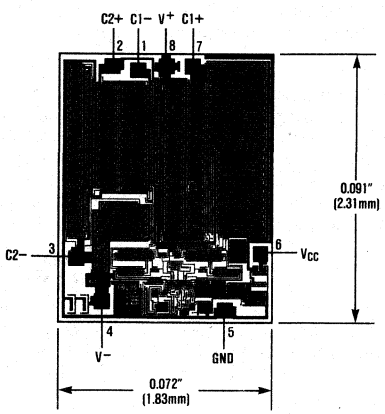


Figure 5. Regulated +5V and -5V From a Single Battery

MAX666 and MAX664 are pre-trimmed at wafer sort and require no external setting resistors, minimizing parts count. The combined quiescent current of the MAX680, MAX663, and MAX664 is less than 500µA, while the output current capability is 5mA. The input to the MAX680 can vary from 3V to 6V without affecting regulation appreciably. With higher input voltage, more current can be drawn from the outputs of the MAX680. With 5V at V_{CC}, 10mA can be drawn from both regulated outputs simultaneously. Assuming 150 ohm source resistance for both converters, with $(I_L^+ + I_L^-) = 20mA$, the positive charge pump will droop 3V, providing +7V for the negative charge pump. The negative charge pump will droop another 1.5V due to its 10mA load, leaving -5.5V at V^-, sufficient to maintain regulation for the MAX664 at this current.

Chip Topography



Note: Connect substrate to V^+.

MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX690 Family of supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include μP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX690 Family significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components.

The MAX690, MAX692 and MAX694 are supplied in 8-pin packages and provide four functions:
1) A Reset output during power-up, power-down and brownout conditions.
2) Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
3) A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
4) A 1.3V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MAX691, MAX693 and MAX695 are supplied in 16-pin packages and perform all MAX690/692/694 functions, plus:
1) Write protection of CMOS RAM or EEPROM.
2) Adjustable reset and watchdog timeout periods.
3) Separate outputs for indicating a watchdog timeout, backup-battery switchover, and low V_{CC}.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μP Power Monitoring

Features

- **Precision Voltage Monitor**
  4.65V in MAX690, MAX691, MAX694 and MAX695
  4.40V in MAX692 and MAX693
- **Power OK/Reset Time Delay – 50, 200ms, or adjustable**
- **Watchdog Timer – 100ms, 1.6 sec, or adjustable**
- **Minimum Component Count**
- **1μA Standby Current**
- **Battery Backup Power Switching**
- **Onboard Gating of Chip Enable Signals**
- **Voltage Monitor for Power Fail or Low Battery Warning**

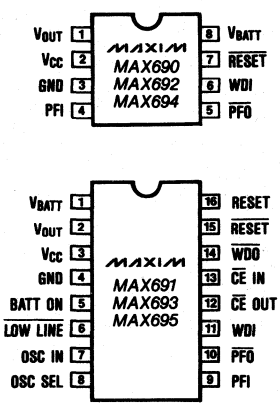
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX690CPA	0°C to +70°C	8 Lead Plastic DIP
MAX690EPA	−40°C to +85°C	8 Lead Plastic DIP
MAX690EJA	−40°C to +85°C	8 Lead CERDIP
MAX690MJA	−55°C to +125°C	8 Lead CERDIP
MAX691C/D	0°C to +70°C	Dice
MAX691CPE	0°C to +70°C	16 Lead Plastic DIP
MAX691CWE	0°C to +70°C	16 Lead Wide SO
MAX691EPE	−40°C to +85°C	16 Lead Plastic DIP
MAX691EJE	−40°C to +85°C	16 Lead CERDIP
MAX691EWE	−40°C to +85°C	16 Lead Wide SO
MAX691MJE	−55°C to +125°C	16 Lead CERDIP

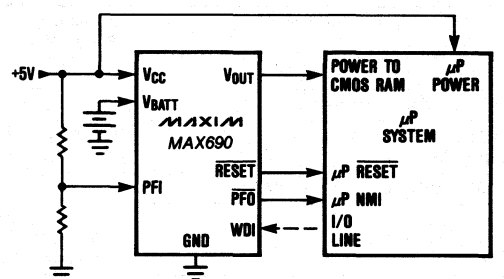
(Ordering information is continued on last page.)

Pin Configuration

Top View



Typical Operating Circuit



MAX690 Typical Application

6

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... −0.3V to 6.0V
- V_{BATT} ..... −0.3V to 6.0V
- All Other Inputs (Note 1) .. −0.3V to (V_{OUT} +0.5V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... short circuit protected
- All Other Outputs 20mA

Rate-of-Rise, V_{BATT}, V_{CC} 100V/μs

Operating Temperature Range
- C suffix ..... 0°C to +70°C
- E suffix ..... −40°C to +85°C
- M suffix ..... −55°C to +125°C

Power Dissipation
- 8 Pin Plastic DIP (Derate 5mW/°C above +70°C) 400mW
- 8 Pin CERDIP (Derate 8mW/°C above +85°C) 500mW
- 16 Pin Plastic DIP (Derate 7mW/°C above +70°C) 600mW
- 16 Pin Small Outline (Derate 7mW/°C above +70°C) 600mW
- 16 Pin CERDIP (Derate 10mW/°C above +85°C) 600mW

Storage Temperature Range ..... −65°C to +160°C

Lead Temperature (Soldering, 10 seconds) .... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATTERY BACKUP SWITCHING					
Operating Voltage Range MAX690, MAX691, MAX694, MAX695 V_{CC} MAX690, MAX691, MAX694, MAX695 V_{BATT} MAX692, MAX693 V_{CC} MAX692, MAX693 V_{BATT}		 4.75 2.0 4.5 2.0		 5.5 4.25 5.5 4.0	V
V_{OUT} Output Voltage	I_{OUT} = 1mA I_{OUT} = 50mA	V_{CC}−0.3 V_{CC}−0.5	V_{CC}−0.1 V_{CC}−0.25		V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250μA, V_{CC} < V_{BATT}−0.2V	V_{BATT}−0.1	V_{BATT}−0.02		V
Supply Current (excludes I_{OUT})	I_{OUT} = 1mA I_{OUT} = 50mA		2 3.5	5 10	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V		0.6	1	μA
Battery Standby Current (+ = Discharge, − = Charge)	5.5V > V_{CC} > V_{BATT}+0.2V T_A = 25°C T_A = Full Operating Range	 −0.1 −1.0		 +0.02 +0.02	μA
Battery Switchover Threshold V_{CC} − V_{BATT}	Power Up Power Down		70 50		mV
Battery Switchover Hysteresis			20		mV
BATT ON Output Voltage	I_{SINK} = 3.2mA			0.4	V
BATT ON Output Short Circuit Current	BATT ON = V_{OUT} = 4.5V Sink Current BATT ON = 0V Source Current	 0.5	25 1	 25	mA μA
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	T_A = Full Operating Range MAX690, MAX691, MAX694, MAX695 MAX692, MAX693	 4.5 4.25	 4.65 4.4	 4.75 4.5	 V V

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Threshold Hysteresis			40		mV
Reset Timeout Delay (MAX690/91/92/93)	Figure 6. OSC SEL HIGH, V_{CC} = 5V	35	50	70	ms
Reset Timeout Delay (MAX694/95)	Figure 6. OSC SEL HIGH, V_{CC} = 5V	140	200	280	ms
Watchdog Timeout Period, Internal Oscillator	Long Period, V_{CC} = 5V Short Period, V_{CC} = 5V	1.0 70	1.6 100	2.25 140	sec ms
Watchdog Timeout Period, External Clock	Long Period Short Period	3840 768		4097 1025	Clock Cycles
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V_{IH} = 3.5V	200			ns
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage	I_{SINK} = 1.6mA, V_{CC} = 4.25V I_{SOURCE} = 1µA, V_{CC} = 5V	 3.5		0.4	V
RESET and $\overline{WDO}$ Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 1µA, V_{CC} = 5V	 3.5		0.4	V
Output Short Circuit Current	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOW\ LINE}$	1	3	25	µA
WDI Input Threshold Logic Low Logic High	V_{CC} = 5V (Note 2)	 3.5		0.8	V
WDI Input current	WDI = V_{OUT} WDI = 0V	 −50	20 −15	50	µA
POWER FAIL DETECTOR					
PFI Input Threshold	V_{CC} = +5V, T_A = Full	1.2	1.3	1.4	V
PFI Input Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 1µA	 3.5		0.4	V V
$\overline{PFO}$ Short Circuit Source Current	PFI = 0V, $\overline{PFO}$ = 0V	1	3	25	µA
CHIP ENABLE GATING					
$\overline{CE}$ IN Thresholds	V_{IL} V_{IH}	 3.0		0.8	V
$\overline{CE}$ IN Pullup Current			3		µA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 3.0mA I_{SOURCE} = 1µA, V_{CC} = 0V	 V_{OUT}−1.5 V_{OUT}−0.05		0.4	V
$\overline{CE}$ Propagation Delay	V_{CC} = 5V		50	200	ns
OSCILLATOR					
OSC IN Input Current			±2		µA
OSC SEL Input Pullup Current			5		µA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V C_{OSC} = 47pF		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

Microprocessor Supervisory Circuits

Pin Description

NAME	PIN		FUNCTION
	MAX690/ 692/694	MAX691/ 693/695	
V_{CC}	2	3	The +5V input.
V_{BATT}	8	1	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	1	2	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	3	4	0V Ground reference for all signals.
$\overline{RESET}$	7	15	$\overline{RESET}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MAX690/ 691/694/695, and 4.4V for the MAX692 and MAX693. $\overline{RESET}$ remains low for 50ms after V_{CC} returns to 5V, (except 200ms in MAX694/695). $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	6	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	4	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	5	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN	—	13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT	—	12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold (4.65V for MAX691 and MAX695, 4.4V for MAX693). See Figure 6.
BATT ON	—	5	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 25mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
$\overline{LOW\ LINE}$	—	6	$\overline{LOW\ LINE}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
RESET	—	16	RESET is an active high output. It is the inverse of $\overline{RESET}$.
OSC SEL	—	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3μA internal pullup. See Table 1.
OSC IN	—	7	When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog timeout period. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 8. When OSC SEL is high or floating, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$	—	14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.

Typical Applications

MAX691, MAX693 and MAX695

A typical connection for the MAX691/693/695 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when 5V power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 25mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 200Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1μA maximum when V_{CC} is between 0V and V_{BATT}-700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a RESET output to hold the microprocessor's Reset line low when V_{CC} is below 4.65V (4.4V for MAX693). An internal monostable holds RESET low for 50ms* after V_{CC} rises above 4.65V (4.4V for MAX693). This prevents repeated toggling of RESET even if the 5V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, RESET must be held low until the microprocessor clock oscillator has started. The MAX690 Family power-up RESET pulse lasts 50ms* to allow for this oscillator start-up time. The manual reset switch and the 0.1μF capacitor connected to the reset bus can be omitted if manual reset is not needed. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MAX691/93/95 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The +5V power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.3V, the Power Fail Output (PFO) drives the processor's NMI input low. If a Power Fail threshold of 4.8V is chosen, the microprocessor will have the time when V_{CC} fails from 4.8V to 4.65V to save data into RAM. An earlier power fail warning can be generated if the unregulated DC input of the 5V regulator is available for monitoring.

RAM Write Protection

The MAX691/93/95 $\overline{CE}$ OUT line drives the Chip Select inputs of the CMOS RAM. $\overline{CE}$ OUT follows $\overline{CE}$ IN as long as V_{CC} is above the 4.65V (4.4V for MAX693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{CE}$ OUT goes high, independent of the logic level at $\overline{CE}$ IN. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The LOW LINE output goes low when V_{CC} falls below 4.65V (4.4V for MAX693).

*200ms for MAX695

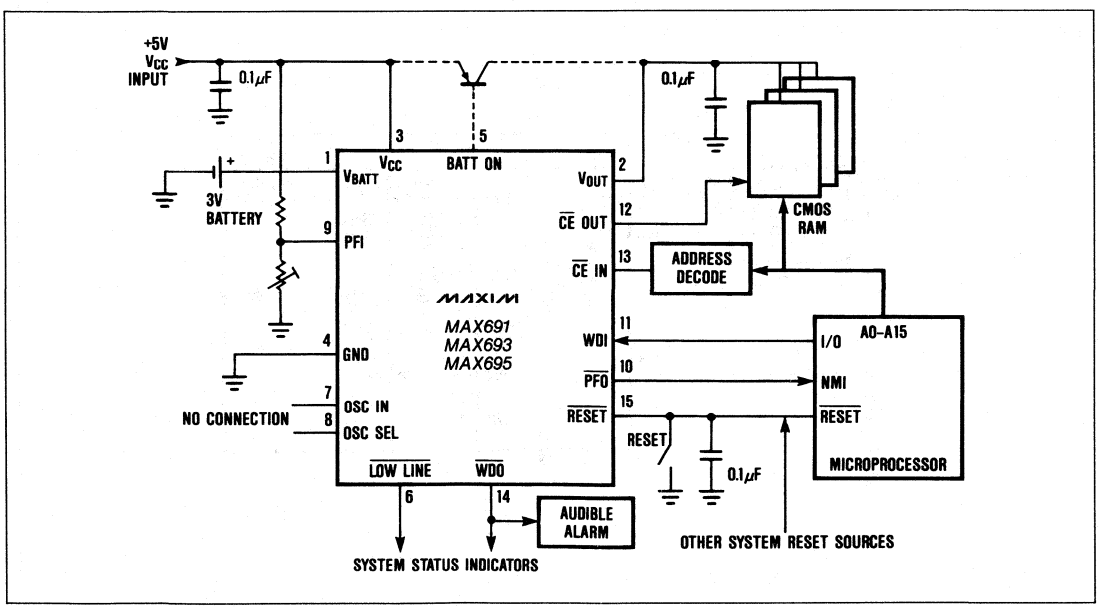


Figure 1. MAX691/693/695 Typical Application

Microprocessor Supervisory Circuits

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI not toggled, the MAX691/93 will issue a 50ms* RESET pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new RESET pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{WDO}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{WDO}$ goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MAX690, MAX692 and MAX694

The 8 pin MAX690, MAX692 and MAX694 have most of the features of the MAX691, MAX693 and MAX695.

*200ms for MAX695

Figure 2 shows the MAX690/692/694 in a typical application. Operation is much the same as with the MAX691/693/695 (Figure 1) but in this case the Power Fail Input (PFI) monitors the unregulated input to the 7805 regulator. The MAX690/694 RESET output goes low when V_{CC} falls below 4.65V. The RESET output of the MAX692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 50mA. The MAX690/692/694 does not have a BATT ON output to drive an external transistor. The MAX690/92/94 also does not include chip enable gating circuitry that is available on the MAX691/93/95. In many systems though, CE gating is not needed since a low input to the microprocessor RESET line prevents the processor from writing to RAM during power-up and power-down transients.

The MAX690/92/94 watchdog timer has a fixed 1.6 second timeout period. If WDI remains either low or high for more than 1.6 seconds, a RESET pulse is sent to the microprocessor. The watchdog timer is disabled if WDI is left floating.

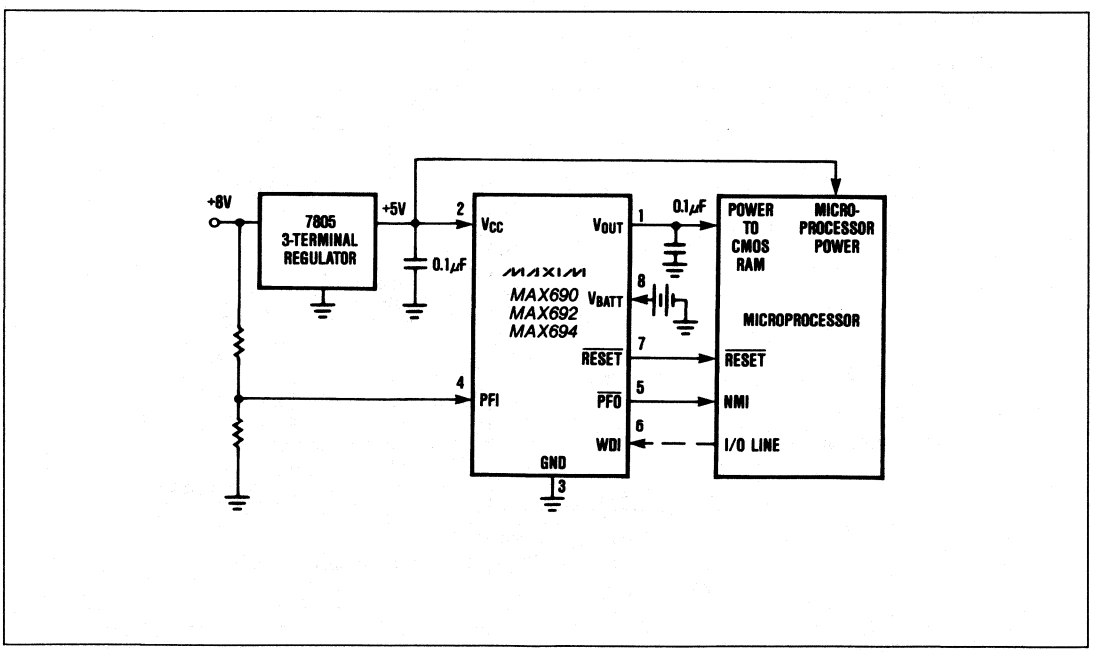


Figure 2. MAX690/692/694 Typical Application

Detailed Description

Battery-Switchover and VOUT

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output (MAX691/693/695 only) can directly drive the base of the external transistor.

It should be noted that the MAX690/91/92/93/94/95 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200Ω MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} – 700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MAX690/691/694/695 operates with battery voltages from 2.0V to 4.25V while the MAX692/693 operates with battery voltages from 2.0V to 4.0V. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small charging current of typically 10nA (0.1µA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (0.1µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

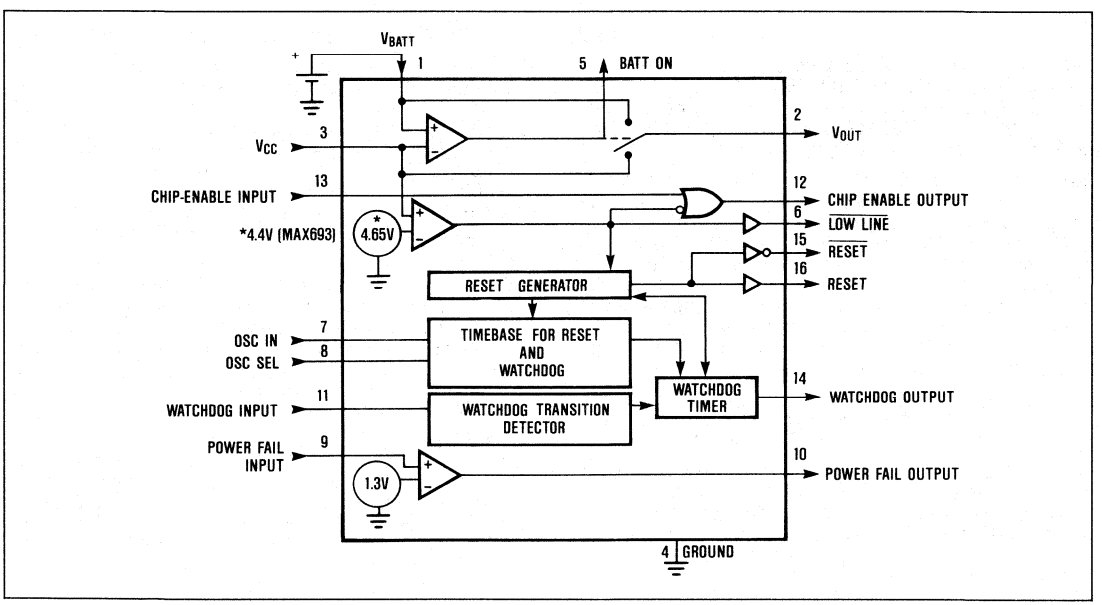


Figure 3. MAX691/693/695 Block Diagram

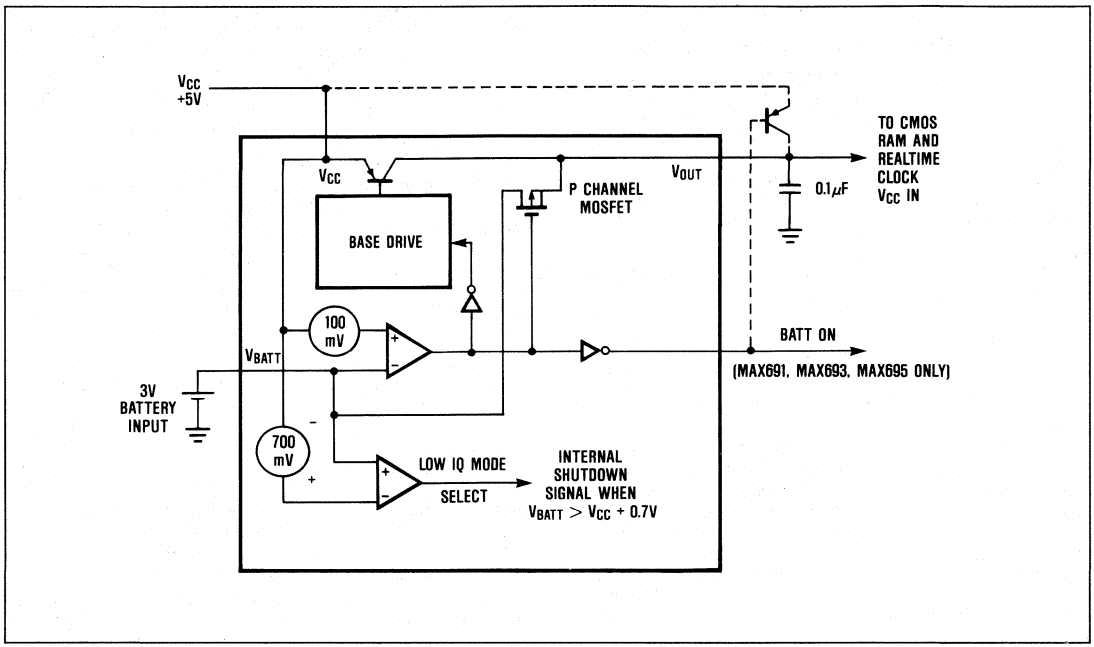


Figure 4. Battery-Switchover Block Diagram

Reset Output

$\overline{\text{RESET}}$ is an active low output which goes low whenever V_{CC} falls below 4.5V (MAX690/691/694/695) or 4.25V (MAX692/693). It will remain low until V_{CC} rises above 4.75V (MAX690/691/694/695) or 4.5V (MAX692/693) for 50 milliseconds*. See Figures 5 and 6.

The guaranteed minimum and maximum thresholds of the MAX690/691/694/695 are 4.5V and 4.75V, while the guaranteed thresholds of the MAX692/693 are 4.25V and 4.5V. The MAX690/691/694/695 is compatible with 5V supplies with a +10%, −5% tolerance while the MAX692/693 is compatible with 5V±10% supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MAX690/691/694/695, and 4.4V in the MAX692/693.

The response time of the reset voltage comparator is about 100μs. V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{\text{RESET}}$ output.

$\overline{\text{RESET}}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{RESET}}$ has an internal 3μA pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

**200ms for MAX694 and MAX695*

$\overline{\text{CE}}$ Gating and RAM Write Protection

The MAX691, MAX693 and MAX695 use two pins to control the Chip Enable or Write inputs of CMOS RAMs. When V_{CC} is +5V, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max) an internal gate forces $\overline{\text{CE}}$ OUT high, independent of $\overline{\text{CE}}$ IN. The MAX693 $\overline{\text{CE}}$ OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The $\overline{\text{CE}}$ output of both devices is also forced high when V_{CC} is less than V_{BATT}. (See Figure 5.)

$\overline{\text{CE}}$ OUT typically drives the $\overline{\text{CE}}$, $\overline{\text{CS}}$, or $\overline{\text{Write}}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{\text{CE}}$ OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{\text{CE}}$ OUT is too long, connect $\overline{\text{CE}}$ IN to GND and use the resulting $\overline{\text{CE}}$ OUT to control a high speed external logic gate. A second alternative is to AND the LOW LINE output with the $\overline{\text{CE}}$ or WR signal. An external logic gate and the $\overline{\text{RESET}}$ output of the MAX690/692/694 can also be used for CMOS RAM write protection.

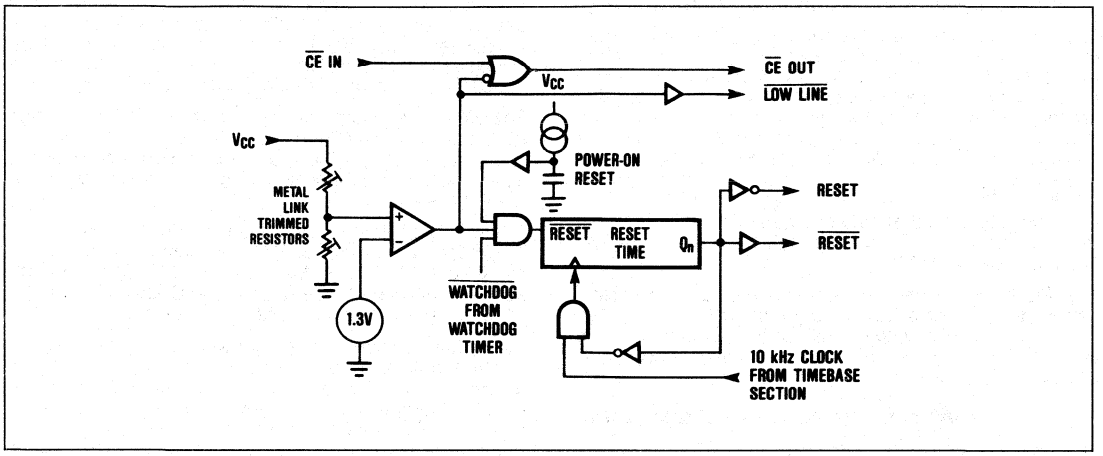


Figure 5. Reset Block Diagram

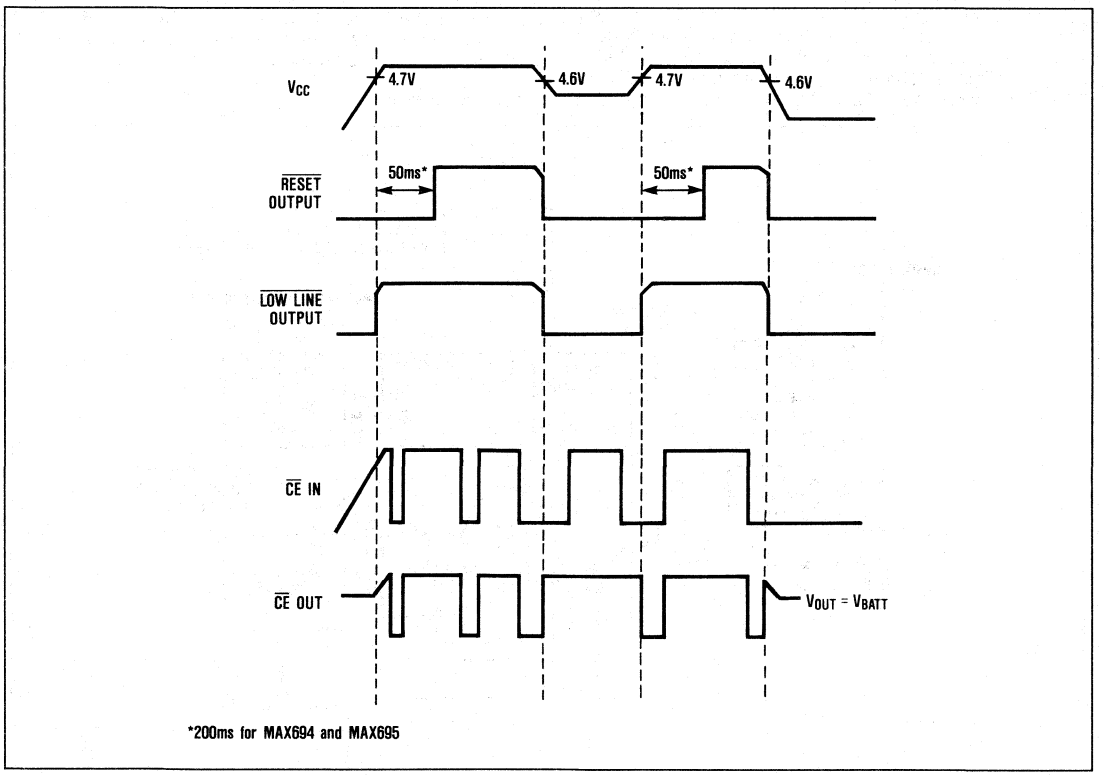


Figure 6. Reset Timing

Microprocessor Supervisory Circuits

1.3V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output (PFO) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the +5V supply falls below 4.75V. PFO is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the RESET output goes low (4.5V for MAX692/93).

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and PFO is forced low when V_{CC} is lower than the V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 millisecond* RESET pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX691/693/695 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after RESET has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output ($\overline{WDO}$, MAX691/693/695 only) goes low if the watchdog timer "times out" and remains low until set high by the next transition on the watchdog input. WDO is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6 seconds and the reset pulse width is fixed at 50ms* on the 8-pin MAX690, MAX692 and MAX694. The MAX691, MAX693 and MAX695 allow these times to be adjusted per Table 1. Figure 8 shows various oscillator configurations.

The internal oscillator is enabled when OSC SEL is floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to re-initialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

*200ms for MAX694

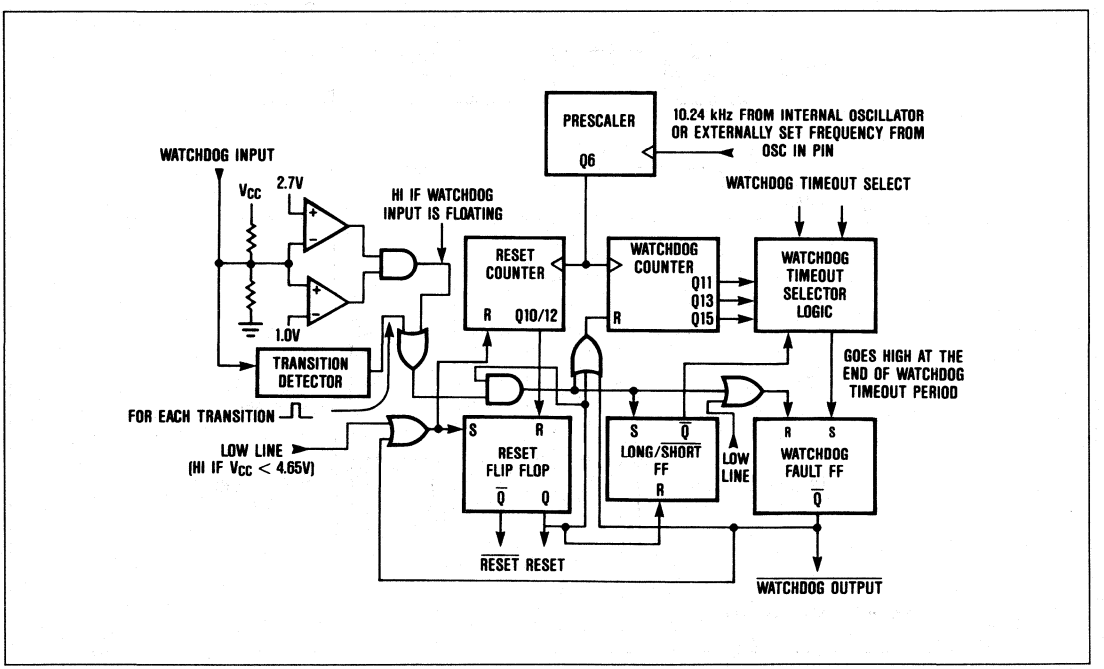


Figure 7. Watchdog Timer Block Diagram

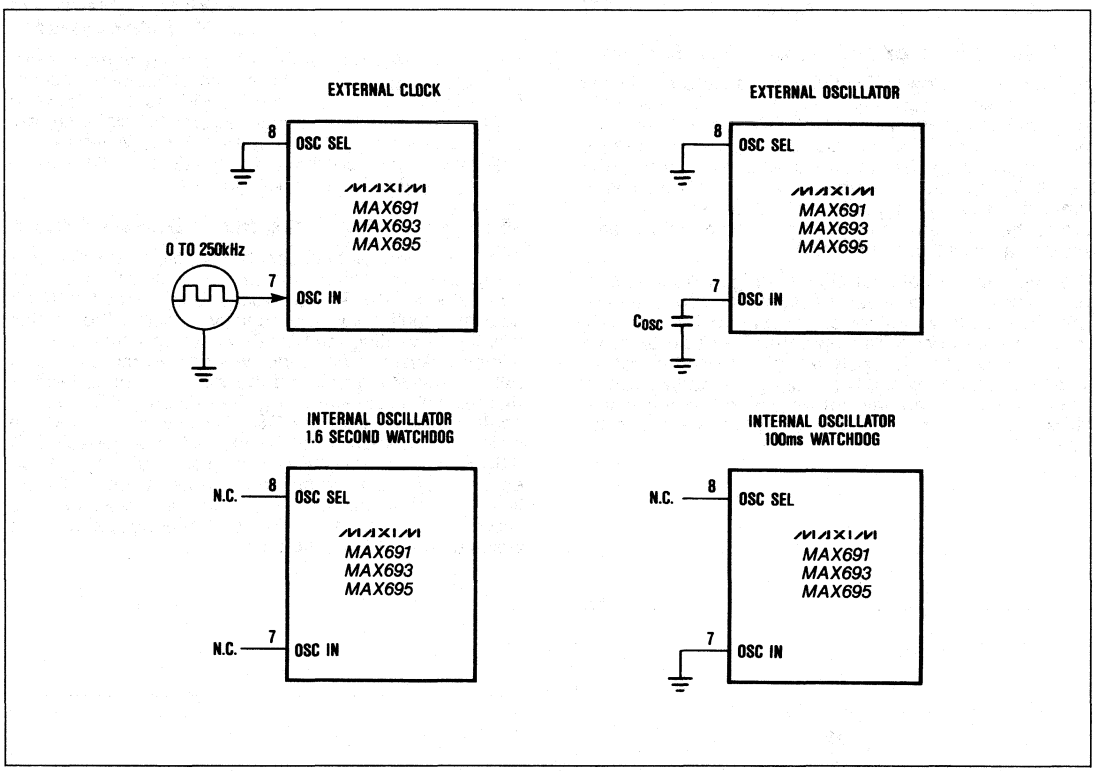


Figure 8. Oscillator Circuits

Table 1. MAX691, MAX693 and MAX695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period	
		Normal	Immediately After Reset	MAX691/93	MAX695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor	$\frac{400ms}{47pF} \times C$	$\frac{1.6\ sec}{47pF} \times C$	$\frac{200ms}{47pF} \times C$	$\frac{800ms}{47pF} \times C$
Floating	Low	100ms	1.6 sec	50ms	200ms
Floating	Floating	1.6 sec	1.6 sec	50ms	200ms

Note 1: The MAX690/692/694 watchdog timeout period is fixed at 1.6 seconds nominal, the MAX690/692 Reset pulse width is fixed at 50ms nominal and the MAX694 is 200ms nominal.

Note 2: When the MAX691 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is

$$F_{OSC}(Hz) = \frac{184,000}{C(pF)}$$

Note 3: See Electrical Characteristics Table for minimum and maximum timing values.

Microprocessor Supervisory Circuits

Application Hints

Other Uses of the Power Fail Detector

In Figure 9 the Power Fail Detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the Power Fail Detector is not as accurate as the onboard Reset voltage detector, a trimpot must be used to adjust the voltage detection threshold. Both the $\overline{PFO}$ and $\overline{RESET}$ outputs have high sink current capability and only 10μA of source current drive. This allows the two outputs to be connected directly to each other in a "wired or" fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 12. When $\overline{PFO}$ is low, resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 13). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01μF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 14 is used.

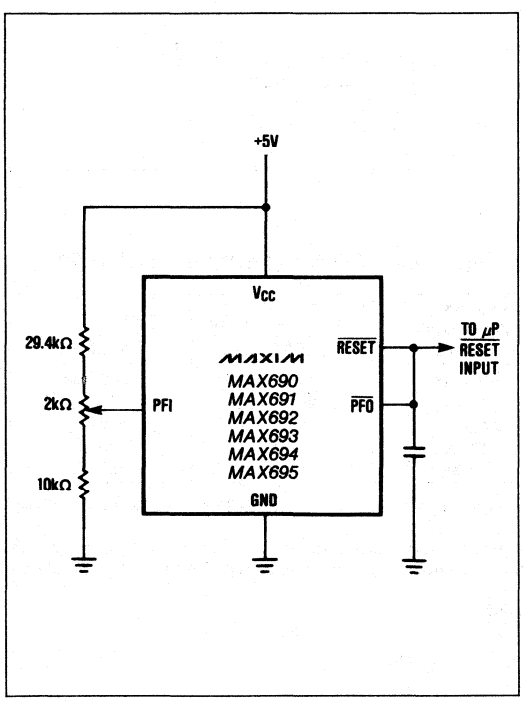


Figure 9. Externally Adjustable V_{CC} Reset Threshold

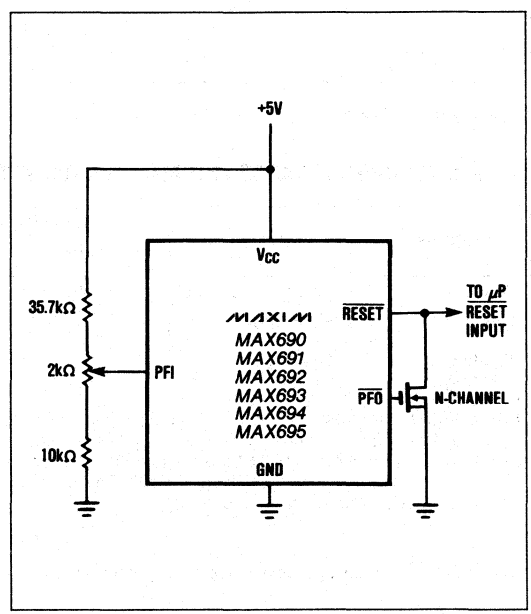


Figure 10. Reset on Overvoltage or Undervoltage

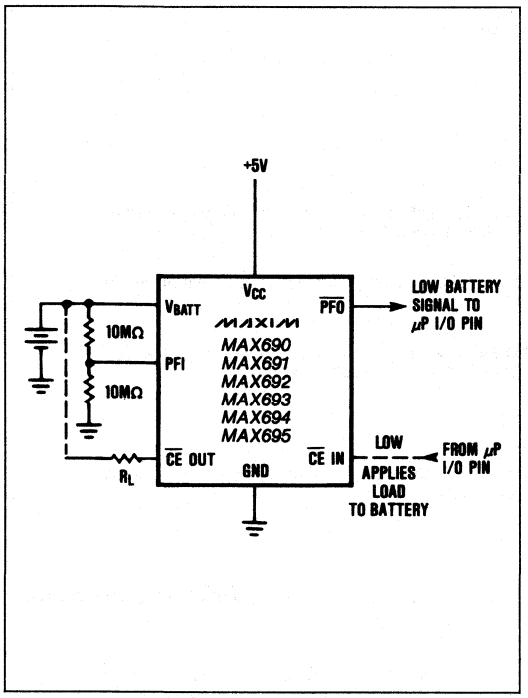


Figure 11. Backup Battery Monitor with Optional Test Load

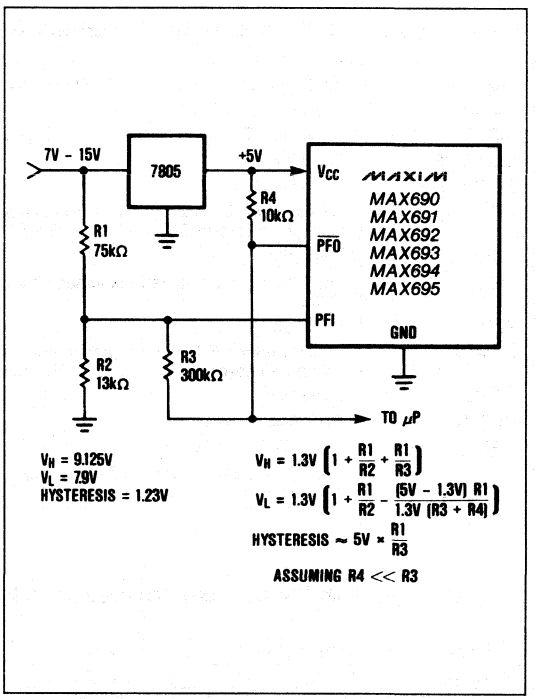


Figure 12. Adding Hysteresis to the Power Fail Voltage Comparator

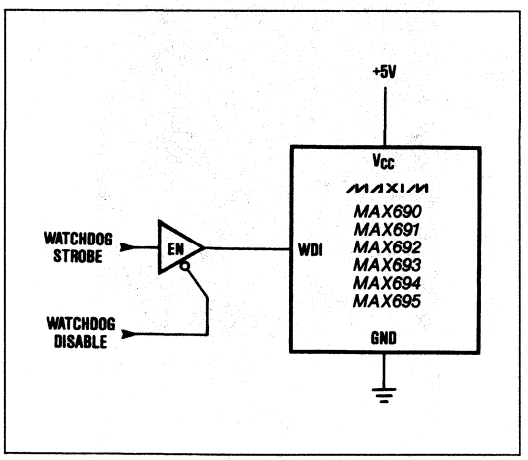


Figure 13. Disabling the Watchdog Under Program Control

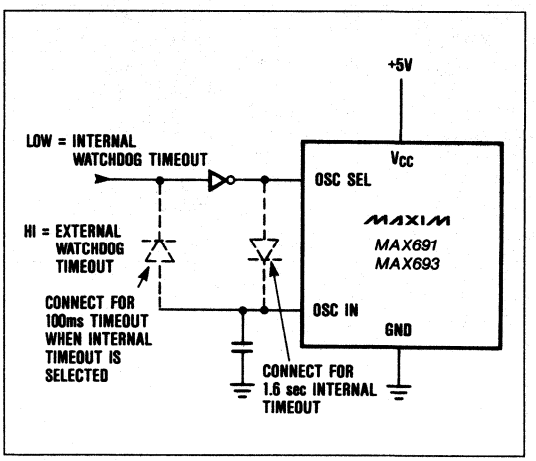


Figure 14. Selecting Internal or External Watchdog Timeout

Microprocessor Supervisory Circuits

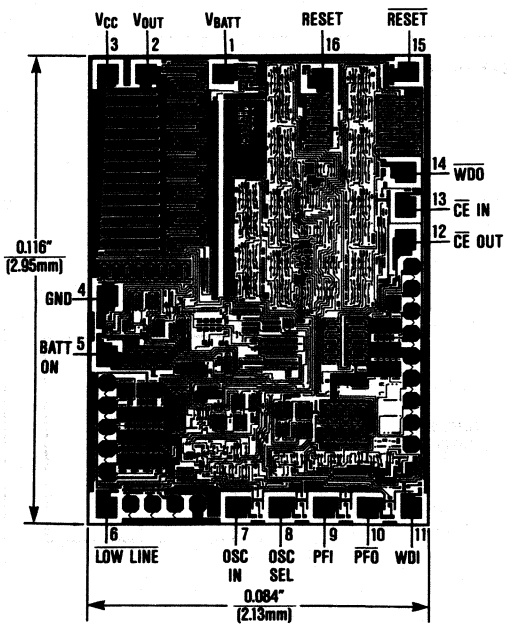
Table 2. Input and Output Status In Battery Backup Mode

V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
$\overline{RESET}$	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
BATT ON	Logic high
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{CE}$ OUT	Logic high
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12μA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} +100mV and V_{BATT} −700mV. The supply current is 1μA maximum when V_{CC} is less than V_{BATT} −700mV.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX692CPA	0°C to +70°C	8 Lead Plastic DIP
MAX692EPA	−40°C to +85°C	8 Lead Plastic DIP
MAX692EJA	−40°C to +85°C	8 Lead CERDIP
MAX692MJA	−55°C to +125°C	8 Lead CERDIP
MAX693C/D	0°C to +70°C	Dice
MAX693CPE	0°C to +70°C	16 Lead Plastic DIP
MAX693CWE	0°C to +70°C	16 Lead Small Outline
MAX693EPE	−40°C to +85°C	16 Lead Plastic DIP
MAX693EJE	−40°C to +85°C	16 Lead CERDIP
MAX693EWE	−40°C to +85°C	16 Lead Small Outline
MAX693MJE	−55°C to +125°C	16 Lead CERDIP
MAX694CPA	0°C to +70°C	8 Lead Plastic DIP
MAX694EPA	−40°C to +85°C	8 Lead Plastic DIP
MAX694EJA	−40°C to +85°C	8 Lead CERDIP
MAX694MJA	−55°C to +125°C	8 Lead CERDIP
MAX695C/D	0°C to +70°C	Dice
MAX695CPE	0°C to +70°C	16 Lead Plastic DIP
MAX695CWE	0°C to +70°C	16 Lead Small Outline
MAX695EPE	−40°C to +85°C	16 Lead Plastic DIP
MAX695EJE	−40°C to +85°C	16 Lead CERDIP
MAX695EWE	−40°C to +85°C	16 Lead Small Outline
MAX695MJE	−55°C to +125°C	16 Lead CERDIP

Chip Topography



MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX696/697 supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include μP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX696/697 significantly improves system reliability and accuracy compared to that obtained with separate ICs or discrete components.

The MAX696 and MAX697 are supplied in 16 pin packages and perform six functions:

1. A Reset output during power-up, power-down and brownout conditions. The threshold for this "low line" reset is adjustable by an external voltage divider.
2. A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
3. Individual outputs for low line and watchdog fault conditions.
4. The Reset time may be left at its default value of 50 ms. or may be varied with an external capacitor or clock pulses.
5. A separate 1.3 volt threshold detector for power fail warning, low battery detection, or to monitor a power supply other than V_{CC}.

The MAX696 also has battery backup switching for CMOS RAM, CMOS microprocessor, or other low power logic.

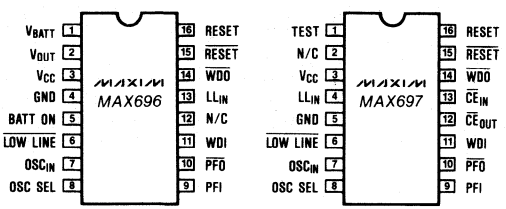
The MAX697 lacks battery backup switching, but has write protection pins ($\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$) for CMOS RAM or EPROM. In addition, it consumes less than 250 microamperes.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μP Power Monitoring

Pin Configurations

Top View



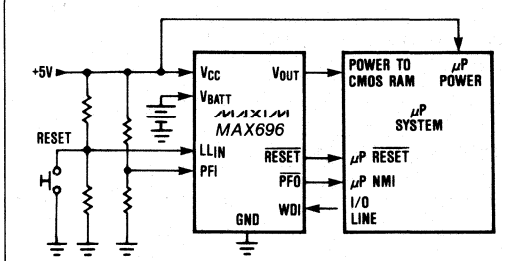
Features

- ◆ **Adjustable Low Line monitor and Power Down Reset**
- ◆ **Power OK/Reset Time Delay**
- ◆ **Watchdog Timer—100ms, 1.6 sec, or adjustable**
- ◆ **Minimum Component Count**
- ◆ **1μA Standby Current**
- ◆ **Battery Backup Power Switching (MAX696)**
- ◆ **Onboard Gating of Chip Enable Signals (MAX697)**
- ◆ **Separate Monitor for Power Fail or Low Battery Warning**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX696C/D	0°C to +70°C	Dice
MAX696CPE	0°C to +70°C	16 Lead Plastic DIP
MAX696CWE	0°C to +70°C	16 Lead Wide SO
MAX696EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX696EJE	-40°C to +85°C	16 Lead CERDIP
MAX696EWE	-40°C to +85°C	16 Lead Wide SO
MAX696MJE	-55°C to +125°C	16 Lead CERDIP
MAX697C/D	0°C to +70°C	Dice
MAX697CPE	0°C to +70°C	16 Lead Plastic DIP
MAX697CWE	0°C to +70°C	16 Lead Wide SO
MAX697EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX697EJE	-40°C to +85°C	16 Lead CERDIP
MAX697EWE	-40°C to +85°C	16 Lead Wide SO
MAX697MJE	-55°C to +125°C	16 Lead CERDIP

Typical Operating Circuit



MAX696 Typical Application

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- V_{BATT} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{OUT} +0.5V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... short circuit protected
- All Other Outputs 20mA

Rate-of-Rise, V_{BATT}, V_{CC} 100V/μs

Operating Temperature Range
- C suffix ..... 0°C to +70°C
- E suffix ..... -40°C to +85°C
- M suffix ..... -55°C to +125°C

Power Dissipation
- 16 Pin Plastic DIP (Derate 7mW/°C above +70°C) 600mW
- 16 Pin Small Outline (Derate 7mW/°C above +70°C) 600mW
- 16 Pin CERDIP (Derate 10mW/°C above +85°C) 600mW

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (Soldering, 10 seconds) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range MAX696 V_{CC} MAX696 V_{BATT} MAX697 V_{CC}	T_A = Full	 3.0 2.0 3.0		 5.5 V_{CC} -0.3V 5.5	V
Supply Current (MAX697)	T_A = Full		160	300	μA
BATTERY BACKUP SWITCHING (MAX696)					
V_{OUT} Output Voltage	I_{OUT} = 1mA, T_A = Full I_{OUT} = 50mA, T_A = Full	V_{CC} -0.3 V_{CC} -0.5		V_{CC} -0.1 V_{CC} -0.25	V
V_{OUT} in Battery Backup Mode	I_{OUT} = 250μA, $V_{CC} < V_{BATT}$ -0.2V, T_A = Full	V_{BATT} -0.1		V_{BATT} -0.02	V
Supply Current (excludes I_{OUT})	I_{OUT} = 1mA I_{OUT} = 50mA		1.5 2.5	4 7	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V, T_A = 25°C V_{CC} = 0V, V_{BATT} = 2.8V, T_A = Full		0.6	1 10	μA
Battery Standby Leakage Current	5.5V > V_{CC} > V_{BATT}+0.3V T_A = 25°C T_A = Full	-100 -1		+20 +0.02	nA μA
Battery Switchover Threshold V_{CC}-V_{BATT}	Power Up Power Down		70 50		mV
Battery Switchover Hysteresis			20		mV
BATT ON Output Voltage	I_{SINK} = 1.6mA			0.4	V
BATT ON Output Short Circuit Current	BATT ON = V_{OUT} = 2.4V Sink Current BATT ON = V_{OUT}, V_{CC} = 0V	 0.5	7 2.5	 25	mA μA
RESET AND WATCHDOG TIMER					
Low Line Voltage Threshold (LL_{IN})	V_{CC} = +5V, +3V, T_A = Full	1.25	1.30	1.35	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Timeout Delay	Figure 6. OSC SEL HIGH, V_{CC} = 5V	35	50	70	ms
Watchdog Timeout Period, Internal Oscillator	Long Period, V_{CC} = 5V Short Period, V_{CC} = 5V	1.0 70	1.6 100	2.25 140	sec ms
Watchdog Timeout Period, External Clock	Long Period Short Period	4032 960		4097 1025	Clock Cycles
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V_{IH} = 3.5V, V_{CC} = 5V	200			ns
$\overline{RESET}$ and RESET Output Voltage (Note 3)	I_{SINK} = 400µA, V_{CC} = 2V, V_{BATT} = 0 I_{SINK} = 1.6mA, 3V < V_{CC} < 5.5V I_{SOURCE} = 1µA, V_{CC} = 5V	 3.5		0.4 0.4 	V
$\overline{LOW\ LINE}$ and $\overline{WDO}$ Output Voltage	I_{SINK} = 800µA, T_A = Full I_{SOURCE} = 1µA, V_{CC} = 5V, T_A = Full	 3.5		0.4 	V
Output Short Circuit Current	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOW\ LINE}$	1	3	25	µA
WDI Input Threshold Logic Low Logic High (MAX696) Logic High (MAX697)	V_{CC} = 5V (Note 2)	 3.5 3.8		0.8 	V
WDI Input Current	WDI = V_{OUT} WDI = 0V	 -50	20 -15	50 	µA
POWER FAIL DETECTOR					
PFI Input Threshold	V_{CC} = 3V, 5V	1.2	1.3	1.4	V
PFI-LL_{IN} Threshold Difference	V_{CC} = 3V, 5V		±15	±50	mV
PFI Input Current			±0.01	±25	nA
LL_{IN} Input Current	MAX697	-25	±0.01	+25	nA
	MAX696	-500	±0.01	+25	
$\overline{PFO}$ Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 1µA, V_{CC} = 5V	 3.5		0.4 	V V
$\overline{PFO}$ Short Circuit Source Current	PFI = 0V, $\overline{PFO}$ = 0V	1	3	25	µA
CHIP ENABLE GATING (MAX697)					
$\overline{CE}$ IN Thresholds	V_{IL} V_{IH}, V_{CC} = 5V	 3.0		0.8 	V
$\overline{CE}$ IN Pullup Current			3		µA
$\overline{CE}$ OUT Output Voltage	I_{SINK} = 1.6mA I_{SOURCE} = 800µA I_{SOURCE} = 1µA, V_{CC} = 0V	 V_{CC} -0.5V V_{CC} -0.05		0.4 	V
$\overline{CE}$ Propagation Delay	V_{CC} = 5V		80	150	ns
OSCILLATOR					
OSC IN Input Current			±2		µA
OSC SEL Input Pullup Current			5		µA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V C_{OSC} = 47pF		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded providing the input current is limited to less than 10mA.
Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.
Note 3: T_A = Full Operating Range.

Microprocessor Supervisory Circuits

Pin Description

NAME	PIN		FUNCTION
	MAX696	MAX697	
V_{CC}	3	3	The +5V input.
V_{BATT}	1	—	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	2	—	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	4	5	0V ground reference for all signals.
$\overline{RESET}$	15	15	$\overline{RESET}$ goes low whenever LL_{IN} falls below 1.3 volts or V_{CC} falls below the V_{BATT} input voltage. $\overline{RESET}$ remains low for 50ms after LL_{IN} goes above 1.3 volts. $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	11	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	9	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	10	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN	—	13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT	—	12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and LL_{IN} is above 1.3V. See Figure 5.
BATT ON	5	—	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
$\overline{LOW\ LINE}$	6	6	$\overline{LOW\ LINE}$ goes low when LL_{IN} falls below 1.3 volts. It returns high as soon as LL_{IN} rises above 1.3 volts. See Figure 5, Reset Timing.
RESET	16	16	RESET is an active high output. It is the inverse $\overline{RESET}$.
OSC SEL	8	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3μA internal pullup. See Table 1.
OSC IN	7	7	OSC IN sets the Reset delay timing and Watchdog timeout period when OSC SEL floats or is driven low. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 7. When OSC SEL is high, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$	14	14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.
NC	12	2	NO CONNECT. Leave this pin open.
LL_{IN}	13	4	LOW LINE INPUT. LL_{IN} is the CMOS input to a comparator whose other input is a precision 1.3 volt reference. The output is $\overline{LOW\ LINE}$ and is also connected to the reset pulse generator. See Figure 2.
TEST	—	1	Used during Maxim manufacture only. Always ground this pin.

Typical Applications

MAX696

A typical connection for the MAX696 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 50mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 7mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 200Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1μA maximum when V_{CC} is between 0V and V_{BATT} -700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{RESET}$ output to hold the microprocessor's $\overline{RESET}$ line low when LL_{IN} is below 1.3V. An internal monostable holds $\overline{RESET}$ low for 50ms after LL_{IN} rises above 1.3V. This prevents repeated toggling of $\overline{RESET}$ even if the V_{CC} power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{RESET}$ must be held low until the microprocessor clock oscillator has started. The power-up $\overline{RESET}$ pulse lasts 50ms to allow for this oscillator start-up time. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MAX696 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.3V, the Power Fail Output ($\overline{PFO}$) drives the processor's NMI input low. An earlier power fail warning can be generated if the unregulated DC input of the regulator is available for monitoring.

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the MAX696 will issue a 50ms $\overline{RESET}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{RESET}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{WDO}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{WDO}$ goes low it remains low until a transition occurs at WDI while $\overline{RESET}$ is high. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 7.

MAX697

The MAX697 is nearly identical to the MAX696. The MAX697 lacks the battery backup feature, so it does not have the V_{BATT}, V_{OUT}, or BATT ON pins. This allows the MAX697 to consume less than 250 microamperes, and it allows the inclusion of RAM write protection pins. See Figure 2.

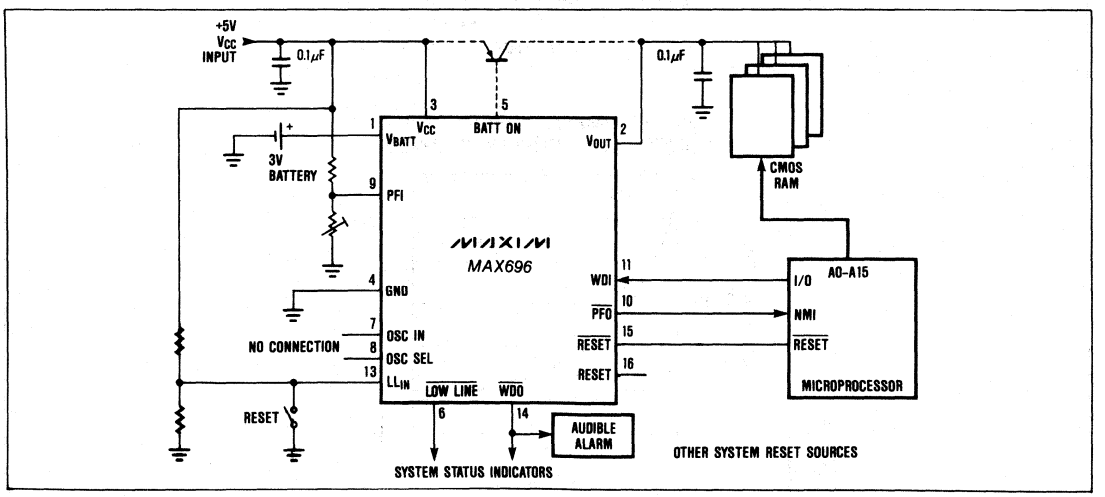
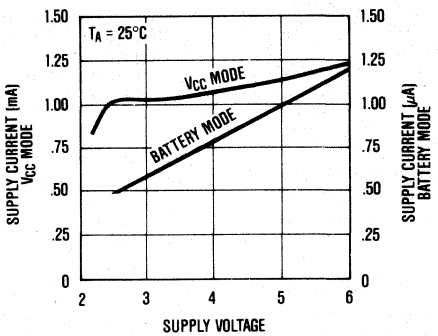
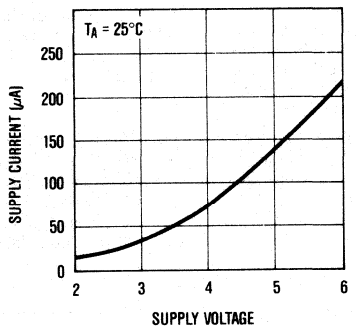


Figure 1. MAX696 Typical Application

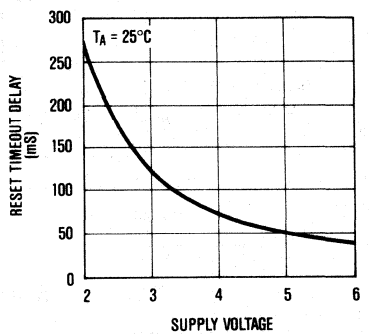
MAX696
SUPPLY CURRENT AS A FUNCTION
OF SUPPLY VOLTAGE



MAX697
SUPPLY CURRENT AS A FUNCTION
OF SUPPLY VOLTAGE



RESET TIMEOUT DELAY AS A
FUNCTION OF SUPPLY VOLTAGE



Detailed Description

Battery-Switchover and V_{OUT} (MAX696)

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (See Figure 3). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with the internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output can directly drive the base of the external transistor.

It should be noted that the MAX696 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200Ω MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} -700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MAX696 operates with battery voltages from 2.0V to 4.25V. The battery voltage should not be within 0.5V of V_{CC} or switchover may occur. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The capacitor charging voltage should include a diode to limit the fully charged voltage to approximately 0.5V less than V_{CC}. The charging resistor for rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small leakage current of typically 10nA (20nA max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum current (20nA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

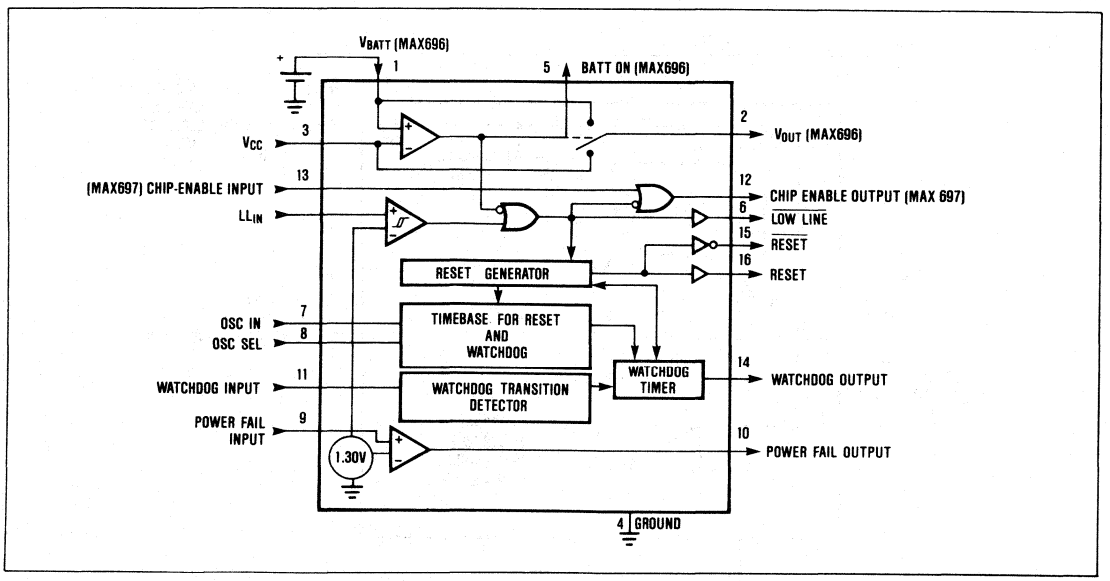


Figure 2. MAX696/697 Block Diagram

Microprocessor Supervisory Circuits

Reset Output

$\overline{\text{RESET}}$ is an active low output which goes low whenever LL_{IN} falls below 1.3 volts. It will remain low until LL_{IN} rises above 1.312 volts for 50 milliseconds. (See Figures 4 and 5.)

The guaranteed minimum and maximum low line thresholds of the MAX696/697 are 1.2 and 1.4 volts. The LL_{IN} comparator has approximately 12mV of hysteresis.

The response time of the reset voltage comparator is about 100 microseconds. LL_{IN} should be bypassed to ensure that glitches do not activate $\overline{\text{RESET}}$ output.

$\overline{\text{RESET}}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{\text{RESET}}$ has an internal 3μA pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

$\overline{\text{CE}}$ Gating and RAM Write Protection

The MAX697 uses two pins to control the Chip Enable or Write inputs of CMOS RAMs. When LL_{IN} is > 1.3V, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN, with a 50ns propagation delay. If LL_{IN} input falls below 1.3V (1.2 min., 1.4 max.) an internal gate forces $\overline{\text{CE}}$ OUT high, independent of $\overline{\text{CE}}$ IN. The $\overline{\text{CE}}$ output is also forced high when V_{CC} is less than V_{BATT}. (See Figure 4.)

$\overline{\text{CE}}$ OUT typically drives the $\overline{\text{CE}}$, $\overline{\text{CS}}$ or Write input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{\text{CE}}$ OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{\text{CE}}$ OUT is too long, connect $\overline{\text{CE}}$ IN to GND and use the resulting $\overline{\text{CE}}$ OUT to control a high speed external logic gate. A second alternative is to AND the LOW LINE output with the $\overline{\text{CE}}$ or $\overline{\text{WR}}$ signal. An external logic gate and the $\overline{\text{RESET}}$ output of the MAX696/697 can also be used for CMOS RAM write protection.

1.25V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output ($\overline{\text{PFO}}$) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's V_{CC} regulator or the regulated output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the LL_{IN} falls below 1.3V. $\overline{\text{PFO}}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before LL_{IN} falls below 1.3V and the $\overline{\text{RESET}}$ output goes low.

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and $\overline{\text{PFO}}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

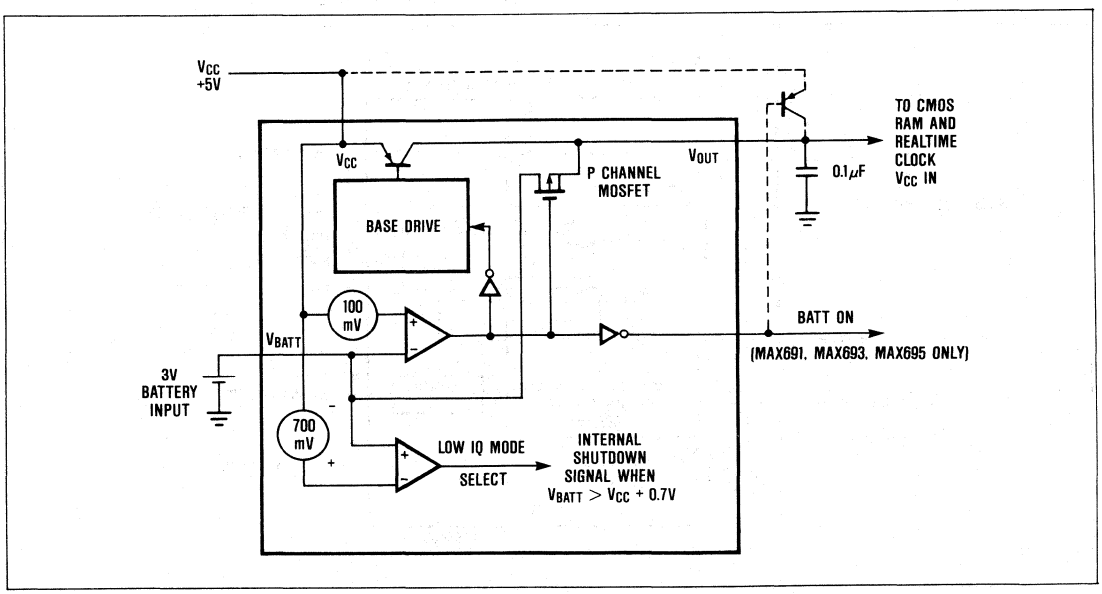


Figure 3. MAX696 Battery-Switchover Block Diagram

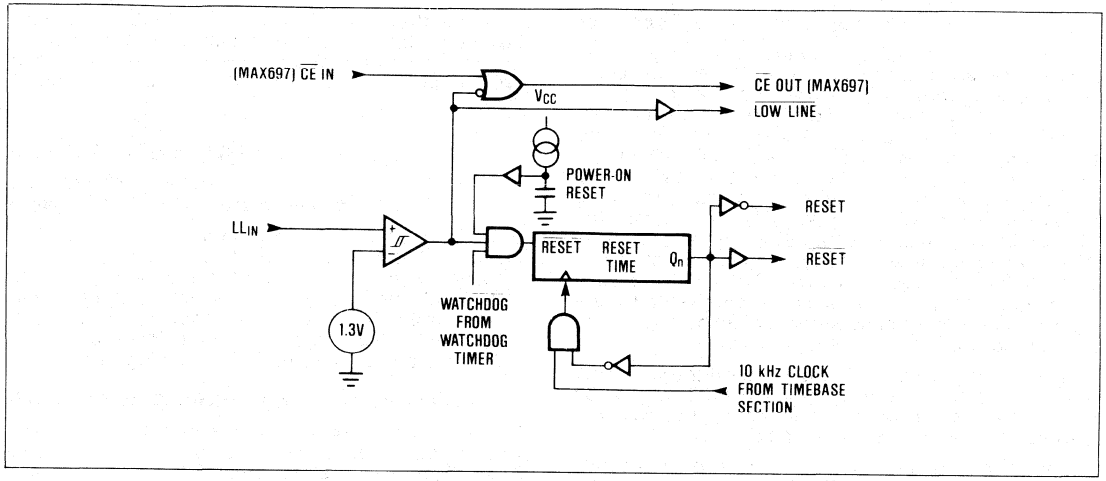


Figure 4. Reset Block Diagram

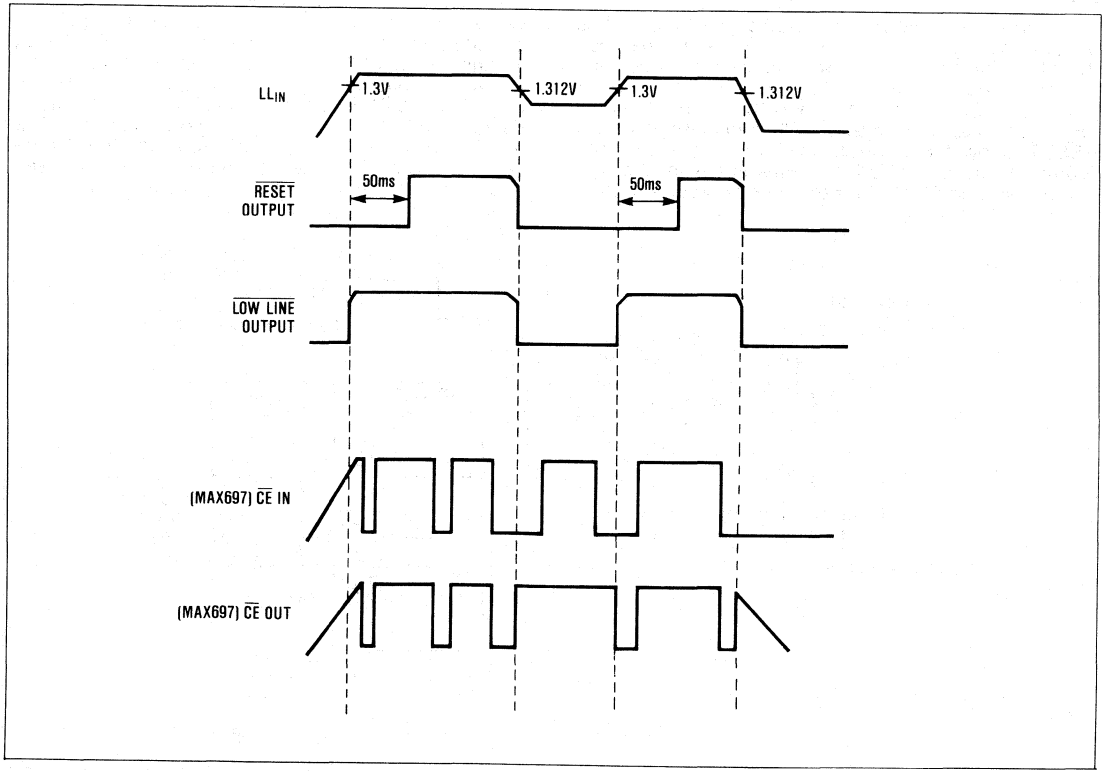


Figure 5. MAX697 Reset Timing

Microprocessor Supervisory Circuits

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 milliseconds $\overline{\text{RESET}}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX696/697 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by LL_{IN} falling below 1.3V. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output $\overline{\text{WDO}}$ goes low if the watchdog timer "times out," and it remains low until set high by the next transition on the watchdog input. $\overline{\text{WDO}}$ is also set high when LL_{IN} goes below 1.3V.

The watchdog timeout period defaults to 1.6 seconds and the reset pulse width defaults to 50ms. The MAX696 and MAX697 allow these times to be adjusted per Table 1.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. WD transmissions while $\overline{\text{RESET}}$ is low are ignored. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

Application Hints

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 7. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 8). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 9. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01μF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 9 is used.

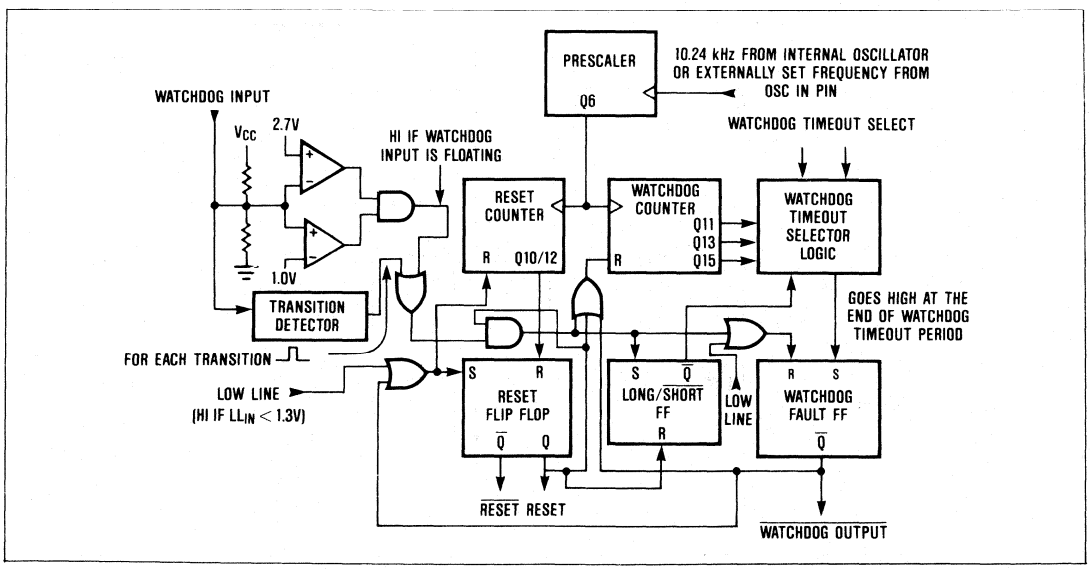


Figure 6. Watchdog Timer Block Diagram

Table 1. MAX696 and MAX697 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL (Note 3)	OSC IN	WATCHDOG TIMEOUT PERIOD NORMAL	WATCHDOG TIMEOUT PERIOD IMMEDIATELY AFTER RESET	RESET TIMEOUT PERIOD
Low	External Clock Input	1024 clks	4096 clks	512 clks
Low	External Capacitor	$\frac{400ms}{47pf} \times C$	$\frac{1.6\ sec}{47pf} \times C$	$\frac{200ms}{47pf} \times C$
High/Floating	Low	100ms	1.6 sec	50ms
High/Floating	Floating	1.6 sec	1.6 sec	50ms

Note 1: When the MAX696/697 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is $F_{OSC(Hz)} = \frac{184,000}{C_{OSC(pF)}}$

Note 2: See Electrical Characteristics Table for minumum and maximum timing values.

Note 3: "HIGH" for the OSC SEL pin should be connected to V_{OUT}, not V_{CC} (on MAX696).

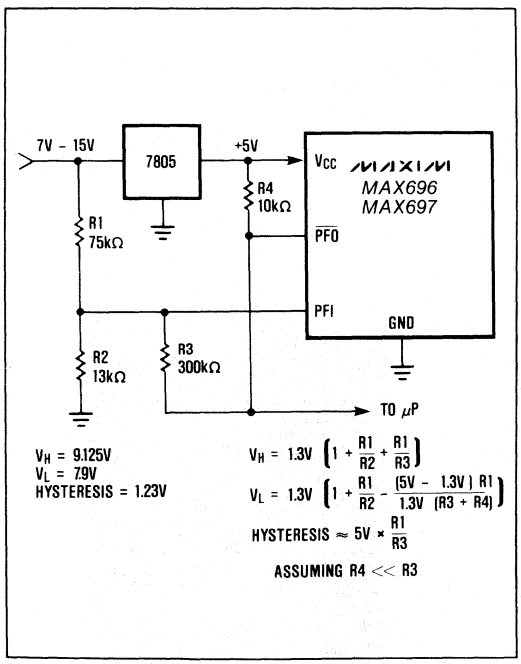


Figure 7. Adding Hysteresis to the Power Fail Voltage Comparator

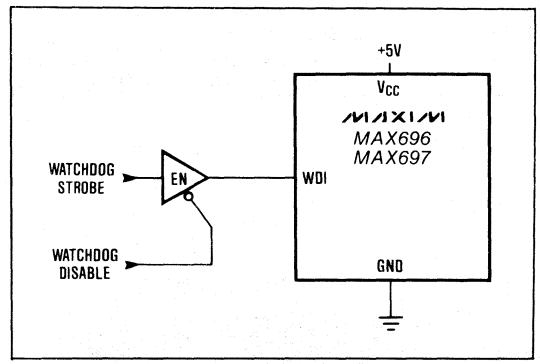


Figure 8. Disabling the Watchdog Under Program Control

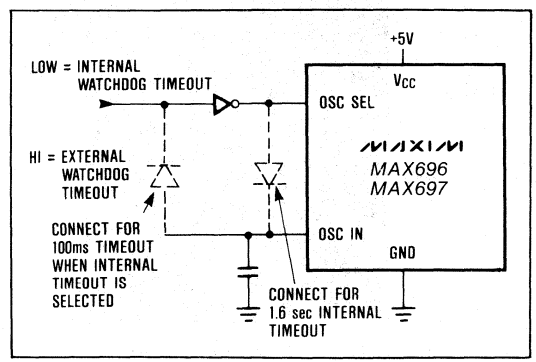


Figure 9. Selecting Internal or External Watchdog Timeout

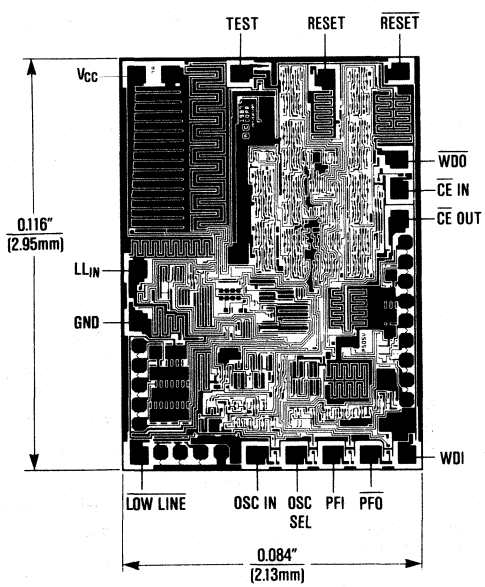
Microprocessor Supervisory Circuits

Table 2. Input and Output Status in Battery Backup Mode

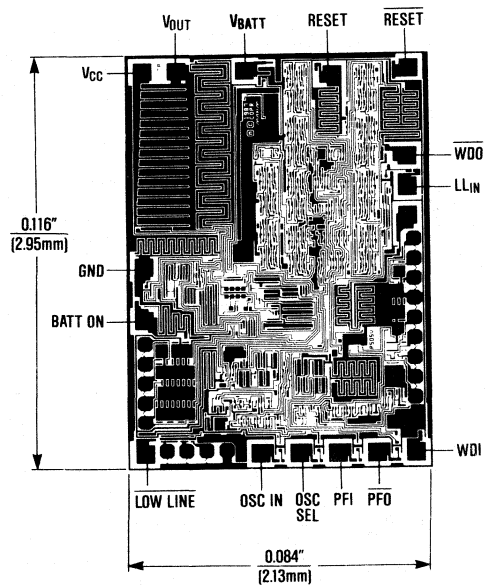
V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET. (MAX696 only)
$\overline{RESET}$	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
BATT ON	Logic high (MAX696 only)
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low
$\overline{CE}$ IN	$\overline{CE}$ IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current. (MAX697 only)
$\overline{CE}$ OUT	Logic high (MAX697 only)
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12µA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} + 100mV and V_{BATT} - 700mV. The supply current is 1µA maximum when V_{CC} is less than V_{BATT} - 700mV.

Chip Topography

MAX697



MAX696



Programmable Voltage Detectors

General Description

Maxim's MAX8211 and 8212 are CMOS micropower voltage detectors. Each contains a comparator, a 1.15V bandgap reference, and an open drain N-channel output driver. Two external resistors are used in conjunction with the internal reference to set the trip voltage to the desired level. A Hysteresis output is also included, allowing the user to apply positive feedback for noise-free output switching.

The MAX8211 provides a 7mA current-limited output sink whenever the voltage applied to the Threshold pin is less than the 1.15V internal reference. In the MAX8212, a voltage greater than 1.15V at the Threshold pin turns the output stage on (no current limit).

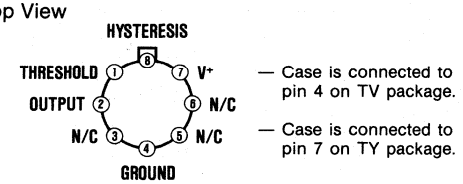
The MAX8211/8212 are plug-in replacements for the bipolar ICL8211/8212 in applications where the maximum supply voltage is less than 16.5V. They offer several performance advantages, including reduced supply current, a more tightly controlled bandgap reference, and more available current from the Hysteresis output.

Applications

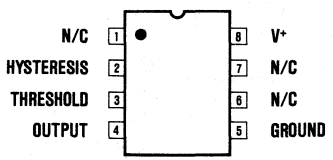
Under Voltage Detection
Over Voltage Detection
Battery Backup Switching
Power Supply Fault Monitoring
Low Battery Detection

Pin Configuration

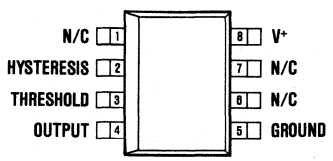
Top View



8 Lead TO-99 Metal Can



DIP



8 Lead Small Outline

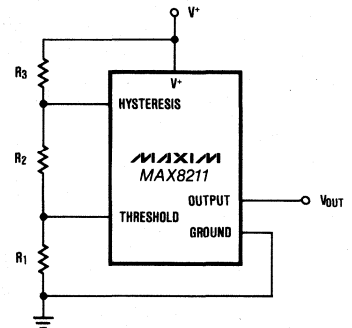
Features

- Improved 2nd Source for ICL8211/8212
- Low Power CMOS Design
- 5μA Quiescent Current
- Onboard Hysteresis Outputs
- ±40mV Threshold Accuracy (±3.5%)
- 2.0V to 16.5V Supply Voltage Range
- Defined Output Current Limit—MAX8211
- High Output Current Capability—MAX8212

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX8211CPA	0°C to +70°C	8 lead Plastic DIP
MAX8211EPA	-40°C to +85°C	8 lead Plastic DIP
MAX8211EJA	-40°C to +85°C	8 lead CERDIP
MAX8211MJA	-55°C to +125°C	8 lead CERDIP
MAX8211CSA	0°C to +70°C	8 lead Small Outline
MAX8211CTY	0°C to +70°C	8 lead TO-99 Metal Can
MAX8211ETY	-40°C to +85°C	8 lead TO-99 Metal Can
MAX8211MTV	-55°C to +125°C	8 lead TO-99 Metal Can
MAX8211C/D	0°C to +70°C	Dice
MAX8212CPA	0°C to +70°C	8 lead Plastic DIP
MAX8212EPA	-40°C to +85°C	8 lead Plastic DIP
MAX8212EJA	-40°C to +85°C	8 lead CERDIP
MAX8212MJA	-55°C to +125°C	8 lead CERDIP
MAX8212CSA	0°C to +70°C	8 lead Small Outline
MAX8212CTY	0°C to +70°C	8 lead TO-99 Metal Can
MAX8212ETY	-40°C to +85°C	8 lead TO-99 Metal Can
MAX8212MTV	-55°C to +125°C	8 lead TO-99 Metal Can
MAX8212C/D	0°C to +70°C	Dice

Typical Operating Circuit



Logic Supply Under-Voltage Detector

(Detailed Circuit Diagram—Figure 5)

Programmable Voltage Detectors

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... -0.5V to +18V
Output Voltage ..... -0.5V to +18V
Hysteresis Voltage ..... +0.5V to -18V w.r.t. V^+
Threshold Input Voltage ..... -0.5V to V^+ +0.5V
Operating Temperature
MAX821XC ..... 0°C to +70°C
MAX821XE ..... -40°C to +85°C
MAX821XM ..... -55°C to +125°C

Current into Any Terminal ..... ±50mA
Power Dissipation
Plastic DIP (derate 6.25mW/°C above +70°C) 500mW
Small Outline (derate 6mW/°C above +70°C) 480mW
CERDIP (derate 8mW/°C above +70°C) 640mW
TO-99 Metal Can (derate 6.7mW/°C above +70°C) ... 536mW
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Storage Temperature Range ..... -65°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = 5V, T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MAX8211			MAX8212			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I^+	$2V \le V^+ \le 16.5V$ $GND \le V_{TH} \le V^+$ T_A = 25°C T_A = Full Temp Range		5	15 20		5	15 20	µA
Threshold Trip Voltage	V_{TH}	$2V \le V^+ \le 16.5V$, V_{OUT} = 2V I_{OUT} = 4mA, T_A = 25°C I_{OUT} = 3mA, T_A = Full Temp Range	1.11 1.05	1.15	1.19 1.25	1.11 1.05	1.15	1.19 1.25	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	I_{OUT} = 4mA I_{HYST} = 1mA		±0.1			±0.1		mV
Guaranteed Operating Supply Voltage Range	V_{SUPP}	T_A = 25°C T_A = Full Temp Range	2.0 2.2		16.5 16.5	2.0 2.2		16.5 16.5	V
Typical Operating Supply Voltage Range	V_{SUPP}	T_A = 25°C	1.5		16.5	1.5		16.5	V
Threshold Voltage Temperature Coefficient	$\Delta V_{TH}/\Delta T$	See Figure 4		-200			-200		ppm/°C
Variation of Threshold Voltage with Supply Voltage	ΔV_{TH}	V^+ = 4.5V to 5.5V		1.0			0.2		mV
Threshold Input Current	I_{TH}	$0 \le V_{TH} \le V^+$, T_A = 25°C T_A = Full Temp Range		0.01	10 20		0.01	10 20	nA
Output Leakage Current	I_{OLK}	T_A = Full Temp Range, E and C Grade V_{OUT} = 16.5V, V_{TH} = 1.0V V_{OUT} = 16.5V, V_{TH} = 1.3V V_{OUT} = 5V, V_{TH} = 1.0V V_{OUT} = 5V, V_{TH} = 1.3V			 10 1			10 1	µA
		T_A = Full Temp Range, M Grade V_{OUT} = 16.5V, V_{TH} = 0.9V V_{OUT} = 16.5V, V_{TH} = 1.3V V_{OUT} = 5V, V_{TH} = 1.3V V_{OUT} = 5V, V_{TH} = 0.9V			 30 10			 30 10	
Output Saturation Voltage	V_{SAT}	I_{OUT} = 2mA, V_{TH} = 1.0V I_{OUT} = 2mA, V_{TH} = 1.3V		0.17	0.4		0.17	0.4	V
Max Available Output Current	I_{OH}	0°C to +70°C, V_{OUT} = 5V V_{TH} = 1.0V (Note 1) V_{TH} = 1.3V (Note 2)	4	7.0		12	35		mA
Hysteresis Leakage Current	I_{LHYS}	T_A = Full Temp Range, C and E Grade V^+ = 10V, V_{TH} = 1.0V V_{HYST} = -16.5V w.r.t. V^+			0.1			0.1	µA
		T_A = Full Temp Range, M Grade V^+ = 10V, V_{TH} = 0.9V V_{HYS} = -16.5V w.r.t. V^+			3			3	
Hysteresis Sat Voltage	$V_{HYS\ (max)}$	I_{HYST} = 0.5mA, V_{TH} = 1.3V measured with respect to V^+		-0.1	-0.2		-0.1	-0.2	V
Max Available Hysteresis Current	$I_{HYS\ (max)}$	V_{TH} = 1.3V V_{HYS} = 0V	2	10		2	10		mA

Note 1: The maximum output current of the MAX8211 is limited by design to 30mA under any operating condition. The output voltage may be sustained at any voltage up to +16.5V as long as the maximum power dissipation of the device is not exceeded.

Note 2: The maximum output current of the MAX8212 is not defined, and systems using the MAX8212 must therefore ensure that the output current does not exceed 50mA and that the maximum power dissipation of the device is not exceeded.

Detailed Description

As shown in the block diagrams of Figures 1 & 2, the MAX8211 and MAX8212 each contain a 1.15V reference, a comparator, an open drain n-channel output transistors, and an open drain p-channel hysteresis output. The MAX8211 output n-channel turns on when the voltage applied to the THRESHOLD pin is less than the internal reference (1.15V). The sink current is limited to 7mA (typical), allowing direct drive of an LED without a series resistor. The MAX8212 output turns on when the voltage applied to the THRESHOLD pin is greater than the internal reference. The output of the MAX8212 is not current limited, and will typically sink 35mA.

Compatibility with ICL8211/8212

The CMOS MAX8211/8212 are plug-in replacements for the bipolar ICL8211/8212 in most applications. The use of CMOS technology has several advantages. The quiescent supply current is much less than in the bipolar parts. Higher value resistors can also be used in the networks that set up the trip voltage, since the comparator input (THRESHOLD pin) is a low leakage MOS transistor. This further reduces system current drain. The tolerance of the internal reference has also been significantly improved, allowing for more precise voltage detection without the use of potentiometers.

The available current from the HYSTERESIS output has been increased from 21μA to 10mA making the hysteresis feature easier to use. The disparity between the voltage required at the THRESHOLD pin to switch the OUTPUT compared with the HYSTERESIS output has also been reduced in the MAX8211 from 8mV to 0.1mV to eliminate output "chatter" or oscillation.

Most voltage detection circuits operate with supplies that are 15V or less: in these applications, the MAX8211/8212 will replace ICL8211/8212s with the performance advantages described above. However it should be noted that the CMOS parts have an absolute maximum supply voltage rating of 18V, and should never be used in applications where this rating could be exceeded. Caution should also be exercised when replacing ICL8211/8212s in closed loop applications such as programmable zeners. Although neither the ICL8211/8212 nor the MAX8211/8212 are internally compensated, the CMOS parts have higher gain and may not be stable for the external compensation capacitor values used in lower gain ICL8211/8212 circuits.

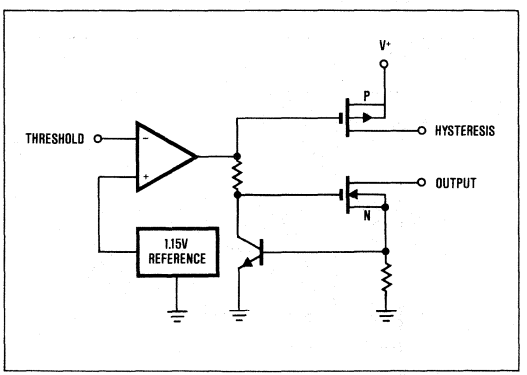


Figure 1. Block Diagram of MAX8211

Typical Applications

Basic Voltage Detectors

Figure 3 shows the basic circuit for both under-voltage detection (MAX8211) and over-voltage detection (MAX8212). For applications where no hysteresis is needed, R_3 should be omitted. The ratio of R_1 to R_2 is then chosen such that, for the desired trip voltage at V_{IN}, 1.15V is applied to the THRESHOLD pin. Since the comparator inputs are very low leakage MOS transistors, the MAX8211/8212 can use much higher resistor values in the attenuator network than the bipolar ICL8211/8212. See Table 1 for Switching Delays.

Table 1. Switching Delays

Typical Delays	MAX8211	MAX8212
$t_{(on)}$	40μs	250μs
$t_{(off)}$	1.5ms	3ms

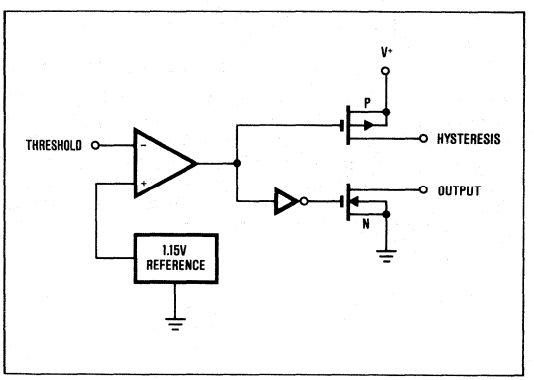


Figure 2. Block Diagram of MAX8212

Programmable Voltage Detectors

Voltage Detectors with Hysteresis

To ensure noise-free output switching, hysteresis is frequently used in voltage detectors. For both the MAX8211 and MAX8212, the HYSTERESIS output is ON for THRESHOLD voltages greater than 1.15V. R_3 (Figure 3) controls the amount of current (positive feedback) supplied from the HYSTERESIS output to the mid-point of the resistor divider, and hence the magnitude of the hysteresis, or dead-band.

Resistor values for Figure 3 should be calculated as follows:

1) Choose a value for R_1. Typical values are in the 10kΩ to 10MΩ range.

2) Calculate R_2 for the desired upper trip point V_U using the formula:

$$R_2 = R_1 \times \frac{(V_U - V_{TH})}{V_{TH}} = R_1 \times \frac{(V_U - 1.15V)}{1.15V}$$

3) Calculate R_3 for the desired amount of hysteresis, where V_L is the lower trip point:

$$R_3 = R_2 \times \frac{(V^+ - V_{TH})}{(V_U - V_L)} = R_2 \times \frac{(V^+ - 1.15V)}{(V_U - V_L)}$$

or if $V^+ = V_{IN}$

$$R_3 = R_2 \times \frac{(V_L - V_{TH})}{(V_U - V_L)} = R_2 \times \frac{(V_L - 1.15V)}{(V_U - V_L)}$$

Figure 5 shows an alternate circuit, suitable only when the voltage being detected is also the power supply voltage for the MAX8211 or MAX8212.

Resistor values for Figure 5 should be calculated as follows:

1) Choose a value for R_1. Typical values are in the 10kΩ to 10MΩ range.

2) Calculate R_2

$$R_2 = R_1 \times \frac{(V_L - V_{TH})}{V_{TH}} = R_1 \times \frac{(V_L - 1.15V)}{1.15V}$$

3) Calculate R_3

$$R_3 = R_1 \times \frac{(V_U - V_L)}{1.15V}$$

Low Voltage Detector for Logic Supply

The circuit of Figure 5 will detect when a 5.0V (nominal) supply goes below 4.5V, which is the V_{min} normally specified in logic systems. Resistor values have been selected which ensure that false under-voltage alarms will not be generated even with worst-case Threshold Trip Voltages and resistor tolerances. R_3 provides approximately 75mV of hysteresis.

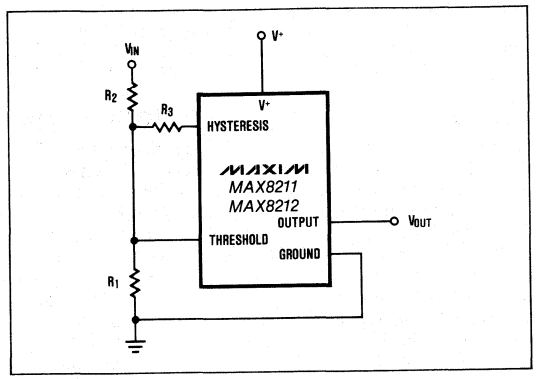


Figure 3. Basic Over-Voltage/Under-Voltage Circuit

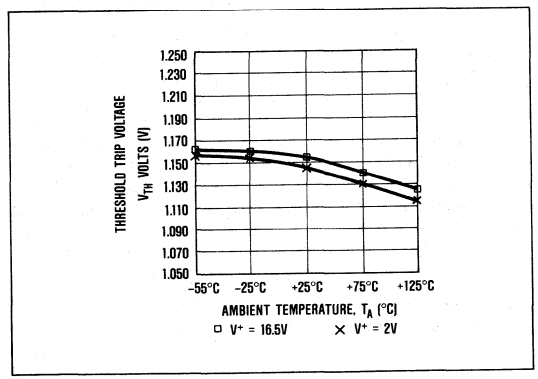


Figure 4. Threshold Trip Voltage vs. Ambient Temperature

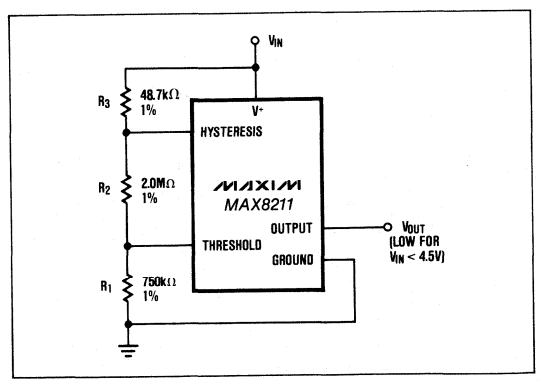


Figure 5. Logic Supply Low Voltage Detector

MAXIM
Monolithic Voltage Converter

General Description

The Maxim ICL7660 is a monolithic charge pump voltage inverter that will convert a positive voltage in the range of +1.5V to +10V to the corresponding negative voltage in the range of −1.5V to −10V. The ICL7660 provides performance far superior to previous implementations of charge pump voltage inverters by combining low quiescent current with high efficiency, and by eliminating diode drop voltage losses. The ICL7660 has an oscillator, control circuitry, and 4 power MOS switches on-chip, with the only required external components being two low cost electrolytic capacitors.

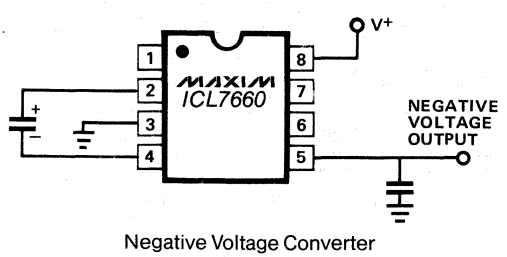
Applications

The ICL7660 can be used wherever negative voltages in the range of −1.5V to −10V are desired. A common use is to generate a −5V supply for use with analog circuitry, using the standard +5V logic supply as the power source. Another popular usage is to convert a +9V battery voltage to −9V, which can then be regulated to −5V by the Maxim ICL7664.

The ICL7660 can also be used to double the output voltage of a battery, generating a 3V total supply voltage from a single 1.5V flashlight battery or generating a 6V total supply voltage from a single lithium cell. Typical applications include:

Handheld instruments
RS-232 power supply
Data acquisition systems
−5V supply from +5V logic supply
Panel meters
Operational amplifier power supplies
Positive to negative voltage conversion

Typical Operating Circuit



Negative Voltage Converter

(Detailed Circuit Diagram — Figure 4)

Features

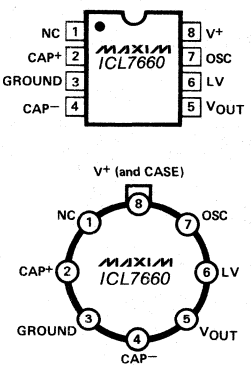
- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **No Diode Required for High Voltage Operation**
- **Simple Voltage Conversion: +5V to ±5V**
- **98% Power Efficiency (typ)**
- **Wide Voltage Range: 1.5V to 10V**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7660C/D	0°C to +70°C	Dice
ICL7660CPA	0°C to +70°C	8 Lead Plastic Dip
ICL7660CSA	0°C to +70°C	8 Lead Small Outline
ICL7660CTV	0°C to +70°C	8 Lead TO-99 Can
ICL7660IJA	-20°C to +85°C	8 Lead CERDIP
ICL7660ITV	-20°C to +85°C	8 Lead TO-99 Can
ICL7660EJA	-40°C to +85°C	8 Lead CERDIP
ICL7660MTV	(Order ICL7660AMTV)	
ICL7660AMTV	-55°C to +125°C	8 Lead TO-99 Can

Pin Configuration

Top View



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Monolithic Voltage Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, (LV Open Circuit) ..... +10.5V
LV and OSC Input Voltage
(Note 1) ..... -0.3V to (V^+ +0.3V) for V^+ < +5.5V
(V^+ -5.5V) to (V^+ +0.3V) for V^+ > +5.5V
Current into LV (Note 1) ..... 20μA for V^+ > +3.5V
Output Short Duration ($V_{SUPPLY} \leq$ +5.5V) ..... Continuous
Power Dissipation (Note 2)
ICL7660CTV 500mW
ICL7660CPA 300mW
ICL7660MTV 500mW
ICL7660CSA (Maxim) 200mW
ICL7660IJA (Maxim) 500mW
Operating Temperature Range
ICL7660M ..... -55°C to +125°C
ICL7660I (Maxim) ..... -20°C to +85°C
ICL7660C (Maxim) ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature
(Soldering, 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, T_A = +25°C unless otherwise indicated)

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I^+		170	500	μA	$R_L = \infty$
Supply Voltage Range - Hi	V^+_{H1}	3.0		6.5	V	0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, LV Open
(D_X out of circuit) (Note 3)		3.0		5.0	V	-55°C ≤ T_A ≤ 125°C, R_L = 10kΩ, LV Open
Supply Voltage Range - Lo (D_X out of circuit)	V^+_{L1}	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND
Supply Voltage Range - Hi (D_X in circuit)	V^+_{H2}	3.0		10.0	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV Open
Supply Voltage Range - Lo (D_X in circuit)	V^+_{L2}	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND
Output Source Resistance	R_{OUT}		55	100	Ω	I_{OUT} = 20mA, T_A = 25°C
				120	Ω	I_{OUT} = 20mA, -20°C ≤ T_A ≤ +70°C
				150	Ω	I_{OUT} = 20mA, -55°C ≤ T_A ≤ +125°C (Note 3)
				300	Ω	V^+ = 2V, I_{OUT} = 3mA, LV to GROUND -20°C ≤ T_A ≤ +70°C
				400	Ω	V^+ = 2V, I_{OUT} = 3mA, LV to GROUND, -55°C ≤ T_A ≤ +125°C, D_X in circuit (Note 3)
Oscillator Frequency	f_{OSC}		10		kHz	
Power Efficiency	P_{Ef}	95	98		%	R_L = 5kΩ
Voltage Conversion Efficiency	$V_{OUT\ Ef}$	97	99.9		%	$R_L = \infty$
Oscillator Impedance	Z_{OSC}		1.0		MΩ	V^+ = 2 Volts
			100		kΩ	V = 5 Volts

NOTE 1: Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.

NOTE 2: Derate linearly above 50°C by 5.5mW/°C.

NOTE 3: ICL7660M only.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Monolithic Voltage Converter

- **Lower supply current**
- **Supply current guaranteed over temperature**
- **No diode required for high voltage operation (Note 1)**
- **Wide 1.5V to 10V operating voltage range**
- **Improved SCR Latch-up protection**
- **Guaranteed 99% voltage conversion efficiency**
- **Improved ESD protection (Note 3)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
($V+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test circuit-Figure 1; unless noted.)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Supply Current	I^+		**110**	**175** **225** **250**	**μA** **μA** **μA**	**$T_A = 25°C$, $R_L = \infty$** **$T_A = 0°C \le T_A \le +70°C$, $R_L = \infty$** **$T_A = -55°C \le T_A \le +125°C$, $R_L = \infty$**
Supply Voltage Range — Hi (Dx out of circuit)(Note 1)	V^+_{H1}	**3.0**		**10.0**	**V**	**MIN $\le T_A \le$ MAX, $R_L = 10k\Omega$, LV Open**
Supply Voltage Range — Lo (Dx out of circuit)	V^+_{L1}	1.5		3.5	V	MIN $\le T_A \le$ MAX, $R_L = 10k\Omega$, LV to GROUND
Output Source Resistance	R_{OUT}		55	100 120 140 150 250 300 400	Ω Ω Ω Ω Ω Ω Ω	$I_{OUT} = 20mA$, $T_A = 25°C$ $I_{OUT} = 20mA$, $0°C \le T_A \le +70°C$ $I_{OUT} = 20mA$, $0°C \le T_A \le +85°C$ $I_{OUT} = 20mA$, $-55°C \le T_A \le +125°C$ (Note 2) $V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND, $T_A = 25°C$ $V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND, $-20°C \le T_A \le +85°C$ $V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND, $-55°C \le T_A \le +125°C$ (Note 2)
Oscillator Frequency	f_{OSC}		10		kHz	
Power Efficiency	P_{EF}	95	98		%	$R_L = 5k\Omega$
Voltage Conversion Efficiency	$V_{OUT\,Ef}$	**99**	**99.9**		**%**	**$R_L = \infty$**
Oscillator Impedance	Z_{OSC}		1.0		MΩ	$V^+ = 2$ Volts
			100		kΩ	$V^+ = 5$ Volts

NOTE 1: The Maxim ICL7660 can operate without an external output diode over the full temperature and voltage range. The Maxim ICL7660 can also be used with the external output diode D_X, when replacing the Intersil ICL7660.

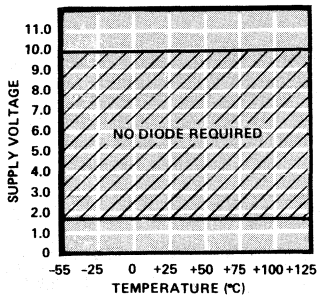
NOTE 2: Maxim ICL7660A only.

NOTE 3: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883B Method 3015.1 Test Circuit).

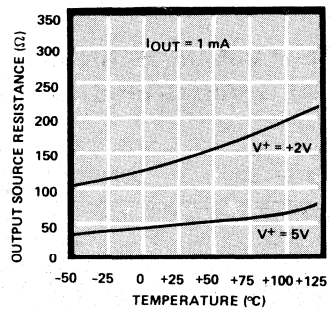
Monolithic Voltage Converter

Typical Operating Characteristics

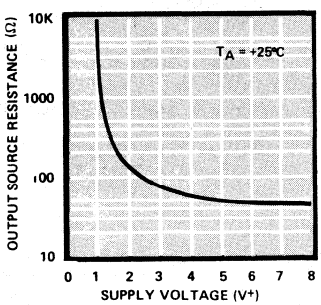
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



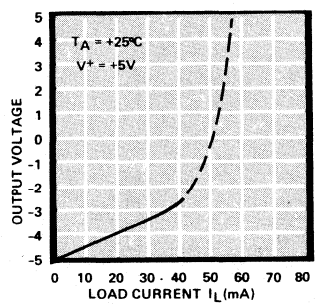
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



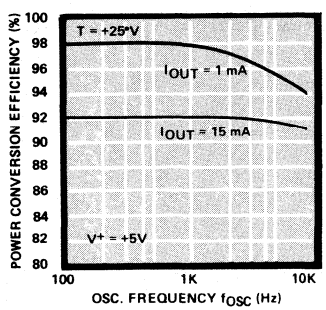
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



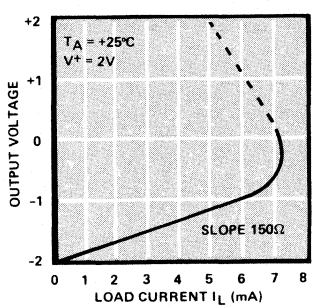
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY

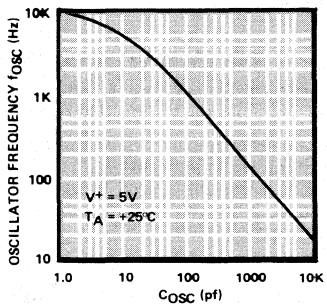


OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

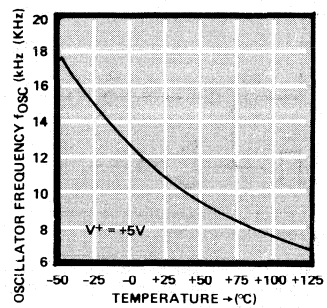


Typical Operating Characteristics

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

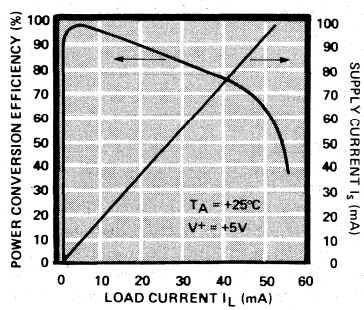


UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

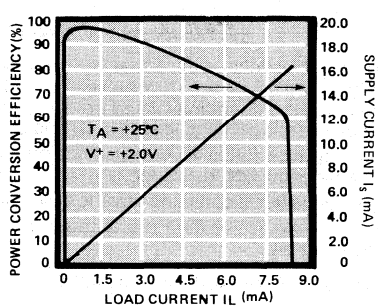


SUPPLY CURRENT CURVES below include current that is fed directly into the load (R_L) from V+ (see Figure 1). The supply current is divided equally into the positive and negative side (via the ICL7660) to the load. Ideally, $V_{OUT} \simeq V_{IN}$, $I_S \simeq 2I_L$ so $V_{IN} \cdot I_S \simeq 2 \cdot V_{OUT} \cdot I_L$.

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



SUPPLY CURRENT POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



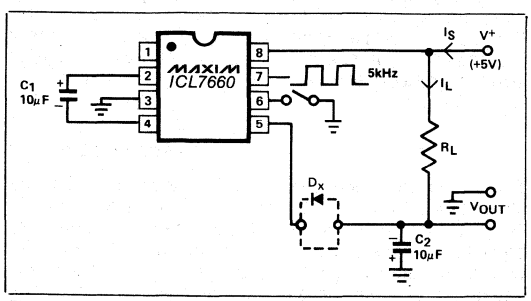


Figure 1. Maxim ICL7660 test circuit. (C_1 and C_2 should be increased to 100μF if C_{OSC} exceeds 10pF.) Note: Dx not required with Maxim ICL7660.

Detailed Description

All the circuitry necessary to complete a voltage doubler is contained on the ICL7660. Only 2 external capacitors are needed. These may be inexpensive 10μF polarized electrolytic capacitors. Figure 2, an idealized voltage doubler, illustrates ICL7660 operation. During the first half of the cycle, switches S_2 and S_4 are open, switches S_1 and S_3 are closed, and the capacitor C_1 is charged to a voltage V^+. During the second half cycle, switches S_1 and S_3 are open, S_2 and S_4 are closed, and the capacitor C_1 undergoes a negative shift equal to V^+ volts. Assuming ideal switches and no load on C_2, charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly $-(V^+)$.

Monolithic Voltage Converter

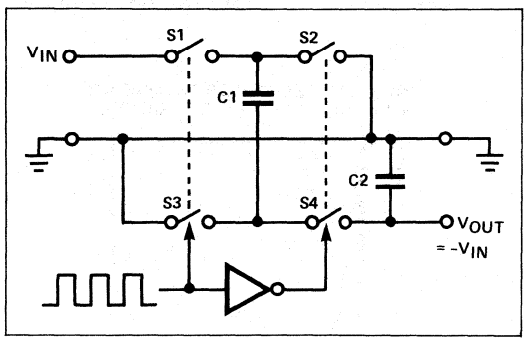


Figure 2. Idealized voltage doubler.

The four switches in Figure 2 are MOS power switches. Switch S_1 is a P-channel device, and switches S_2, S_3, and S_4 are N channel devices.

To improve low voltage operation the regulator should be disabled by connecting the "LV" pin to Ground. This is recommended to compensate for the inherent voltage drop associated with the voltage regulator portion of the ICL7660. To prevent device damage and insure latch-free operation, the "LV" pin must be left open if the supply voltage exceeds 3.5V.

Efficiency Considerations

Theoretically a voltage multiplier can approach 100% efficiency if certain conditions are met. The ICL7660 approaches the conditions listed below for negative voltage multiplication if large values of C_1 and C_2 are used.

◊ The output switches have virtually no offset and extremely low ON resistance.

◊ Minimal power is consumed by the drive circuitry.

◊ The impedances of the reservoir and pump capacitors are negligible.

The energy loss per charge pump cycle is:

$$E = \frac{1}{2} C_1 (V^{+2} - V_{OUT}^2)$$

There will be a substantial voltage difference between V^+ and V_{OUT} if the impedances of C_1 and C_2 at the pump frequency are high compared to the output load R_L. To reduce output ripple, make C_2 as large in value as is practical. Increasing the value of both C_1 and C_2 will improve the efficiency.

General Precautions

◊ The positive terminal of C_1 must be connected to Pin 2 of the ICL7660 and the positive terminal of C_2 must be connected to Ground.

◊ Never exceed maximum supply voltages.

◊ Do not connect the "LV" terminal to Ground for supply voltages greater than 3.5V.

◊ The output to V^+ supply should not be short-circuited for extended periods of time when supply voltages exceed 5.5V. Transient conditions including startup are acceptable.

Maximum Operating Limits

The Maxim ICL7660 will operate over the entire operating temperature range with an input voltage of 1.5V to 10V.

The Maxim ICL7660, unlike the Intersil device, does not require a protective diode in series with the output. Leaving this diode in the circuit will have no effect on the Maxim ICL7660, although the diode does reduce the output voltage by approximately 0.6V.

Applications

Changing Oscillator Frequency

Normally the OSC pin of the ICL7660 is left open and the 10kHz nominal oscillator frequency (5kHz charge pump frequency) is used. The oscillator frequency can be lowered by connecting an external capacitor between OSC and V^+. A graph in the Typical Characteristics section shows the nominal frequency vs. capacitor value. Lowering the oscillator frequency will improve the conversion efficiency with very low output current levels. An undesirable effect of lowering the oscillator frequency is that the impedance level of the pump capacitors will increase. Increasing the value of C_1 and C_2 will compensate for this increase in impedance.

In some applications, particularly audio amplifiers, the 5kHz output ripple frequency is objectionable. The oscillator frequency may be increased by overdriving the OSC pin with an external oscillator. The threshold of the Oscillator Input is $V^+ - 2.5V$ when $V^+ \geq 5V$, and is $1/2\ V^+$ for $V^+ < 5V$. To eliminate the possibility of SCR latchup, insert a 1kΩ resistor in series with the OSC input. If the external clock source does not swing all the way to V^+, a 10kΩ pullup resistor should be used. The pump frequency, and therefore the output ripple frequency, will be one-half the external clock frequency. Driving the ICL7660 with a higher frequency clock will slightly increase the quiescent current, but allows the use of smaller value external capacitors and increases the ripple frequency.

Cascading Devices

To produce larger negative multiplication of the initial supply voltage, the ICL7660 may be cascaded as shown in Figure 3. The resulting output resistance is approximately equal to the weighted sum of the individual ICL7660 R_{OUT} values. For light loads, the practical limit is 10 devices. The output voltage where n is an integer representing the number of devices cascaded, is defined by $V_{OUT} = -n\ (V_{IN})$.

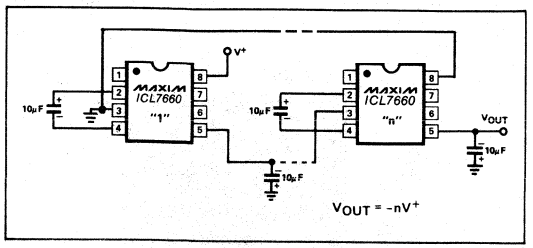


Figure 3. Cascading ICL7660's for increased output voltage.

Negative Voltage Converter

The most common application of the ICL7660 is as a charge pump voltage inverter, converting a positive voltage to the corresponding negative voltage. The simple circuit of Figure 4 shows that only two external components, C_1 and C_2 are needed. In most applications C_1 and C_2 are low cost 10μF electrolytic capacitors. The ICL7660 is NOT a voltage regulator and the output source resistance is approximately 70Ω with +5V input. This means that with an input voltage of +5V, the output voltage will be −5V under light load, but will decrease to about −4.3V with a 10mA load current. The output source resistance vs. temperature and supply voltage is depicted in the typical characteristics graphs. The output impedance of the complete circuit is the sum of the ICL7660 output resistance and the impedance of the pump capacitors at the pump frequency.

The ripple voltage on the output can be calculated by noting that the output current is supplied solely from capacitor C_2 during one-half of the charge pump cycle. This introduces a ripple of:

$$V_{RIPPLE} = \frac{I_{OUT}}{2(F_{PUMP})(C_2)}$$

For the nominal F_{PUMP} of 5kHz (one-half of the nominal 10kHz oscillator frequency) and a 10μF C_2, the ripple will be approximately 100mV with an output current of 10mA.

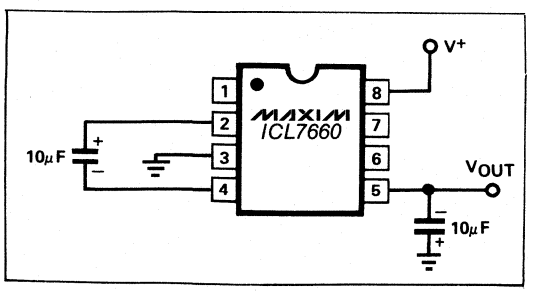


Figure 4. Negative voltage converter.

Paralleling Devices

Paralleling multiple ICL7660's reduces the output resistance. As illustrated in Figure 5, each device requires its own pump capacitor C_1, however the reservoir capacitor, C_2, serves all devices. The equation for calculating output resistance is shown in Figure 5.

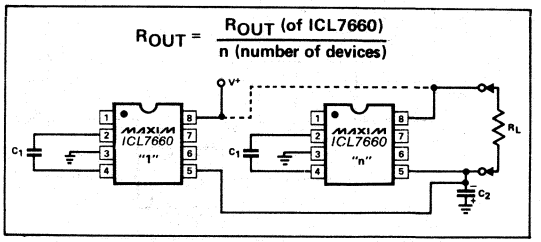


Figure 5. Paralleling ICL7660's to reduce output resistance.

Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 6. In this circuit, capacitor C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage. Capacitor C_2 and C_4 are respectively pump and reservoir for the multiplied positive voltage. This circuit configuration, however, does lead to higher source impedances of the generated supplies. This is due to the finite impedance of the common charge pump driver.

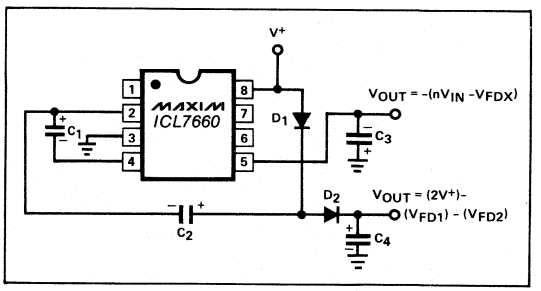


Figure 6. Combined positive multiplier and negative converter.

±5V Supply From a Single 9V Battery

Figure 7 shows a complete ±5V power supply using one 9V battery. The ICL7660 inverts the +9V input voltage for −9V which is then regulated by the ICL7664 negative regulator to a constant −5V output. The ICL7663 positive voltage regulator uses the +9V input directly to generate a regulated +5V output. The combined quiescent current of the Maxim ICL7660 and the two regulators is less than 100μA, while the output current capability is 40mA.

Monolithic Voltage Converter

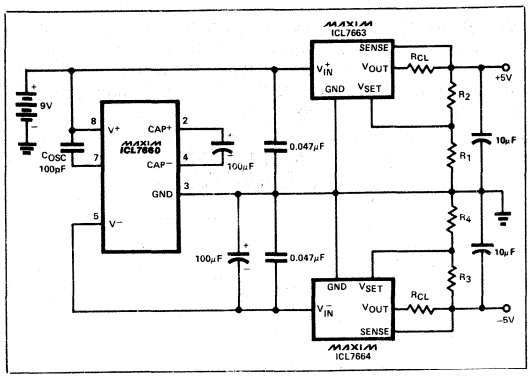
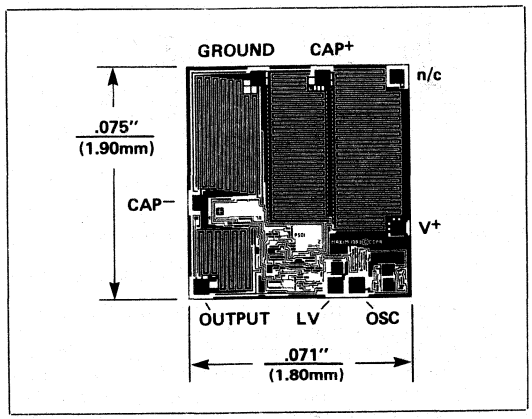


Figure 7. Regulated ±5 Volts from a battery using the Maxim ICL7663 and ICL7664.

Chip Topography



MAXIM

Programmable Positive Voltage Regulator

General Description

The Maxim ICL7663 is a high efficiency positive voltage regulator with a quiescent current of less than 10μA. The output voltage is set by two external resistors to any voltage in the 1.3–16V range, with an input voltage range of 1.5–16V. The ICL7663 is well suited for battery powered supplies, featuring low quiescent current, 40mA output current capability, low V_{IN} to V_{OUT} differential, and a logic input level shutdown control. In addition, the ICL7663 has a negative temperature coefficient output suitable for generating a temperature compensated display drive voltage for multiplexed LCD display systems.

The Maxim ICL7663A is an enhanced version of the ICL7663, with a 1% accurate voltage reference, which eliminates the need for trimming the output voltage in most applications.

The ICL7663B is a reduced input voltage range version limited to a maximum of 10V input.

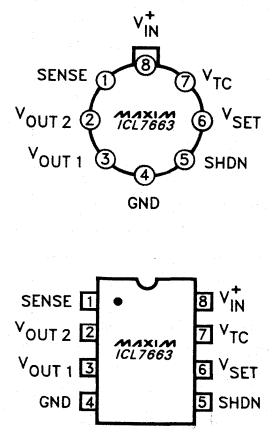
Applications

Designed specifically for battery powered systems, the ICL7663 positive voltage regulator excels wherever low quiescent power, wide voltage range operation, medium output current levels, current limiting, and logic-controlled shutdown is desired.

Handheld Instruments
Pagers
LCD Display Module and Systems
Remote Data Loggers

Pin Configuration

Top View



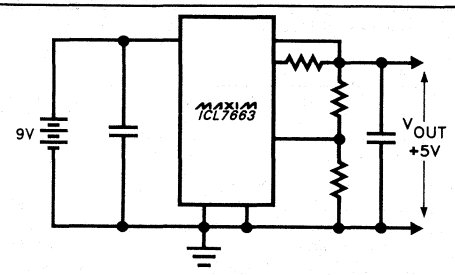
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **1% Output Voltage Accuracy (ICL7663A)**
- **Quiescent Current guaranteed over Temperature**
- **Improved Temperature Coefficient of Output Voltage**
- **40mA Output Current, with Current Limiting**
- **1.5V to 16V Operating Range**
- **Adjustable Output Voltage**
- **Low Input-to-Output Voltage Drop**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7663C/D	0°C to +70°C	Dice
ICL663CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7663CSA	0°C to +70°C	8 Lead Small Outline
ICL7663IJA	-20°C to +85°C	8 Lead CERDIP
ICL7663ITV	-20°C to +85°C	8 Lead TO-99
ICL7663AC/D	0°C to +70°C	Dice
ICL7663ACPA	0°C to +70°C	8 Lead Plastic DIP
ICL7663ACSA	0°C to +70°C	8 Lead Small Outline
ICL7663AIJA	-20°C to +85°C	8 Lead CERDIP
ICL7663AITV	-20°C to +85°C	TO-99
ICL7663BC/D	0°C to +70°C	Dice
ICL7663BCPA	0°C to +70°C	8 Lead Plastic DIP
ICL7663BIJA	-20°C to +85°C	8 Lead CERDIP
ICL7663BITV	-20°C to +85°C	8 Lead TO-99

Typical Operating Circuit



Positive Voltage Regulator

(Detailed Circuit Diagram—Figure 3)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Programmable Positive Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... +18V
Any Input or Output Voltage (Note 1)
(Terminals 1, 2, 3, 5, 6, 7) (GND − 0.3V) to (V_{IN}^+ + 0.3V)
Output Source Current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output Sinking Current
(Terminal 7) ..... −10mA
Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW
Cerdip (Maxim) 500mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{IN}^+ = 9V, V_{OUT} = 5V, T_A = +25°C, test circuit unless noted.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Voltage	V_{IN}^+	ICL7663				
		T_A = 25°C	1.5		16.0	V
		20°C ≤ T_A ≤ +70°C	1.6		16.0	V
		ICL7663B				
		T_A = 25°C	1.5		10	V
		20°C ≤ T_A ≤ +70°C	1.6		10	V
Quiescent Current	I_Q	R_L = ∞, 1.4V ≤ V_{OUT} ≤ 8.5V; V_{IN}^+ = 16V, ICL7663 only		4.0	12	µA
		R_L = ∞, 1.4V ≤ V_{OUT} ≤ 8.5V; V_{IN}^+ = 9V		3.5	10	µA
Reference Voltage	V_{SET}		1.2	1.3	1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	8.5V < V_{IN}^+ < 9V		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	2V < V_{IN}^+ < 15V, ICL7663		0.03		%/V
		2V < V_{IN}^+ < 9V, ICL7663B		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled	1.4			V
		V_{SHDN}LO: Both V_{OUT} Enabled			0.3	
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	V_{CL} = V_{OUT2} − V_{SENSE} (Current-Limit Threshold)		0.7		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	V_{IN}^+ = 2V		200		Ω
		V_{IN}^+ = 9V		70		Ω
		V_{IN}^+ = 15V, ICL7663 only		50		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	ΔI_{OUT1} = 100µA @ V_{OUT1} = 5V		2.0		Ω
		ΔI_{OUT2} = 10mA @ V_{OUT2} = 5V		1.0		
Available Output Current (V_{OUT2})	I_{OUT2}	V_{IN}^+ = 3V V_{OUT} = V_{SET}	10			mA
		V_{IN}^+ = 9V V_{OUT} = 5V	25			mA
		V_{IN}^+ = 15V V_{OUT} = 5V, ICL7663 only	40			mA
Negative Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(min)}$	(Includes V_{SET} Divider)			1.0	µA

Note 1: Connecting any terminal to voltages greater than (V_{IN}^+ + 0.3V) or less than (GND − 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note 4: This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 5 for details. Pin will not source current.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Programmable Positive Voltage Regulator

- **1% Output Voltage Accuracy (ICL7663A)**
- **Key Specifications Guaranteed Over Temperature**
- **Improved Output Voltage Temperature Coefficient**
- **Guaranteed Line and Load Regulation**
- **Improved ESD Protection (Note 5)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS Specifications below satisfy or exceed all "tested" parameters on adjacent page.

V_{IN}^+ = 9V, V_{OUT} = 5V, T_A = 25°C, test circuit unless noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}^+	ICL7663 T_A = +25°C	1.5		16	V
		Over Temperature	1.6		16	V
		ICL7663A				
		Over Temperature	**2.0**		**16**	**V**
		ICL7663B T_A = +25°C	1.5		10	V
		Over Temperature	1.6		10	V
Quiescent Current	I_Q	1.4V ≤ V_{OUT} ≤ 8.5V, no load				
		V_{IN}^+ = 9V				
		ICL7663, ICL7663A, Over Temperature			**10**	**µA**
		ICL7663B, T_A = 25°C			10	µA
		V_{IN}^+ = 16V				
		ICL7663, ICL7663A, Over Temperature			**12**	**µA**
Reference Voltage	V_{SET}	I_{OUT1} = 100µA, V_{OUT} = V_{SET}, T_A = +25°C				
		ICL7663, ICL7663B	1.2		1.4	V
		ICL7663A	**1.275**	**1.3**	**1.305**	**V**
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	**Over Temperature**		**100**		**ppm/°C**
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	**ICL7663, ICL7663A, V_{IN} = 2 – 15V,**				
		Over Temperature		**0.03**	**0.35**	**%/V**
		ICL7663B, V_{IN} = 2 – 9V		0.03		%/V
V_{SET} Input Current	I_{SET}	**ICL7663, ICL7663A, Over Temperature**		**0.01**	**10**	**nA**
		ICL7663B, T_A = +25°C		0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled	1.4			V
		V_{SHDN}LO: Both V_{OUT} Enabled			0.3	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold	V_{CL}			0.5		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	**ICL7663A, ICL7663**				
		V_{IN}^+ = 2V, I_{OUT1} = 1mA		**200**	**500**	**Ω**
		V_{IN}^+ = 9V, I_{OUT1} = 2mA		**70**	**150**	**Ω**
		V_{IN}^+ = 15V, I_{OUT1} = 5mA		**50**	**100**	**Ω**
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	**ICL7663A, ICL7663**				
		1mA ≤ I_{OUT2} ≤ 20mA		**1**	**5**	**Ω**
		50µA ≤ I_{OUT1} ≤ 5mA		**2**	**10**	**Ω**
Available Output Current (V_{OUT2})	I_{OUT2}	3V ≤ V_{IN} ≤ 16, V_{IN} – V_{OUT2} = 1.5V	40			mA
Negative-Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(min)}$	(Includes V_{SET} Divider) T_A = +25°C			1.0	µA
		Over Temperature		**0.2**	**5**	**µA**

Note 1: Connecting any terminal to voltages greater than (V_{IN}^+ + 0.3V) or less than (GND – 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for plastic minidip, 7.5mW/°C for TO-99 can, and 10mW/°C for CERDIP.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

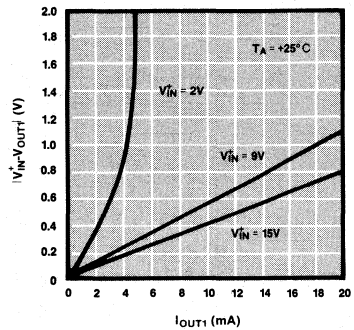
Note 4: This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

Note 5: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)

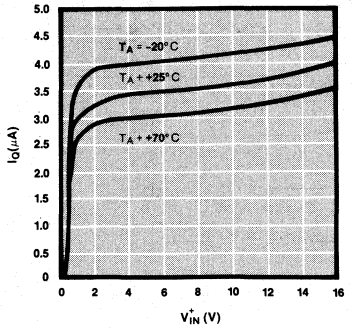
Programmable Positive Voltage Regulator

Typical Operating Characteristics

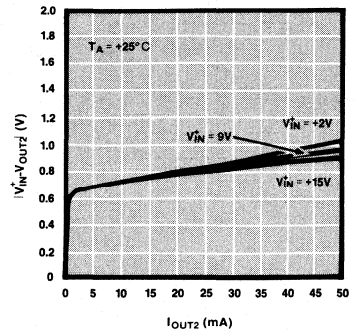
V_{OUT1} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



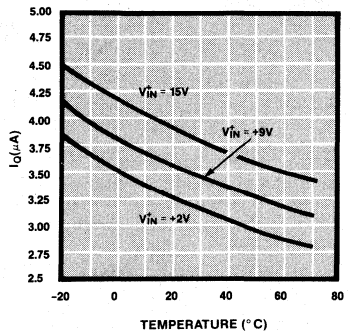
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



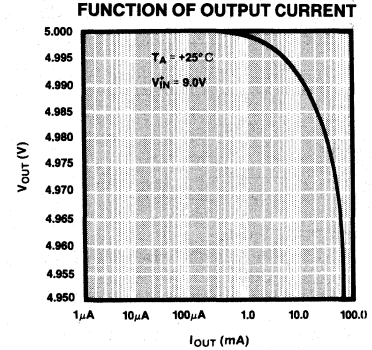
V_{OUT2} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



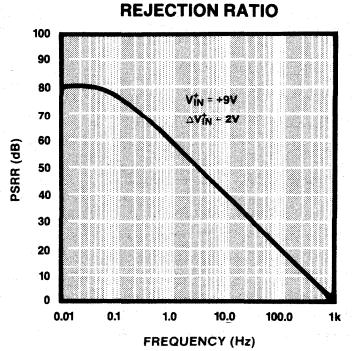
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



INPUT POWER SUPPLY REJECTION RATIO



Programmable Positive Voltage Regulator

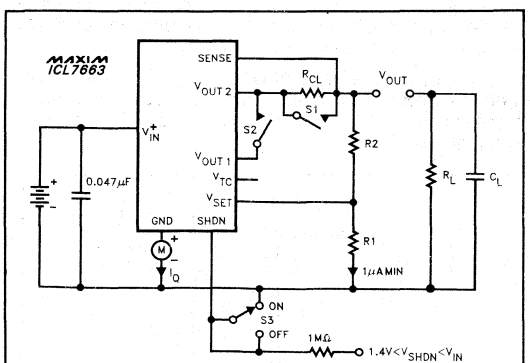
Detailed Description

Block Diagram

As shown in the block diagram of Figure 2, the main elements of the ICL7663 are a micropower bandgap reference, an error amplifier, and an output driver with both FET and NPN bipolar transistors.

The bandgap reference of the Maxim ICL7663A, which uses less than 1μA of quiescent current, is precisely trimmed to 1.29V ± 15mV. The output of the bandgap reference and the input voltage at the V_{SET} terminal are compared in Amplifier A. This output drives the series pass FET output driver which is connected to V_{OUT1}. This output, suitable for output currents less than 5mA, can drive low current loads with a input-to-output voltage differential that approaches 0V with low current loads. The minimum input-to-output differential voltage is the product of the output current and the output saturation resistance. For higher current loads, use the V_{OUT2} pin. The V_{OUT2} pin is driven by an on-chip NPN bipolar transistor whose base is internally connected to the V_{OUT1} output. The NPN bipolar transistor of the Maxim ICL7663 can drive up to 40mA loads with a guaranteed input-to-output differential of 1.5V maximum.

Also onboard the ICL7663 is a sense comparator that will current limit the output when the voltage across the current sense resistor, R_{CL}, is greater than approximately 0.5V; a logic shutdown input that turns off the output by logic level control; and an auxiliary output, V_{TC}, that has a positive temperature coefficient. Using it in combination with the inverting input of Amplifier A, a negative coefficient results in the output voltage.



Note 1: S_1 when closed disables output current limiting

Note 2: Close S_2 for V_{OUT1}, open S_2 for V_{OUT2}

Note 3: $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$

Note 4: I_Q quiescent current is measured at GND pin by meter M

Note 5: S_3 when ON, permits normal operation, when OFF, shuts down both V_{OUT1} and V_{OUT2}

Figure 1. Maxim ICL7663 Test Circuit.

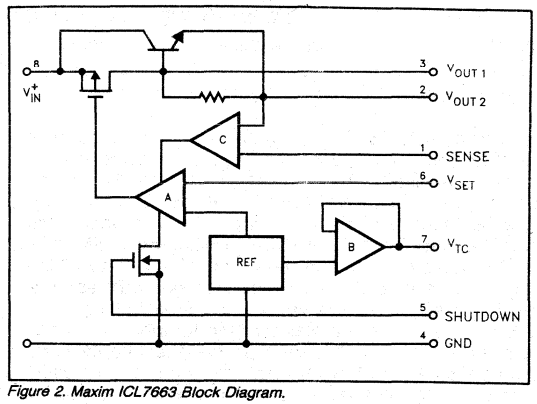


Figure 2. Maxim ICL7663 Block Diagram.

Basic Circuit Operation

Figure 3 shows a typical positive voltage regulator using the ICL7663. The input voltage, V_{IN}^{+} can range from a maximum of 16V to a minimum of the output voltage plus the input-output differential. The output voltage is set by the resistors R2 and R1, and the output current limit is set by R_{CL}. The 0.047μF capacitor on the input limits the rate-of-rise during power-up and also removes some of the high frequency noise on the input voltage. In Figure 3, the logic shutdown is not used and is therefore grounded. V_{OUT2} should be connected directly to SENSE if current limiting is not used.

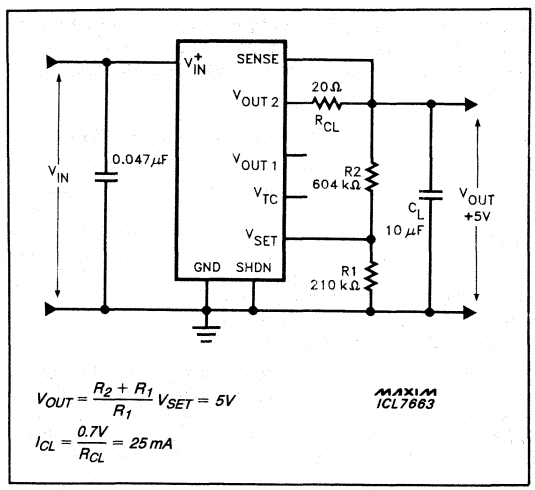


Figure 3. Maxim's Application of ICL7663 (Positive Regulator, Current Limit).

Programmable Positive Voltage Regulator

Output Voltage Selection

The output voltage can be calculated from the formula:

$$V_{OUT} = V_{SET} \times \left(1 + \frac{R_2}{R_1}\right) = V_{SET} \times \left(\frac{R_1 + R_2}{R_1}\right)$$

The Maxim ICL7663A V_{SET} voltage is guaranteed to be 1.29V ± 15mV, eliminating the need for trim pots in most cases. Specifically, using the Maxim ICL7663A and the resistor values shown in Figure 3, the initial voltage will be within ±2.7% of 5V, assuming ±1% tolerance resistors. The output voltage will remain within 5V ± 5%, over 0–70°C. This tolerance includes the effect of ICL7663A V_{SET} error, the ±1% initial tolerance on both resistors, and the resistor ratio temperature coefficient of nearly 200 ppm/°C. Since the resistor ratio temperature coefficient is generally much lower than the absolute temperature coefficient, 100 or 200 ppm resistors can be used, even over the full temperature range while still allowing the output to stay within 4.75V–5.25V.

For 5V supplies that have a looser tolerance, the 5% resistor values of 150kΩ and 430kΩ or 560kΩ and 1.6MΩ are suitable values for R2 and R1. With resistors of ±5% initial tolerance, the initial output voltage will be 5V ± 8.8% and, neglecting the tempco of the resistors, will stay within 5V ± 10% over the entire temperature range.

Current Limiting

The circuit in Figure 3 will limit the output current to approximately 35mA. Current limiting will start, when the output current exceeds 35mA and the voltage drop across the 20Ω R_{CL} is 500mV. For other current limits the value of R_{CL} can be calculated from the formula:

$$R_{CL} = \frac{0.7V}{I_{CL}}; \text{ where } I_{CL} \text{ is the current limit value.}$$

The current limit resistor should be chosen so that neither the 50mA absolute maximum output current specification nor the maximum power dissipation specification is violated.

Input-Output Differential Voltage

The minimum input-output differential voltage (also called dropout voltage) sets the lower limit for the battery voltage in battery powered supplies. The ICL7663 has a dropout voltage of less than one volt. For example, the ICL7663 will continue to supply a regulated 5V output at 40mA until the battery voltage is less than 6.0V. This is significantly better performance than the standard 3 terminal regulators which require a minimum input-output differential of 2–3V to maintain regulation.

As shown in the Typical Characteristics graphs, the minimum input-output differential for the high current output, V_{OUT2}, is relatively independent of output current, varying from 0.6V at low current to about 0.9V at 40mA. This minimum 0.6V input-output differential is caused by the base-emitter voltage drop of the NPN bipolar transistor that drives V_{OUT2}.

By using V_{OUT1} this 0.6V minimum input-output differential voltage is eliminated, but the required input-output differential rises more rapidly (at the rate set by the output saturation resistance — see Electrical Specifications). Ordinarily, it is advantageous to use V_{OUT1} for output currents less than 5mA, and to use V_{OUT2} for higher currents.

If a current limiting resistor is used, the voltage drop across it at the desired operating current must be added to obtain the minimum input-output differential required.

Output Current Booster

Figure 4 shows a circuit that will supply 5 volts at 1 ampere, with a 6.5V input. The high power external series pass NPN transistor is connected in parallel with the internal NPN transistor. The 100Ω resistor in series with V_{OUT2} keeps the current supplied by the ICL7663, and therefore the power dissipation, within the absolute maximum ratings.

This circuit is particularly useful for battery powered systems that alternately draw high current, then shutdown to extend the battery life.

Logic Level Shutdown

The ability to turn off the output of the ICL7663 using a single logic level pin is useful in systems where the equipment is on intermittently. By shutting down the output, the total battery drain is reduced to only the quiescent current of the ICL7663, typically 4μA. The shutdown input should preferably be driven by CMOS logic since the input logic low level is only 0.3V. An alternate way of driving is with an open collector PNP transistor and a resistive pulldown. The pulldown resistor need only draw a fraction of a microamp since the Shutdown terminal input current is less than 10nA.

Figure 4 shows a system that will supply up to 1 ampere of output current when active, but will shutdown to 4μA quiescent current by merely switching the Shutdown pin to the high state.

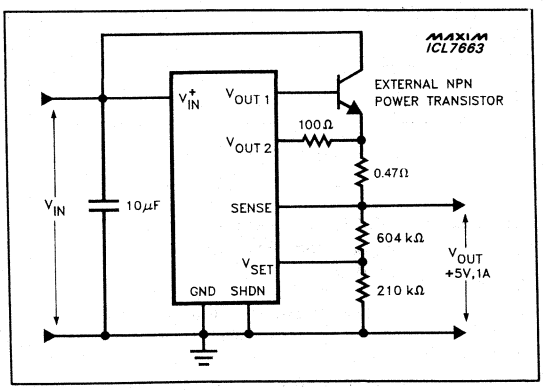


Figure 4. Boosting Output Current with External Transistor.

Programmable Positive Voltage Regulator

Negative Temperature Coefficient Output

The V_{TC} pin has a positive temperature coefficient of about +2.5mV. When connected via a resistor to the inverting summing junction of the error amplifier (the V_{SET} terminal), this positive coefficient results in a controllable negative temperature coefficient at the output of the ICL7663. Figure 5 shows a simplified diagram of the ICL7663 and the pertinent equations for setting both the output voltage and the output tempco.

Negative output temperature coefficients are most commonly used in multiplexed LCD modules or dislay systems to compensate for the negative temperature coefficient of the LCD threshold. Figure 6 shows an ICL7663 generating a temperature compensated V_{DIS} for the Maxim ICM7233 triplexed LCD display driver.

Cautions

The ICL7663 is designed for low quiescent current battery powered systems and has limited line and load regulation at frequencies above 10Hz. The high frequency load and line regulation is easily improved by adding an output filter capacitor across the load.

As with all junction isolated CMOS devices, the ICL7663 can be destroyed by SCR latchup if standard precautions are not observed. First, no pins should ever be driven more than 0.3V below ground or more than 0.3V above V_{IN}^+. Secondly, the rate-of-rise on V_{IN}^+ should not be excessive. The rate-of-rise can be several hundred volts per microsecond if the V_{IN}^+ source has a low internal impedance (such as Nicad or lead-acid batteries). There is no current limiting resistance or inductance between the battery and the ICL7663, and there is no input filtering.

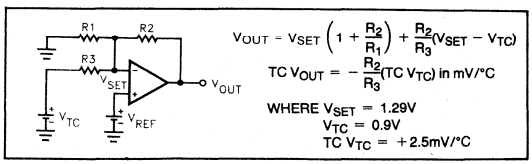


Figure 5. Maxim's Generation of Negative Temperature Coefficients.

Carbon-zinc or alkaline batteries normally do not have sufficient current output capability to cause a rate-of-rise SCR, but the simple addition of a 0.1μF or greater bypass capacitor on the input will ensure that these batteries will not cause SCR latchup.

±5V Power Supply Using One 9V Battery

The ICL7660 inverts the +9V input voltage to −9V which is then regulated by the ICL7664 negative regulator to a constant −5V output (Refer to Figure 7). The ICL7663 positive voltage regulator uses the +9V input directly to generate a regulated +5V output. The combined quiescent current of the Maxim ICL7660 and the two regulators is less than 100μA, while the output current capability is 40mA. The external oscillator capacitor reduces the oscillation frequency of the ICL7660. This allows the battery voltage to be inverted more efficiently.

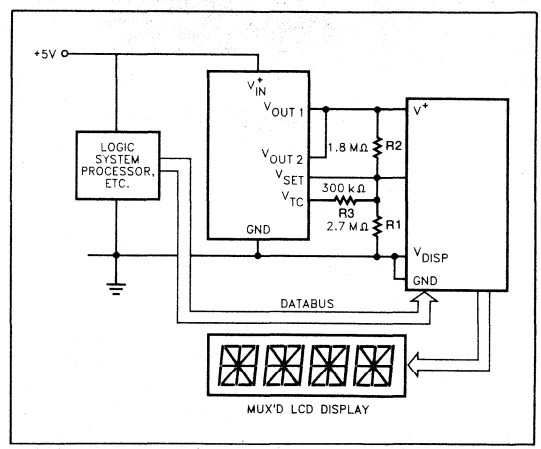


Figure 6. Driving a Multiplexed LCD Display. Consistent operation over more than 40°C temperature span, as opposed to about 10°C with a fixed drive voltage, is allowed by negative temperature coefficient drive voltage to the displays. Based on EPSON LDB-728 Display or equivalent.

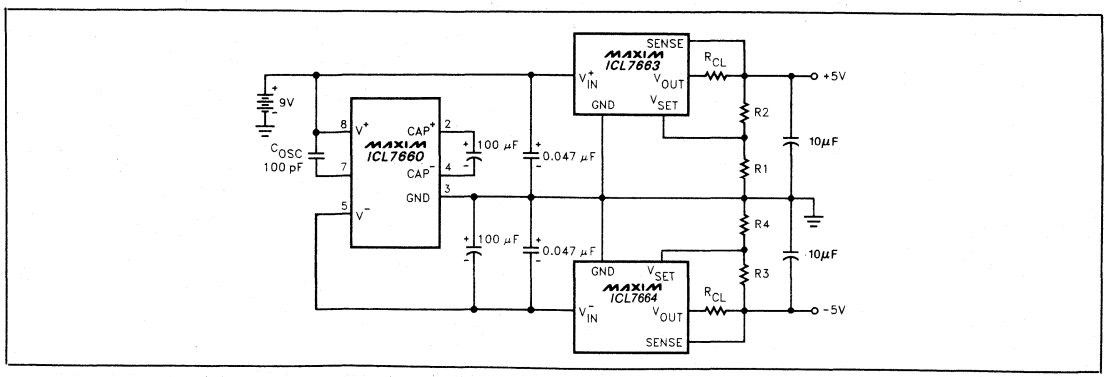
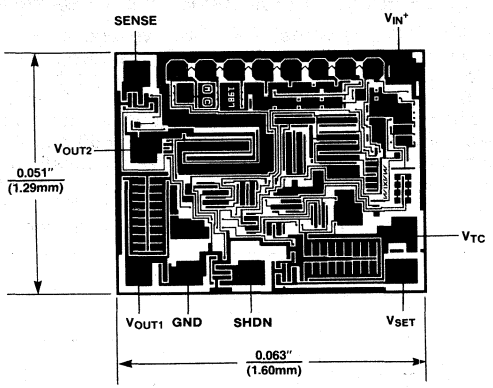


Figure 7. ±5V power supply using one 9V battery.

Programmable Positive Voltage Regulator

Chip Topography



MAXIM
Programmable Negative Voltage Regulator

General Description

The ICL7664 is a high efficiency negative voltage regulator with a quiescent current of less than 10μA. The output voltage is set by two external resistors to any voltage in the -1.3V to -16V range, with an input voltage range of -2V to -16V. The ICL7664 is well suited for battery powered supplies, with a 10μA quiescent current, an output current capability of 25mA, low V_{IN} to V_{OUT} differential, current limiting, and a logic input level shutdown control.

The Maxim ICL7664 is compatible with existing ICL7664 designs when used with an output filter capacitor of 10μF or greater.

The ICL7664A is an enhanced version of the ICL7664, with a 1% accurate voltage reference, which eliminates the need for trimming the output voltage in most applications.

Applications

Designed specifically for battery powered systems, the ICL7664 negative voltage regulator excels wherever low quiescent power, wide voltage range operation, medium output current levels, current limiting, and logic-controlled shutdown is desired.

Handheld Instruments
LCD Display Modules and Systems
Pagers
Remote Data Loggers

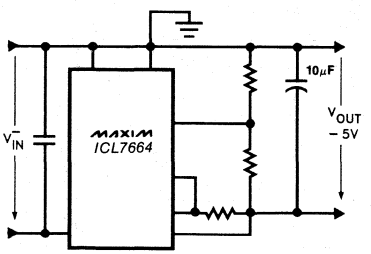
Features

- **1% Output Voltage Accuracy (ICL7664A)**
- **-2V to -16V Operating Range**
- **25mA Output Current, with Current Limiting**
- **Adjustable Output Voltage**
- **Low Input-to-Output Voltage Drop**
- **Low Power CMOS: 4μA Quiescent Current**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7664C/D	0°C to +70°C	Dice
ICL7664CJA	0°C to +70°C	8 Lead Cerdip
ICL7664CPA	0°C to +70°C	8 Lead Plastic Dip
ICL7664CSA	0°C to +70°C	8 Lead Small Outline
ICL7664CTV	0°C to +70°C	8 Lead TO-99 Can
ICL7664AC/D	0°C to +70°C	Dice
ICL7664ACJA	0°C to +70°C	8 Lead Cerdip
ICL7664ACPA	0°C to +70°C	8 Lead Plastic Dip
ICL7664ACSA	0°C to +70°C	8 Lead Small Outline
ICL7664ACTV	0°C to +70°C	8 Lead TO-99 Can

Typical Operating Circuit

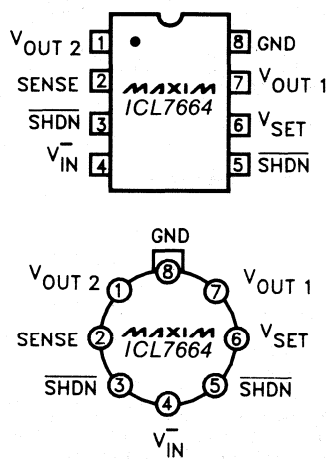


Negative Regulator with Current Limit

(Detailed Circuit Diagram—Figure 3)

Pin Configuration

Top View



6

Programmable Negative Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... -18V
Input or Output Voltage (Note 1) ..... (GND + 0.3V) to
Terminals (1, 3, 5, 6, 7) (V_{IN}^- - 0.3V)
Sense Pin ..... (GND + 0.3V) to
(Pin 2) (V_{OUT1} - 0.3V)
Output Sink Current
(Terminals 1, 7) ..... -25mA
Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW
CERDIP 500mW

Operating Temperature Range
ICL7664C/D ..... 0°C to +70°C
ICL7664CPA ..... 0°C to +70°C
ICL7664IJA ..... -20°C to +85°C
ICL7664ITV ..... -20°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{IN} = -9V, V_{OUT} = -5V, T_A = +25°C, test circuit unless noted

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	$0°C \le T_A \le +70°C$	-2.0		-16.0	V
Quiescent Current	I_Q	$R_L = \infty$, $-1.4V \le V_{OUT} \le -8.5V$ V^-_{IN} = -16V, $0°C \le T_A \le +70°C$ V^-_{IN} = -9V, $0°C \le T_A \le +70°C$		4.0 3.5	12 10	µA µA
Reference Voltage	V_{SET}	I_{OUT} = 100µA, $V_{OUT} = V_{SET}$ ICL7664A ICL7664	 -1.275 -1.2	 -1.29 -1.3	 -1.305 -1.4	 V V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$			±100		ppm/°C
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	$-2V \le V^-_{IN} \le -15V$		0.03	0.35	%/V
V_{SET} Input Current	I_{SET}	$0°C \le T_A \le +70°C$		±0.01	±10	nA
Shutdown Input Current	$I_{\overline{SHDN}}$	$GND \le V_{\overline{SHDN}} \le V_{IN}$		±0.01	±10	nA
Shutdown Input Voltage	$V_{\overline{SHDN}}$	$V_{\overline{SHDN}}$HI: Both V_{OUT} Enabled $V_{\overline{SHDN}}$LO: Both V_{OUT} Disabled	-0.7		 -1.7	V V
Sense Pin Input Current	I_{SENSE}	$V_{SENSE} = V_{OUT1}$		±0.01	±10	nA
Sense Pin Input Threshold	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		-0.7		V
Input-Output Saturation Resistance (Note 3)	R_{OUT}	V_{OUT1} Connected to V_{OUT2} V^-_{IN} = -2V V^-_{IN} = -9V V^-_{IN} = 15V		 150 40 30	 500 80 60	 Ω Ω Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	ΔI_{OUT} = 100µA		2.0	5.0	Ω
Output Current, V_{OUT1} connected to V_{OUT2}	I_{OUT}	V^-_{IN} = -3V $V_{OUT} = V_{SET}$ V^-_{IN} = -9V V_{OUT} = -5V		-2 -20		mA mA
Minimum Load Current (Includes V_{SET} Divider)	$I_{L(MIN)}$	$0°C \le T_A \le +70°C$			1.0	µA

Note 1: Connecting any terminal to voltages greater than (GND + 0.3V) or less than (V^-_{IN} -0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664 power-up.

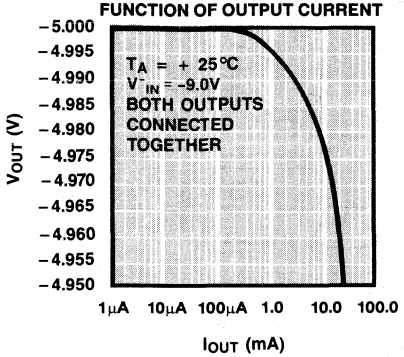
Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

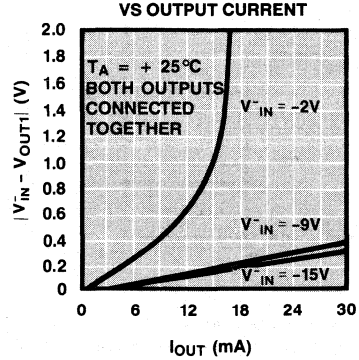
Programmable Negative Voltage Regulator

Typical Operating Characteristics

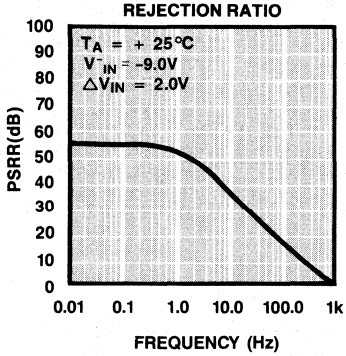
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



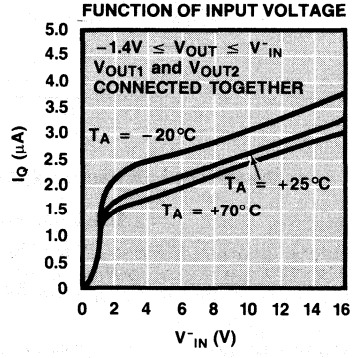
INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



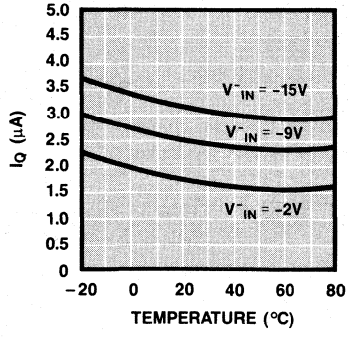
INPUT POWER SUPPLY REJECTION RATIO



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

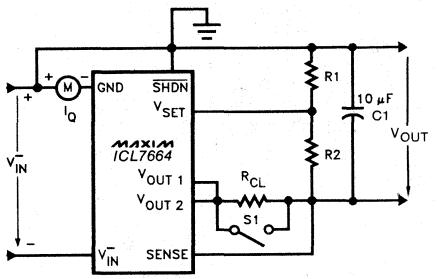


QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



6

Programmable Negative Voltage Regulator



Note 1: Closing S_1 disables current limiting.

Note 2: Quiescent current, I_Q, is measured at the GND pin by meter M.

Note 3: $V_{OUT} = \frac{R_1 + R_2}{R_1} \times V_{SET}$

$$I_{CL} \approx \frac{0.7V}{R_{CL}}$$

Note 4: The value of C1 must be 10µF or greater to ensure stability.

Figure 1. Test Circuit

Detailed Description

Block Diagram

As shown in the block diagram of Figure 2, the main elements of the ICL7664 are a micropower bandgap reference, an error amplifier, and two n channel FET output drivers.

The bandgap reference of the ICL7664A, which uses less than 1µA of quiescent current, is precisely trimmed to 1.29 ± 15mV. The output of the bandgap reference and the input voltage at the V_{SET} terminal are compared in Amplifier A. This output drives the series pass FET output drivers which are connected to V_{OUT1} and V_{OUT2}. These outputs, suitable for output currents of up to 50mA total, can drive low current loads with an input-to-output voltage differential that approaches 0V. The minimum input-to-output voltage increases at the rate of $I_{OUT} \times R_{SAT}$.

Also onboard the ICL7664 is a sense comparator that will current limit the output when the voltage across the current sense resistor, R_{CL}, is greater than approximately 0.7V; and a logic shutdown input that turns off the output by logic level control.

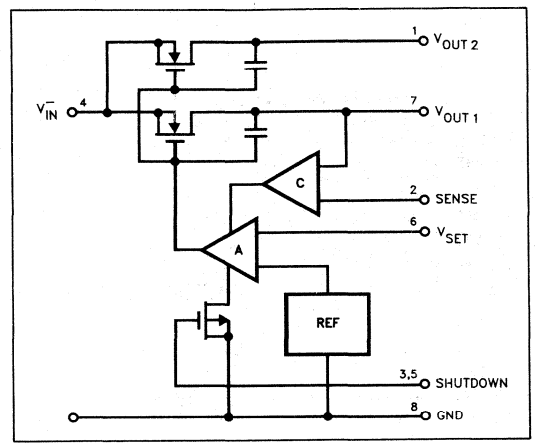


Figure 2. Block Diagram of the ICL7664.

Basic Circuit Operation

Figure 3 shows a typical negative voltage regulator using the ICL7664. The input voltage, V_{IN}, can range from a maximum of -16V to a minimum of the output voltage plus the input-output differential. The output voltage is set by the resistors R2 and R1, and the output current limit is set by R_{CL}. The 0.047µF capacitor on the input is used to limit the rate-of-rise during power-up and also removes some of the high frequency noise on the input voltage. In Figure 3, the logic shutdown is not used and is therefore grounded. V_{OUT1} and V_{OUT2} should be connected directly to SENSE if current limiting is not used.

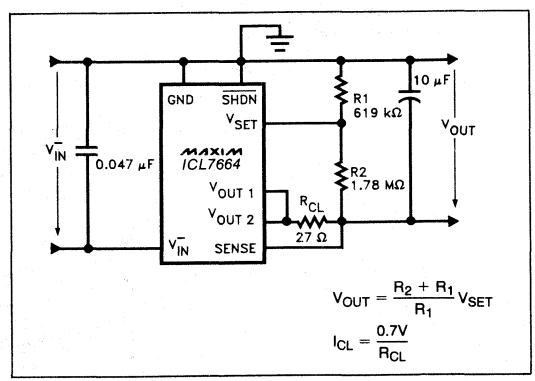


Figure 3. ICL7664 as Negative Regulator with Current Limit

Programmable Negative Voltage Regulator

Output Voltage Selection

The output voltage can be calculated from the formula:

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1}$$

The ICL7664A V_{SET} voltage is guaranteed to be 1.29V ± 15mV at 25°C, eliminating the need for trim pots in most cases. Specifically, using the ICL7664A and the resistor values shown in Figure 3, the initial voltage will be within ±2.7% of 5V, assuming ±1% tolerance resistors. The output voltage will still be within 5V ± 5%, including the ICL7664A effects of the V_{SET} error, the ±1% initial tolerance on both resistors, and the resistor ratio temperature coefficient of nearly 200ppm. Since the resistor ratio temperature coefficient is generally much lower than the absolute temperature coefficient, 100 or 200ppm resistors can be used, even over the full temperature range while still guaranteeing that the output will stay within 4.75V to 5.25V.

For 5V supplies that have a looser tolerance, the 5% resistor values of 1.6MΩ and 560kΩ are suitable values for R2 and R1. With resistors of ±5% initial tolerance, the initial output voltage will be 5V ± 8.7%.

Current Limiting

The circuit in Figure 3 will limit the output current to approximately 25mA. Current limiting will start when the output current exceeds 25mA and the voltage drop across the 27Ω R_{CL} is 700mV. For other current limits the value of R_{CL} can be calculated from the formula:

$$R_{CL} = \frac{0.7V}{I_{CL}}; \text{ where } I_{CL} \text{ is the current limit value.}$$

The current limit resistor should be chosen so that neither the 50mA absolute maximum output current specification (25mA each from V_{OUT1} and V_{OUT2}) nor the maximum power dissipation specification is violated.

The ICL7664 activates current limiting by internally pulling the V_{SET} terminal down towards V_{IN}. The main error amplifier then reacts as if the output voltage is greater than the desired output voltage, and shuts off the output. For this current limiting action to work, the parallel resistance of the voltage divider connected to V_{SET} must be greater than 10kΩ.

Input-Output Differential Voltage

The minimum input-output differential voltage (also called dropout voltage) sets the lower limit for usable battery voltage in battery powered supplies. In the ICL7664, the minimum input-output differential voltage is the product of the output current and the ICL7664 output saturation resistance. See the typical characteristics graphs for a plot of input-output differential vs. output current.

Output Current Booster

Figure 4 shows a circuit that will supply -5 volts at 2 amperes, with a 6.5V input. The base of the high power external series pass PNP transistor is driven by V_{OUT1} and V_{OUT2} in parallel. This circuit is useful in circuits where the 50mA maximum output current of the ICL7664 is inadequate, with the only limitation to output current being that the ICL7664 must not supply more than 50mA of base drive to the external PNP transistor. With a beta of 40, the output current would be a maximum of 2 amperes.

This circuit is particularly useful for battery powered systems that alternately draw high current, then shut down to extend the battery life. In the shutdown state, the circuit will draw only the 4μA typical quiescent current of the ICL7664, plus the leakage current of the transistor, which is normally less than 1μA.

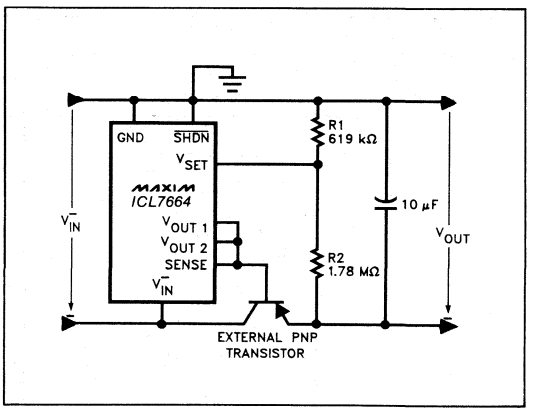


Figure 4. Output Current Boosting

Logic Level Shutdown

The ability to turn off the output of the ICL7664 using a single logic level pin is useful in systems where the equipment is on intermittently. The Shutdown input should preferably be driven by CMOS logic since the input logic high level is only -0.3V. An alternate way of driving is with an open collector PNP transistor and a resistive pullup to ground. The pullup resistor need only draw a fraction of a microamp since the Shutdown terminal input current is less than 10nA.

Figure 4 shows a circuit that will supply up to 2 amperes of output current when active, but will shut down to 4μA quiescent current by merely switching the Shutdown pin to the high state.

Cautions

While the ICL7664 is stable under most conditions, **a 10μF output filter capacitor is required** to ensure stability under all conditions. This output filter capacitor will also improve the high frequency line and load regulation.

As with all junction isolated CMOS devices, the ICL7664 can be destroyed by SCR latchup if standard precautions are not observed. First, no pins should ever

Programmable Negative Voltage Regulator

be driven more than ±0.3V above ground or more than -0.3V below the V_{IN}. Secondly, the rate-of-rise on V_{IN} should not be excessive. The rate-of-rise can be several hundred volts per microsecond if the V_{IN} source has a low internal impedance (such as Nicad or lead-acid batteries). There is no current limiting resistance or inductance between the battery and the ICL7664, and there is no input filtering. Carbon-zinc and alkaline batteries normally do not have sufficient current output capability to cause a rate-of-rise SCR, but the simple addition of a 0.1μF or greater bypass capacitor on the input will ensure that these batteries will not cause SCR latchup.

Figure 5 shows a combined application of the ICL7664, an ICL7663 positive regulator, and the ICL7660 voltage inverter in a ±5V regulated power supply whose power source is a single +9V battery. The ICL7660 inverts the +9V input voltage to -9V which is then regulated by the ICL7664 negative regulator to a constant -5V output. The ICL7663 positive voltage regulator uses the +9V input directly to generate a regulated +5V output. The combined quiescent current of the Maxim ICL7660 and the two regulators is less than 100μA, while the output current capability is 40mA.

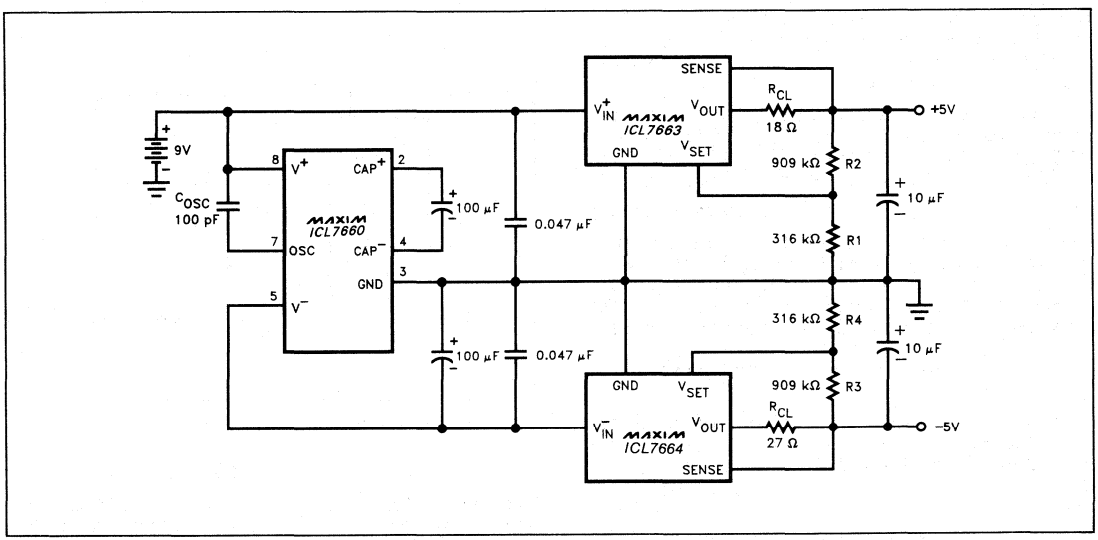
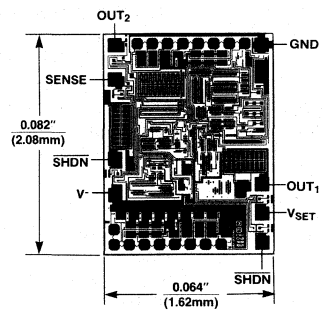


Figure 5. ±5V Power Supply Using One 9V Battery

Chip Topography



MAXIM

Dual Over/Under Voltage Detector

General Description

The ICL7665 is a low power dual over/under voltage detector drawing a typical operating current of only 3μA. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors to any voltage greater than 1.3V. The ICL7665 will operate from any supply voltage in the 1.6V to 16V range, while monitoring voltages from 1.3V to several hundred volts.

The Maxim ICL7665 and ICL7665B are equivalent to the original manufacturer's parts in both pinout and specification. The Maxim ICL7665A is an improved version with a 2% accurate V_{SET1} threshold and guaranteed performance over temperature. All three versions of the Maxim ICL7665 undergo 100% burn-in and are rigorously tested at temperature extremes to enhance their quality and reliability.

Applications

The 3μA quiescent current of the ICL7665 makes it ideal for voltage monitoring in battery powered systems. In both battery and line-powered systems, the unique combination of a reference, two comparators and hysteresis outputs reduces size and component count of many circuits.

Low Battery Detection
Power Fail and Brownout Detector
Battery Backup Switching
Power Supply Fault Monitoring
Over/Under-Voltage Protection
Hi/Low Temperature, Pressure and Voltage Alarms

Features

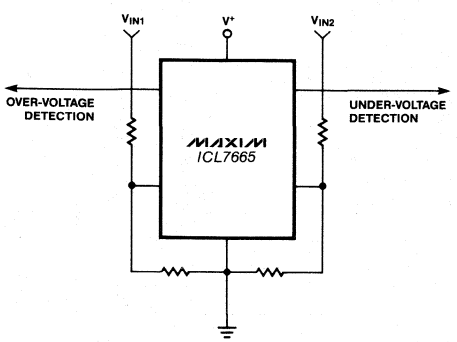
- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Dual Comparator with Precision Internal Reference**
- **3μA Operating Current**
- **2% Threshold Accuracy (ICL7665A)**
- **1.6V to 16V Supply Voltage Range**
- **Onboard Hysteresis Outputs**
- **Trip Points Externally Programmable**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7665C/D*	0°C to +70°C	Dice
ICL7665CJA*	0°C to +70°C	8 Lead Cerdip
ICL7665CPA*	0°C to +70°C	8 Lead Plastic Dip
ICL7665CSA*	0°C to +70°C	8 Lead Small Outline
ICL7665CTV*	0°C to +70°C	8 Lead TO-99
ICL7665AC/D	0°C to +70°C	Dice
ICL7665ACJA	0°C to +70°C	8 Lead Cerdip
ICL7665ACPA	0°C to +70°C	8 Lead Plastic Dip
ICL7665ACSA	0°C to +70°C	8 Lead Small Outline
ICL7665ACTV	0°C to +70°C	8 Lead TO-99

*"B" version also available. Order part number ICL7665BXXX

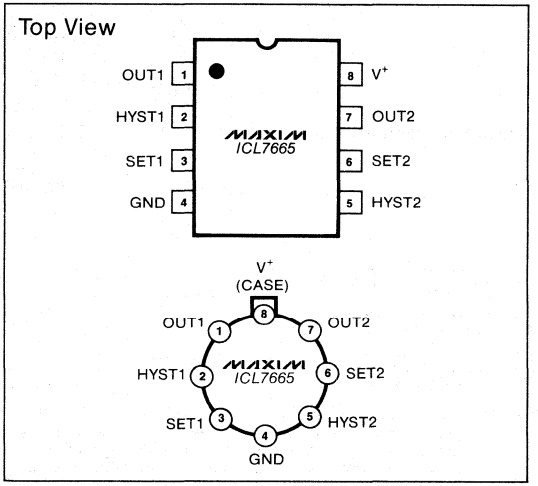
Typical Operating Circuit



SIMPLE THRESHOLD DETECTOR

(Detailed Circuit Diagram — Figure 3)

Pin Configuration



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Dual Over/Under Voltage Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ..... -0.3V to +18V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) ..... -0.3V to +18V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) ..... +0.3V to -18V
Input Voltages SET1 and SET2
(Note 2) ..... (GND - 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current
OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... -25mA

Power Dissipation (Note 1) 200mW
Operating Temperature Range
ICL7665BCPA* ..... 0°C to +70°C
ICL7665BCTV* ..... 0°C to +70°C
ICL7665BCSO* ..... 0°C to +70°C
ICL7665BC/D* ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature
(Soldering, 10 seconds) ..... +300°C

*Also applies to "A" version (Maxim).

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = +25°C$, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	$T_A = +25°C$ $-20°C \le T_A \le +70°C$	1.6 1.8		16.0 16.0	V
Supply Current	I^+	$GND \le V_{SET1}, V_{SET2} \le V^+$ All Outputs Open Circuit $V^+ = 2V$ $V^+ = 9V$ $V^+ = 15V$		 2.5 2.6 2.9	 10 10 15	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	$R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1M\Omega$		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	$V_{SET} = 0V$ or $V_{SET} \ge 2V$		10 -10	200 -100	nA
	I_{OLK} I_{HLK}	$V^+ = 15V$, $T_A = 70°C$ $V^+ = 15V$, $T_A = 70°C$			2000 -500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	$V^+ = 2V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$ $V^+ = 5V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$ $V^+ = 15V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$		0.2 0.1 0.06	0.5 0.3 0.2	V
	V_{HYST1} V_{HYST1} V_{HYST1}	$V^+ = 2V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$ $V^+ = 5V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$ $V^+ = 15V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$		-0.15 -0.05 -0.02	-0.3 -0.15 -0.10	
	V_{OUT2} V_{OUT2} V_{OUT2}	$V^+ = 2V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$ $V^+ = 5V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$ $V^+ = 15V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$		0.2 0.15 0.11	0.5 0.3 0.25	
	V_{HYST2} V_{HYST2} V_{HYST2}	$V^+ = 2V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.2mA$ $V^+ = 5V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.5mA$ $V^+ = 15V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.5mA$		-0.25 -0.43 -0.35	-0.8 -1.0 -0.8	
V_{SET} Input Leakage Current	I_{SET}	$GND \le V_{SET} \le V^+$		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	$R_{OUT} = 4.7k\Omega$, $R_{HYST} = 20k\Omega$ $V_{OUT}LO = 1\% V^+$, $V_{OUT}HI = 99\% V^+$		1		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	$R_{OUT}, R_{HYST} = 1M\Omega$		±5	±50	
Output/Hysteresis Difference		$R_{OUT}, R_{HYST} = 1M\Omega$		±1		

Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Dual Over/Under Voltage Detector

- ♦ 2% V_{SET} Threshold Accuracy (ICL7665A)
- ♦ Key Specifications Guaranteed over Temperature
- ♦ Improved Temperature Coefficient (ICL7665A)
- ♦ Significantly Improved ESD Protection (Note 1)
- ♦ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: ICL7665 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = 5V, T_A = +25°C, test circuit unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7665A MIN	ICL7665A TYP	ICL7665A MAX	ICL7665 MIN	ICL7665 TYP	ICL7665 MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C				1.6		16.0	V
		−20°C ≤ T_A ≤ +70°C				1.8		16.0	V
		0°C ≤ T_A ≤ +70°C	2.0		16.0				V
Supply Current	I^+	**GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit 0°C ≤ T_A ≤ +70°C (ICL7665A only)**							
		V^+ = 2V		**2.5**	**10**		2.5	10	µA
		V^+ = 9V		**2.6**	**10**		2.6	10	µA
		V^+ = 15V		**2.9**	**15**		2.9	15	µA
Input Trip Voltage	**V_{SET1}**		**1.275**	**1.3**	**1.325**	1.15	1.3	1.45	V
	V_{SET2}		**1.225**	**1.3**	**1.375**	1.2	1.3	1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			**100**			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		.004			.004		%/V
Output Leakage Currents of OUT and HYST	I_{OLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10	200		10	200	nA
	I_{HLK}			−10	−100		−10	−100	nA
	I_{OLK}	V^+ = 15V, T_A = 70°C			2000			2000	nA
	I_{HLK}	V^+ = 15V, T_A = 70°C			−500			−500	nA
Output Saturation Voltages	V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2			0.2	0.5	V
	V_{OUT1}	V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.1	0.3		0.1	0.3	V
	V_{OUT1}	V^+ = 15V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.06	0.2		0.06	0.2	V
	V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.15	−0.3		−0.15	−0.3	V
	V_{HYST1}	V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.05	−0.15		−0.05	−0.15	V
	V_{HYST1}	V^+ = 15V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.02	−0.10		−0.02	−0.10	V
	V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2	0.5		0.2	0.5	V
	V_{OUT2}	V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.15	0.3		0.15	0.3	V
	V_{OUT2}	V^+ = 15V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.11	0.25		0.11	0.25	V
	V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = −0.2mA		−0.25	−0.8		−0.25	−0.8	V
	V_{HYST2}	V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.43	−1.0		−0.43	−1.0	V
	V_{HYST2}	V^+ = 15V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.35	−1.0		−0.35	−0.8	V
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		±0.01	±10		±0.01	±10	nA
ΔV_{SET} Input for Complete Output Change	**ΔV_{SET}**	**R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT} LO = 1% V^+, V_{OUT} HI = 99% V^+**		**0.1**			1.0		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ		±5	±50		±5	±50	mV
Output/Hysteresis Difference		**R_{OUT}, R_{HYST} = 1MΩ**		**±0.1**			±1		mV

Note 1: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Dual Over/Under Voltage Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ..... -0.3V to +12V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) ..... -0.3V to +12V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) ..... +0.3V to -12V
Input Voltages SET1 and SET2
(Note 2) ..... (GND - 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current
OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... -25mA

Power Dissipation (Note 1) 200mW
Operating Temperature Range
ICL7665BCPA ..... 0°C to +70°C
ICL7665BCTV ..... 0°C to +70°C
ICL7665BCSO ..... 0°C to +70°C
ICL7665BC/D ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature
(Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, ICL7665B

(V^+ = 5V, T_A = +25°C, test circuit unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C 0 ≤ T_A ≤ +70°C	1.6 1.8		10 10	V
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit V^+ = 2V V^+ = 9V		2.5 2.6	10 10	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			±200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10 -10	200 -100	nA
	I_{OLK} I_{HLK}	V^+ = 9V, T_A = 70°C V^+ = 9V, T_A = 70°C			2000 -500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 9V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2 0.1 0.06	0.5 0.3 0.25	V
	V_{HYST1} V_{HYST1} V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = -0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = -0.5mA V^+ = 9V, V_{SET1} = 2V, I_{HYST1} = -0.5mA		-0.15 -0.05 -0.02	-0.3 -0.15 -0.15	
	V_{OUT2} V_{OUT2} V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 9V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.3	
	V_{HYST2} V_{HYST2} V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = -0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = -0.5mA V^+ = 9V, V_{SET2} = 2V, I_{HYST2} = -0.5mA		-0.25 -0.43 -0.35	-0.8 -1 -1	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±1		

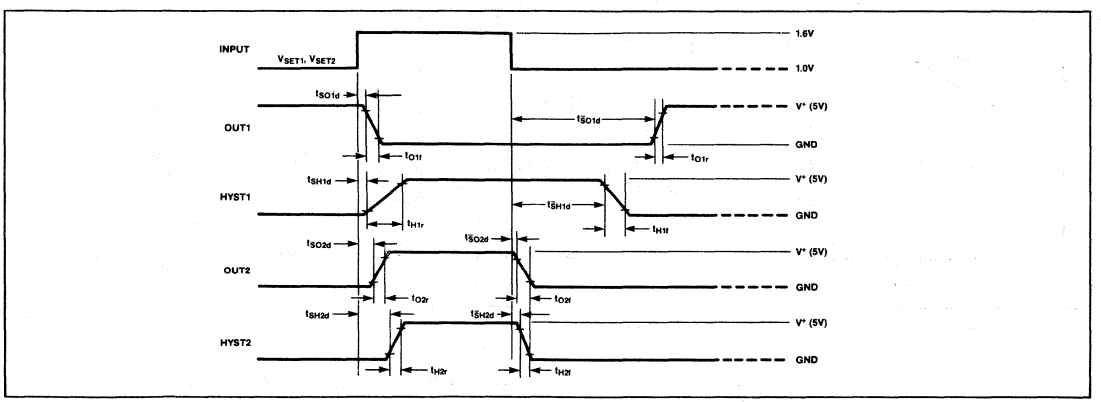
Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

AC OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Delay Times Input Going HI	t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	V_{SET} Switched from 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		85 90 55 55		µs
Input Going LO	$t_{\overline{S}O1d}$ $t_{\overline{S}H1d}$ $t_{\overline{S}O2d}$ $t_{\overline{S}H2d}$	V_{SET} Switched from 1.6V to 1.0V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		75 80 60 60		µs
Output Rise Times	t_{O1r} t_{O2r} t_{H1r} t_{H2r}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		0.6 0.8 7.5 0.7		µs
Output Fall Times	t_{O1f} t_{O2f} t_{H1f} t_{H2f}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		0.6 0.7 4 1.8		µs

Switching Waveforms



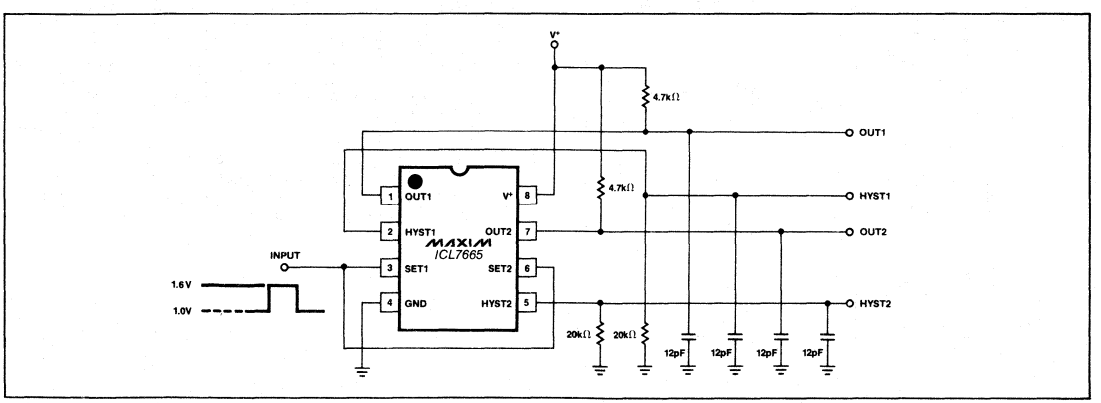
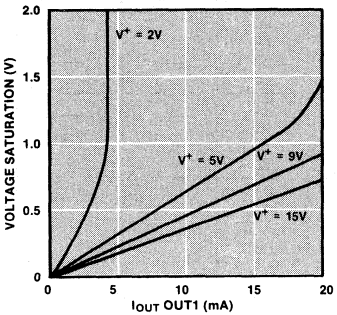


Figure 1. Maxim ICL7665 Test Circuit

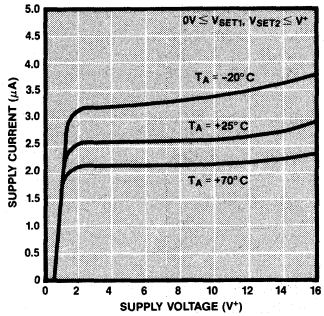
Dual Over/Under Voltage Detector

Typical Operating Characteristics

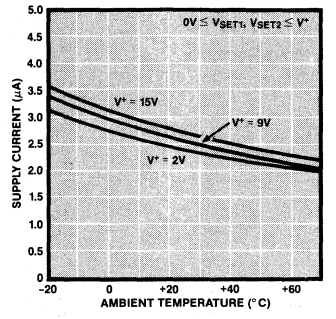
OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



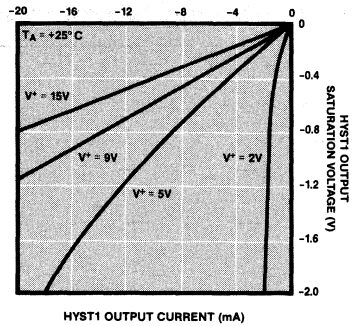
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



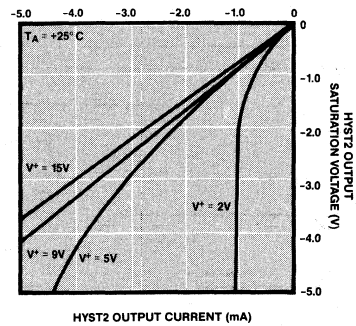
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



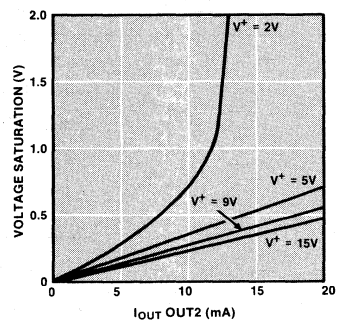
HYST1 OUTPUT SATURATION VOLTAGE vs HYST1 OUTPUT CURRENT



HYST2 OUTPUT SATURATION VOLTAGE vs HYST2 OUTPUT CURRENT



OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



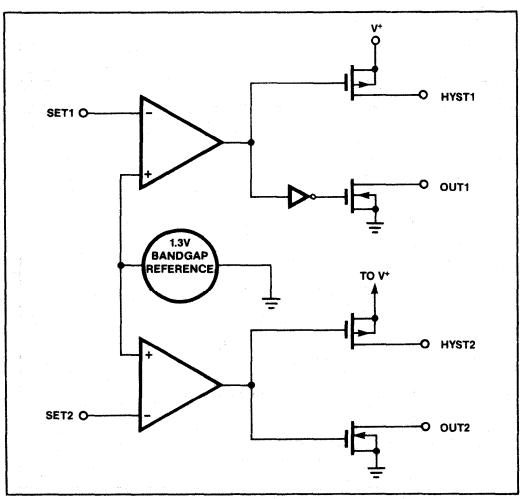


Figure 2. Block Diagram

Table I: ICL7665 TRUTH TABLE

INPUT*	OUTPUT	HYSTERESIS
V_{SET1} > 1.3V	OUT1 = ON = LOW	HYST1 = ON = HI
V_{SET1} < 1.3V	OUT = OFF = HI	HYST1 = OFF = LOW
V_{SET2} > 1.3V	OUT2 = OFF = HI	HYST2 = ON = HI
V_{SET2} < 1.3V	OUT2 = ON = LOW	HYST2 = OFF = LOW

OUT1 is an inverting output, all others are non-inverting.
OUT1 and OUT2 are open drain N-channel current sinks.
HYST1 and HYST2 are open drain P-channel current sources.
*See Electrical Characteristics for exact input threshold range.

Dual Over/Under Voltage Detector

Detailed Description

As shown in the block diagram of Figure 2, the Maxim ICL7665 combines a 1.3V reference with two comparators, two open drain n-channel outputs, and two open drain p-channel hysteresis outputs. The reference and comparator are very low power linear CMOS circuits, with a total operating current of 10μA maximum, 3μA typical. The n-channel outputs can sink greater than 10mA but are unable to source any current. These outputs are suitable for wired OR connections and capable of driving TTL inputs when an external pullup resistor is added.

The ICL7665 Truth Table is shown in Table I. OUT1 is an inverting output, all other outputs are non-inverting. HYST1 and HYST2 are p-channel current sources whose sources are connected to V+. OUT1 and OUT2 are n-channel current sinks with their sources connected to ground. Both OUT1 and OUT2 can drive at least one TTL load with a V_{OL} of 0.4V.

In spite of the very low operating current, the ICL7665 has a typical propagation delay of only 75μs. Since the comparator input bias current and the output leakages are very low, high impedance external resistors can be used. This design feature minimizes both the total supply current used and loading on the voltage source that is being monitored.

Basic Over/Under-Voltage Detection Circuits

Figures 3, 4, and 5 show the three basic voltage detection circuits.

The simplest circuit, depicted in Figure 3, does not have any hysteresis. The comparator trip point formulas can easily be derived by observing that the comparator changes state when the V_{SET} input is 1.3V. The external resistors are simply a voltage divider that attenuates the input signal. This ensures that the V_{SET} terminal is at 1.3V when the input voltage is at the desired comparator trip point. Since the bias current of the comparator is only a fraction of a nA the current in the voltage divider can be less than one μA without losing accuracy due to bias currents. The ICL7665A has a 2% threshold accuracy at 25°C and a typical temperature coefficient of 100 ppm/°C including comparator offset drift, eliminating the need for external potentiometers in most applications.

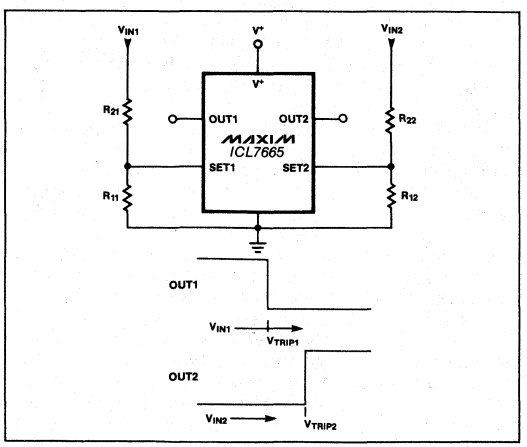


Figure 3. Simple Threshold Detector

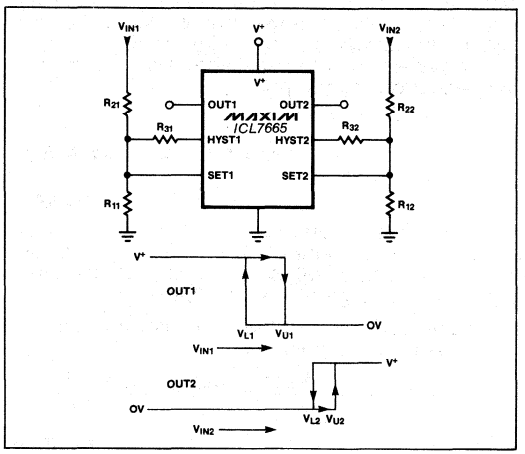


Figure 4. Threshold Detector with Hysteresis

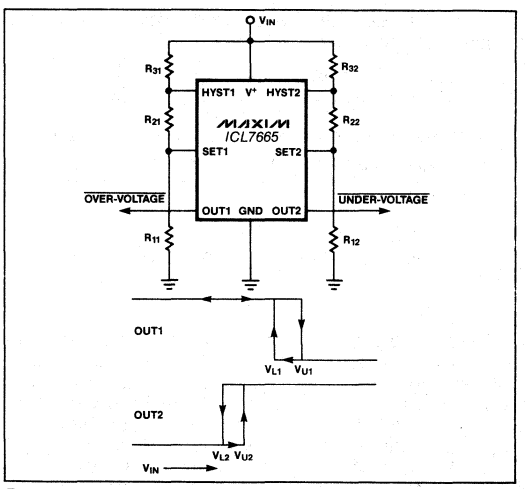


Figure 5. Threshold Detector, V_{IN} = V+

Dual Over/Under Voltage Detector

Figure 4 adds another resistor to each voltage detector. This third resistor supplies current from the HYST output whenever the V_{SET} input is above the 1.3V threshold. As the formulas show, this hysteresis resistor affects only the lower trip point. Hysteresis (defined as the difference between the upper and lower trip points) keeps noise or small variations in the input signal from repeatedly switching the output when the input signal remains near the trip point for a long period of time.

The third basic circuit (Figure 5), is suitable only when the voltage to be detected is also the power supply voltage for the ICL7665. This circuit has the advantage that all of the current flowing through the input divider resistors flows through the hysteresis resistor. This allows the use of higher value resistors without hysteresis output leakage having an appreciable effect on the trip point.

Resistor Value Calculations

Figure 3

1) First choose a value for R11. The value of R11 determines the amount of current flowing through the input divider, equal to $V_{SET}/R11$. R11 can typically be in the range of 10kΩ to 10MΩ.

2) Choose R21 based on the previously chosen R11 and the desired trip point.

$$R21 = R11 \times \frac{V_{TRIP} - V_{SET}}{V_{SET}} = R11 \times \frac{V_{TRIP} - 1.3V}{1.3V}$$

Figure 4

1) Choose a resistor value for R11. Typical values are in the 10kΩ to 10MΩ range.

2) Calculate R21 for the desired upper trip point, V_U using the formula

$$R21 = R11 \times \frac{V_U - V_{SET}}{V_{SET}} = R11 \times \frac{V_U - 1.3V}{1.3V}$$

3) Calculate R31 for the desired amount of hysteresis:

$$R31 = \frac{R21 \times (V^+ - V_{SET})}{V_U - V_L} = \frac{R21 \times (V^+ - 1.3V)}{V_U - V_L}$$

or if $V^+ = V_{IN}$:

$$R31 = \frac{R21 \times (V_L - V_{SET})}{V_U - V_L} = \frac{R21 \times (V_L - 1.3V)}{V_U - V_L}$$

4) The trip voltages are not affected by the absolute value of the resistors as long as the impedances are high enough that the resistance of R31 is much greater than the HYST output's resistance and the current through R31 is much higher than the HYST output's leakage current. Normally R31 will be in the 100kΩ to 22MΩ range. Multiplying or dividing all three resistors by the same factor will not affect the trip voltages.

Figure 5

1) First select a value for R11, usually between 10kΩ and 10MΩ.

2) Calculate R21.

$$R21 = R11 \times \frac{V_L - V_{SET}}{V_{SET}} = R11 \times \frac{V_L - 1.3V}{1.3V}$$

3) Calculate R31

$$R31 = R11 \times \frac{V_U - V_L}{V_{SET}}$$

4) As in the other circuits, all three resistor values may be scaled up or down in value without changing V_U and V_L. V_U and V_L depend only on the ratio of the three resistors if the absolute values are such that the hysteresis output resistance and the leakage currents of the V_{SET} input and hysteresis output can be ignored.

Typical Applications

Fault Monitor for a Single Supply

Figure 6 shows a typical over/under-voltage fault monitor for a single supply. In this case the upper trip points (controlling OUT1) are centered on 5.5V, with 100mV of hysteresis (V_U = 5.55V, V_L = 5.45V); and the lower trip points (controlling OUT2) are centered on 4.5V, also with 100mV of hysteresis. OUT1 and OUT2 are connected together in a wired OR configuration to generate a Power OK signal.

Multiple Supply Fault Monitor

The ICL7665 can simultaneously monitor several power supplies, as shown in Figure 7. The easiest way to calculate the resistor values is to note that when the V_{SET} input is at the trip point (1.3V), the current through R11 is 1.3V/R11. The sum of the currents through R21A, R21B and R31 must equal this current when the two input voltages are at the desired low voltage detection point. Ordinarily R21A and R21B are chosen so that the current through the two resistors is equal. Note that since the voltage at the ICL7665 V_{SET} input depends on the voltage of both supplies being monitored, there will be some interaction between the low voltage trip points for the two supplies. In this example OUT1 will go low when either supply is 10% below nominal (assuming the other supply is at the nominal voltage), or when both supplies are 5% or more below their nominal voltage. R31 sets the hysteresis, in this case, to about 43mV at the 5V supply or 170mV at the 15V supply. The second section of the ICL7665 can be used to detect overvoltage, or as shown in Figure 7, can be used to detect the absence of negative supplies. Note that the trip points for OUT2 depend on both the voltages of the negative power supplies and the actual voltage of the +5V supply.

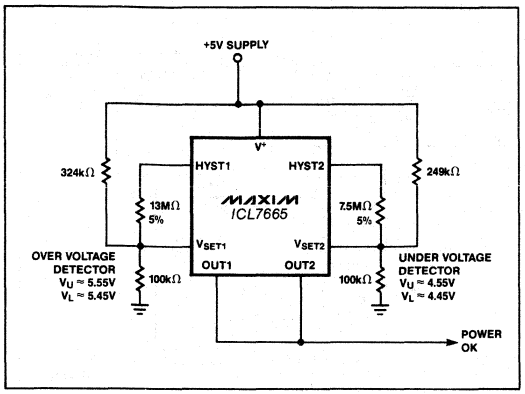


Figure 6. Fault Monitor for a Single Supply

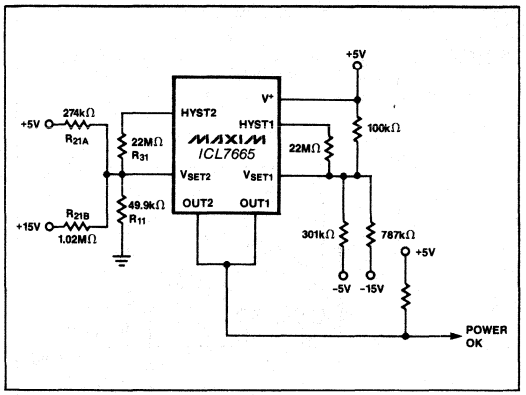


Figure 7. Multiple Supply Fault Monitor

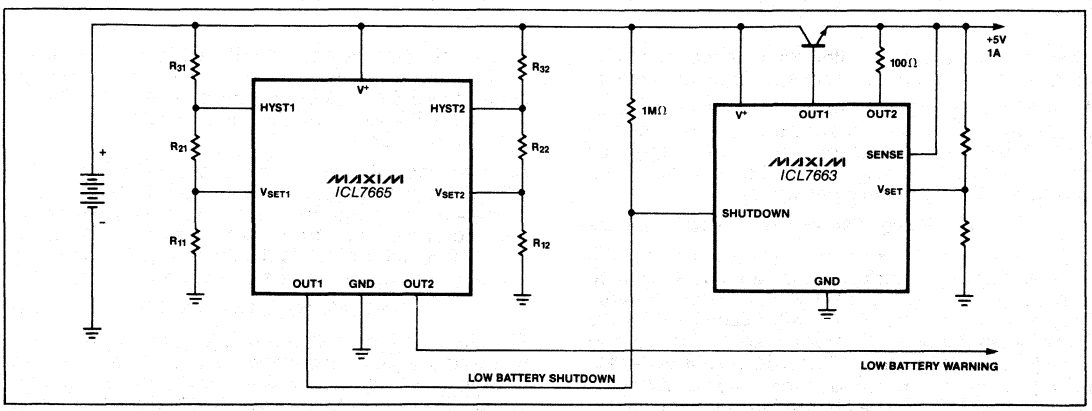


Figure 8. Low Battery Warning and Low Battery Disconnect

Combination Low Battery Warning and Low Battery Disconnect

Nickel Cadmium (NiCad) batteries are excellent rechargeable power sources for portable equipment, but care must be taken to ensure that NiCad batteries are not damaged by overdischarge. Specifically, a NiCad battery should not be discharged to the point where the polarity of lowest capacity cell is reversed and that cell is reverse charged by the higher capacity cells. This reverse charging will dramatically reduce the life of a NiCad battery. Figure 8 both prevents reverse charging and also gives a low battery warning. A typical low battery warning voltage is 1V per cell. Since a NiCad "9V" battery is ordinarily made up of 6 cells with a nominal voltage of 7.2V, a low battery warning of 6V is appropriate, with a small hysteresis of 100mV. To prevent overdischarge of a battery the load should be disconnected when the battery voltage is 1V x (N–1), where N = number of cells. In this case the low battery load disconnect should occur at 5V. Since the battery voltage will rise when the load is disconnected, 800mV of hysteresis is used to prevent repeated on-off cycling.

Power Fail Warning and Powerup/Powerdown Reset

Figure 9 illustrates a power fail warning circuit which monitors raw DC input voltage to the 7805 three terminal 5V regulator. The Power Fail warning signal goes high when the unregulated DC input falls below 8.0V. When the raw DC power source is disconnected or the AC power fails, the voltage on the input of the 7805 decays at a rate of I_{OUT}/C (in this case 200mV/ms). Since the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will give at least 3.5ms of warning before the 5V output begins to drop. If additional warning time is needed,

Dual Over/Under Voltage Detector

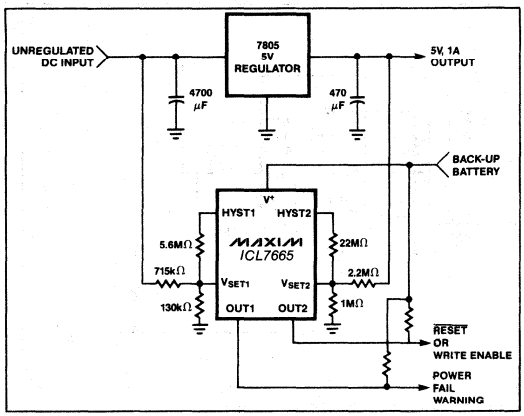


Figure 9. Power Fail Warning and Powerup/Powerdown Reset

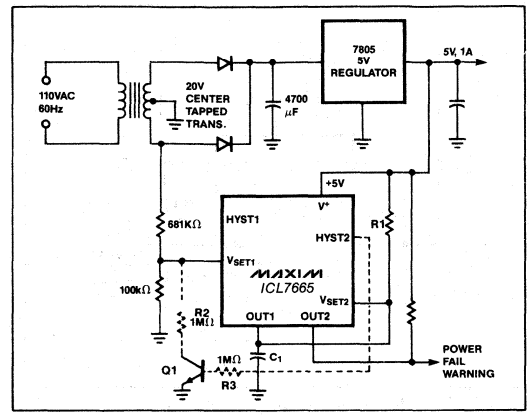


Figure 10. AC Power Fail and Brownout Detector

either the trip voltage or filter capacitance should be increased or the output current should be decreased.

The ICL7665 OUT2 is set to trip when the 5V output has decayed to 3.9V. This output can be used to prevent the microprocessor from writing spurious data to a CMOS battery backup memory, or can be used to activate a battery backup system.

AC Power Fail and Brownout Detector

By monitoring the secondary of the transformer, the circuit in Figure 10 performs the same power failure warning function as Figure 9. With a normal 110VAC input to the transformer, OUT1 will discharge C1 every 16.7ms when the peak transformer secondary voltage exceeds 10.2V. When the 110VAC power line voltage is either interrupted or reduced so that the peak voltage is less than 10.2V, C1 will be charged through R1. OUT2, the Power Fail Warning output, goes high when the voltage on C1 reaches 1.3V. The time constant R1 x C1 determines the delay time before the Power Fail Warning signal is activated, in this case 42ms or 2½ line cycles. Optional components R2, R3 and Q1 add hysteresis by increasing the peak secondary voltage required to discharge C1 once the Power Fail Warning is active.

Battery Switchover Circuit

The circuit in Figure 11 performs two functions: switching the power supply of a CMOS memory to a backup battery when the line-powered supply is turned off, and lighting a low-battery-warning LED when the backup battery is nearly discharged. The PNP transistor, Q1, connects the line-powered +5V to the CMOS memory whenever the line-powered +5V supply voltage is greater than 3.5V. The voltage drop across Q1 will only be a couple of hundred mV since it will be saturated. Whenever the input voltage falls below 3.5V. OUT1 goes high, turns off Q1 and connects the 3V lithium cell to the CMOS memory. The second voltage detector of the ICL7665 monitors the voltage of the lithium cell. If the battery voltage falls below 2.6V, OUT2 goes low and the low-battery-warning LED turns on (assuming that the +5V is present, of course).

Another possible use for the second section of the ICL7665 is the detection of the input voltage falling below 4.5V. This signal could then be used to prevent the microprocessor from writing spurious data to the CMOS memory while its power supply voltage is outside its guaranteed operating range.

Simple High/Low Temperature Alarm

The circuit in Figure 12 is a simple high/low temperature alarm which uses a low cost NPN transistor as the sensor and an ICL7665 as the high/low detector. The NPN transistor and potentiometer R1 form a Vbe multiplier whose output voltage is determined by the Vbe of the transistor and the position of R1's wiper arm. The voltage at the top of R1 will have a temperature coefficient of approximately -5mV/°C. R1 is set so that the voltage at V_{SET2} is equal to the V_{SET2} trip voltage when the temperature of the NPN transistor reaches the temperature selected for the high temperature alarm desired. R2 can be adjusted so that the voltage at V_{SET1} is 1.3V when the NPN transistor's temperature reaches the low temperature limit.

SCR Latchup

Like all junction isolated CMOS circuits, the ICL7665 has an inherent 4 layer or SCR structure that can be triggered into destructive latchup under certain conditions. Avoid destructive latchup by following these precautions:

1) If either V_{SET} terminal can be driven to a voltage greater than V^+ or less than ground, limit the input current to 500µA maximum. Usually an input voltage

divider resistance can be chosen to ensure the input current remains below 500μA, even when the input voltage is applied before the ICL7665 V+ supply is connected.

2) Limit the rate-of-rise of V+ by using a bypass capacitor near the ICL7665. Rate-of-rise SCRs rarely occur unless: a) the battery has a low impedance — as is the case with NiCad and lead acid batteries; b) the battery is connected directly to the ICL7665 or is switched on via a mechanical switch with low resistance and c) there is little or no input filter capacitance near the ICL7665. In line-powered systems the rate-of-rise is usually limited by other factors and will not cause a rate-of-rise SCR action under normal circumstances.

3) Limit the maximum supply voltage (including transient spikes) to 18V. Likewise limit the maximum voltage on OUT1 and OUT2 to +18V and the maximum voltage on HYST1 and HYST2 to 18V below V+.

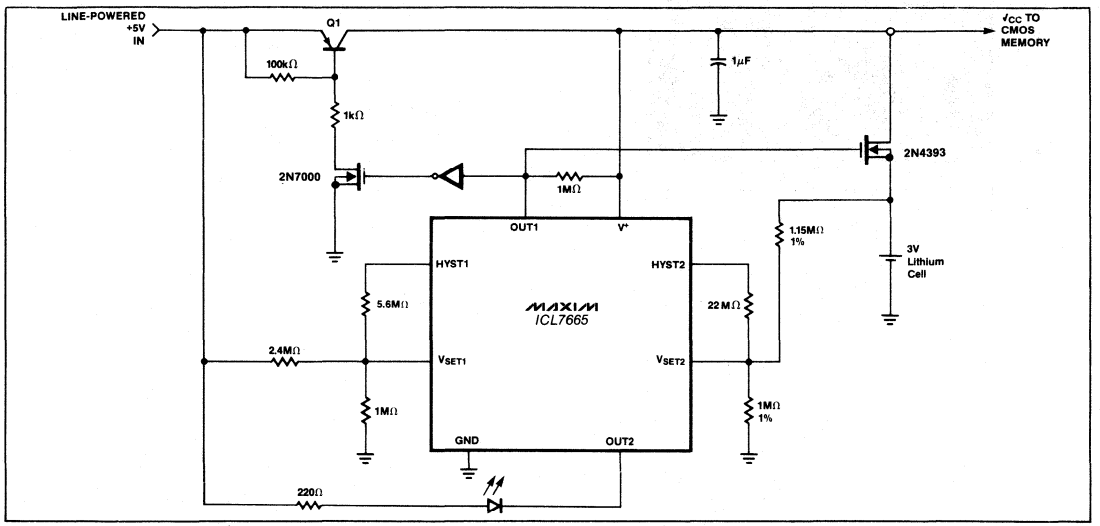


Figure 11. Battery Switchover Circuit

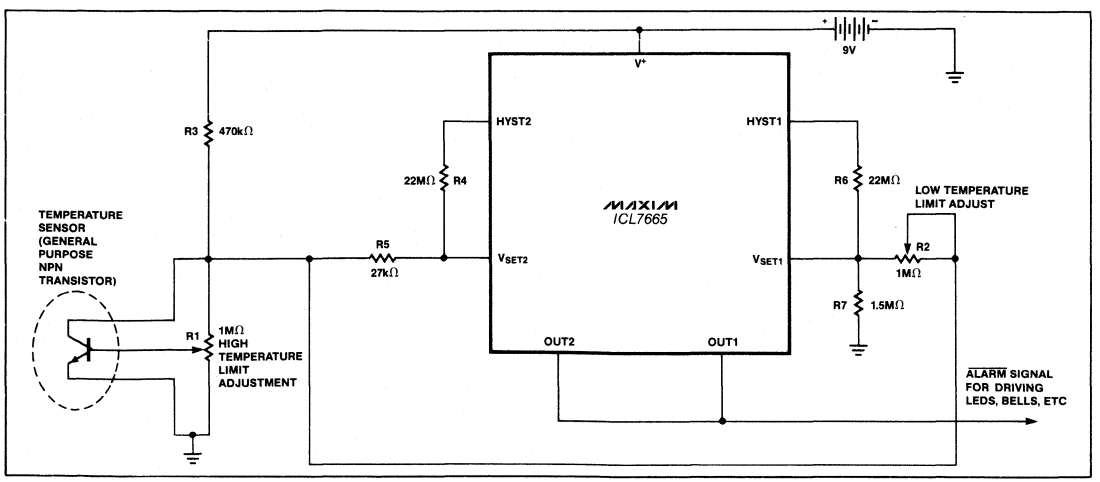
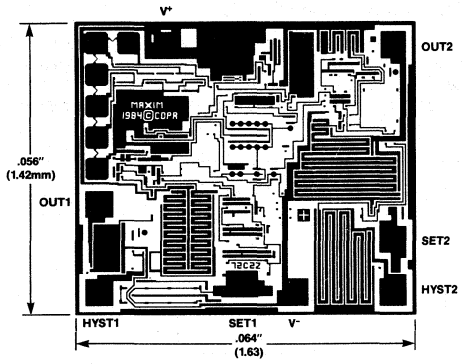


Figure 12. Simple High/Low Temperature Alarm

Dual Over/Under Voltage Detector

Chip Topography



Display Drivers/Counters

LCD and LED Display Drivers

Part Number	Input Formula	Display Formats	4-Digit	8-Digit	10-Digit	4-Char	5-Char	LCD	LED	Page No.
MAX7231	6-bit Parallel	Hex, BCD, or Code B, plus 16 annunciators		X				X		7-1
MAX7232	Bit Serial	Hex, BCD, or Code B, plus 20 annunciators			X			X		7-1
MAX7233	6-bit Parallel	Upper Case ASCII				X		X		7-1
MAX7234	Bit Serial	Upper Case ASCII					X	X		7-1
ICM7211	µP and Muxed 4-bit	Hex, BCD and Code B	X					X		7-17
ICM7212	µP and Muxed 4-bit	Hex, BCD and Code B	X						X	7-17
ICM7218/ ICM7228	8-bit Parallel	Hex, BCD, Code B, plus No Decode		X					X	7-41

Counters and Timers

Part Number	Description	Maximum Count	Output	Speed (MHz max)	Supply Voltage	Supply Current	Features	Page No.
ICM7217	4 Digit Up/Down	9999	C.A. LED	2	4.5V to 5.5V	350mA typ	Equals and Zero outputs, counter preset and pre-determining register set by thumb-wheel switches	7-33
ICM7217A	4 Digit Up/Down	9999	C.C. LED	2	4.5V to 5.5V	100mA typ		7-33
ICM7217B	4 Digit Up/Down	5959	C.A. LED	2	4.5V to 5.5V	200mA typ		7-33
ICM7217C	4 Digit Up/Down	5959	C.C. LED	2	4.5V to 5.5V	100mA typ		7-33
ICM7224	4-1/2 Digit	19,999	LCD	15	3V to 6V	25µA max		7-53
ICM7225	4-1/2 Digit	19,999	C.A. LED	15	3V to 6V	25µA max		7-53
ICM7240	8 Bit Binary	1-255	open drain	15	2V to 16V	500µA max	RC oscillator or ext. clock	8-1
ICM7242	Fixed 8 Bit	128/256	CMOS	15	2V to 16V	500µA max	Programmable Time outs	8-1
ICM7250	2 Digit BCD	1-99	open drain	15	2V to 16V	500µA max	RC oscillator or ext. clock	8-1
ICM7260	2 Digit Timer	1-59	open drain	15	2V to 16V	500µA max	RC oscillator or ext. clock	8-1
ICM7555	CMOS 555 Timer		CMOS	0.5	2V to 16.5V	250µA max		8-9
ICM7556	CMOS 556 Timer		CMOS	0.5	2V to 16.5V	500µA max		8-9
MM74C945	4 Digit Up/Down	9,999	LCD	3	3V to 6V	60µA max		7-61
MM74C947	4 Digit Up/Down	9,999	LCD	3	3V to 6V	60µA max		7-61

NOTE:
C.A. LED = Common Anode LED Display
C.C. LED = Common Cathode LED Display

MAXIM

Triplexed LCD Decoder/Drivers

General Description

The MAX7231/32/33/34 family of integrated circuits is a complete line of triplexed liquid crystal display (LCD) drivers. These devices interface microprocessors (or digital systems) to multiplexed numeric and alphanumeric displays. The MAX7231 drives 8 digits and accepts data in a parallel format. The MAX7232 drives 10 digits and accepts data in a serial format. Both devices feature two independent annunciators per digit. The MAX7233 drives 4 alphanumeric 18 segment characters. The MAX7234 drives 5 alphanumeric 18 segment characters.

Each device includes an input buffer, digit address decoding circuitry and mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of each digit. This offloads the microprocessor system, reducing the ROM space and CPU time needed to service a display.

Applications

These low-power LCD drivers are ideal for microprocessor-based portable applications where power consumption is a primary concern. Many applications also take advantage of the annunciator drive capability, which allows unlimited variations of display layout.

Portable instrumentation
Industrial equipment
Telecommunications
Medical equipment
Panel Meters
Machine control

Features

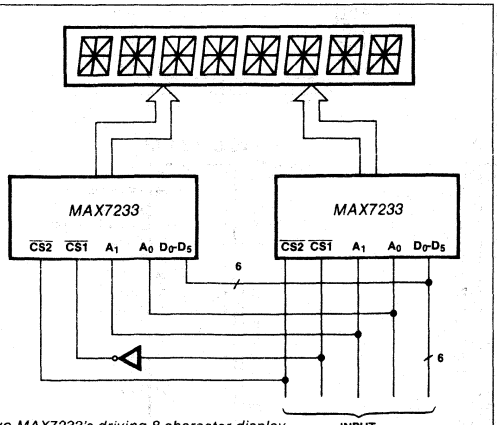
- **MAX7231 drives 8 digits/7 segments; parallel input format; 2 annunciators per digit**
- **MAX7232 drives 10 digits/7 segments; serial input format; 2 annunciators per digit**
- **MAX7233 drives 4 alphanumeric characters/ 18 segments; parallel input format**
- **MAX7234 drives 5 alphanumeric characters/ 18 segments; serial input format**
- **On-chip oscillator**
- **Direct interface to microprocessors**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX7231AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7231BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7231CFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232CFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7233AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7233BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7234AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7234BFIPL	-20°C to +85°C	40 Lead Plastic DIP

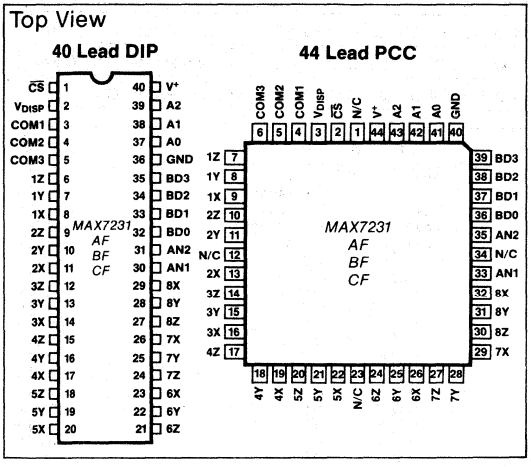
Ordering information continued on next page

Typical Operating Circuit



Two MAX7233's driving 8 character display (Detailed Circuit Diagram — Figure 21)

Pin Configuration



Triplexed LCD Decoder/Drivers

OPTION TABLE

DEVICE	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
MAX7231AF	Hexdecimal	Both Annunicators on COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
MAX7231BF	Code B			
MAX7231CF	Code B	1 Annunciator COM1 1 Annunciator COM3		
MAX7232AF	Hexadecimal	Both Annunciators on COM3	Serial Entry 4 bit Data 2 Bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
MAX7232BF	Code B			
MAX7232CF	Code B	1 Annunciator COM1 1 Annunciator COM3		
MAX7233AF	64 Character (ASCII) 18 Segment (Half width numbers)	No independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
MAX7233BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
MAX7234AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters
MAX7234BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

Ordering Information

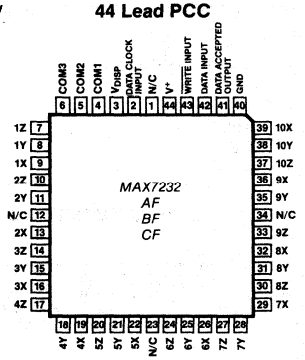
(Continued from front page)

PART	TEMP. RANGE	PACKAGE
MAX7231AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7231BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7231CFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232CFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7233AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7233BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7234AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7234BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier

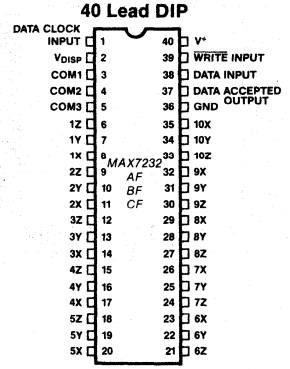
Pin Configuration

Top View

44 Lead PCC



40 Lead DIP



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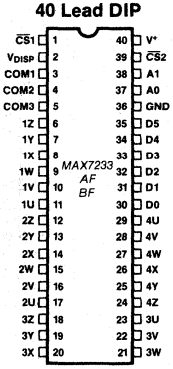

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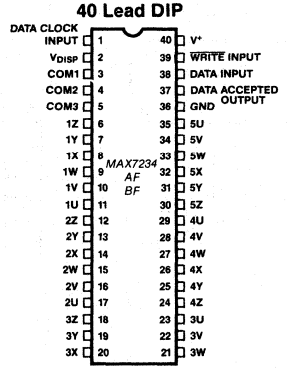

Continued on last page of data sheet.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 85°C
Supply Voltage (V^+) 6.5V
Input Voltage (Note 2) ..... $-0.3V \le V_{IN} \le 6.5V$
Display Voltage (Note 2) ..... $-0.3V$ to $V^+ + 0.3V$
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Soldering Temperature (10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not limited. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = +5V \pm 10\%$, $T_A = -20°C$ to +85°C unless noted)

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Power Supply Voltage	V^+		4.5		5.5	V
Data Retention Supply Voltage	V^+	Guaranteed Retention at 2V	2	1.6		V
Logic Supply Current	I^+	Current from V^+ to Ground excluding Display, $V_{DISP} = 2V$		30	100	µA
Shutdown Total Current	I_S	V_{DISP} Pin 2 Open, $T_A = +25°C$		1	10	µA
Display Voltage Range	V_{DISP}	Ground $\le V_{DISP} \le V^+$	0		V^+	V
Display Voltage Setup Current	I_{DISP}	$V_{DISP} = (V^+ - 3V)$, Current from V^+ to V_{DISP} On-Chip (Note 3), $T_A = +25°C$		15	25	µA
Display Voltage Setup Resistor Value	R_{DISP}	One of Three Identical Resistors in String (Note 3), $T_A = +25°C$	40	75		kΩ
DC Component of Display Signals		Sample Test only, $V_{DISP} = 0V$		1/4	1	% (V^+-V_{DISP})
Display Frame Rate	f_{DISP}	See Figure 2, $T_A = +25°C$	60	90	120	Hz
Input Low Level (Note 3)	V_{IL}	MAX7231, MAX7233 / MAX7232, MAX7234			0.8	V
Input High Level (Note 3)	V_{IH}	Pins 1, 30-35, 37-39 / Pins 1, 38, 39	2.0			V
Input Leakage	I_{ILK}	MAX7231, MAX7233 / MAX7232, MAX7234		0.1	1	µA
Input Capacitance	C_{IN}	Pins 1, 30-35, 37-39 / Pins 1, 38, 39		5		pF
Output Low Level	V_{OL}	Pin 37, MAX7232, MAX7234, $I_{OL} = 1mA$,			0.4	V
Output High Level	V_{OH}	$V^+ = 4.5V$, $I_{OH} = -500µA$	4.1			V

AC CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$, 0-3V INPUT SWINGS **PARALLEL INPUT (MAX7231, MAX7233) See Figure 5**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Chip Select Pulse Width	t_{cs}		500	350		ns
Address/Data Setup Time	t_{ds}		350			ns
Address/Data Hold Time	t_{dh}		0	-20		ns
Inter-Chip Select Time	t_{ics}		3.5			µs

AC CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$, 0-3V INPUT SWINGS **SERIAL INPUT (MAX7232, MAX7234) See Figures 6, 7, 8**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Data Clock Low Time	t_{cl}		350			ns
Data Clock Period	t_{cl}		1			µs
Data Setup Time	t_{ds}		350			ns
Data Hold Time	t_{dh}		0	-20		ns
Write Pulse Width	t_{wp}		500	350		ns
Write Pulse to Clock at Initialization	t_{wll}		4.0			µs
Data Accepted Low Output Delay	t_{odl}				1	µs
Data Accepted High Output Delay	t_{odh}			1.5	3	µs
Write Delay After Last Clock	t_{cws}		350			ns

Note 1: This limit refers to that of the package and will not be obtained during normal operation.
Note 2: Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above V^+ but not more than 6.5 volts above GND.
Note 3: $V^+ = 5V$, $T_A = +25°C$.

Triplexed LCD Decoder/Drivers

TERMINAL DEFINITIONS

MAX7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF — See Table 1
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant Most Significant } 4 Bit Binary Data Inputs	Input Data (See Table 2) — HIGH = Logical One (1), LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant Most Significant } 3 Bit Digit Address Inputs	Input Address (See Table 4)
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit

Note 3: CS has a special "mid-level" sense circuit that establishes a test mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, and driving it with fast rise and fall times.

MAX7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant Most Significant } 6 Bit (ASCII) Data Inputs	Input Data (See Table 3) — HIGH = Logical One (1), LOW = Logical Zero (0)
A0 A1	37 3	Least Significant Most Significant } Address Inputs	Input Add. (See Table 5)
$\overline{CS1}$ $\overline{CS2}$	39 1	Chip Select Inputs (Note 3)	Both Inputs LOW, load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.

MAX7232 and MAX7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic is reset. When DATA ACCEPTED Output is HIGH, positive going edge of WRITE triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. MAX7232: Eleventh edge resets shift register and control logic. MAX7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; MAX7232: 8, 9 or 10 bits. MAX7234: 9 bits.

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V^+) chip is shutdown; oscillator stops, all display pins to V^+.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6-29 6-35	(On MAX7231/33) (On MAX7232/34)	Drive display segments, or columns.
V^+	40	Positive Supply	
GND	36	Ground	

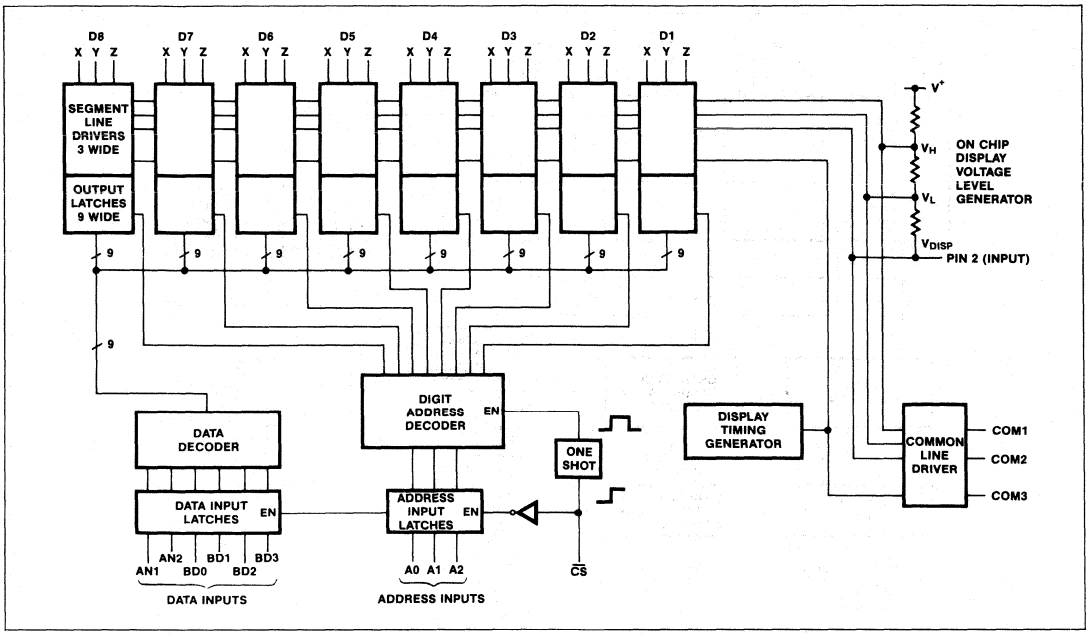

Figure 1. Block Diagram of MAX7231.

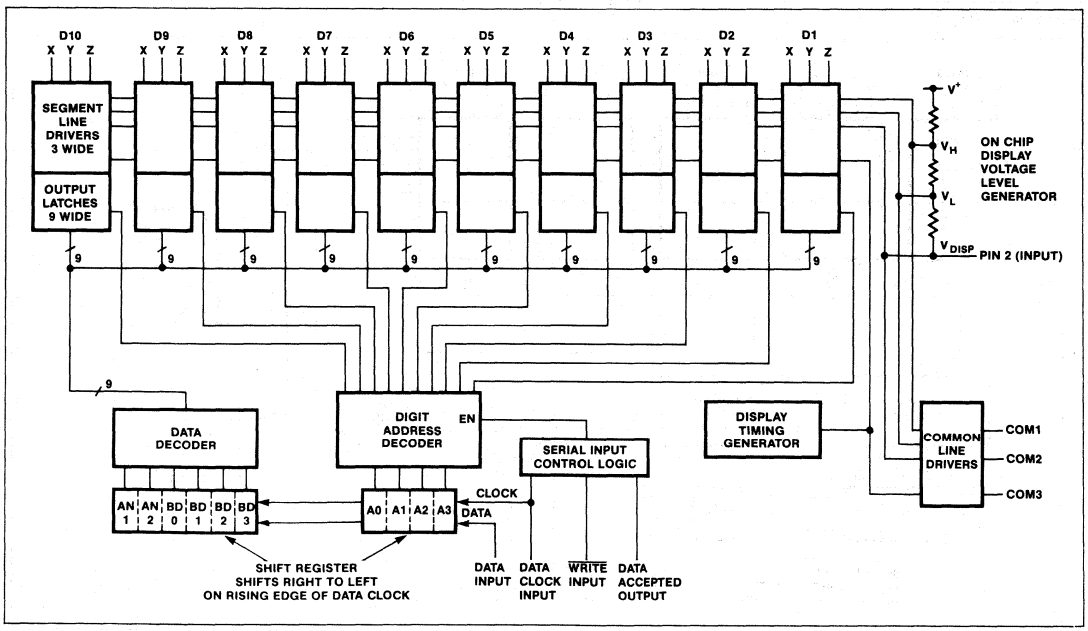

Figure 2. Block Diagram of MAX7232

7

Triplexed LCD Decoder/Drivers

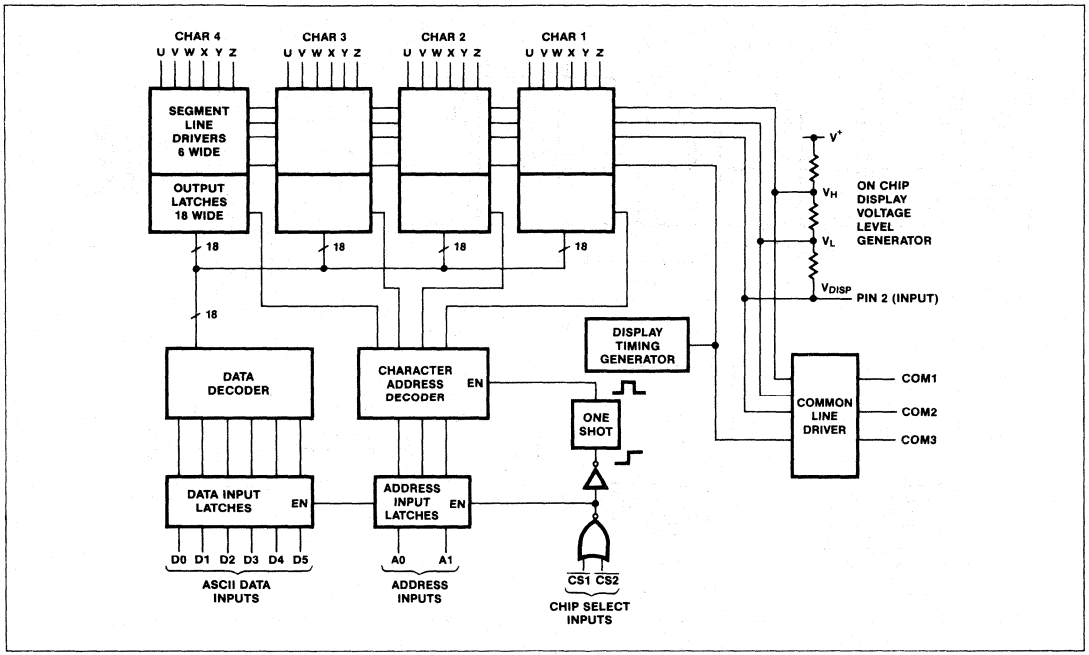

Figure 3. Block Diagram of MAX7233

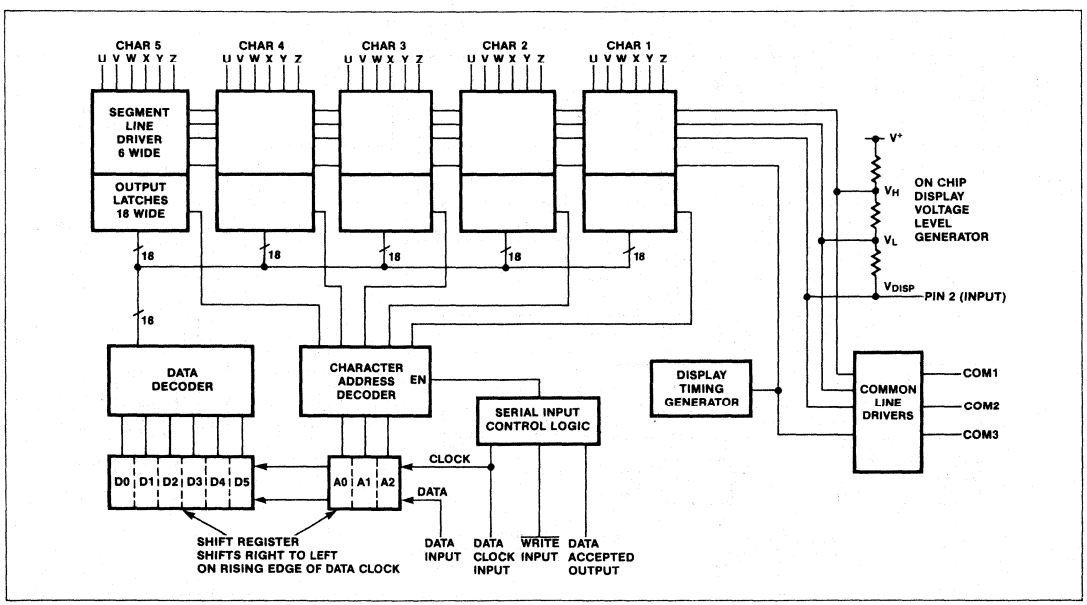

Figure 4. Block Diagram of MAX7234

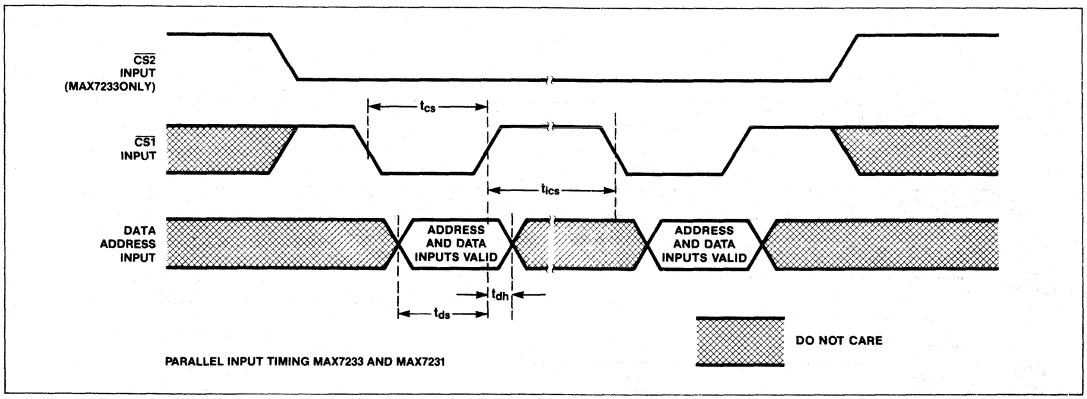

Figure 5. Parallel Input Timing

Detailed Description

Parallel Input Interface

The MAX7231 and MAX7233 have a parallel interface allowing direct parallel connection to microprocessors. The address and data bits are latched on the positive going edge of the Chip Select. The positive going edge of Chip Select also triggers an internal monostable that enables the address decoder and latches the decoded data into the digit/character output latches.

Figure 5 shows the timing requirements for the parallel input devices (7231 and 7233). To ensure that the new data does not appear at the decoder inputs before the previous decoded data is written to the outputs, there is a minimum time required between CHIP SELECT pulses.

Serial Input Interface

A $\overline{\text{WRITE}}$ pulse while Data Accepted Output is high will reset the serial input control logic, but will not latch any data. A $\overline{\text{WRITE}}$ pulse while Data Accepted Output is low will cause the MAX7232 and MAX7234 to decode the data, latch the data into the output latches and then reset the serial input control logic.

This assures that each data bit will be entered into the correct position in the shift register, depending on the subsequent data clock inputs. The MAX7232's Data Accepted Output goes low after 8 Data Clock pulses, whereas the MAX7234's Data Accepted Output goes low after 9 Data Clock Inpulses. Further Data Clock pulses occuring before a $\overline{\text{WRITE}}$ pulse will cause the Data Accepted Output to go high after 11 Data Clock pulses in the MAX7232 and the 10 Data Clock pulses in the MAX7234. In both cases, the serial input control logic is also reset when Data Accepted goes high.

The serial input timing diagram shown in Figure 6 illustrates the recommended procedure for entering data.

Note that the eleventh clock resets the shift register and control logic for the MAX7232, but the Data Accepted Output goes low after the eighth clock. As Figure 7 illustrates, this allows the user to reduce the data to eight bits. The MAX7232 then writes to the 7 segment display, but leaves the annunciators off. Nine Bits are clocked in if only AN2 is turned on.

The control logic of the MAX7234 is similar to the MAX7232, but nine bits are always required. As illustrated in Figure 8, the data bits are only latched if the $\overline{\text{WRITE}}$ input occurs after the ninth data bit has been entered and Data Accepted Output is low.

Triplexed LCD Decoder/Drivers

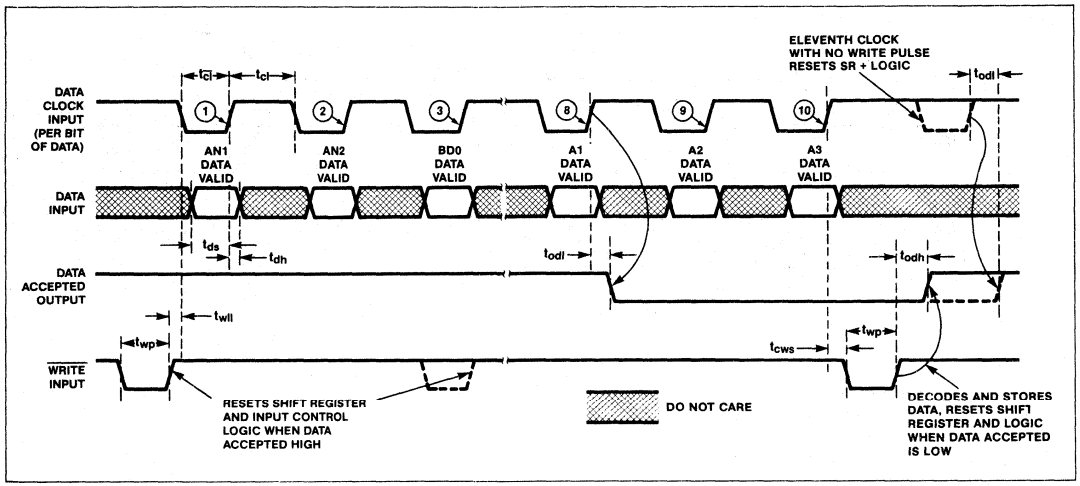

Figure 6. One Digit Timing Diagram for the MAX7232, Writing Both Annunciators.

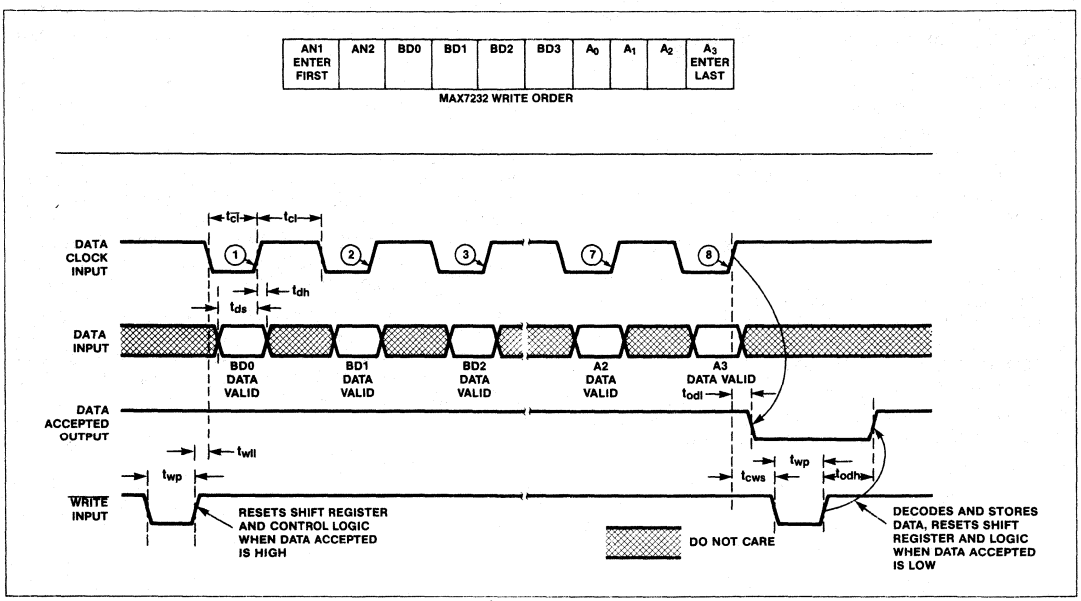

Figure 7. Input Timing Diagram of the MAX7232. Both Annunciators OFF.

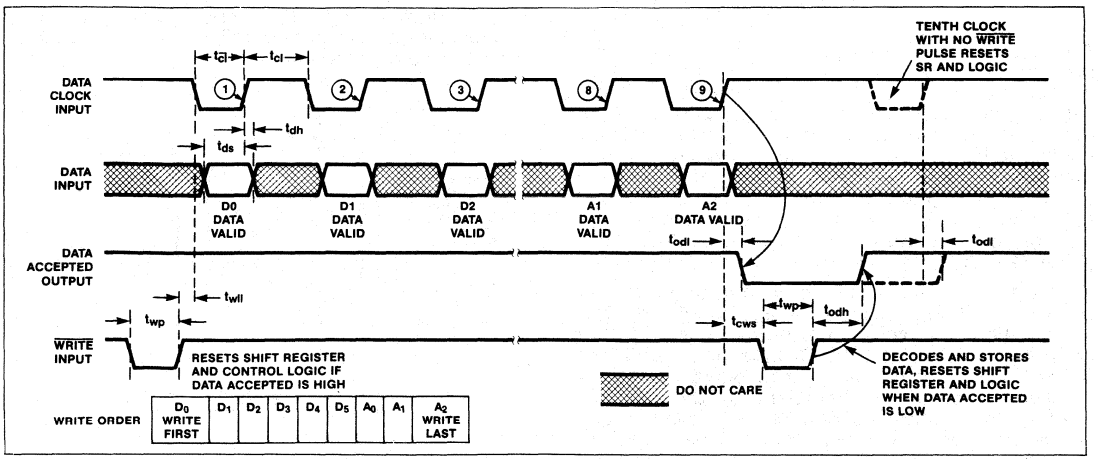

Figure 8. One Character Input Timing Diagram of the MAX7234.

Temperature Compensation

Temperature Effects

Temperature affects the performance of liquid crystal displays (LCD's) in two ways. As the display temperature drops, the response time of the display becomes longer. At very low temperatures, some displays may take several seconds to change to a new character. However, high-speed liquid crystal materials are available for low temperature environments.

Temperature has a significant effect on the variation of liquid crystal threshold voltage. The peak voltage (V_P) required to turn on the display has a temperature coefficient of -7 to -14 mV/°C for typical liquid crystal materials used in multiplexed LCD's. This means that as the temperature increases, the threshold voltage decreases. Figure 9 illustrates the dependence of peak voltage (V_P) on temperature for the same liquid crystal material described in Figure 10. Assuming a fixed value for V_P, OFF segments begin to be visible when the threshold voltage drops below $V_P/3$. To avoid this problem at high temperature, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This is appropriate where display temperatures do not vary widely.

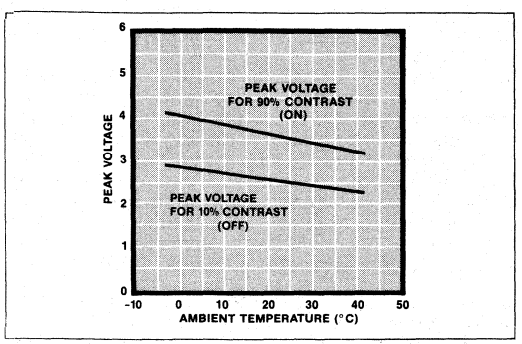

Figure 9. Temperature Dependence of Liquid Crystal Threshold.

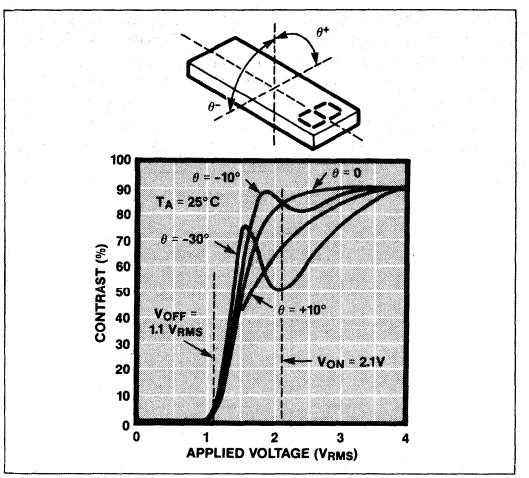

Figure 10. Applied RMS Voltage vs. Contrast.

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Triplexed LCD Decoder/Drivers

Display Voltage

An internal resistor string of three equal value resistors is used to generate the display drive voltages. One end of the string is available at Pin 2 (V_{DISP}) and the other end is connected to V^+ on the chip. Pin 2, the user's input, allows the display voltage to be optimized for a particular liquid crystal material. Note that V_P should be three times the threshold voltage for the liquid crystal material used ($V_P = V^+ - V_{DISP}$). To avoid device latchup and possible destruction of the chip, never drive Pin 2 below Ground or above V^+.

Figure 11 illustrates a simple method of generating a display voltage suitable for a particular display. A potentiometer with a maximum value of 200kΩ connected from Pin 2 to Ground gives sufficient range adjustment to suit most displays. Due to the positive temperature coefficient of the resistors on-chip, this method for generating display voltage should be used only in applications where the temperature variation of the chip and display will not vary more than ±5°C (15°F). The power supply voltage also effects the display voltage.

The chip may be operated at the display voltage with V_{DISP} connected to Ground in battery powered applications where the display voltage is the same as the battery voltage (typically 3 to 4.5 volts). The inputs of the chip are designed such that they may be driven above V^+ without damage. This allows the chip and display to operate at a regulated 3V while its inputs are driven by a microprocessor that is operating at a less well controlled 5V supply. Under no circumstances should the inputs be driven more than 6.5V above Ground. Independent adjustment of both voltage and temperature compensation is illustrated in Figure 12. Temperature compensation is performed by the ICL7663.

Another method of setting up a display voltage is illustrated in Figure 13. The five diodes (1N914 or equivalent), each have a forward drop of approximately 0.65V, with 20 (μA) at room temperature. This configuration is suitable for the 3V display using the material properties as shown in Figures 9 and 10. More diodes may be added for higher voltage displays. Each diode has a negative temperature coefficient of -2mV/°C (5 in series gives -10mV/°C). Consequently, this circuit will provide reasonable temperature compensation.

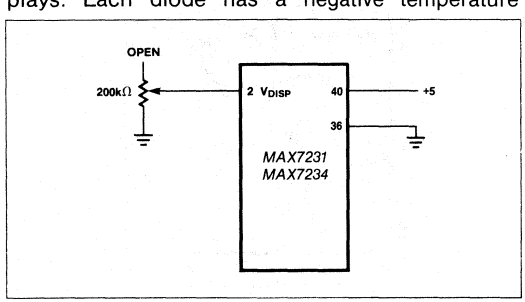

Figure 11. Simple Display Voltage Adjustment.

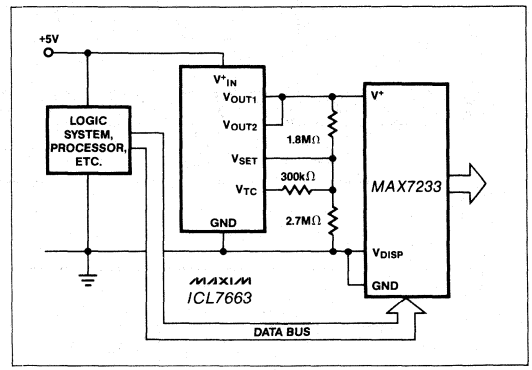

Figure 12. Flexible Temperature Compensation.

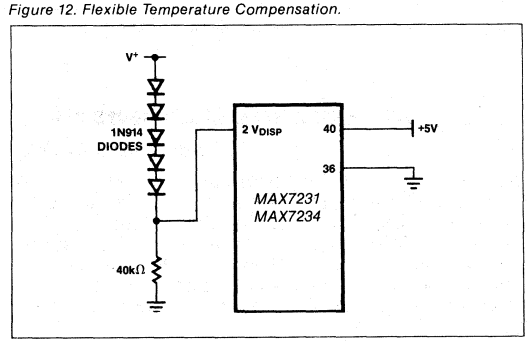

Figure 13. Diode String VDISP Generator.

Triplexing

The connection diagram for a typical 7-segment display font with 2 annunciators is illustrated in Figure 15. The MAX7231 and MAX7232 (A and B suffix versions) numeric display drivers use this configuration. The voltage waveforms of the common lines and one segment line are illustrated in Figure 14. The "Y" segment line has been chosen as an example. This line intersects with COM1 to form the "A" segment, COM2 to form the "G" segment, and COM3 to form the "D" segment. Four different ON/OFF combinations of the "A", "G" and "D" segments and their corresponding waveforms of the "Y" segment line are illustrated in Figure 14. The schematic diagram in Figure 16 shows that each intersection acts as a capacitance from segment line to common line. Figure 17 illustrates the voltage across the "G" segment for the same four combinations of ON/OFF segments shown in Figure 14.

The RMS voltage across the segment determines the degree of polarization for the liquid crystal material and thus the contrast of the segment. The

RMS OFF voltage is always $V_P/3$, whereas the RMS ON voltage is always 1.92 $V_P/3$. This is illustrated in Figure 17. The ratio of RMS ON to OFF voltage is fixed at 1.92 for a triplexed liquid crystal display.

Contrast vs. applied RMS voltage is shown in Figure 10. With a V_P of 3.1V, the RMS ON voltage is 2.1V and the RMS OFF voltage is 1.1V. The OFF segment will have a contrast of less than 5%, while the ON segments will have greater than 85% contrast.

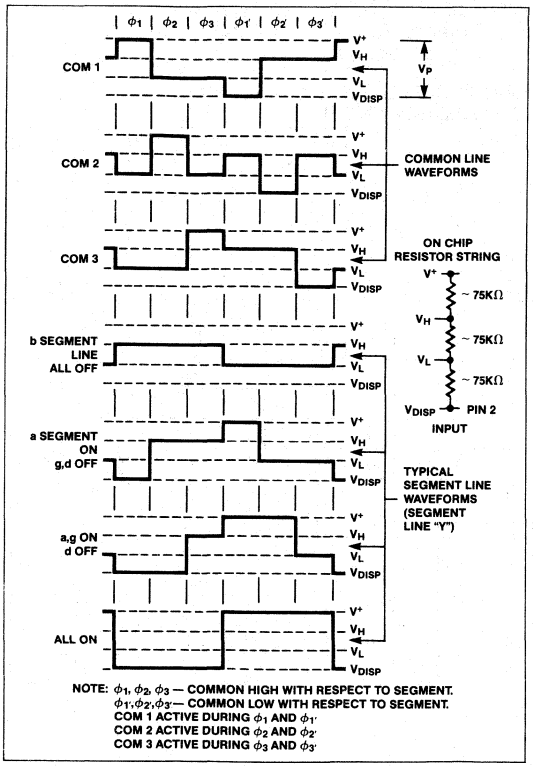

Figure 14. Display Voltage Waveforms.

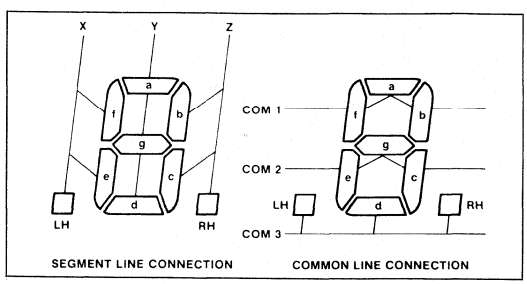

Figure 15. Connection Diagrams for Typical 7-Segment Displays.

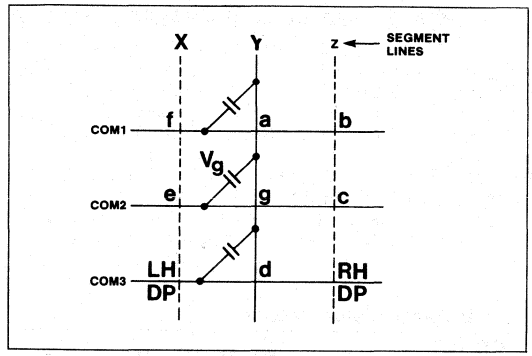

Figure 16. Schematic of Display.

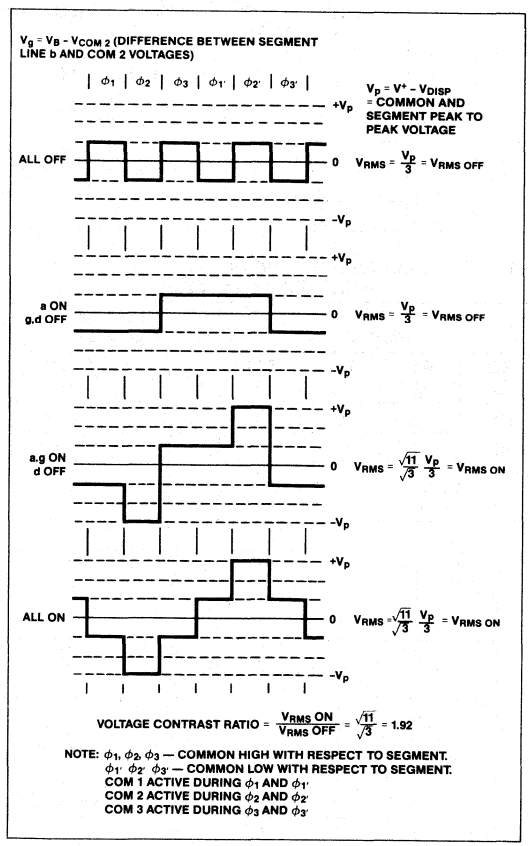

Figure 17. Voltage Waveforms on Segment g (Vg).

Triplexed LCD Decoder/Drivers

Output Codes and Display Fonts

The MAX7231 and MAX7232 numeric display drivers are programmed to drive 7-segment displays plus 2 annunciators per digit. Refer to Table 1 for annunciator input controls. The display connections for one digit are shown in Figure 18. Both annunciators are placed on COM3 on the "A" and "B" suffix devices. The "A" devices offer a "hexadecimal" 7-segment output, while the "B" devices offer "Code B" outputs. This is illustrated in Table 2. Figure 19 illustrates the "C" device configuration. The Left hand annunciator is placed on COM1 (AN2) and the right hand annunciator (usually a decimal point) is placed on COM3 (AN1). Only a "Code B" output is offered for the "C" devices.

Both the MAX7233 and MAX7234 are supplied in "A" and "B" versions, decoding an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and 2 "dots". Figure 20 illustrates the layout for a single character. The "A" devices have numbers which are half-width and the "B" devices have full-width numbers. Refer to Table 3 for output decoding.

Table 1: Annunciator Decoding

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	MAX7231 A/B MAX7232 A/B BOTH ANNUNCIATORS ON COM 3	MAX7231C MAX7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0	8	8
0	1	.8	8.
1	0	8.	.8
1	1	.8.	.8.

Table 2: Binary Data Decoding (MAX7231/MAX7232)

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

Table 3: Data Decoding — 18 Segment (MAX7233/MAX7234)

CODE INPUT				DISPLAY OUTPUT				
				D5 D4			A VERSION	B VERSION
D3	D2	D1	D0	0,0	0,1	1,0	1,1	
0	0	0	0	P	P		0	0
0	0	0	1	A	Q	!	1	1
0	0	1	0	B	R	"	2	2
0	0	1	1	C	S	#	3	3
0	1	0	0	D	T	$	4	4
0	1	0	1	E	U	%	5	5
0	1	1	0	F	V	&	6	6
0	1	1	1	G	W	'	7	7
1	0	0	0	H	X	(	8	8
1	0	0	1	I	Y	)	9	9
1	0	1	0	J	Z	*	:	
1	0	1	1	K	[	+	;	
1	1	0	0	L	\	,	<	
1	1	0	1	M	]	-	=	
1	1	1	0	N	^	.	>	
1	1	1	1	O	←	/	?	

Table 4: Address Decoding (MAX7231/7232)

CODE INPUT				DISPLAY OUTPUT
MAX 7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

Table 5: Address Decoding (MAX7233/7234)

CODE INPUT			DIGIT SELECTED
MAX 7234 ONLY A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

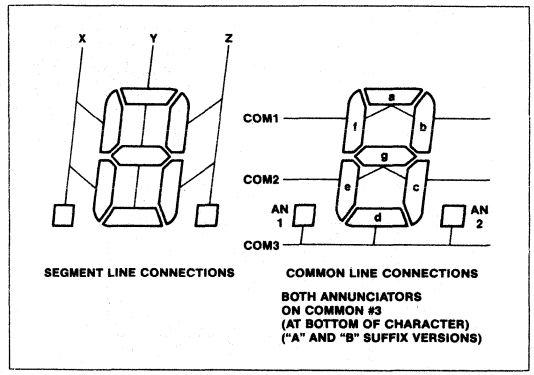

Figure 18. Display Fonts for MAX7231 and 7232. (Suffix Versions "A" and "B").

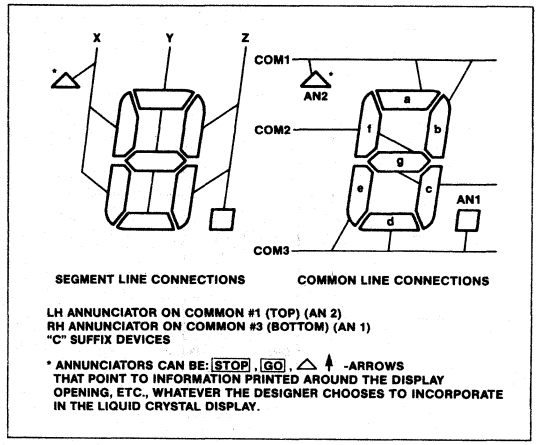

Figure 19. Display Fonts for MAX7231 and 7232. (Suffix Version "C").

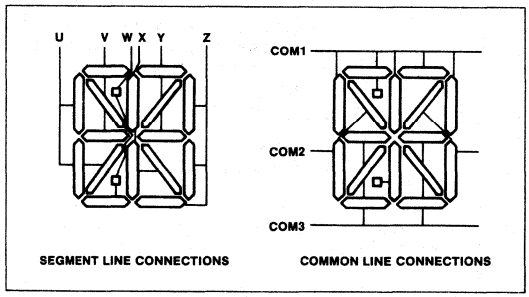

Figure 20. Display Fonts for MAX7233 and 7234. (18-Segment Alphanumeric).

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Triplexed LCD Decoder/Drivers

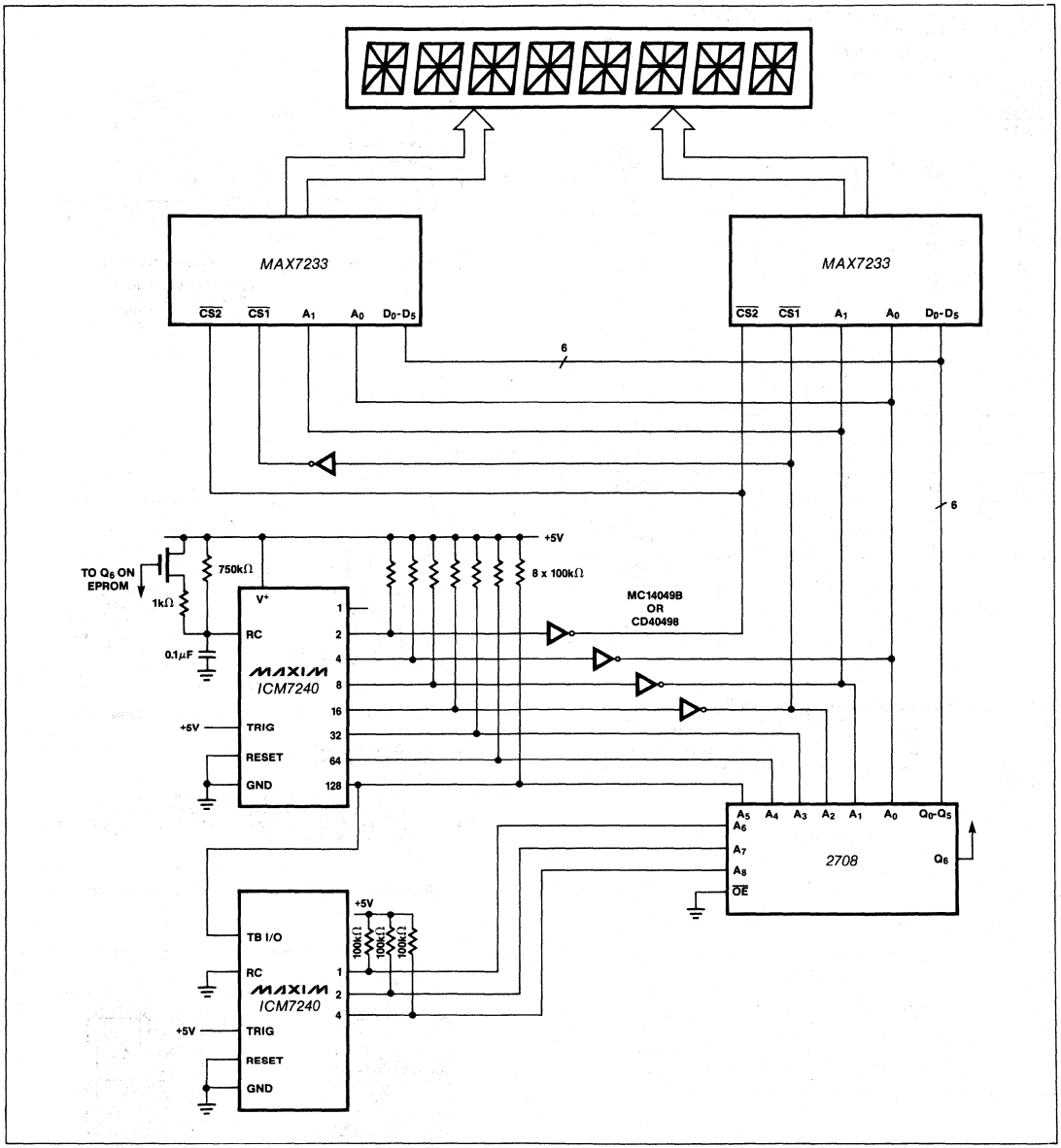

Figure 21. EPROM-Coded Message System. This circuit cycles through a message coded in the EPROM, pausing at the end of each line, or whenever coded on Q_6.

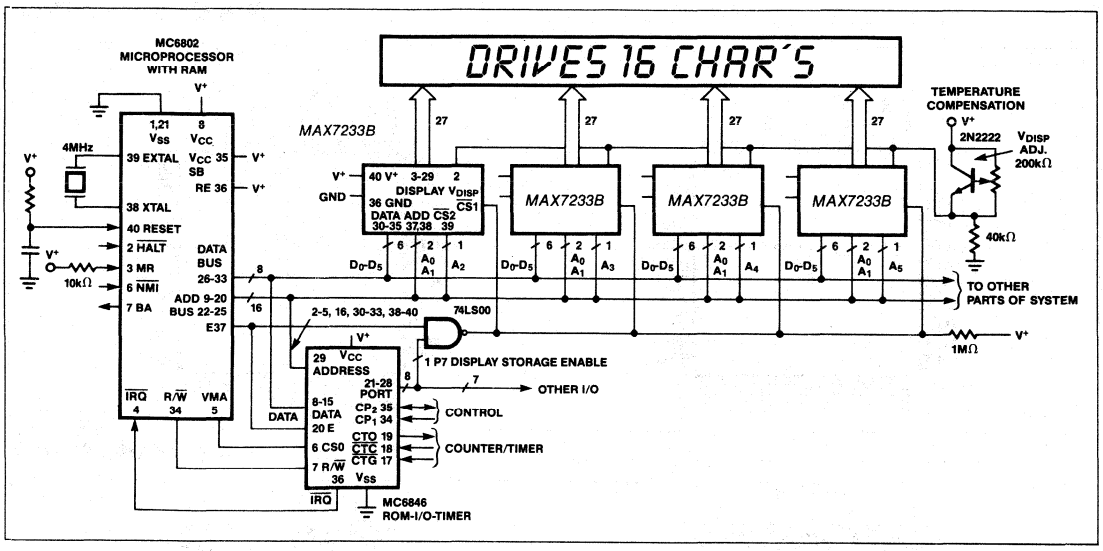

Figure 22. MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display.

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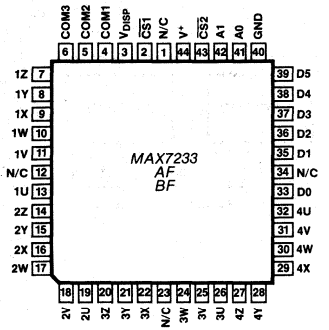
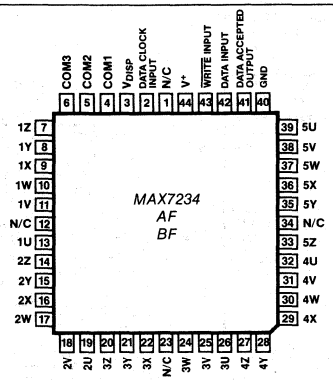
Triplexed LCD Decoder/Drivers

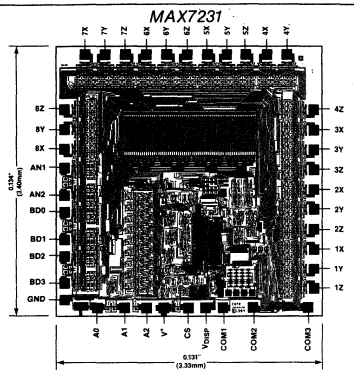
Pin Configuration

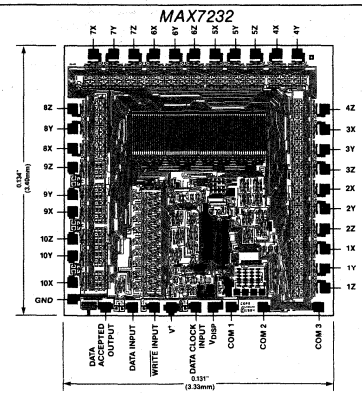
Top View

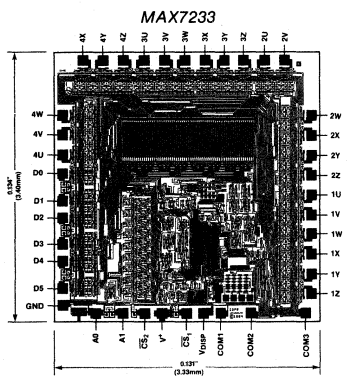


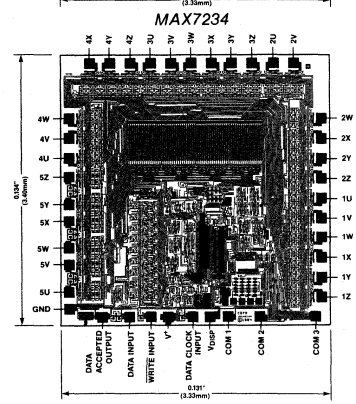


Chip Topography









MAXIM

Four Digit Display Decoder/Drivers

General Description

The Maxim ICM7211 (LCD) and ICM7212 (LED) four digit, seven segment display drivers include input data latches, BCD to segment decoders, and all level translation and timing circuits needed to drive non-multiplexed displays.

Both the ICM7211 and ICM7212 are available in two data input configurations: a multiplexed BCD interface version and a microprocessor interface version. The multiplexed BCD interface version has four BCD data inputs and four separate digit strobes. The microprocessor interface versions, designated by an "M" suffix, have four BCD data inputs, two digit address lines, and two chip selects or WRITE inputs.

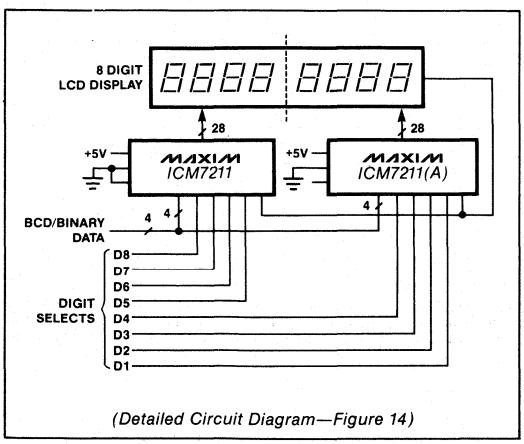
The ICM7211 and ICM7212 decode the BCD data via an onboard character font ROM. There are two different character fonts available, hexadecimal and Code B.

Applications

The low power consumption of the ICM7211 LCD driver makes it ideal for battery powered and portable applications. The ICM7212 LED display driver reduces system cost by eliminating external level translators, external segment drivers, and segment current limiting resistors.

Digital Panel Displays
Intelligent Instruments
Remote Display Units
Microprocessor-to-Visual Communication

Typical Operating Circuit



(Detailed Circuit Diagram—Figure 14)

Features

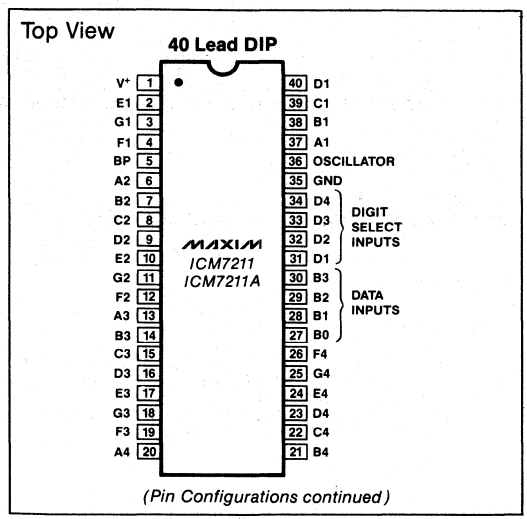
- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Directly drives Four Digit, 7 Segment Displays**
  ICM7211 - Non-multiplexed Liquid Crystal Display (LCD)
  ICM7212 - Non-multiplexed Common Anode LED
  Multiplexed BCD Interface and μP Interface Versions
- **No external components needed**
- **Low Power CMOS - 25μW typ. (display blanked)**

Ordering Information

DEVICE TYPE	OUTPUT CODE	INPUT CONFIGURATION
ICM7211 (LCD)	Hexadecimal	Multiplexed 4-Bit
ICM7211A (LCD)	Code B	
ICM7211M (LCD)	Hexadecimal	μP Interface
ICM7211AM (LCD)	Code B	
ICM7212 (LED)	Hexadecimal	Multiplexed 4-Bit
ICM 7212A (LED)	Code B	
ICM7212M (LED)	Hexadecimal	μP Interface
ICM7212AM (LED)	Code B	

(Ordering information continued).

Pin Configurations



(Pin Configurations continued)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Four Digit Display Decoder/Drivers

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W@ 70°C
Supply Voltage 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, GROUND -0.3V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V; T_A = 25°C, Test circuit unless noted)

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Test circuit, Display blank		10	50	μA
Oscillator Input Current	I_{OSCI}	Pin 36		±2	±10	
Segment Rise/Fall Time	t_{RFS}	C_L = 200pF		0.5		μs
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{OSC}	Pin 36 Floating		16		kHz
Backplane Frequency	f_{BP}	Pin 36 Floating		125		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pin 27-34 - GROUND		10	50	μA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment On Current	I_{SEG}	Segment On, V_O = +3V	5	8		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}		3			V
Logical "0" input voltage	V_{IL}				1	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	μA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	μA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{SA}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{DS}		500			ns
Data Hold Time	t_{DH}		200			
Inter-Digit Select Time	t_{IDS}		2			μs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{CSA}	other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{DS}		100			
Data Hold Time	t_{DH}		10	0		
Inter-Chip Select Time	t_{ICS}		2			μs

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1981) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Four Digit Display Decoder/Drivers

- ◆ Key Parameters Guaranteed Over Temperature
- ◆ Low Power (Typically 25μW)
- ◆ Increased Segment-On Current
- ◆ Maxim Quality and Reliability
- ◆ Improved ESD Protection (Note 3)

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +5V; T_A = 25°C, Test circuit unless noted.)

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	**I_{OP}**	**Test circuit, Display blank**		**5**	**25**	**μA**
Oscillator Input Current	I_{OSCI}	Pin 36, V_{OSC} = 2.5V		±2	±10	μA
Segment Rise/Fall Time	t_{RFS}	C_L = 200pF		0.5		μs
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{OSC}	Pin 36 Floating		19		kHz
Backplane Frequency	f_{BP}	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pin 27-34 - GROUND		5	50	μA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment On Current	**I_{SEG}**	**Segment On, V_O = +3V; T_A = 25°C 0°C ≤ T_A ≤ +70°C**	**6 5**	**9**		**mA**

INPUT CHARACTERISTICS (ICM7211 AND ICM7212)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" input voltage	**V_{IH}**	**Pins 27-34, -20°C to +85°C**	**3**			**V**
Logical "0" input voltage	**V_{IL}**	**Pins 27-34, -20°C to +85°C**			**1**	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	μA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	μA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{SA}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{DS}		-100			ns
Data Hold Time	t_{DH}		200			
Inter-Digit Select Time	t_{IDS}		2			μs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{CSA}	Other chip select either held active, or both driven together		200		ns
Data Setup Time	t_{DS}		100			
Data Hold Time	t_{DH}		10	0		
Inter-Chip Select Time	t_{ICS}		2			μs

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

Note 3: All pins except pin 29 are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883B Method 3015.1 Test Circuit). Due to the special test functions associated with pin 29, this pin is designed to withstand up to 1500V (same test circuit).

Four Digit Display Decoder/Drivers

Ordering Information (Cont.)

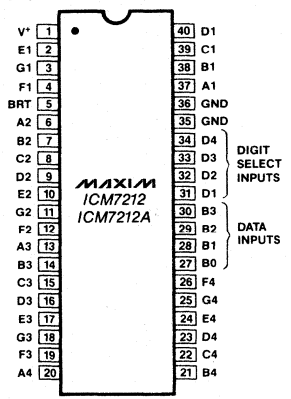
PART	TEMP. RANGE	PACKAGE
ICM7211IQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211AIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211MIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211AMIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212IQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212AIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212MIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212AMIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier

PART	TEMP. RANGE	PACKAGE
ICM7211IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211AIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211MIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211AMIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212AIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212MIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212AMIPL	-20°C to +85°C	40 Lead Plastic DIP

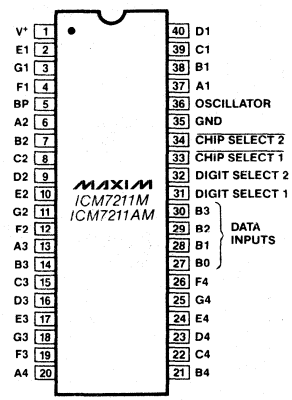
Each device type listed is available in dice form; Order basic part number followed by C/D; (i.e. ICM7211C/D).

Pin Configurations (Cont.)

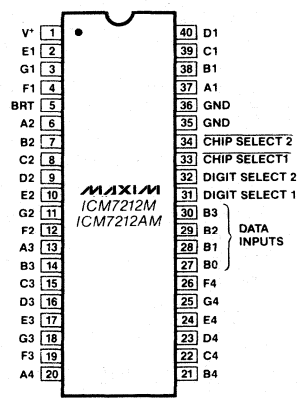
Top View **40 Lead DIP**



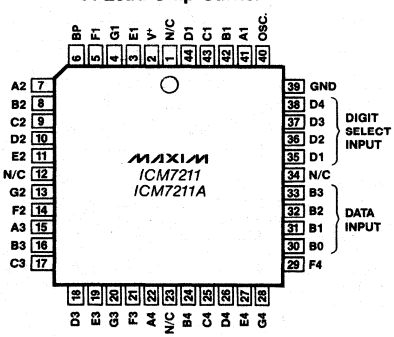
40 Pin DIP



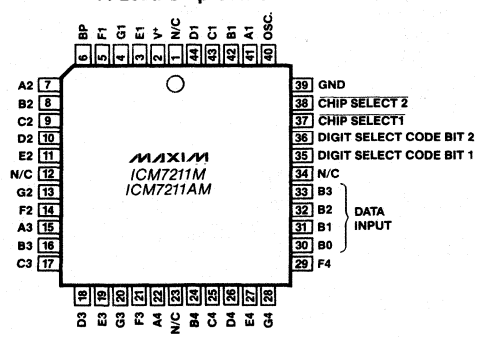
40 Lead DIP



44 Lead Chip Carrier



44 Lead Chip Carrier

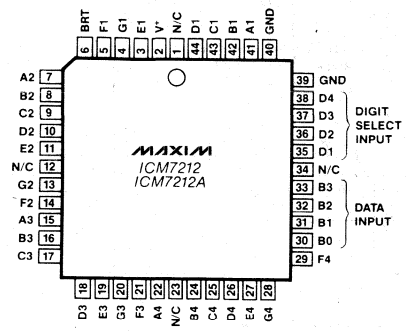


Four Digit Display Decoder/Drivers

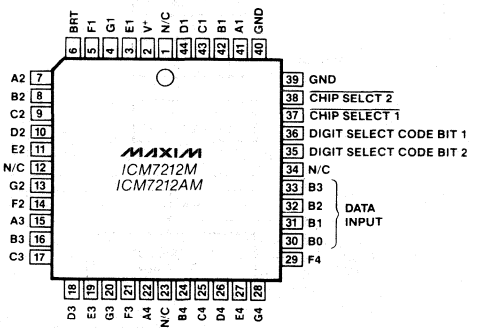
Pin Configurations (Cont.)

Top View

44 Lead Chip Carrier

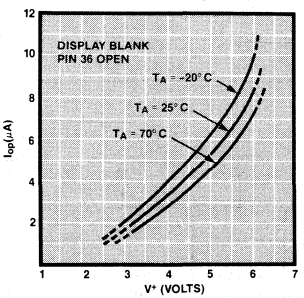


44 Lead Chip Carrier

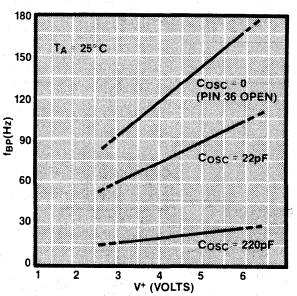


Typical Operating Characteristics

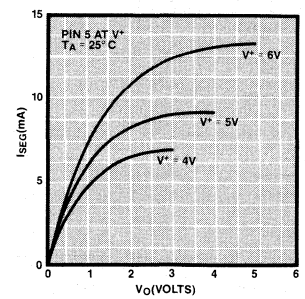
ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



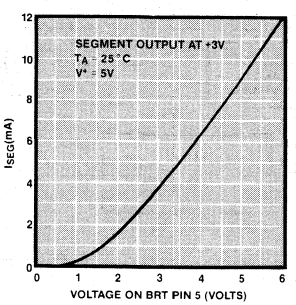
ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



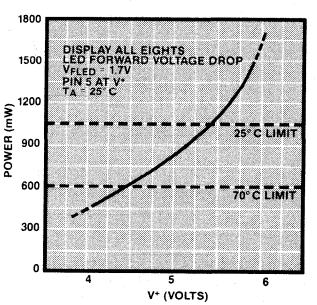
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



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Four Digit Display Decoder/Drivers

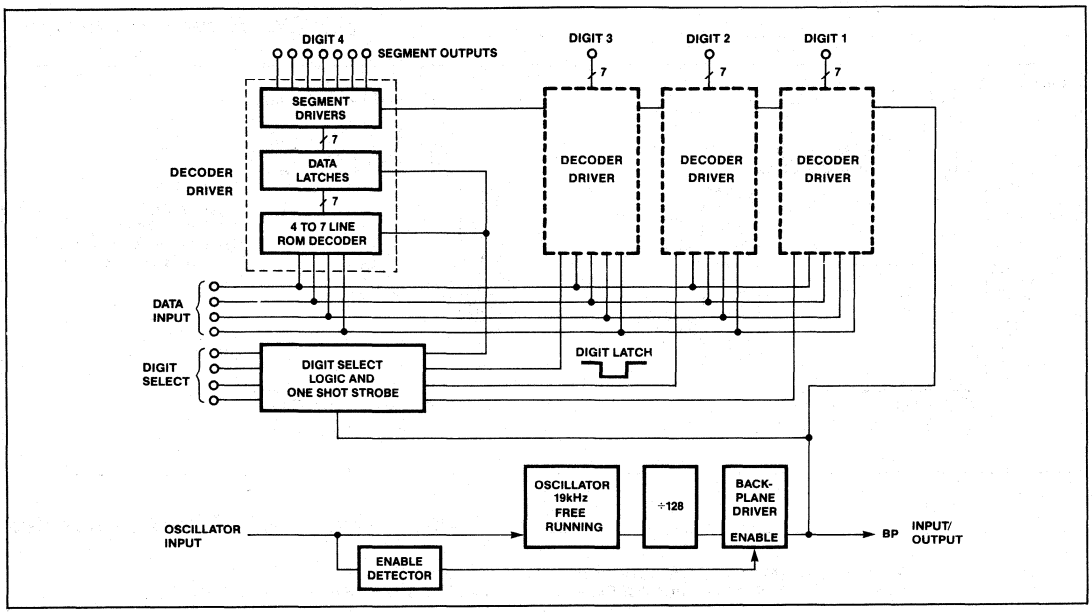

Figure 1. Block diagram of ICM7211 and ICM7211A.

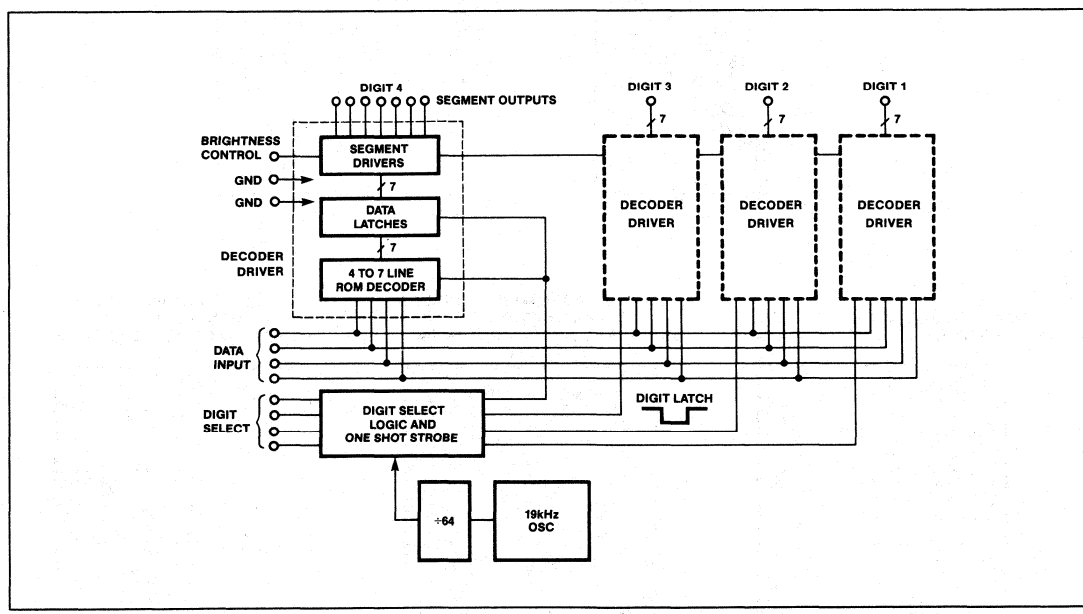

Figure 2. Block diagram of ICM7212 and ICM7212A.

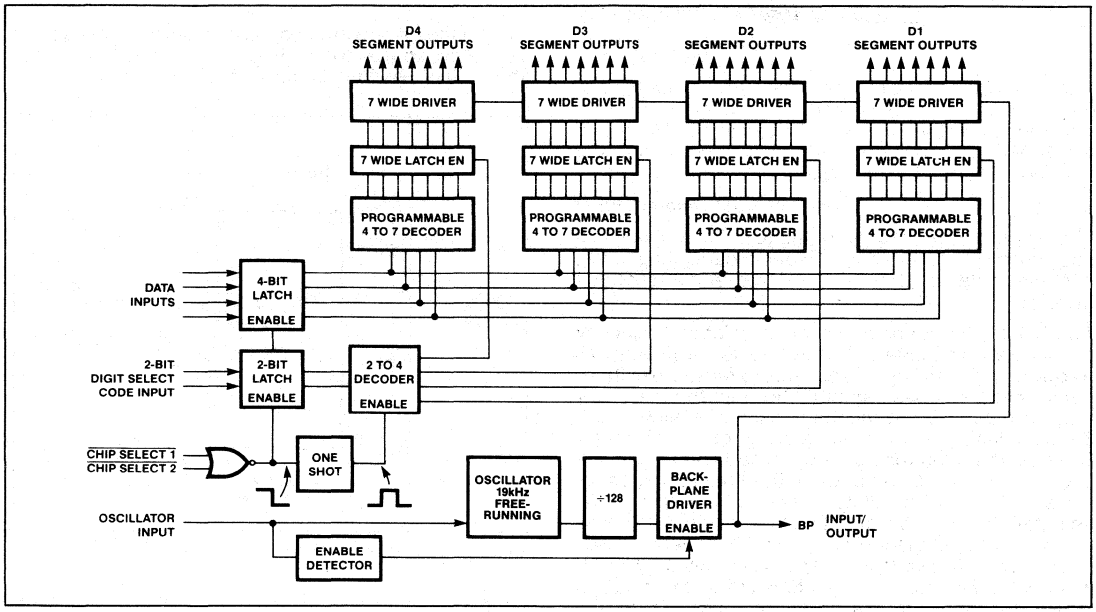

Figure 3. Block diagram of ICM7211M and ICM7211AM.

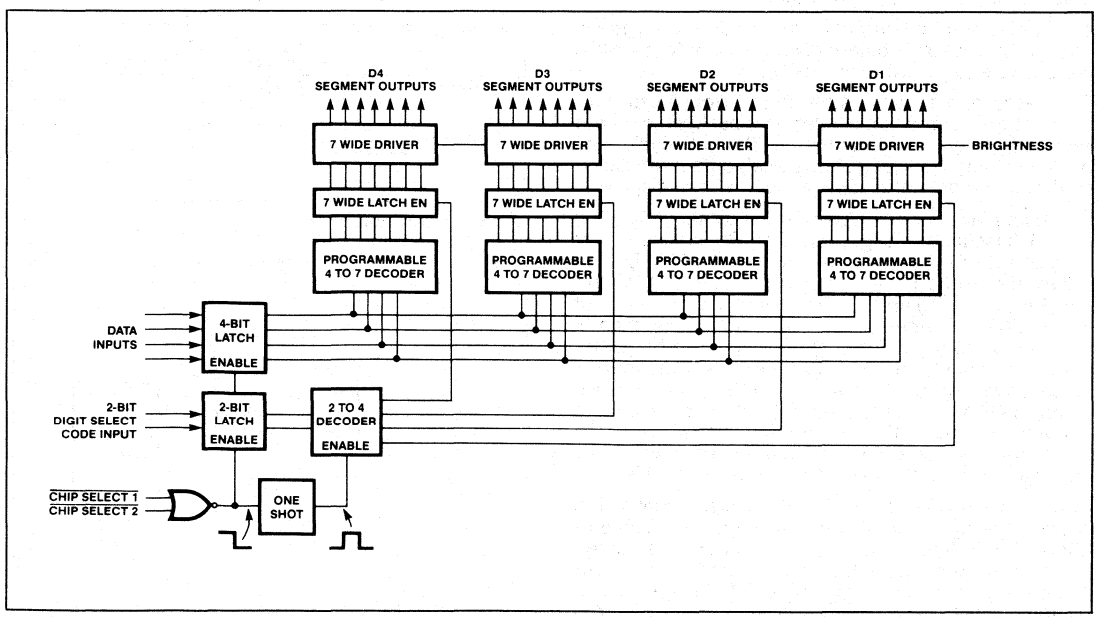

Figure 4. Block diagram of ICM7212M and ICM7212AM.

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Four Digit Display Decoder/Drivers

Detailed Description

Display Interface

The ICM7211 and ICM7212 differ only in the type of display interface. The ICM7211 is designed to drive non-multiplexed liquid crystal displays (LCDs), while the ICM7212 is designed to drive non-multiplexed, common anode LED displays.

ICM7211 LCD Display Driver

The display driver section of the ICM7211 includes an oscillator, a 7 stage binary divider, a backplane driver, backplane slaving detector and logic, and 28 segment drivers.

The RC oscillator has a nominal oscillation frequency of 19kHz with no external components. Ordinarily this frequency is suitable and no external oscillator components are needed, but if desired, the frequency may be lowered by connecting a capacitor between pin 36 (Oscillator) and either ground or V^+. A graph showing the relationship between capacitor value and oscillator frequency is shown in the Typical Characteristics section. The oscillator may also be overdriven by an external clock source with a frequency of 128 times the desired backplane frequency. The external clock source should swing from approximately 1.5V to 5V when V^+ is 5V. The external clock signal must not go below 1V for more than one microsecond, or the backplane disable circuitry may be activated (see below). Figure 7 shows an external clock drive circuit that meets the above requirements.

The 19kHz nominal output of the onboard oscillator is divided by a 7 stage binary divider (÷128) to generate the backplane frequency of 150Hz.

The backplane drive is simply an inverter whose input is the output of the last divider. The backplane output swings from ground to V^+ with a 50% duty cycle. The backplane has a low (200 ohm typical) output resistance so that it can drive the capacitance of large displays.

The backplane output driver can be disabled by tying pin 36 (Oscillator) to ground. The Backplane Input/Output (pin 5) then becomes an input which can be driven by the backplane output of another ICM7211 (see Figures 14, 16 and 17). Each backplane is a load of about 200 pF when driven, and no more than 4 ICM7211's (16 digits total) should be slaved together using one "master" ICM7211 as the backplane source, since power dissipation and the DC offset increase when the ICM7211 backplane output drives very large capacitive loads. For more than 16 digits on a common backplane, a separate, external driver with a low impedance should be used to drive all ICM7211s.

The segment drivers are CMOS inverters that swing between ground and V^+ with an output resistance of about 2 kΩ. The input to the inverter is switched between two signals, so that the segment driver output is the same as the backplane when LCD segment is to be turned OFF, and is BACKPLANE when the LCD segment is to be turned ON. The segment and backplane drivers are designed to have equal rise and fall times, so that the average DC component across the LCD is less than 25 millivolts.

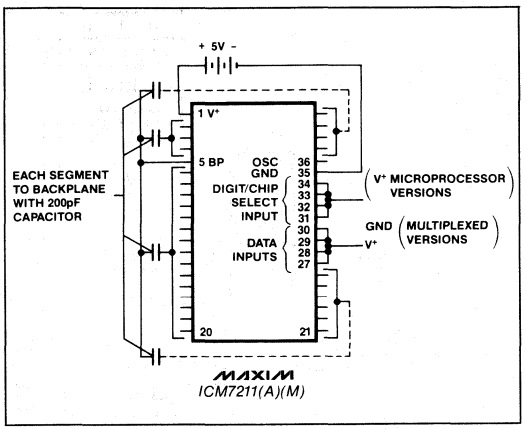


Figure 5. ICM7211 Test Circuit (all versions).

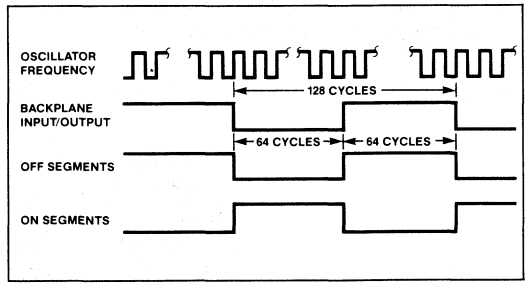


Figure 6. Display Waveforms.

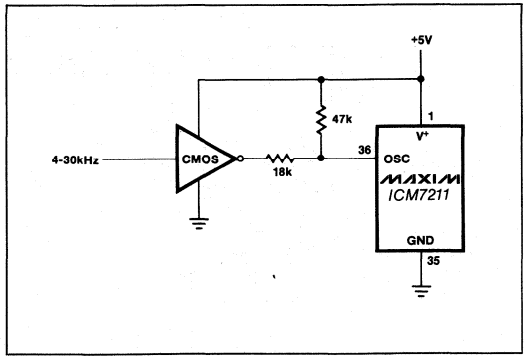


Figure 7. External Clock Drive.

ICM7212 LED Drivers

The ICM7212 has 28 open drain constant current n-channel outputs, which eliminate the need for external segment resistors. The LED current vs. output voltage of a typical segment driver is shown in the Typical Characteristics section. The Brightness input (pin 5) supplies the segment driver gate voltage, and it can be used to either control the brightness of the LED display or to completely blank the display. Two methods of controlling display brightness are shown in Figure 8. The first method simply controls the voltage on the brightness pin by means of a potentiometer. The Brightness input draws negligible current and the potentiometer is normally in the range of 100 kilohms to 1 megohm. By replacing the potentiometer with a resistor and a photoresistor, the display brightness can be automatically adjusted in response to changes in the ambient lighting. A second method of display brightness control is to duty-cycle modulate the Brightness input between "full on" and "blanked" states. As with the simple potentiometer method, the display brightness can be automatically adjusted for ambient lighting conditions by replacing one of the timing resistors with a photoresistor.

The ICM7212 has two ground pins to support the high total display current that flows into the segment outputs and then is returned to ground through the ICM7212 ground pins.

Since the ICM7212 will drive the LED display at high total display current, care must be taken not to exceed the absolute maximum power dissipation limit of the ICM7212 at high ambient temperatures. For example, at 70°C, the absoulute maximum power dissipation specification is 500 mW. If all 28 segments are turned on (a display of 8888), and each segment is drawing 8 mA, the total power dissipation in the ICM7212 would be

$Pd = 28 \text{ segments}.(8mA).(V_{seg})$
Where $V_{seg} = V^+ - V_{led} = 5V - 1.6V = 3.4V$
Therefore $Pd = 28.(8).(3.4) = 760$ mW; greater than the absolute maximum limit.

There are two ways to keep the power dissipation below the ICM7212 power dissipation limits: reduce the LED current, or reduce the voltage across the ICM7212 segment drivers. The LED current can be reduced by the display brightness control circuits shown in figure 8. The other alternative, reducing the voltage across the segment drivers can be accomplished by either reducing the V^+ supply to the entire system, or by reducing the V^+ supply to just the LED display by placing diodes in series with the LED display (see Figure 9). Two silicon diodes in series with the anode of the LED display will reduce the voltage across the segment drivers from 3.4V to 2.2V, resulting in a power reduction of approximately 35%, while only slightly reducing the LED current and brightness. A third diode in series with the LED display would further reduce the power dissipation, but the segment current would also be reduced since there would be only about 1.6V across the n-channel segment driver.

Digital Interface

There are two different types of digital interfaces available for the ICM7211 and ICM7212, a multiplexed BCD interface and a microprocessor interface.

Multiplexed BCD Data Interface

On the multiplexed BCD data entry versions of ICM7211 and ICM7212 there are 8 lines used for entering data: 4 BCD data lines and 4 digit strobes. The multiplexed BCD input timing and truth table is shown in Figure 10. When one of the four digit strobes is taken high, a short internal pulse is generated which latches the decoded segment data in the 7 bit latch associated with that digit. If the digit strobe is continuously held high, each transition of the backplane will cause another internal latch pulse to be generated, latching new segment data if the BCD data has changed. When the digit strobe goes low the data in the latch is held constant with no further updates until the digit strobe is again taken high. As shown in the electrical specifications table, the data setup time is is a negative 100ns, which means that the digit strobe can be taken high as much as 100ns before the BCD data is valid.

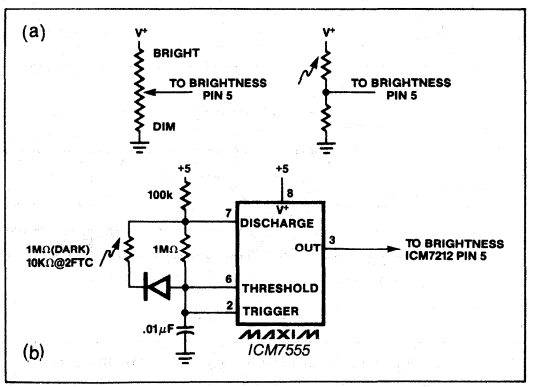


Figure 8A & 8B. Brightness Control

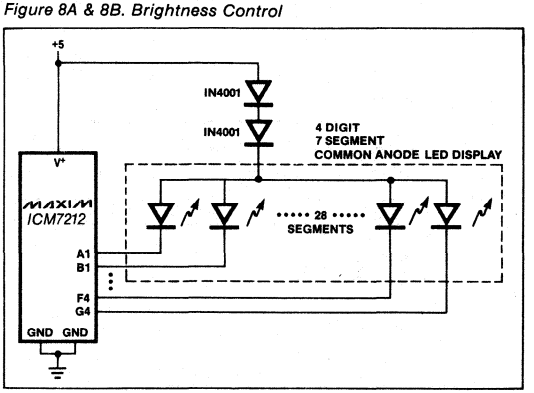


Figure 9. Reducing ICM7212 Power Dissipation.

Four Digit Display Decoder/Drivers

Character Fonts

Table 1 shows the two different output codes or fonts available. Both versions have the same display for 0-9 and differ only in the display of the last 6 input codes. The Code B versions have the suffix "A" in their part number.

Table 1: Output Codes

BINARY				HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(Blank)

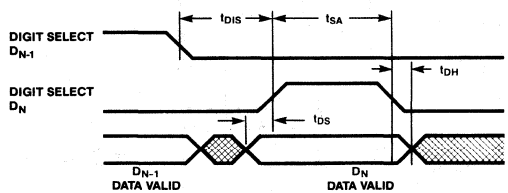
Microprocessor or Data Interface

The microprocessor data interface versions of the ICM7211 and ICM7212 are denoted by an "M" suffix in their part number. The microprocessor data interface also uses 8 lines for the data interface: 4 BCD data lines, 2 digit address lines, and 2 active low chip select lines. A typical data write cycle and the truth table are shown in Figure 11. Data is entered into the input latches whenever both CS (chip select) lines are low. When either CS line goes high an internal one shot is activated, transferring the decoded 7-segment data to the appropriate digit latch. One CS line is ordinarily driven by an address decoder and the other CS line is driven by the microprocessor WR (write) line (see Figure 15). In this type of application, the ICM7211/12 is accessed as 4 "write only" memory locations.

Application Notes

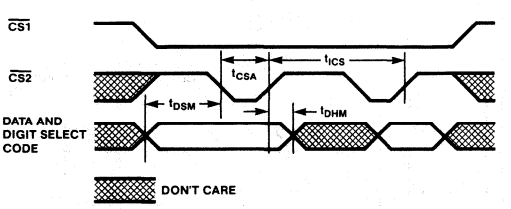
Backplane Frequency

The ICM7211 onboard oscillator generates a backplane frequency of approximately 150Hz with no external components. This is suitable for most displays, but



TRUTH TABLE				
D1	D2	D3	D4	Function
0	0	0	0	No change
0	0	0	1	Store Data in D4 Latch
0	0	1	0	Store Data in D3 Latch
0	1	0	0	Store Data in D2 Latch
1	0	0	0	Store Data in D1 Latch
1	1	1	1	Store Data in All Data Latches

Figure 10. Multiplexed input timing diagram and truth table.



TRUTH TABLE				
DS2	DS1	$\overline{CS2}$	$\overline{CS1}$	Function
X	X	X	1	No change
X	X	1	X	
0	0	0	↑	Store D4 Data
0	0	↑	0	
0	1	0	↑	Store D3 Data
0	0	↑	0	
1	0	0	↑	Store D2 Data
1	0	↑	0	
1	1	0	↑	Store D1 Data
1	1	↑	0	

Figure 11. Microprocessor Interface input timing diagram and truth table.

150Hz is too high a frequency when driving very large displays or low threshold displays with high segment trace resistance. When driving very large displays (>1" height), the very large capacitance of the display will significantly slow the rise and fall times of the backplane and segment drivers. These drivers are designed to have matching rise and fall times, but any residual mismatch will result in a DC offset across the LCD. This DC offset is directly proportional to the backplane frequency, so the lowest acceptable backplane frequency (usually 30Hz) should be used when driving very large LCDs. A simple way of lowering the backplane frequency is to connect an external capacitor from the OSCillator (pin 36) to either ground or V^+. The graph in the Typical Characteristics curves shows the relationship between the value of this external capacitor and the backplane frequency. The backplane frequency can also be controlled by externally driving the OSCillator pin. Figure 12 shows a method of setting the backplane frequency to precisely 32Hz.

If the indium traces on the LCD glass itself are very long and they have high sheet resistance, the resistance of the trace will form an RC delay with the capacitance of the LCD. The phase shift caused by this RC delay causes a small voltage to appear across the LCD segments that are supposed to be in the off state. This may cause "ghosting" or a slight turn-on of segments that are supposed to be off. Reducing the backplane frequency or using LCDs that have a higher threshold will eliminate this problem.

Annunciators or Flags

Many LCD displays have annunciators or flags in addition to the 7 segment digits. Figure 13 shows several different methods of driving LCD segments used as annuciators or flags. Output A of Figure 13 is driven by a CMOS exclusive OR (XOR) gate. The XOR's output is either the same as the backplane or the complement of the backplane, depending on the logic level on the input. With a "1" at the logic input the XOR output is the complement of the backplane and the LCD segment is turned on. Output B is connected to the backplane through a 1 MΩ resistor. When the analog switch is open, output B will be the backplane signal and the segment will be off. When the analog switch is closed, output B will be the complement of the backplane signal and the segment will be on. Output C is simply the complement of the backplane signal, and any segment (such as a decimal point) connected to output C will always be turned on. Output D is another way of turning on a decimal point, but since the voltage at D is simply the average DC voltage of the backplane signal, the total applied voltage across a segment connected to D is only 5 Vpk-pk (assuming 5V V^+) rather than the 10Vpk-pk drive received by a segment connected to output C. The resistor-capacitor drive method of output D should be used only with low threshold LCDs. Unused LCD segments should be tied to the backplane, NOT allowed to float. A floating segment, while usually remaining off, may be driven by leakage currents or capacitive coupling with other segments and become a "ghost" or slightly turned on.

If one or more of the ICM7211 digits are not used, they can be used to drive annunciator segments without using any external logic. If only two annunciator segments need to be driven, connect the annunciators to segments B and D of the unused digit. That digit is then loaded with the data $\overline{A2}$, $\overline{A1}$ 11, where A1 and A2 are the data for the two annunciators.

Three annunciators can be driven from one unused digit, but the input data to select all 8 possible combinations of annunciator states must be obtained from a look-up table. Two possible arrangements are shown in Table 2.

Driving an 8 Digit LCD with Common Backplane

In order to drive 8 LCD digits that have a common backplane, the backplanes of two ICM7211s must be synchronized. In figure 14 the left hand ICM7211's Backplane pin is turned into an input by grounding its oscillator pin. The right hand ICM7211 then drives both the LCD backplane and the Backplane pin of the left hand ICM7211.

Memory Mapped 8048 Microprocessor Interface

In figure 15 the digit select lines DS1 and DS2 are driven by the address latched from the 8048's multiplexed data and address bus. The data is then written into the selected digit by the $\overline{WR}$ line. The 74LS138 is used to decode eight blocks, each four bytes long, starting at address 32 (decimal). The ICM7211s are addressed by MOVX instructions to these external ram locations. The extra decoded outputs of the 74LS138 can be used as chip selects for other I/O devices.

Microprocessor Interface via I/O Port

Figure 16 shows one 8 bit I/O port driving two ICM7211s or ICM7212s. The data and digit selects are controlled by the lower 6 bits, while the upper two bits control which display driver receives the data.

Remote Display via UART

The serial input stream is assembled into an 8 bit parallel output by the UART, then the UART brings the DR (data ready) line high (See Figure 17). The schmitt trigger and RC delay drive both the $\overline{CS}$ inputs of the ICM7211s and the $\overline{DRR}$ (data ready reset) pin of the UART. When the schmitt trigger drives the $\overline{DRR}$ low, the DR pin goes low, and after a short delay, the output of the schmitt trigger output goes back high. This low-going pulse on the schmitt trigger output latches the data into the ICM7211s.

Display Interface for ICL7135 A/D

Figure 18 shows an ICM7212 interfaced to the 4½ digit A/D, ICL7135. The polarity and ½ digit segments are driven by D flip-flops that latch polarity and ½ digit data at the end of each measurement. The ICL7135

Four Digit Display Decoder/Drivers

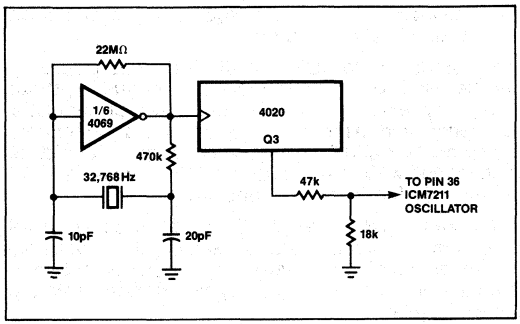


Figure 12. Crystal Controlled Backplane Frequency.

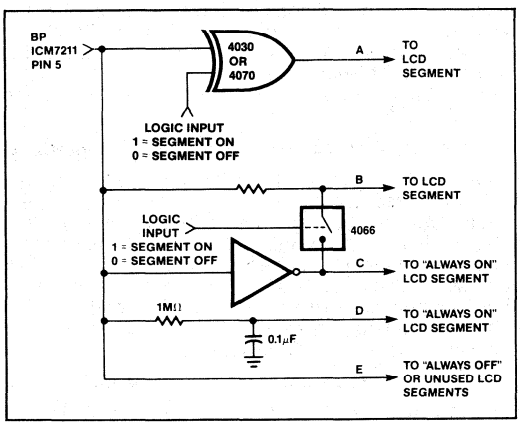


Figure 13. Driving Annunciators, Flags and Decimal Points.

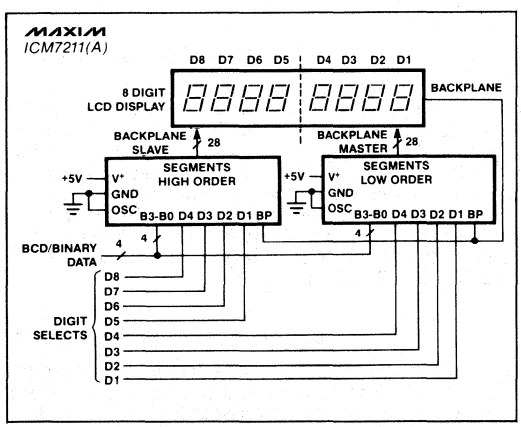


Figure 14. Two ICM7211's Driving 8-Digit LCD Display.

Overrange output drives the ICM7212 Brightness input, blanking the four least significant digits when the input voltage is greater than full-scale.

Similar to the LED display system, Figure 19 uses Maxim's ICM7211 LCD display driver to drive 4 digits of LCD display. The backplane signal of the ICM7211 and the CMOS exclusive OR gates are used to drive the 1/2 digit and the polarity sign. The 4 AND gates combine the ICM7135's digit outputs with its Strobe output to generate the digit select signals that latch data into the ICL7211. Since the Strobe occurs in the middle of each digit's data there is more than enough data setup and hold time to ensure that valid data is latched. The OR gates will force the BCD data to all ones when overrange goes high. The ICM7211A will blank the display when all ones (hex F) is loaded.

SEGMENT			INPUT DATA FOR ICM7211			
F	E	A	B3	B2	B1	B0
0	0	0	0	0	0	1
0	0	1	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	1	0	1	1
1	1	1	0	0	0	0

0 = OFF
1 = ON

Table 2A: Using Segments to Drive Annunciators, ICM7211

SEGMENT			INPUT DATA FOR ICM7211			
F	E	A	B3	B2	B1	B0
0	0	0	1	1	1	1
0	0	1	0	1	0	1
0	1	0	0	0	0	1
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	0	1	0	1	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	0

0 = OFF
1 = ON

Table 2B: Using Segments to Drive Annunciators, ICM7211A

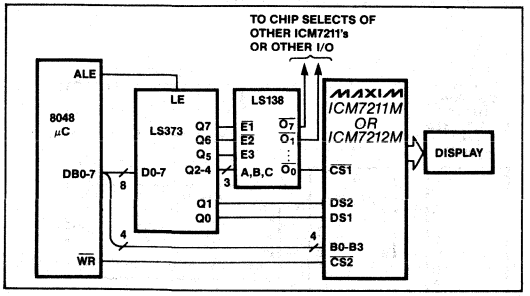


Figure 15. 8048 Memory Mapped Interface

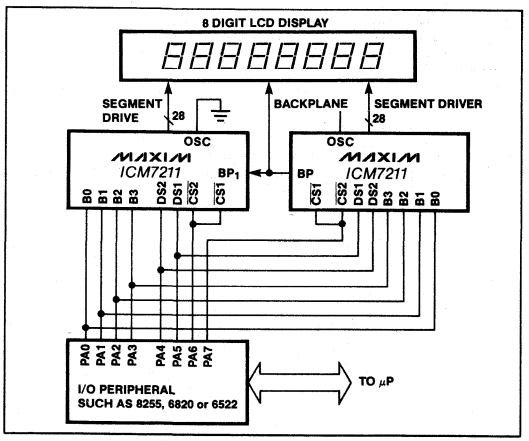


Figure 16. uP Interface via I/O Port

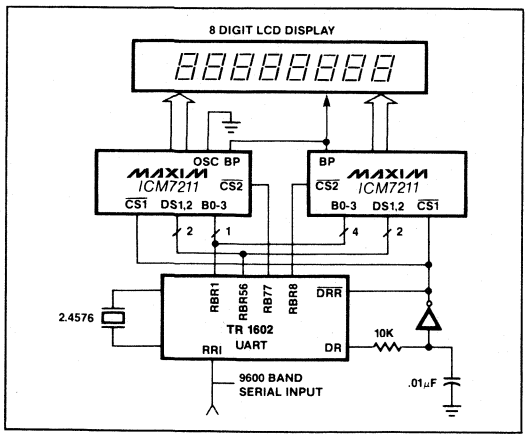


Figure 17. Remote Display via UART

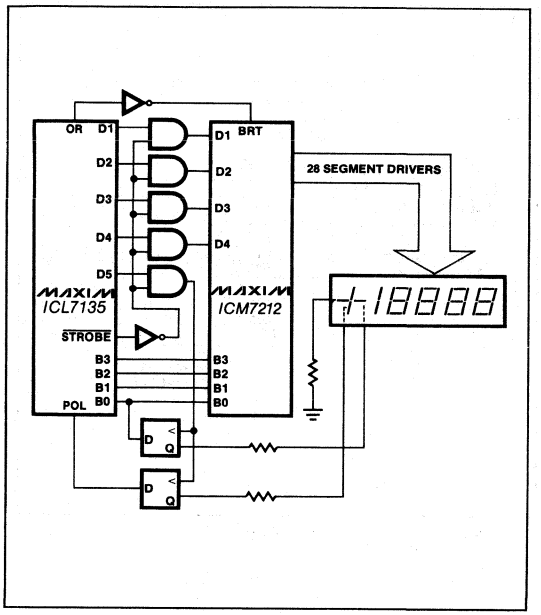


Figure 18. LED Display Interface for ICL7135 A/D

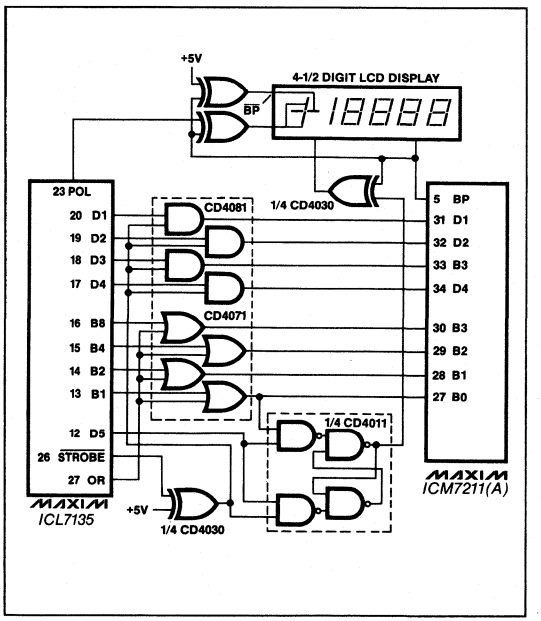


Figure 19. LCD Display for ICL7135 A/D

Four Digit Display Decoder/Drivers

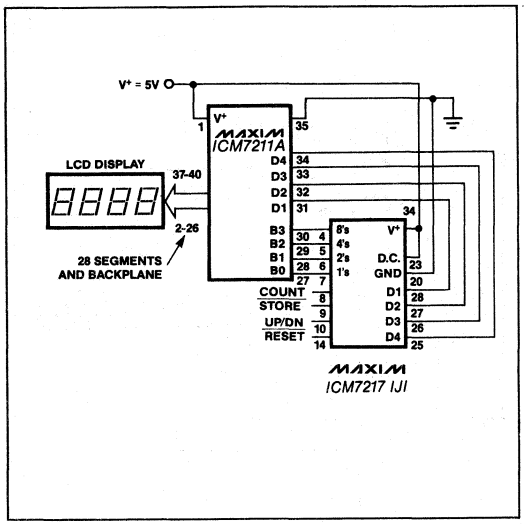


Figure 20. ICM7217 to LCD Interface.

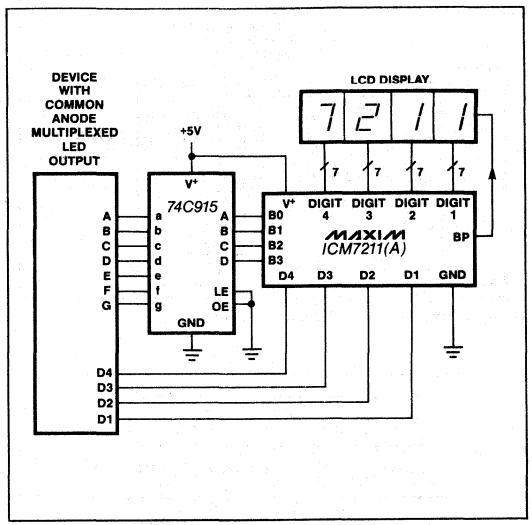
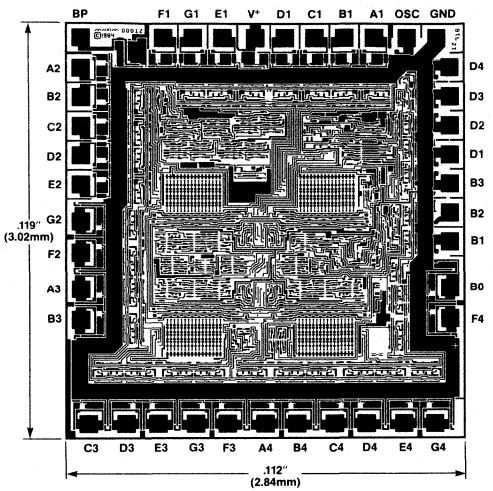


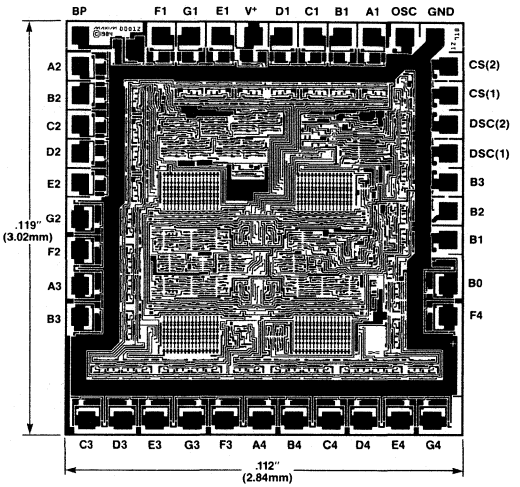
Figure 21. Multiplexed LED Driver to LCD Interface.

Chip Topography

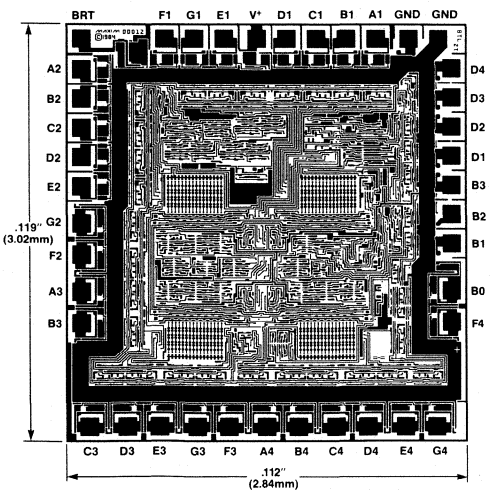
ICM7211, 7211A



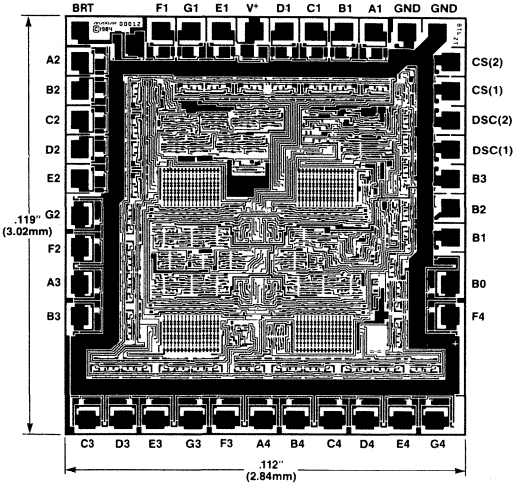
ICM7211M, 7211AM



ICM7212, 12A



ICM7212M, 7212AM



MAXIM
4 Digit (LED) Presettable Up/Down Counter

General Description

The Maxim ICM7217 family of 4 digit presettable up/down counters contain a 4 digit, 7 segment LED display driver and a presettable comparison (predetermining) register. The counter and comparison register can be preset using either thumbwheel switches, jumpers, or external digital logic.

The ICM7217 (common anode) and ICM7217A (common cathode) are decade counters with a maximum count of 9999. The ICM7217B (common anode) and ICM7217C (common cathode) are modulo 60 counters intended for hours/minutes or minute/seconds timing applications, and have a maximum count of 5959.

These devices also provide multiplexed BCD outputs, a Carry/Borrow output allowing ICM7217s to be cascaded, a Zero output which indicates when the count is equal to zero, and an Equal output which indicates when the count is equal to the value contained in the comparison register. The ICM7217 also has a Reset input and a display latch with store input.

Applications

The Maxim ICM7217 significantly reduces the number of components required in many timing, counting and frequency counter applications.

Typical applications include:

Predetermining Batch Counter
Tachometer
Over/Under Speed Detector
Count Down/Elapsed Timer
Unit Counter
Frequency Counter

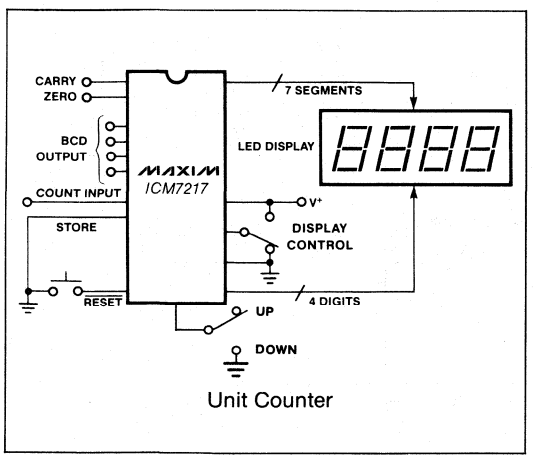
Features

- **Pin for Pin Second Source!**
- **4 Digit Up/Down Counter**
- **Directly Drives LED Display**
- **Presettable Counter and Compare Register**
- **Interfaces with Thumbwheel Switches or Digital Logic**
- **Can Be Cascaded**
- **Multiplexed BCD I/O**
- **Up/Down, Store and Reset Inputs**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7217IJI	-20°C to +85°C	28 Lead CERDIP
ICM7217IPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217AIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217AIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217BIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217BIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217CIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217CIPI	-20°C to +85°C	28 Lead Plastic DIP

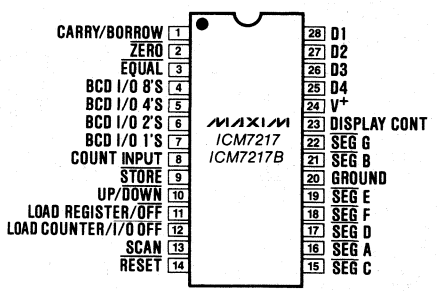
Typical Operating Circuit



Unit Counter

Pin Configuration

Top View



4 Digit (LED) Presettable Up/Down Counter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 500mA
Power Dissipation
28 Pin CERDIP 1.0W
derate 25mW/°C above 50°C
28 Pin Plastic (copper leadframe) 1.0W
derate 25mW/°C above 50°C

Temperature Range
Operating ..... -20°C to +85°C
Plastic Chip Carrier (Quad) Package (Q) ..... 0°C to +70°C
Storage ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Segment Output Current 100mA
Input Voltage (any terminal) (Note 1) ..... -0.3V to (V^+ +0.3V)

Note 1: The maximum input voltage may be exceeded if the maximum input current is limited to 1mA.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C, test circuit, display diode drop = 1.7V, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Lowest Power Mode)	I^+ (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 2)		350	500	µA
Supply Current OPERATING	I^+_{ON}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+		4.5	5	5.5	V
Digit Driver Output Current	I_{DIG}	Common Anode, $V_{OUT} = V^+ - 2.0V$	140	200		mA peak
SEGment Driver Output Current	I_{SEG}	Common Anode, V_{OUT} = +1.5V	-20	-30		mA peak
Digit Driver Output Current	I_{DIG}	Common Cathode, V_{OUT} = +1.0	-50	-70		mA peak
SEGment Driver Output Current	I_{SEG}	Common Cathode, $V_{OUT} = V^+ - 2V$	10	12.5		mA peak
Digit and Segment Leakage Current	I_{LK}	LR Low	-100		+100	µA
ST, RS, UP/DN Input Low Voltage	V_{IL}				0.8	V
ST, RS, UP/DN Input High Voltage	V_{IH}		2.4			V
ST, RS, UP/DN Input Pullup Current	I_P	$V_{OUT} = V^+ - 2V$ (Note 2)	5	25	100	µA
Three Level Input Voltages Input High Input Floating Input Low	 V_{INH} V_{INF} V_{INL}	LR, LC, DC, V^+ = 5V	 4.2 2.0		 2.7 0.6	V
Three Level Impedance	Z_{IN}			100		kΩ
BCD I/O Input High Voltage	V_{BIH}	Common Anode V^+ = 5.0V	1.8			V
		Common Cathode V^+ = 5.0V	$V^+ - 0.6$			V
BCD I/O Input Low Voltage	V_{BIL}	Common Anode V^+ = 5.0V			0.8	V
		Common Cathode V^+ = 5.0V			$V^+ - 1.8$	V
BCD I/O Pullup Current	V_{BPU}	Common Cathode $V_{IN} = V^+ - 2V$ (Note 2)	5	25	300	µA
BCD I/O Pulldown Current	V_{BPD}	Common Anode V_{IN} = +1.3V (Note 2)	5	25	300	µA
BCD I/O, CARRY/BORROW, ZERO, EQUAL Outputs Output High Current	I_{BOH}	$V_{OH} = V^+ - 1.5V$	-1			mA
BCD I/O, CARRY/BORROW, ZERO, EQUAL Outputs Output Low Current	I_{BOL}	V_{OL} = +0.4V	+2			mA

Note 2: The Up/Down, Store, Reset and BCD I/O as inputs have pullup or pulldown devices which typically draw 50µA each when connected to the opposite supply.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C, test circuit, display diode drop = 1.7V, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Count Input Frequency	f_{IN}	V^+ = 5V ± 10%, -20°C < T_A < +70°C	0	5	2	MHz
Count Input Threshold	V_{TH}	V^+ = 5V	0.8	2	3.5	V
Count Input Hysteresis	V_{HYS}	V^+ = 5V		0.5		V
Count Input Leakage	I_{IN}		-1		+1	µA
Display Multiplex Rate	f_{MUX}	Not Loading	100	625		Hz
		Loading	200	—	5000	
Display Scan Oscillator Frequency	f_{DS}	Free-running (SCAN Terminal Open Circuit)		2.5		kHz
Interdigit Blanking Time	t_{idb}		750	3000		ns
Operating Temperature Range	T_A	Industrial Temperature Range	-20		+85	°C

Pin Descriptions

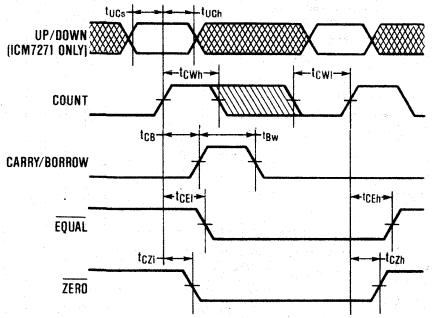
PIN NUMBER		PIN NAME	FUNCTION
COMMON ANODE ICM7217 ICM7271B	COMMON CATHODE ICM7217A ICM7217C		
24	24	V^+	Positive Power Supply. 5V ± 10%
20	19	GROUND	Ground.
28,27,26,25	18,17,16,15	D1,D2,D3,D4	These Digit Drive outputs directly drive the anodes (ICM7217 and ICM7217B) or the cathodes (ICM7217A and ICM7217C) of seven segment LED displays. D1 is the rightmost or least significant digit.
16,21,15,17, 19,18,22	23,27,25,28 22,26,21	Segments A-G	These Segment Drive outputs directly drive 7 segment LED displays. Current limiting resistors are NOT required.
7,6,5,4	7,6,5,4	BCD I/O 1,2,4,8	During normal operation these pins are BCD outputs, whose data corresponds to the count latched into the Store register. The data is multiplexed, digit by digit, going from the most significant digit (1000's) to the least significant digit (1's). The BCD data is valid approximately 6µs before the leading edge of each digit (rising edge of ICM7217/B digit outputs, falling edge of ICM7217A/C common Cathode outputs). During Load Counter and Load Register operations, the BCD I/O pins are inputs. BCD input data is latched by the trailing edge each digit period during Load Counter and Load register operations. The BCD input voltage levels are skewed to allow the use of thumbwheel switches connected to the digit driver to load BCD data. A positive voltage level is an input logic zero for the ICM7217A/C common cathode versions.
8	8	COUNT	Positive-going transitions of the COUNT input increment or decrement the counter, except when RESET is low or a load counter operation is in progress. The COUNT input is compatible with CMOS. TTL compatibility can be ensured by using a 4.7 kilohm pullup resistor on the TTL output. The COUNT input has 500mV of hysteresis, allowing the use of slow risetime input signals.
9	9	STORE	When STORE is low, the counter's contents appear at the LED digit and segment outputs, and at the BCD outputs. When STORE goes high, the current count is latched into the display latch, and that latched data appears at the LED drive and BCD outputs. Store has an internal 25µA pullup.
10	10	UP/DOWN	The counter counts up with each rising edge of Count when UP/DOWN is high. Conversely, the counter decrements with each rising edge of Count when UP/DOWN is low. UP/DOWN must be set up 300 nanoseconds before the rising edge of Count, and must be held stable for 750 nanoseconds after the rising edge of Count. Transitions on UP/DOWN during the 750 nanoseconds after the rising edge of Count may erroneously increment or decrement the upper counter stages.

4 Digit (LED) Presettable Up/Down Counter

Pin Descriptions

PIN NUMBER		PIN NAME	FUNCTION
COMMON ANODE ICM7217 ICM7271B	COMMON CATHODE ICM7217A ICM7217C		
14	14	RESET	Driving RESET low resets the counter to 0000. RESET does not clear the display latch unless both RESET and STORE are low. Since the RESET operation is performed by placing 0 on the internal BCD data bus and presetting all four counter stages, simultaneous RESET and Load register operations will load 0000 into the comparison registers. To avoid erroneous loading of zeroes into the comparison register, do not take RESET low unless LOAD REGISTER has been low or floating for at least 5 milliseconds. The RESET input has an internal 25μA pullup, but it should be actively driven or pulled up with an external 4.7 kilohm when the ICM7217 is used in electrically noisy environments.
1	1	CARRY/BORROW	The CARRY/BORROW output is a short positive going pulse (typically 1μs long) that occurs at the 9999 to 0000 transition when counting up, and the 0000 to 9999 transition when counting down. The CARRY/BORROW output is used to drive the COUNT input of a second ICM7217 in an 8 digit counter.
2	2	ZERO	This output is low whenever the counter's contents are 0000, independent of the display latch contents. The ZERO output is not valid during a load counter operation (while LOAD COUNTER is high and for 5 milliseconds after LOAD COUNTER was high).
3	3	EQUAL	This output is low whenever the counter's contents equals the contents of the comparison register. This output is not valid during Load Counter and Load Register operations (while LOAD COUNTER or LOAD REGISTER is high, and for 5 milliseconds after either LOAD COUNTER or LOAD REGISTER was high).
13	13	SCAN	In most applications, the scan pin is left floating and the internal multiplex scan frequency of 2500Hz is used. Connecting a capacitor between V^+ and the SCAN pin lowers the multiplex oscillator frequency. If desired, the SCAN pin can be externally driven. The internal digit multiplex counter advances with each positive-going edge at SCAN, and the digit outputs are enabled only while the SCAN pin is low. LED display brightness can be controlled by varying the duty cycle at the SCAN input. The SCAN pin is internally disconnected and the internal oscillator is used during Load Counter and Load Register operations. This increases the scan frequency to 8kHz, reducing the time required for a load counter or load register operation.
23	20	DISPLAY CONTROL	This is a three-level input with internal 100 kilohm resistors which bias the pin to 2.5V when it is floating. Leading Zero Blanking is enabled when this pin is floated or driven to 2.5V. Leading Zero Blanking is inhibited when this pin is connected to Ground. The segment drivers are disabled and the LED display is blanked when this pin is connected to V^+. BCD outputs and digit outputs remain active.
11	11	LOAD REGISTER/OFF	This is a three-level input. Leave the pin floating or drive it to 2.5V for normal operation. Connect the LOAD REGISTER/OFF pin to ground to put the ICM7217 into the shutdown mode. This puts the segments drivers, the digit drivers, and the BCD I/O into a high impedance state. The ICM7217 will continue to count normally while in the shutdown mode. A high pulse (100ns minimum) starts the LOAD REGISTER operation. The SCAN pin is disconnected from external circuitry and the multiplex counter is reset to D4. The digits are then scanned in the sequence D4, D3, D2, D1; and the internal comparison register is loaded with the data present at the BCD I/O pins at the end of each digit period. At the end of the D1 digit period, the LOAD REGISTER is still high. If thumbwheel switches are connected as shown in Figure 1, the value on the thumbwheel switches is loaded into the comparison register.
12	12	LOAD COUNTER/ I/O OFF	The LOAD COUNTER/I/O OFF pin is a three-level input. Leave it floating or drive it to 2.5V for normal operation. Connecting LOAD COUNTER/I/O OFF to ground puts the BCD output into a high impedance state, but does not affect the LED drive outputs. A high pulse (100ns minimum) starts the LOAD COUNTER operation. The LOAD COUNTER operation presets counter contents to the value on the thumbwheel switches (Figure 1), in the same manner as the load register operation described above.

4 Digit (LED) Presettable Up/Down Counter



ICM7217/COUNT and Output Timing

SYM.	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{UCs}	UP/$\overline{DOWN}$ setup time (min.)		300		ns
t_{UCh}	UP/$\overline{DOWN}$ hold time (min.)		750		ns
t_{CWh}	COUNT pulse high (min.)		100	250	ns
t_{CWi}	COUNT pulse low (min.)		100	250	ns
t_{CB}	COUNT to CARRY/ BORROW delay		750		ns
t_{Bw}	CARRY/ BORROW pulse width		100		ns
t_{CEI}	$\overline{COUNT}$ to EQUAL delay		500		ns
t_{CZI}	$\overline{COUNT}$ to $\overline{ZERO}$ delay		300		ns

Typical Applications

Four Digit, Preset and Predetermining Counter

The test circuits, Figures 1 and 2, are complete four digit up/down counters with preset and predetermining (comparison) capability. Momentarily pressing the Load Counter switch will preset the counter to the number set into the thumbwheel switches. Similarly, momentarily pressing the Load Register switch will load the predetermining or comparison register with the number set into the thumbwheel switches.

When the Store switch is closed, the displayed count follows the counter. Opening the Store switch "freezes" the display at the current count. Closing the Reset switch at any time clears the counter to 0000.

The ZERO output goes low whenever the counter content is 0000, and the EQUAL output goes low whenever the count reaches the value in the predetermining or comparison register.

Eight Digit Counter

The CARRY/BORROW output is used to cascade two 4 digit counter sections to form an eight digit counter. If leading zero blanking is desired, drive the Display Control pin of the least significant ICM7217 with an NPN transistor whose base is connected to the Zero output of the most significant ICM7217.

Multiple Setpoints

Analog switches such as the CD4066 can drive the BCD I/O pins. In Figure 3, the number set on thumbwheel switch A is loaded into the comparison register, the number on thumbwheel switch B presets the counter.

Trailing Zero Display

In some applications leading zero blanking is desired, but a count of 0000 must result in a display of a single 0 in the rightmost digit. Figure 4 performs this task by driving Display Control to the "disable leading zero blanking" state whenever digit D1 is active.

Batch Counter or Divide by N Counter

The circuit of Figure 5A will put out a pulse each time the count reaches the number loaded into the comparison register.

RESET is taken low each time the count reaches the preset number, resetting the counter to 0000. The AND gate is used for feedback to RESET, since a simple RC circuit can "lockup" if the comparison register is loaded with 0000.

Figure 5B is a similar circuit, except that the counter counts down, and is preset each time the count reaches zero. Since the Load Counter (preset) operation may take as long as 5 milliseconds, this circuit should be used only with signals of 12,000 counts per minute (200Hz) or less.

4 Digit (LED) Presettable Up/Down Counter

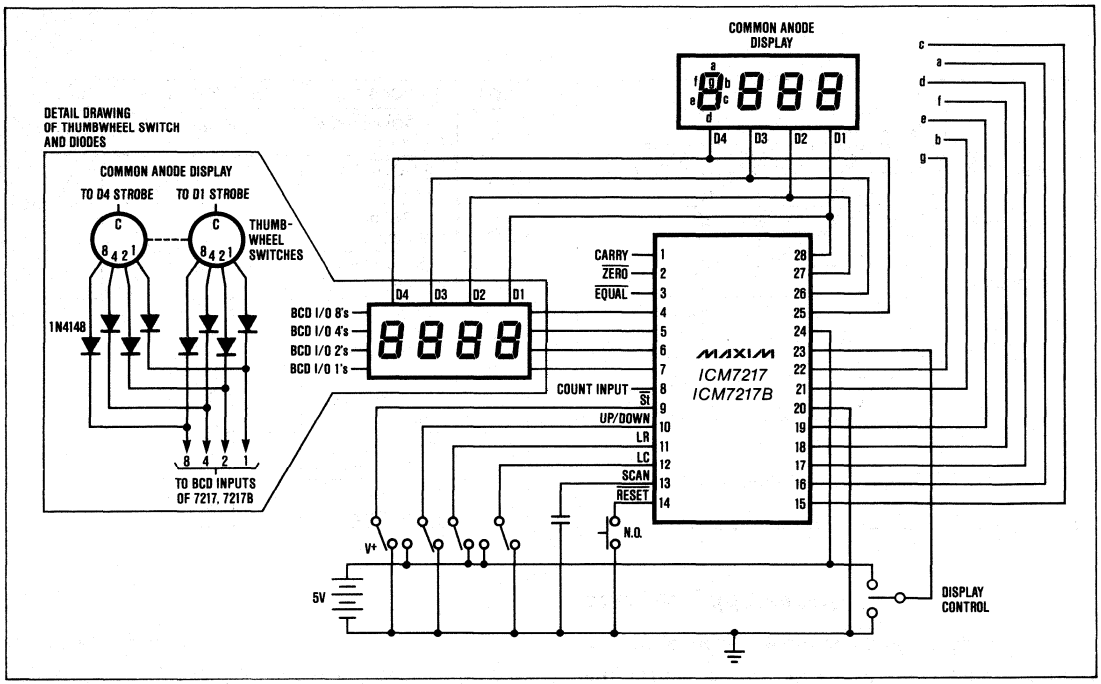


Figure 1. Basic Up/Down Counter with Common Anode LED Display.

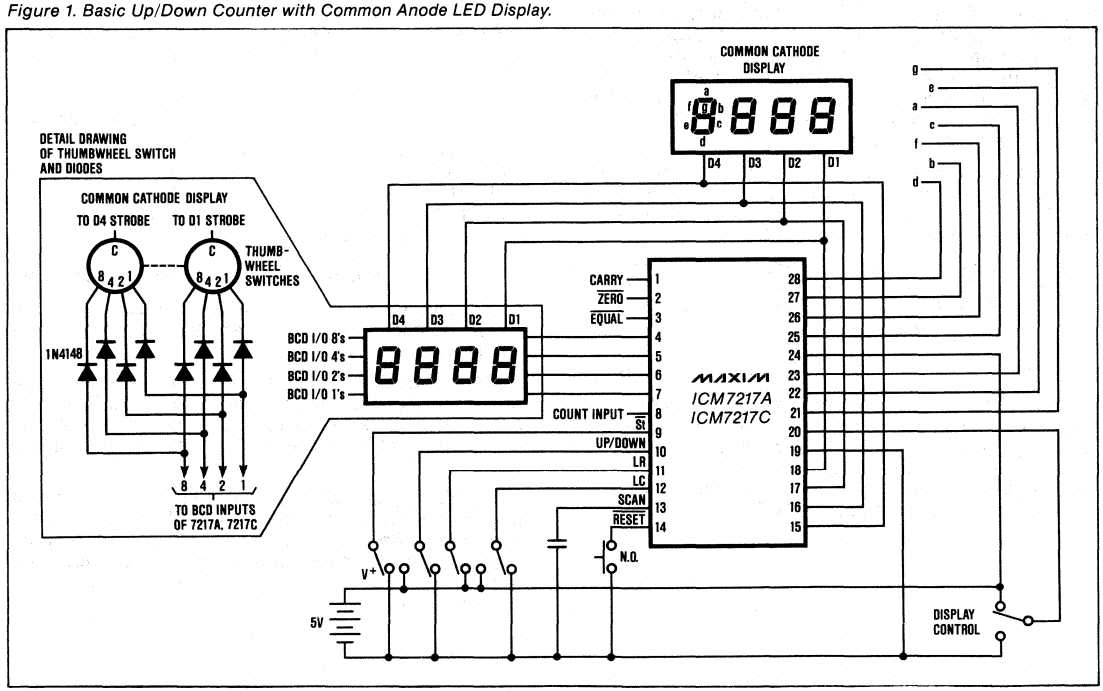


Figure 2. Basic Up/Down Counter with Common Cathode LED Display.

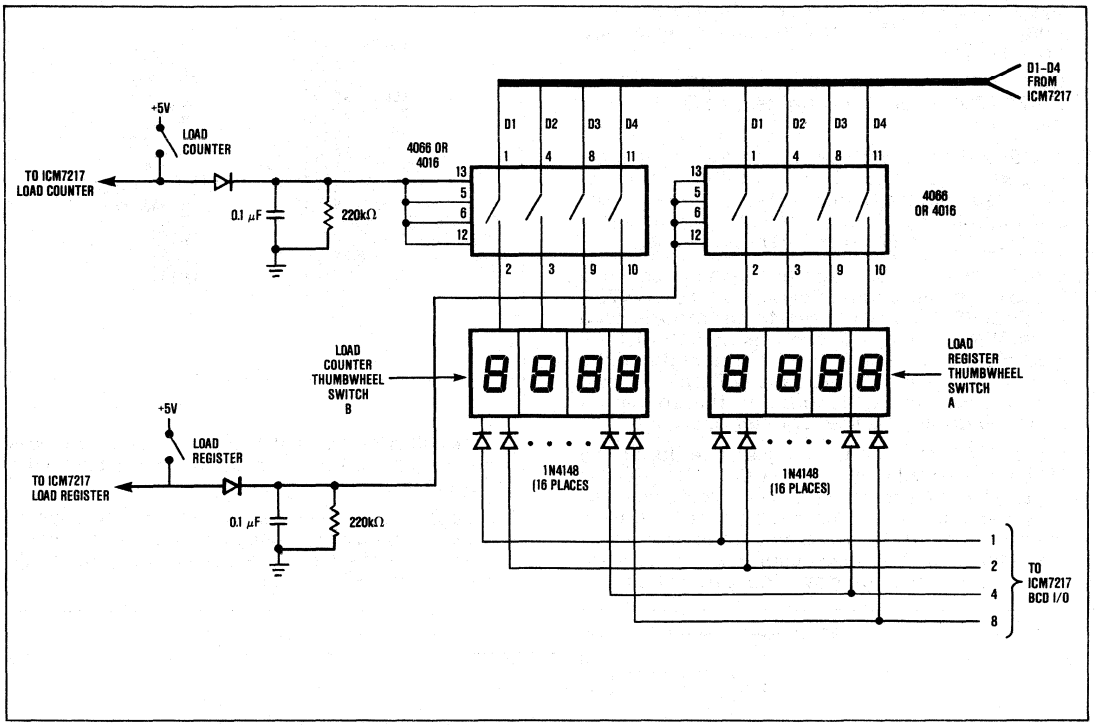


Figure 3. Multiple Thumbwheel Switches

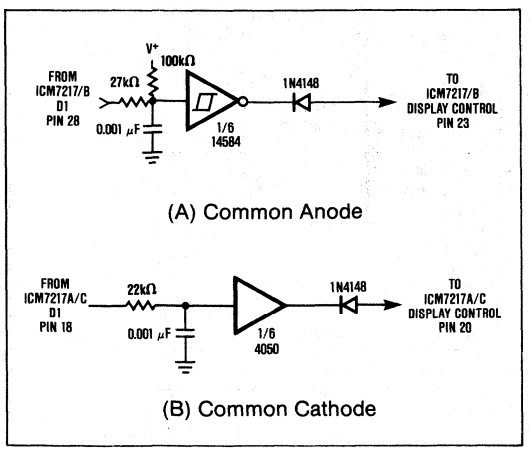


Figure 4. Trailing Zero Display

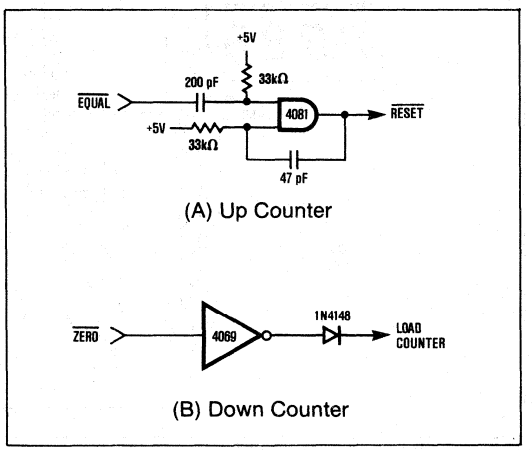


Figure 5. Connections for Divide-By-N Batch Counters.

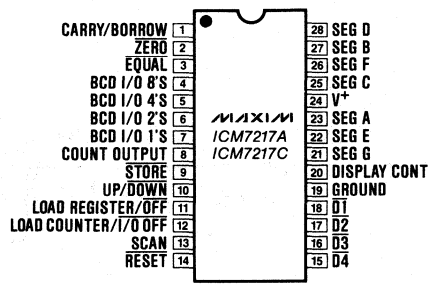
4 Digit (LED) Presettable Up/Down Counter

Application Hints

1. Use a minimum of 47μF in parallel with a 0.1μF ceramic bypass capacitor between V^+ and ground, in the immediate vicinity of the ICM7217. This bypassing is required to reduce the power supply ripple created by the high current multiplexed LED drive signals.
2. Use the Common Anode versions (ICM7217 and ICM7217B) where the brightest LED display is desired.
3. The SCAN pin can be used to control digit sequencing while reading BCD output data with a microprocessor, but the SCAN pin is disconnected and the multiplex rate is increased to 2kHz during the load register and load counter operations.
4. Load counter and load register operations continue for up to 5 milliseconds after the LOAD COUNTER or LOAD REGISTER pin has returned to the floating state. During this 5 millisecond period, RESET will load a zero into some or all of the digits of the counter or register. EQUALS and ZERO are not valid during this loading period, and the counter is inhibited during the load counter operation.
5. If the UP/DOWN input changes state during the 750ns after a positive transition at COUNT, the upper digits of the counter may be erroneously incremented or decremented. This is caused by the transmission of erroneous carry/borrow signals to adjacent digits when major bit changes occur in a digit counter coincident with an up/down input transition.
6. If the 200ns STORE high to RESET low setup time is not met, RESET may clear some of the bits in the display latch.
7. Data cannot be transferred directly from the counter to the comparison register. Use a 74C915 7-segment-to-BCD reverse decoder between the segment outputs and the BCD inputs.

Pin Configuration

Top View



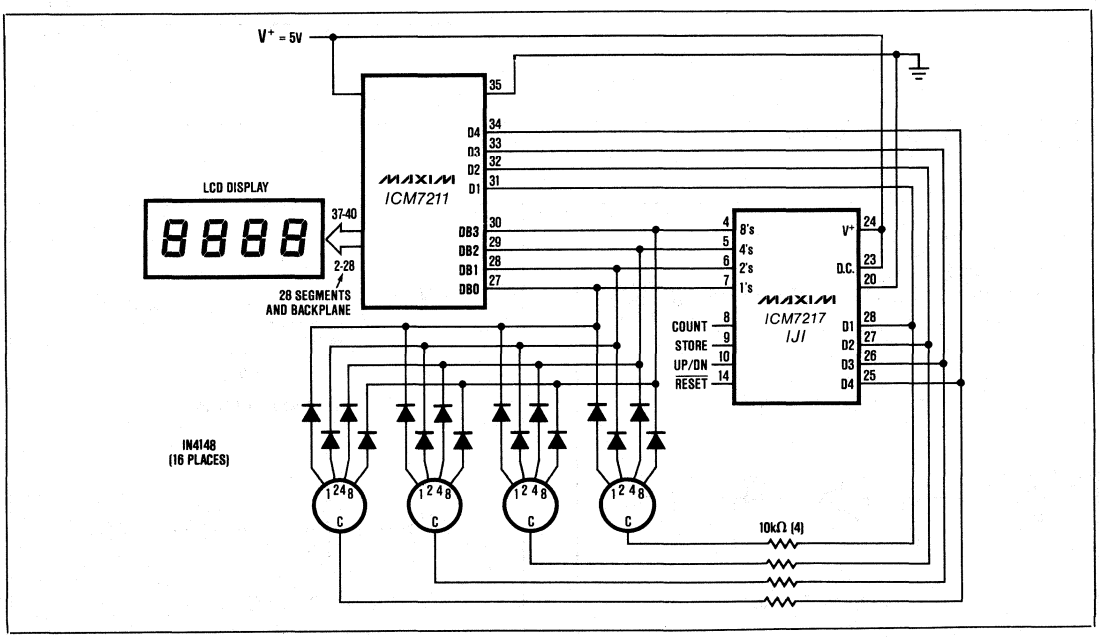


Figure 7. LCD Interface using ICM7211

MAXIM

8 Digit LED Display Driver

General Description

The Maxim ICM7218 display driver interfaces microprocessors to an 8 digit, 7 segment, numeric LED display. Included on chip are two types of 7 segment decoders, multiplex scan circuitry, segment and digit drivers, and an 8 × 8 static memory.

The ICM7218A and ICM7218B accept data in a serial format and drive common anode (ICM7218A) or common cathode (ICM7218B) displays. The ICM7218C and ICM7218D accept data in a parallel format and drive common anode (ICM7218C) or common cathode (ICM7218D) displays. All four versions can display the data in either hexadecimal or code B format. The ICM7218A and ICM7218B also feature a No Decode mode where each individual segment can be independently controlled. This is particularly useful in driving bar graphs.

The Maxim ICM7218 is an alternative for both the Intersil ICM7218 and ICM7228. When ordering, specify ICM7218 for both devices.

Applications

Instrumentation

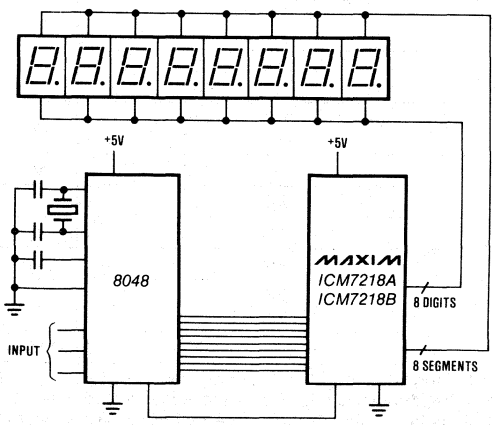
Test Equipment

Hand Held Instruments

Bargraph Displays

Panel Meters

Typical Operating Circuit



8 Digit Microprocessor Display

Features

- **Improved 2nd Source! See 3rd page of this data sheet for our "Maxim Advantage™"**
- **Fast Access Time: 200ns Write Pulse Width**
- **Microprocessor Compatible**
- **Hexadecimal and Code B Decoders**
- **Individual Segment Control with "No Decode" Feature**
- **Digit and Segment Drivers On-Chip**
- **Common Anode and Common Cathode LED versions available**
- **Low Power CMOS**

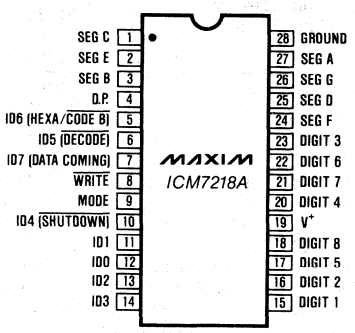
Ordering Information

PART	TEMP. RANGE	PACKAGE*
ICM7218AIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218AIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218BIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218BIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218CIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218CIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218DIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218DIJI	-20°C to +85°C	28 Lead CERDIP

(Ordering Information Continued on Last Page.)

Pin Configuration

Top View



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

8 Digit LED Display Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 500mA
Segment Output Current 100mA
Input Voltage (any terminal) ..... V^+ + 0.3V to GND -0.3V (Note 1)
Power Dissipation (28 Pin CERDIP) ..... 1.0W (Note 2)
Power Dissipation (28 Pin Plastic with Copper Leadframe) ..... 1.0W (Note 2)
Power Dissipation (28 Pin Quad Pack) ... 0.8W (Note 2)
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -65°C to 160°C
Lead Temperature (Soldering 10 sec) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = 5V ± 10%, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V^+	Power Down Mode	4 2		6 6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	µA
Operating Supply Current	I_{OP}	Decoder On, Outputs Open Ckt No Decode, Outputs Open Ckt	250 200		950 450	µA
Digit Drive Current	I_{DIG}	Common Anode V_{OUT} = V^+ - 2.0V Common Cathode V_{OUT} = V^- + 1V	-170 50			mA
Digit Leakage Current	I_{DLK}				100	µA
Peak Segment Drive Current	I_{SEG}	Common Anode V_{OUT} = V^- + 1.5V Common Cathode V_{OUT} = V^+ - 2.0V	20 -10	25		mA
Segment Leakage Current	I_{SLK}				50	µA
Display Scan Rate	f_{MUX}	Per Digit		250		Hz
Three Level Input Logical "1" Input Voltage Floating Input Logical "0" Input Voltage	 V_{INH} V_{INF} V_{INL}	 Hexadecimal ICM7218C, D (Pin 9) Code B ICM7218C, D (Pin 9) Shutdown ICM7218C, D (Pin 9)	 4.0 2.0		 3.0 1.75	V
Three Level Input Impedance	Z_{IN}	Note 3		100		kΩ
Logical "1" Input Voltage Logical "0" Input Voltage	V_{IH} V_{IL}		3.5		 0.8	V
Write Pulse Width (Negative) Write Pulse Width (Positive)	t_W $t_{\overline{W}}$	7218A, B	550 550	400 400		ns
Write Pulse Width (Negative) Write Pulse Width (Positive)	t_W $t_{\overline{W}}$	7218C, D	400 400	250 250		ns
Mode Hold Time	t_{mh}	7218A, B		150		ns
Mode Pulse Width	t_m	7218A, B	500			ns
Data Set Up Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		25			ns
Digit Address Set Up Time Digit Address Hold Time	t_{das} t_{dah}	ICM7218C, D ICM7218C, D	500 100			ns
Data Input Impedance	Z_{IN}	5-10pF Gate Capacitance		10^{10}		Ohms

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

Note 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

Note 3: In the ICM7218C and D (random access versions) the Hexa/Code B/Shutdown Input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50µA. The ICM7218A and B devices do not have these biasing resistors and thus are not subject to this condition.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983, 1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The Electrical Characteristics Table along with the descriptive excepts from manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

8 Digit LED Display Driver

- ◆ 200ns Write Pulse Width
- ◆ Zero Hold Time - Mode, Data and Address
- ◆ Single Digit Update Mode ICM7218A, B
- ◆ Guaranteed Interdigit Blanking Time
- ◆ Increased LED Display Drive Current
- ◆ Improved ESD Protection (Note 4)
- ◆ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V^+	-20°C ≤ T_A ≤ +85°C Operating Data Retention	4 2		6 6	V
Shutdown Supply Current	I_Q	ICM7218A, B ICM7218C, D (3 level input open)		5 25	300 300	µA
Operating Supply Current	I_{OP}	**Decoding all 8's, display open** **No Decode, display outputs open** **Display blank, driving display** Decoding all 8's and D.P.s, driving display		**200** **200** **200** 240	**450** **450** **450**	**µA** **µA** **µA** mA
Digit Drive Current	I_{DIG}	**Common Anode V_{OUT} = V^+ - 2.0V** Common Cathode V_{OUT} = 1.0V	**-200** 50	**-300** 70		**mA** mA
Digit Leakage Current	I_{DLK}	Shutdown, V^+ = 5V Common Anode, V_{OUT} = 0V Common Cathode, V_{OUT} = 5V		-10 10	-100 100	µA µA
Peak Segment Drive Current	I_{SEG}	Common Anode V_{OUT} = 1.5V Common Cathode V_{OUT} = V^+ - 2.0V	20 -10	30 -20		mA
Segment Leakage Current	I_{SLK}	Shutdown, V^+ = 5V Common Anode, V_{OUT} = 5V Common Cathode, V_{OUT} = 0V		-1 1	-50 50	µA µA
Input Leakage Current	I_{IL}	**All inputs except pin 9 of ICM7218C, D** **V^+ = 5V, -20°C ≤ T_A ≤ +85°C** **V_{IN} = 0V** **V_{IN} = 5V**		**-0.01** **0.01**	**-1** **1**	**µA** **µA**
Display Scan Rate	f_{MUX}	**V^+ = 5V**	**75**	**250**		**Hz**
Interdigit Blanking Time	t_{idb}	**V^+ = 5V**	**2**	**10**		**µs**
Three Level Input	V_{INH} V_{INF} V_{INL}	Pin 9, ICM7218 C, D only, V^+ = 5V Input "high" voltage Floating input Input "low" voltage	 4.2 2.0		 3.0 0.8	 V V V
Three Level Input Impedance	Z_{IN}	**Pin 9, ICM7218C, D only**	**50**	**100**		**kΩ**
Input High Voltage Input Low Voltage	V_{IH} V_{IL}	All inputs except pin 9 of ICM7218C, D -20°C ≤ T_A ≤ +85°C	2.0		 0.8	V V
Write Pulse Width (Low)	t_{wl}		**200**	**100**		**ns**
Write Pulse Width (High)	t_{wh}		1.0			µs
Input Setup Time	t_{ids}	**All inputs except pin 9 of ICM7218C, D (Note 5)**	**250**	**150**		**ns**
Input Hold Time	t_{idh}	**All inputs except pin 9 of ICM7218C, D (Note 5)**	**0**	**-20**		**ns**

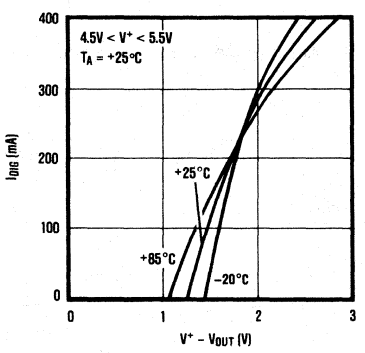
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883B Method 3015.1 Test Circuit).

Note 5: This specification replaces the original manufacturer's separate specifications for data, address, and mode inputs.

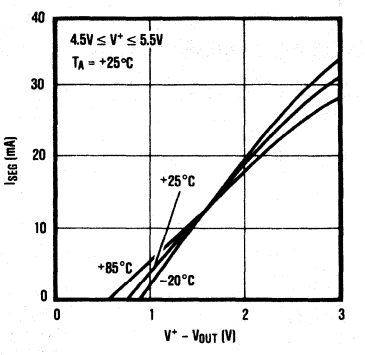
8 Digit LED Display Driver

Typical Operating Characteristics

COMMON ANODE DIGIT DRIVER
I_{DIG} VS. ($V^+ - V_{OUT}$)

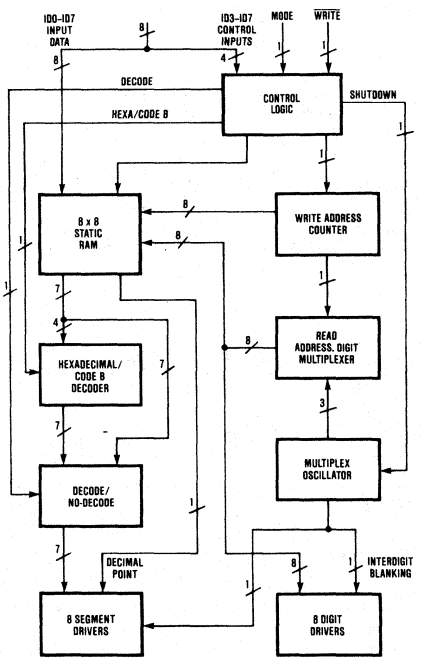


COMMON CATHODE SEGMENT DRIVER
I_{SEG} VS. ($V^+ - V_{OUT}$)



ICM7218 BLOCK DIAGRAMS

ICM7218A/B



ICM7218C/D

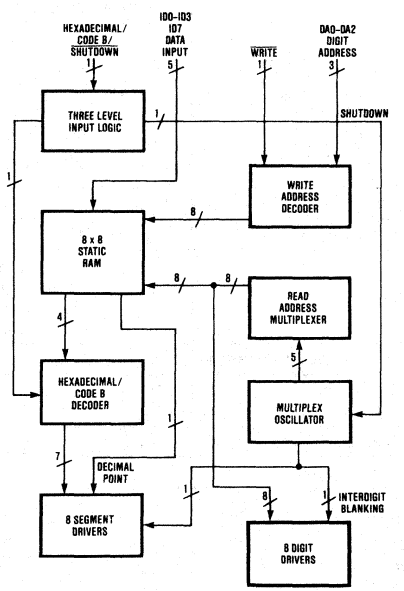


Table 1. Input Definitions, ICM7218A and ICM7218B
Note: Pin Configurations for the ICM7218A/B are shown on last page.

INPUT	PIN	STATE	FUNCTION
WRITE	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
MODE	9	High Low	Loads Control Word on WR Loads Input Data on WR
ID0–ID2, DIGIT ADDRESS	12, 11, 13	High Low	Loads "one" Loads "zero"
ID3, BANK SELECT	14	High Low	Select RAM Bank A (Hex or Code B Select RAM Bank B Data only)
ID4, SHUTDOWN (MODE High)	10	High Low	Normal Operation Shutdown
ID5, DECODE/NO DECODE (MODE High)	6	High Low	No Decode Decode
ID6, HEX/CODE B (MODE High)	5	High Low	Hexadecimal Decoding Code B Decoding
ID7, DATA COMING (MODE High)	7	High Low	Data Coming (control word) No Data Coming (control word)
ID0–ID7, INPUT DATA (MODE Low)	5–7, 10–14	High Low	Loads "one" (Note 1) Loads "zero" (Note 1)

Note 1: A "zero" or low level on ID7 turns ON the decimal point. In the NO DECODE mode, a "one" or high input turns ON the corresponding segment, except for the decimal point which is turned OFF by a high level on ID7.

Detailed Description

Input Data Formats

The ICM7218A and ICM7218B have three possible data formats: Hexadecimal, Code B, and No Decode. Figure 7 lists the character sets for the decode modes.

The data format of the ICM7218A/B is selected by writing to bits ID4, ID5, and ID6 of the control register (See Table 1, Input Definitions). Hexadecimal and Code B data is entered via ID0–ID3 while ID7 controls the decimal point.

The No Decode mode of the ICM7218A and ICM7218B allows the direct segment-by-segment control of all 64 segments driven by the ICM7218. In the No Decode mode, the inputs directly control the outputs as follows:

Data Input	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Controlled Segment	Decimal Point	A	B	C	E	G	F	D

An input high level turns on the respective segment, except for the decimal point, which is turned on by an input low level on ID7.

The ICM7218C and ICM7218D have only Hexadecimal and Code B formats. The MODE input, pin 9, a three level input, selects the Hexadecimal format when driven high, the Code B format when floating or driven to mid-supply, and the shutdown mode when driven low.

Shutdown and Display Blanking

When shutdown, the ICM7218 enters a low power standby mode which typically uses only 10μA of supply current. In this mode the ICM7218 turns off the multiplex scan oscillator as well as the digit and segment drivers, however input data can still be entered when in the shutdown mode. Data is retained in memory even with the supply voltage as low as 2V. The ICM7218A/B is shutdown by writing a control word with Shutdown (ID4) low. The ICM7218C/D is put into shutdown mode by driving MODE low.

The ICM7218 operating current with the display blanked is 200μA. All versions of the ICM7218 can be blanked by writing Hex FF to all digits and selecting Code B format. The ICM7218A and ICM7218B can also be blanked by selecting No Decode mode and writing Hex 80 to all digits.

Microprocessor Interface, ICM7218A and ICM7218B

All Maxim ICM7218A/B inputs, including MODE, feature a 250ns minimum data setup and 0ns hold time. With a 200ns minimum write pulse, the ICM7218 can directly interface to most microprocessor buses. Input logic levels are TTL and CMOS compatible. Figure 8 shows a typical method of driving the ICM7218A/B

8 Digit LED Display Driver

Table 2. Input Definitions, ICM7218C and ICM7218D
Note: Pin Configurations for the ICM7218C/D are shown on last page.

INPUT	PIN	STATE	FUNCTION
WRITE	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
MODE (Note 1)	9	High Float Low	Hexadecimal Decode Code B Decode Shutdown
DA0-DA2, DIGIT ADDRESS	5, 6, 10	High Low	Loads "ones" Loads "zeros"
ID0-ID3, INPUT DATA and ID7, D.P.	11-14 7	High Low	Loads "ones" Loads "zeros"

Note 1: Pin 9 of the ICM7218C and ICM7218D controls the selection of Hex, Code B, and Shutdown modes and is independent of the WRITE pulse.
Note 2: A "zero" or low level on ID7 turns ON the decimal point segment.

from a microprocessor bus. The MODE input is driven by A0 and writing to an odd address updates the control register.

The ICM7218A/B has three data entry modes: control word update without data update, 8 digit data update, and single digit data update. In all three modes the control register is first updated by pulsing the WRITE input while the MODE input is high, thereby latching data into the control register. The control register selects Shutdown, Decode/No Decode, and Hex/Code B operation as shown in Table 1. A unique feature of the Maxim ICM7218A/B is that there are two banks of internal RAM in the Hexadecimal and Code B display formats. ID3 selects which bank of the internal RAM is displayed.

The logic state of DATA COMING (ID7) is also latched during a control register update. If the latched value of DATA COMING (ID7) is high, the display is blanked and an 8 digit data update is initiated. The next 8 write pulses latch data into the 8 bytes of RAM onboard the ICM7218A/B, starting with digit 1 and ending with digit 8. After the eighth write pulse, the display unblanks and the new data is displayed. Additional write pulses after the eighth pulse are ignored. All 8 digits are displayed in the data format (Hex/Code B/No Decode) specified by the control word that preceded the 8 digit update.

The control register can be rewritten without updating all 8 digits by writing to the ICM7218A/B with MODE high and DATA COMING low. No further action is necessary.

Single Digit Update Mode

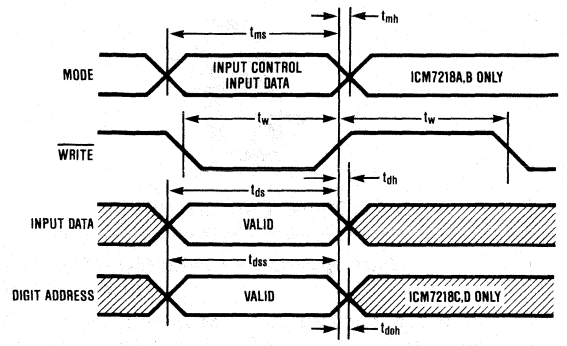
The Maxim ICM7218A/B has a "single digit update" mode which allows one digit to be changed without updating the entire display. First the control register is updated with MODE high, DATA COMING (ID7) low, the desired data format on ID4 and ID6, and the address of the digit to be updated on data lines ID0-ID2 (See Table 3). A second write to the ICM7218, this time with MODE low, transfers the data from ID0-ID7 into the selected digit's RAM location. The data format (Hex/Code B/No Decode) can be specified independently for each digit when in the single digit update mode.

Compatibility with the Intersil ICM7218A and ICM7218B

The Maxim ICM7218A/B is upwardly compatible with the Intersil ICM7218A/B. The Maxim ICM7218A/B adds two functions: bank select and single digit update.

ID0-ID3 are "don't care" when writing a control word to the Intersil ICM7218A/B. When writing a control word to the Maxim ICM7218A/B, ID0-ID2 select the address for a single digit update, while ID3 selects either bank A or bank B for Hex and Code B data. ID3 is a "don't care" for No Decode data. The bank select feature is upwardly compatible with the Intersil ICM7218A/B; software written for the Intersil ICM7218A/B will work with the Maxim ICM7218A/B provided all control word updates have the same value for ID3, either high or low.

The single digit update is upwardly compatible; it is an invalid operation with the Intersil ICM7218A/B and is unlikely to occur in software originally written for the Intersil ICM7218A/B.



Notes:
1. $t_{ms} = t_{ds} = t_{das} \geq 250ns$
2. $t_{mh} = t_{dh} = t_{dah} \geq 0ns$
3. $t_w \geq 200ns$
4. WRITE is rising edge sensitive, not level sensitive.

Figure 3. Write Cycle Timing

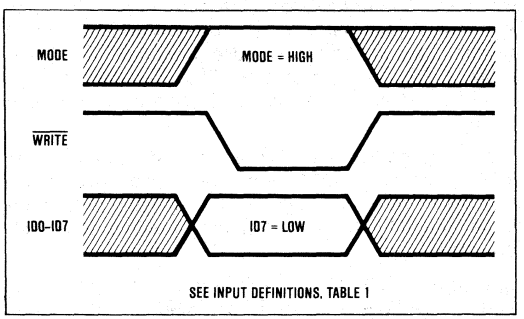


Figure 4. Control Word Update Timing—ICM7218A/B

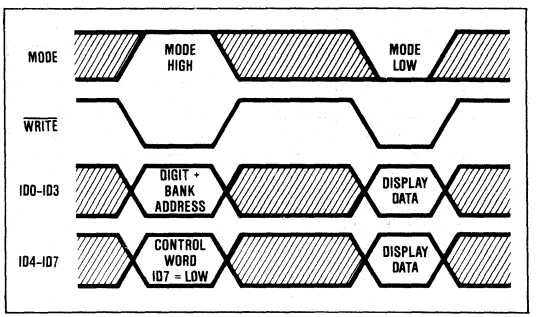
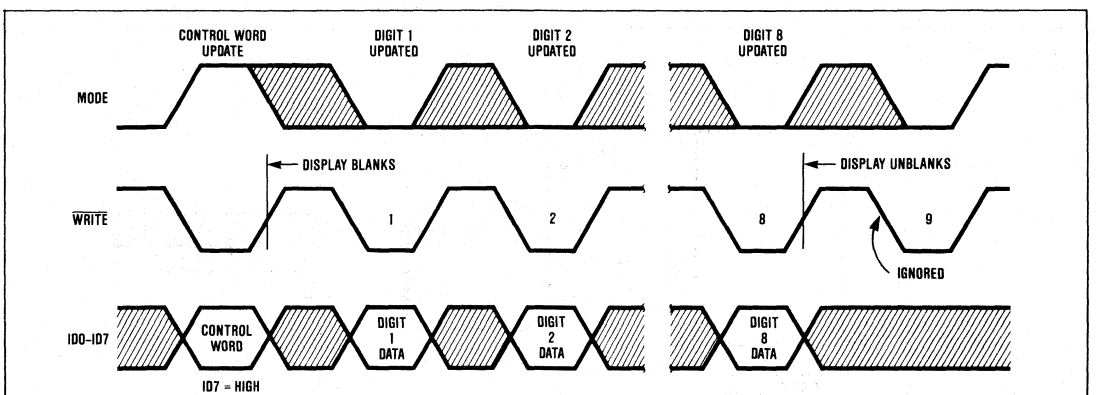


Figure 5. Single Digit Update Timing—ICM7218A/B



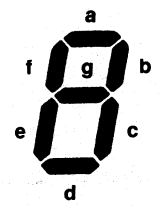
Notes:
1. Any write cycle with Mode high restarts data entry sequence at Control Word Update.
2. Display blanked by Control Word with Data Coming (ID7) high.
3. Display unblanks with rising edge of WRITE to Digit 8.

Figure 6. 8 Digit Update Timing—ICM7218A/B

8 Digit LED Display Driver

ID3	ID2	ID1	ID0	HEXADECIMAL	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(Blank)

Figure 7. Display Font



Segment Assignments

Microprocessor Interface, ICM7218C and ICM7218D

All Maxim ICM7218C and IMC7218D inputs are TTL and CMOS compatible with the exception of the three-level input, HEX/CODE B/SHUTDOWN (Pin 9). All other data and address inputs have identical 250ns setup and 0ns hold times. The minimum write pulse width is 200ns, allowing direct interface to most microprocessor buses. Figure 9 shows a typical ICM7218C/D bus interface. The 8 digits of the ICM7218C/D are addressed as 8 contiguous bytes of RAM.

The interface to the ICM7218C and ICM7218D is similar to that of a RAM. Select the digit to be updated with the address lines DA0-DA2, place the data to be written on ID0-ID3 and ID7, then pulse the WRITE input low.

Since the ICM7218C/D does not have a control register, Hexadecimal or Code B font selection and shutdown mode are directly controlled through the three-level input at Pin 9. The ICM7218C/D does not have a No Decode mode.

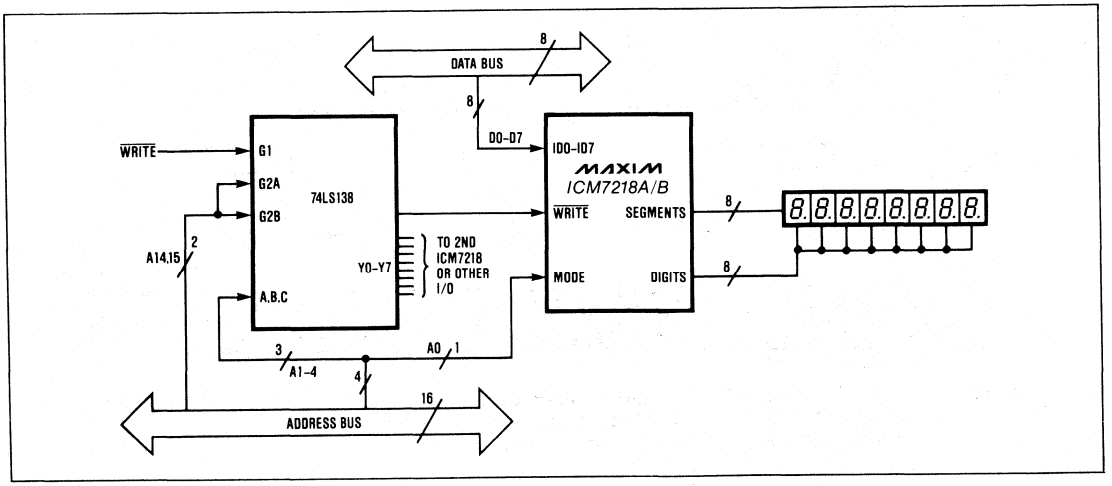


Figure 8. ICM7218A/B µP Bus Interface

Applications Information

Common Anode Display Interface, ICM7218A and ICM7218C

The common anode digit and segment driver output schematics are shown in Figures 10 and 11. The common anode digit driver output impedance is approximately 4 ohms. This provides a nearly constant voltage to the display digits. The N-channel segment driver output impedance of 50Ω limits the segment current to approximately 30mA peak current per segment. Segment current limiting resistors are NOT required. Both the segment and digit outputs can directly drive the display.

Each segment's current is not significantly affected by whether other segments are on or off. This is because the segment driver output impedance is much higher than that of the digit driver. This feature is important in bar graph applications, where each bar graph element should be the same brightness, independent of the number of elements turned on.

Common Cathode Display Interface, ICM7218B and ICM7218D

The common cathode digit and segment driver output schematics are shown in Figures 12 and 13. The N-channel digit drivers have an output impedance of approximately 15Ω. The NPN segment drivers have an output impedance of approximately 75 ohms. The common cathode display driver output currents are only 1/4 the common anode display driver currents. Therefore, the ICM7218A and ICM7218C common anode display drivers are recommended for those applications where high brightness is desired. The ICM7218B and ICM7218D common cathode display drivers are suitable for driving bubble-lensed monolithic 7 segment displays. They can also drive individual LED displays up to 0.3" height when high brightness is not required.

Table 3. Digit Addressing

DATA LINES ID2	ID1	ID0	Selected Digit
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	D6
1	1	0	D7
1	1	1	D8

Display Multiplexing

Each digit of the ICM7218 is on for approximately 500μs, with a multiplexing frequency of approximately 250Hz. The interdigit blanking time is 10μs typical, 2μs minimum. The Maxim ICM7218 turns off both the digit drivers and the segment drivers during the interdigit blanking period. The digit multiplexing sequence is: D1, D7, D8, D6, D4, D3, D2, and D5.

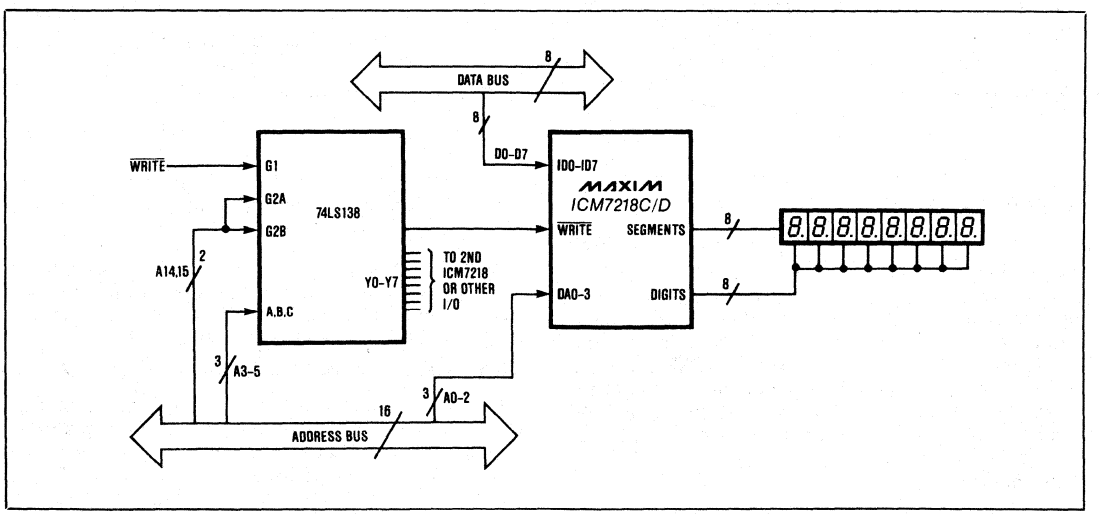


Figure 9. ICM7218C/D μP Bus Interface

8 Digit LED Display Driver

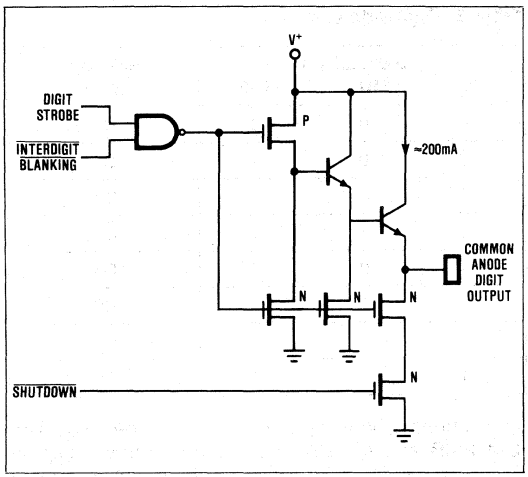


Figure 10. Common Anode Digit Driver

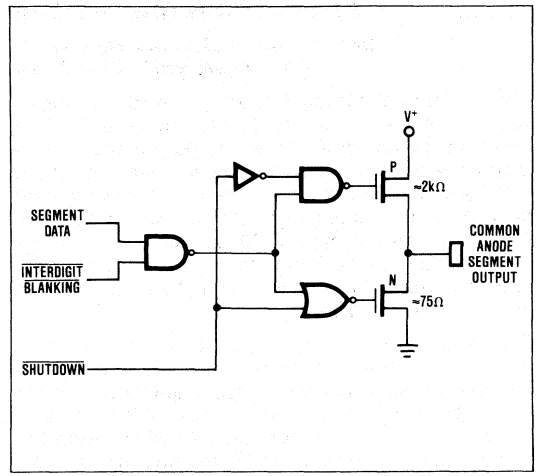


Figure 11. Common Anode Segment Driver

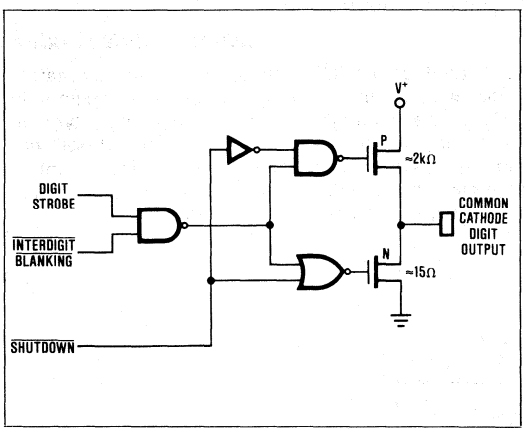


Figure 12. Common Cathode Digit Driver

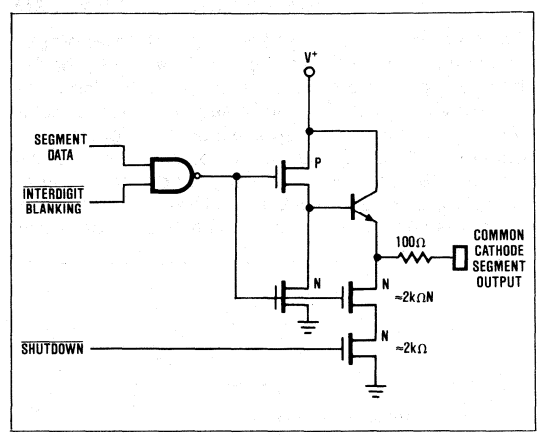


Figure 13. Common Cathode Segment Driver

Driving Larger Displays

If very high display brightness is desired, the ICM7218 display driver outputs can be externally buffered. Figures 14 and 15 show how to drive either common anode or common cathode displays using the ICM7218B or ICM7218D. The Maxim ICM7218 has a guaranteed 2μs interdigit blanking time. This eliminates the ghosting (faint display of the data from another digit) that would occur if the external buffer turnoff time were to overlap the beginning of the next digit period.

Another method of doubling display currents is to connect two digit outputs together and load the same data into both digits. This drives the display with the same peak current, but the average current doubles because each digit of the display is on for twice as long, i.e. for 1/4 duty cycle rather than 1/8.

Three Level Input, ICM7218C and ICM7218D.

As shown in Table 1, pin 9 controls three functions: Hexadecimal display decoding, Code B display decoding, and shutdown mode. In many applications pin 9 will be permanently wired to one state. When pin 9 cannot be permanently left in one state, use the circuits illustrated in Figure 16 to drive this three level input.

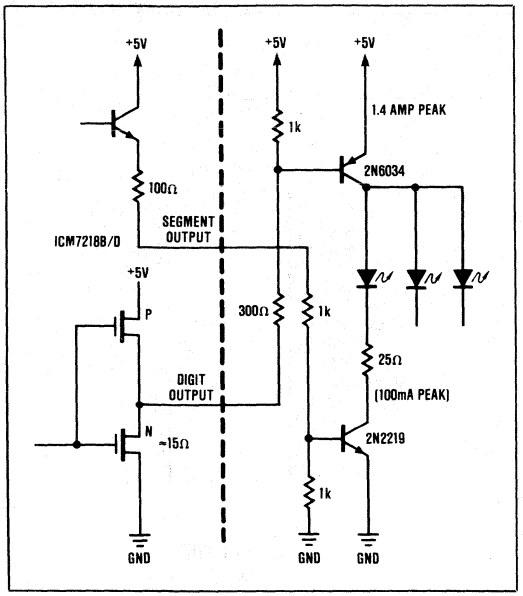


Figure 14. Driving Larger Common Anode Displays with External Transistors

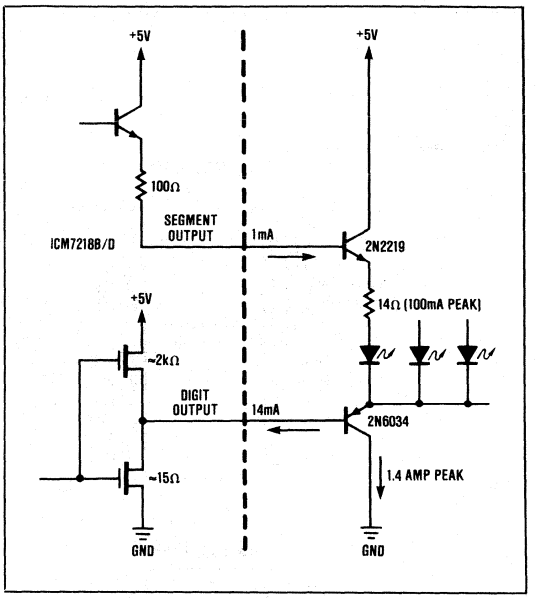


Figure 15. Driving Larger Common Cathode Displays with External Transistors

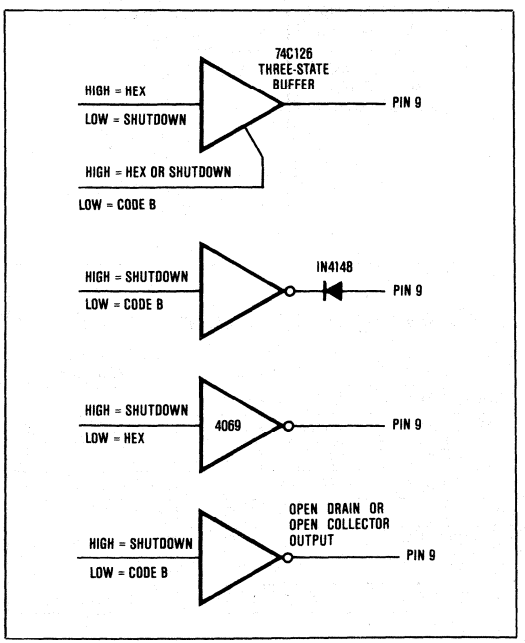


Figure 16. Drive Circuits for ICM7218C/D MODE Input

Power Supply Bypassing

Connect a minimum of 47μF in parallel with 0.1μF between V^+ and ground. These capacitors should be placed in close proximity to the ICM7218 to reduce the power supply ripple caused by the 200mA multiplexed LED display drive current pulses.

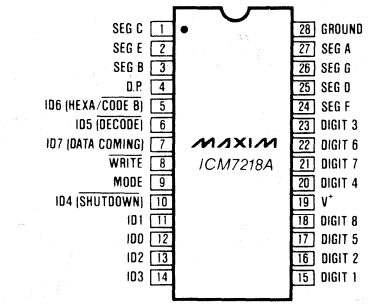
7

8 Digit LED Display Driver

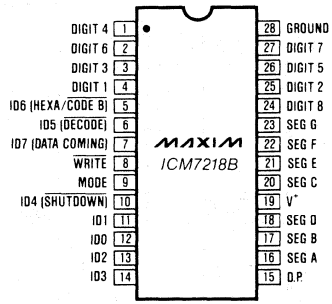
Pin Configurations

Top View

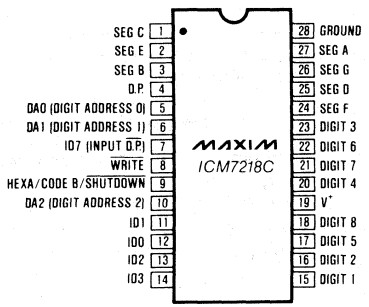
28 Pin DIP



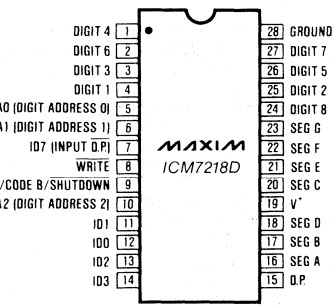
28 Pin DIP

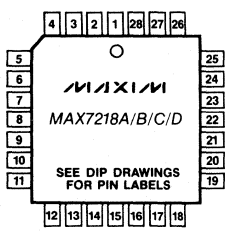


28 Pin DIP



28 Pin DIP





28 Lead Quad Pack

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
ICM7218AI/D	-20°C to +85°C	Dice
ICM7218AIQI	-20°C to +85°C	28 Lead Quad Pack
ICM7218BI/D	-20°C to +85°C	Dice
ICM7218BIQI	-20°C to +85°C	28 Lead Quad Pack
ICM7218CI/D	-20°C to +85°C	Dice
ICM7218CIQI	-20°C to +85°C	28 Lead Quad Pack
ICM7218DI/D	-20°C to +85°C	Dice
ICM7218DIQI	-20°C to +85°C	28 Lead Quad Pack

4½ Digit Counter/Decoder/Driver

General Description

The Maxim ICM7224(LCD) and ICM7225(LED) are high speed 4½ digit counters, featuring segment decoders, leading zero blanking, store and reset inputs, and a carry output that allows cascading of 8 or more digits. The ICM7224 directly drives a non-multiplexed liquid crystal display(LCD). The ICM7225 has 29 constant current outputs for driving a non-multiplexed common anode LED display.

These counters operate with inputs from DC to 25MHz while using only 10μA of supply current. A Schmitt trigger on the count input ensures reliable operation in noisy environments and in applications with slowly varying inputs.

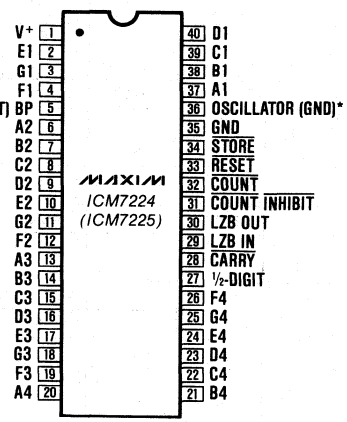
The ICM7224 and ICM7225 are available in a 44 lead plastic chip carrier package in addition to the standard 40 lead plastic DIP.

Applications

Unit Counter
Frequency Counter
Tachometer
Hour Meter
Totalizer

Pin Configuration

Top View



*Note:

PIN #	ICM7224 FUNCTION	ICM7225 FUNCTION
5	Backplane	Brightness
36	Oscillator	Ground

See Last Page for 44 Lead Chip Carrier Pin Configuration.

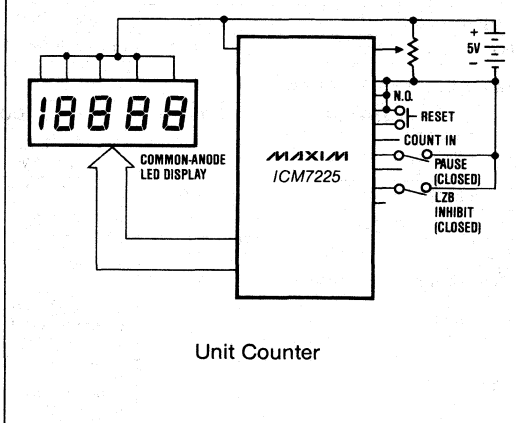
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **High Speed Up Counter: 25MHz Typ.**
- **Leading Zero Blanking**
- **Can Be Cascaded for 8 or More Digits**
- **STORE and RESET Inputs for Frequency Counter Applications**
- **On-Board Oscillator to Provide Backplane Frequency (ICM7224)**
- **Brightness Control Input (ICM7225)**
- **Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7224IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7224CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICM7224C/D	0°C to +70°C	Dice
ICM7225IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7225CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICM7225C/D	0°C to +70°C	Dice

Typical Operating Circuit



Unit Counter

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

4½ Digit Counter/Decoder/Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Input Voltage (any terminal, Note 1) ..... -0.3V to V^+ +0.3V
Power Dissipation
40 Lead Plastic Dip 1W
(derate 10mW/°C above 25°C.)
44 Lead Plastic Chip Carrier 1W
(derate 10mW/°C above 25°C.)

Operating Temperature Range
Plastic Package (IPL) ..... -20°C to +85°C
Plastic Chip Carrier (Quad) Package (Q) ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Note 1: The input voltage may exceed this rating if the input current is limited to 1mA.
Connecting any terminal to a voltage greater than V+ or less than Ground and exceeding 1mA input current may activate the parasitic SCR inherent in the junction isolated CMOS process, causing destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/25 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(All parameters measured with V^+ = 5V, unless otherwise indicated)

ICM7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	Test circuit, Display blank		10	50	µA
Operating supply voltage range	V^+		3	5	6	V
OSCILLATOR input current	I_{OSCI}	Pin 36		±2	±10	µA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		µs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		µs
Oscillator frequency	f_{osc}	Pin 36 Floating		19		kHz
Backplane frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (BRighTness) at GROUND Pin 29, 31-34 at V^+		10	50	µA
Operating supply voltage range	V^+		4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment on current	I_{SEG}	Segment On, V_{out} = +3V	5	8		mA
Half-digit on current	I_H	Half-digit On, V_{out} = +3V	10	16		mA

FAMILY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pull-up Currents	I_P	Pins 29, 31, 33, 34 $V_{out} = V^+ - 3V$		10		µA
Input High Voltage	V_{IH}	Pin 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pin 29, 31, 33,			1	V
$\overline{COUNT}$ Input Threshold	V_{CT}			2		V
$\overline{COUNT}$ Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 $V_{out} = V^+ - 3V$	350	500		µA
Output Low Current	I_{OL}	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{out} = +3V	350	500		µA
Count Frequency	f_{count}	$4.5V < V^+ < 6V$	0	DC-25	15	MHz
$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width	t_S, t_R		3			µs

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

4½ Digit Counter/Decoder/Driver

- **Key Parameters Guaranteed Over Temperature**
- **Low Power (Typically 25μW)**
- **Increased Segment-On Current**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 1)**

ABSOLUTE MAXIMUM RATINGS:

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS:

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 5V, T_A = 25°C unless otherwise noted)

ICM7224 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	**Display blank**		5	25	μA
Operating supply voltage range	V^+	**-20°C ≤ T_A ≤ +85°C**	3	5	6	V
OSCILLATOR input current	I_{OSCI}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		
Oscillator frequency	f_{osc}	Pin 36 Floating		19		kHz
Backplane frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7225 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	**Pin 5 (BRighTness) at GROUND Pin 29, 31-34 at V^+**		10	25	μA
Operating supply voltage range	V^+	**-20°C ≤ T_A ≤ +85°C**	4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		275		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment on current	I_{SEG}	**Segment On, V_{out} = +3V**	6	9		mA
Half-digit on current	I_H	**Half-digit On, V_{out} = +3V**	12	18		

FAMILY DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pull-up Currents	I_P	**Pins 29, 31, 33, 34 V_{out} = V^+ - 3V**	2	10	25	μA
Input High Voltage	V_{IH}	**Pin 29, 31, 33, 34, -20°C ≤ T_A ≤ +85°C**	3			V
Input Low Voltage	V_{IL}	**Pin 29, 31, 33, 34, -20°C ≤ T_A ≤ +85°C**			1	
$\overline{\text{COUNT}}$ Input Threshold	V_{CT}		1.5	2	3.25	
$\overline{\text{COUNT}}$ Input Hysteresis	V_{CH}		0.1	0.5	1.75	
Output High Current	I_{OH}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{out} = V^+ -3V	350	500		μA
Output Low Current	I_{OL}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{out} = +3V	350	500		

Note 1: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883C Method 3015.2 Test Circuit).

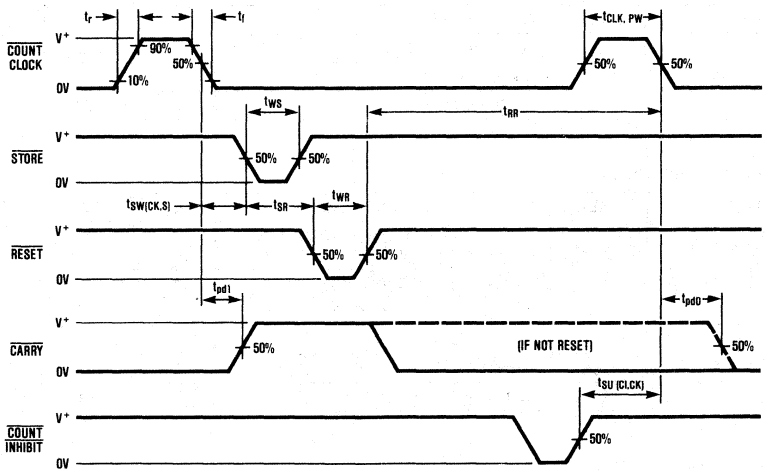
4½ Digit Counter/Decoder/Driver

FAMILY AC ELECTRICAL CHARACTERISTICS (C_L = 50pF unless noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Clock to Carry	t_{pd0}, t_{pd1}			0.6		µs
Maximum Clock Frequency	f_{CLK}		0	DC-25	15	MHz
Minimum Clock Pulse Width	$t_{CLK,PW}$			25		ns
Clock Input Rise or Fall Time	t_r, t_f				No Limit	
Reset Pulse Width	t_{WR}			125		ns
Store Pulse Width	t_{WS}			1		µs
Clock to Store Set-Up Time	$t_{SU(CK,S)}$			0.4		µs
Store to Reset Wait Time	t_{SR}			1.3		µs
Inhibit to Clock Set-Up Time	$t_{SU(CI,CK)}$			0		ns
Reset Removal	t_{RR}			20		ns
Input Capacitance	C_{IN}	Logic Inputs (Note 1)		5		pF

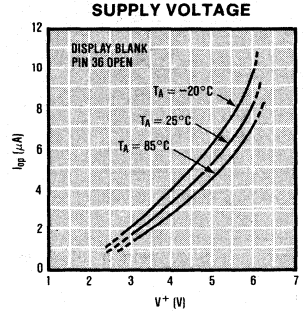
Note 1: Does not apply to backplane and oscillator pins.

Timing Diagram

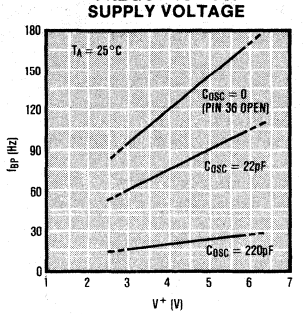


Typical Operating Characteristics

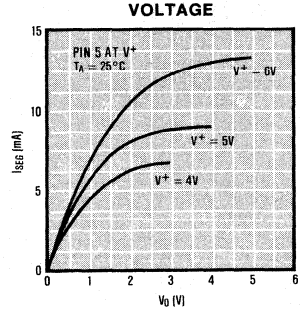
ICM 7224 OPERATING SUPPLY CURRENT VS. SUPPLY VOLTAGE



ICM 7224 BACKPLANE FREQUENCY VS. SUPPLY VOLTAGE



ICM 7225 LED SEGMENT CURRENT VS. OUTPUT VOLTAGE



MAXIM

TABLE 1. PIN DESCRIPTIONS

PIN	FUNCTION	DESCRIPTION
1	V^+	Positive power supply input.
2-4, 6-26, 37-40	Segment Outputs	These 28 pins directly drive LCD segments (ICM7224) or common anode LED segments (ICM7225). Segments A1-G1 drive the least significant digit, segments A4-G4 drive the 1000s digit.
27	½ Digit	This segment output drives both segments of the most significant half digit. This segment output turns on when the count reaches 10,000 and is reset only by a low level on the Reset input.
5 (ICM7224)	BP	The backplane pin is both an input and an output. As an output it drives the LCD backplane with an internally generated backplane signal. The backplane pin is an input when the slave mode is selected by grounding pin 36 (Oscillator).
5 (ICM7225)	BRT	An analog input voltage applied to the brightness (BRT) pin controls the output current of the LED segment drivers. Connecting this pin to ground shuts off the display. Connecting this pin to V^+ drives the display with the maximum available output current. Intermediate voltage levels will adjust the brightness to any level between full off and full brightness.
28	$\overline{\text{CARRY}}$	Connect this logic output to the Count input of another ICM7224/5 to make an 8 digit counter/display driver. The Carry output goes high at count 6000 and goes low on the transition between count 9999 and count 10,000. The Carry output repeats this cycle every 10,000 counts.
29	LZB IN	The ICM7224 displays leading zeroes when this pin is grounded. Connecting this pin to V^+ or leaving it floating enables leading zero blanking. The entire display will be blanked if this pin is high or floating, the count is 0000, and the half digit is reset. This pin has an internal 10μA pullup.
30	LZB OUT	This output allows the proper blanking of cascaded counters. The Leading Zero Blanking (LZB) output goes high when all digits are blanked.
31	$\overline{\text{COUNT INHIBIT}}$	A low level on this input pin disables the counter. Connecting this pin to V^+ or floating this pin enables the counter. This pin has an internal 10μA pullup.
32	$\overline{\text{COUNT}}$	Every negative-going transition at the Count input clocks the counter. This input has 500 mV of hysteresis to prevent multiple clocking with slow rate-of-fall inputs.
33	$\overline{\text{RESET}}$	A low level on Reset will reset the counter. Reset also clears the half-digit flip-flop and turns off the half-digit output. This input has an internal 10μA pullup and is inactive when either connected to V^+ or left floating.
34	$\overline{\text{STORE}}$	When the Store input is low, the latches are transparent and the counter contents are displayed. When Store is taken high or floated, the counter contents are latched and this latched data is displayed.
35	GND	The negative power supply input.
36 (ICM7225)	GND	An additional ground pin for the ICM7225. The ICM7225 has two ground pins to handle the high LED drive currents.
36 (ICM7224)	Oscillator	When this pin is left floating, the ICM7224 oscillates at approximately 19kHz. Connecting an external capacitor between this pin and either V^+ or GND lowers the oscillator frequency as shown in the Typical Characteristics graphs. The Oscillator can be externally driven using the circuit of Figure 4. Grounding this pin puts the ICM7224 into the slave mode, turning pin 5, BP, into an input.

Table 2. TYPICAL LCD DISPLAYS

Manufacturer	PART #	HEIGHT	# DIGITS
Epson	LD-H7924	0.350"	4½
(213) 534-0360	LD-H7916	0.500"	4
	LD-K7994	0.700"	4
LXD	44D3F-85	0.800"	4½
(216) 292-3300	44D3F-45	0.400"	4½
Hamlin	3909	0.400"	4½
(414) 648-2361	3912	0.800"	4½
AND	FE0202W-DU	0.500"	4
(415) 347-9916	FE0206W-DU	0.400"	4½

Table 3. TYPICAL LED DISPLAYS

Manufacturer	PART #	HEIGHT	COLOR
Hewlett Packard	5082-7731	0.3"	Red
(Contact local	5082-7611	0.3"	Red (Hi Eff.)
sales office)	5082-7621	0.3"	Yellow
	5082-7631	0.3"	Green
General Inst.	MAN 71A	0.3"	Red
(415) 493-0400	MAN 3910A	0.3"	Red (Hi Eff.)
	MAN 3810A	0.3"	Yellow
	MAN 3410A	0.3"	Green
Siemens Opto	HD1075R	0.3"	Red
(408) 257-7910	HD1075O	0.3"	Red (Hi Eff.)
	HD1075Y	0.3"	Yellow
	HD1075G	0.3"	Green

4½ Digit Counter/Decoder/Driver

Detailed Description

The ICM7224 and ICM7225 have identical counter and control sections, but have different display driver sections. The ICM7224 is designed to drive a non-multiplexed liquid crystal display (LCD). The ICM7225 is designed to drive a non-multiplexed, common anode LED display.

Counter and Control Logic

The counter in both the ICM7224 and ICM7225 is a 4 decade up counter with a Carry output. An overflow flip-flop, which is clocked by Carry, controls the half-digit output. This half-digit output can be used as an overflow indicator or as a half-digit to extend the count range to 19,999. Once set by Carry, the overflow flip-flop will remain set until the counter is reset by taking the Reset pin low.

The counter advances with each negative going transition on the Count input, provided the Count Inhibit and Reset inputs are high.

The Count Inhibit input disables the counter when it is low. The Count Inhibit input is similar to the J-K inputs of a J-K flip-flop; transitions on Count Inhibit do not increment the counter.

Reset is an active low input that resets the 4 digit counter and the overflow (½ digit) flip-flop. Reset does not clear the data in the display latches unless Store is low.

Store controls the flow of data into the display latches. When Store is low the latches are transparent and the counter data is displayed. When Store goes high the display latches go into the hold mode and the displayed count no longer follows the counter.

The LZB IN pin determines whether leading zeroes are blanked. Leading zeroes are displayed when LZB IN is low. Leading zeroes are blanked when LZB IN is high or floating. The LZB OUT allows proper leading zero blanking when cascading two ICM7224/ICM7225 devices to make an 8 digit counter/display driver (Figure 3). LZB OUT will go high only when LZB IN is high or floating, the count is 0000, and the overflow flip-flop is reset.

When the ICM7224/25 is used in electrically noisy environments (around solenoids, motor starters, etc.), do NOT rely upon the internal 10μA pullups on Reset, Count Inhibit, LZB IN and Store inputs. Stray pickup of transients may momentarily override the weak, 10μA pullup. Connect these pins directly to V^+, drive them with a logic gate, or parallel the internal pullup with a 4.7kΩ resistor to V^+.

ICM7224 LCD Driver Section

The LCD driver section of the ICM7224 is similar to the Maxim ICM7211 4 digit display driver. It includes an internal 19kHz oscillator with a backplane driver, and 29 segment drivers.

The 19kHz nominal output of the onboard oscillator is divided by 128 in the 7 stage divider chain to generate a 150Hz backplane frequency. The Backplane output, pin 5, is a low impedance (200Ω typical) output that swings from ground to V^+ at the backplane frequency with a 50% duty cycle. The 29 segment drivers also swing from ground to V^+ and have an output impedance of approximately 2kΩ. The ICM7224 drives an LCD segment in phase with the backplane to turn the

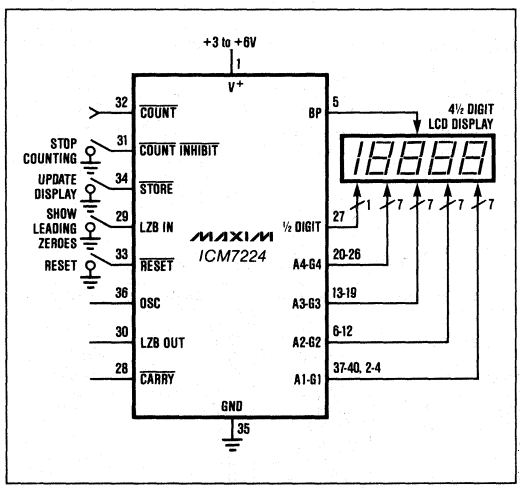


Figure 1. Simple 4½ Digit Event or Unit Counter with LCD Display

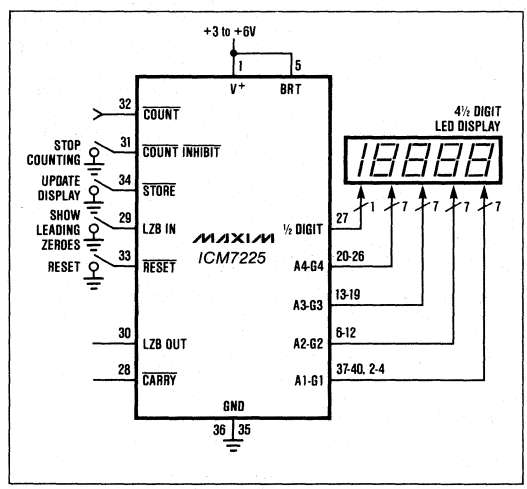


Figure 2. Simple 4½ Digit Event or Unit Counter with LED Display

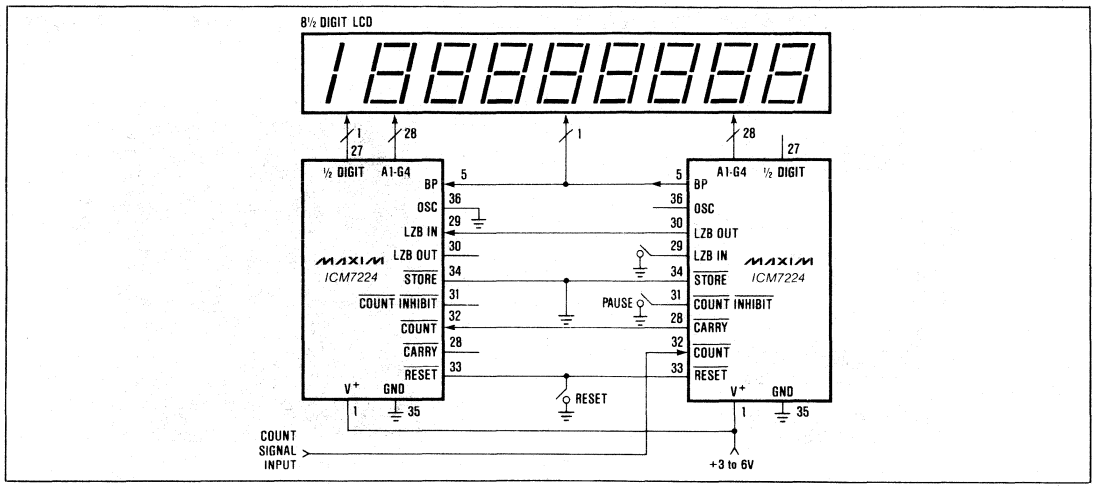


Figure 3. 8½ Digit Totalizer

segment off, and drives the LCD segment 180° out of phase with the backplane to turn the segment on.

The internal oscillator has a nominal oscillation frequency of 19kHz with no external components. This frequency can be lowered by connecting a capacitor from pin 36 (Oscillator) to either ground or V^+. See Typical Characteristics graph, Backplane Frequency vs. Supply Voltage. The oscillator can also be overdriven by an external source as shown in Figure 4. The two resistors connected from the driver to pin 36 keep the voltage at pin 36 (Oscillator) above the 1.5V threshold of the backplane slaving detector which is internally connected to pin 36.

When two or more ICM7224 counter/display drivers drive one LCD with a single backplane, the backplane outputs of the ICM7224 counter/display drivers must be synchronized. This is performed by grounding the Oscillator (pin 36) on all but one device; and connecting together the Backplanes (pin 5) of all devices. The one device with the Oscillator input not grounded will drive both its own Backplane pin and the Backplane pins of the other devices. The devices with the Oscillator input grounded disable their backplane drivers and use the Backplane pin as an input. See Figure 3.

ICM7225 LED Display Interface

The ICM7225 has 29 open drain N channel segment drivers. These drivers are constant current sinks, whose sink current varies from 0 to 9mA as the voltage on BRT (pin 5) varies from ground to V^+ (0 to 18mA for pin 27, the ½ digit output). Segment current limiting resistors are not needed.

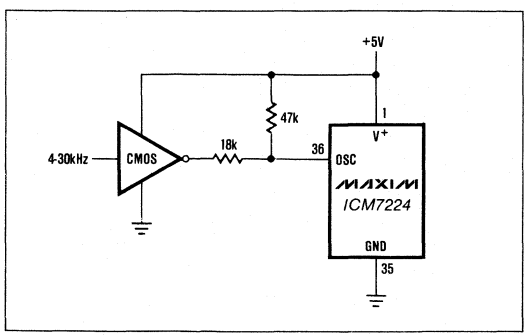


Figure 4. External Clock Drive.

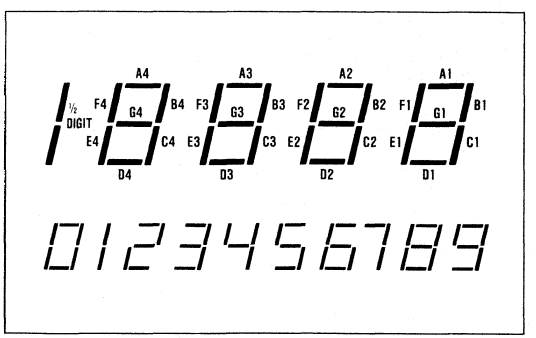
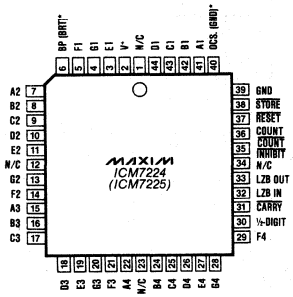


Figure 5. Segment Assignment and Display Font

7

4½ Digit Counter/Decoder/Driver

Pin Configuration

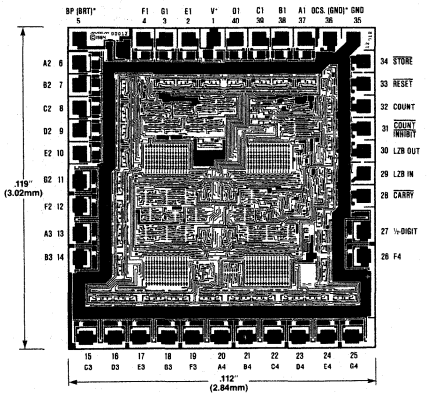


44 Lead Plastic Chip Carrier
(Quad Pack) (Q)

*Note:

PIN #	ICM7224 FUNCTION	ICM7225 FUNCTION
6	Backplane	Brightness
40	Oscillator	Ground

Chip Topography



4 Digit Up/Down Counter/Decoder/Driver

General Description

The MM74C945 and MM74C947 are synchronous 4 digit up/down counters with latches, 7-segment decoders, and all segment and backplane driver, and oscillator circuitry necessary to directly drive LCD displays.

Maxim's MM74C945 has a select input which allows the counter contents or the latch contents to be displayed, and a blanking input which allows the display to be blanked.

The MM74C947 only displays the latch contents, but provides leading zero blanking. The leading zero blanking input allows the user to force leading zeros to be displayed, and the leading zero output allows cascaded counters to blank leading zeroes properly.

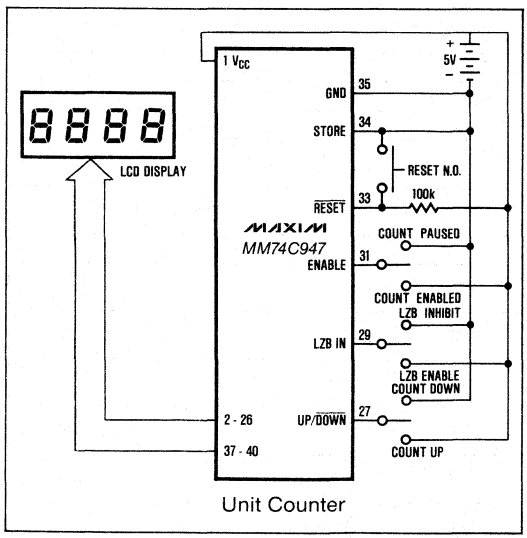
Both devices provide 28 segment outputs and a backplane input/output. When the oscillator pin is open, the device generates its own display waveform timing. When the oscillator pin is grounded, the backplane pin becomes an input.

The MM74C945 and MM74C947 are available in a 44 lead plastic chip carrier package in addition to the standard 40 lead plastic DIP.

Applications

Unit Counter
Frequency Counter
Tachometer
Hour Meter
Totalizer

Typical Operating Circuit



Unit Counter

Features

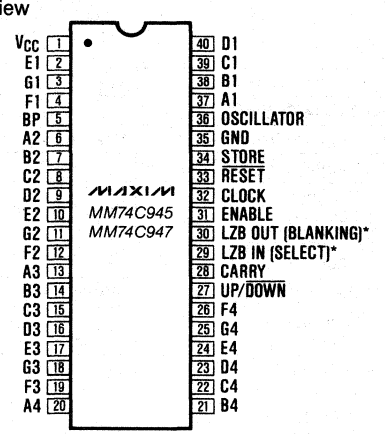
- **4 Decade Synchronous Up/Down Counter**
- **All Circuitry for Segments and Backplane of 4-Digit LCD**
- **Carry/Borrow Output Allows Ripple or Synchronous Cascading**
- **Schmitt Trigger Count Input**
- **Store and Reset Inputs Allow Operation as Frequency or Period Counter**
- **MM74C945 Provides Input to Select Display of Counter or Latch**
- **MM74C947 Provides Leading Zero Blanking Input and Output. Least Significant Digit May be Blanked.**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MM74C945N	-40°C to +85°C	40 Lead Plastic DIP
MM74C945CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MM74C945C/D	0°C to +70°C	Dice
MM74C947N	-40°C to +85°C	40 Lead Plastic DIP
MM74C947CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MM74C947C/D	0°C to +70°C	Dice

Pin Configuration

Top View



*Note:

PIN #	MM74C945 FUNCTION	MM74C947 FUNCTION
29	Select	LZB In
30	Blanking	LZB Out

See Last Page for 44 Lead Chip Carrier Pin Configuration.

4 Digit Up/Down Counter/Decoder/Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Input Voltage ..... -0.3V to V^+ +0.3V
Power Dissipation
40 Lead Plastic Dip 0.5W
44 Lead Plastic Chip Carrier 0.5W

Operating V_{CC} Range ..... 3.0V to 6.0V
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Min/max limits apply across temperature range , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Only)	V_{CC} = 5V, V_{IN} (0 → 5) V	2.5	2.9	3.25	V
V_{T-} Negative Going Threshold Voltage (Clock Only)	V_{CC} = 5V, V_{IN} (5 → 0) V	1.5	2.2	2.4	V
Hysteresis ($V_{T+} - V_{T-}$) (Clock Only)	V_{CC} = 5V	0.1	0.7	1.75	V
Logical "1" Input Voltage ($V_{IN\ (1)}$)	V_{CC} = 5V	3.5			V
Logical "0" Input Voltage ($V_{IN\ (0)}$)	V_{CC} = 5V			1.5	V
Logical "1" Output Voltage ($V_{OUT\ (1)}$)(LZO and Carry)	V_{CC} = 5V, I_O = -10 μA	4.5			V
Logical "0" Output Voltage ($V_{OUT\ (0)}$)(LZO and Carry)	V_{CC} = 5V, I_O = +10 μA			0.5	V
Clock Input Current $\|I_{IN}\|$	V_{CC} = 5V, V_{IN} = 5V/0V		0.005	1.0	μA
Input Current @ Pins 27, 29, 31, 33, and 34 (Note 1)	V_{CC} = 5V, V_{IN} = 0V V_{IN} = 5V			±1.0 ±1.0	μA μA
Oscillator Input Current (I_{OSL})	V_{CC} = 5V, V_{IN} = 0V/5V		±5	±15.0	μA
Supply Current (I_{CC})(Note 2)	V_{CC} = 5V, V_{IN} = 0V/5V		10	60	μA
Oscillator Input Voltage $V_{IH\ (OSC)}$ $V_{IL\ (OSC)}$	When Driving Oscillator Pin with External Signal	 0.2 V_{CC}		V_{CC} -0.2	 V V
DC Offset Voltage (Note 3)	V_{CC} = 5V			25	mV
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN\ (1)}$)	V_{CC} = 4.75V	V_{CC}-1.5V			V
Logical "0" Input Voltage ($V_{IN\ (0)}$)	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT\ (1)}$)(LZO and Carry)	V_{CC} = 4.75V, I_O = -360 μA	2.4			V
Logical "0" Output Voltage ($V_{OUT\ (0)}$)(LZO and Carry)	V_{CC} = 4.75V, I_O = +360 μA			0.4	V
OUTPUT DRIVE (SHORT CIRCUIT CURRENT)					
Output Source Current (I_{SOURCE})(LZO and Carry)	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C	1.75	2.7		mA
Output Sink Current (I_{SINK})(LZO and Carry)	V_{CC} = 5V, V_{OUT} = 5V T_A = 25°C	1.75	3.2		mA
Output Source Current (I_{SOURCE})(Segment Outputs)	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C	1.4	2.0		mA
Output Sink Current (I_{SINK})(Segment Output)	V_{CC} = 5V, V_{OUT} = 5V T_A = 25°C	1.4	2.2		mA
Output Source Current (I_{SOURCE})(Backplane Output)	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C	12.6	15.0		mA
Output Sink Current (I_{SINK})(Backplane Output)	V_{CC} = 5V, V_{OUT} = 5V T_A = 25°C	12.6	20.0		mA

Note 1: Does not apply to backplane and oscillator pins. Does apply to pin 30 on MM74C945.
Note 2: Display blanked. See Test Circuit.
Note 3: DC offset voltage is the effective DC voltage the LCD will have between any segment and the backplane.

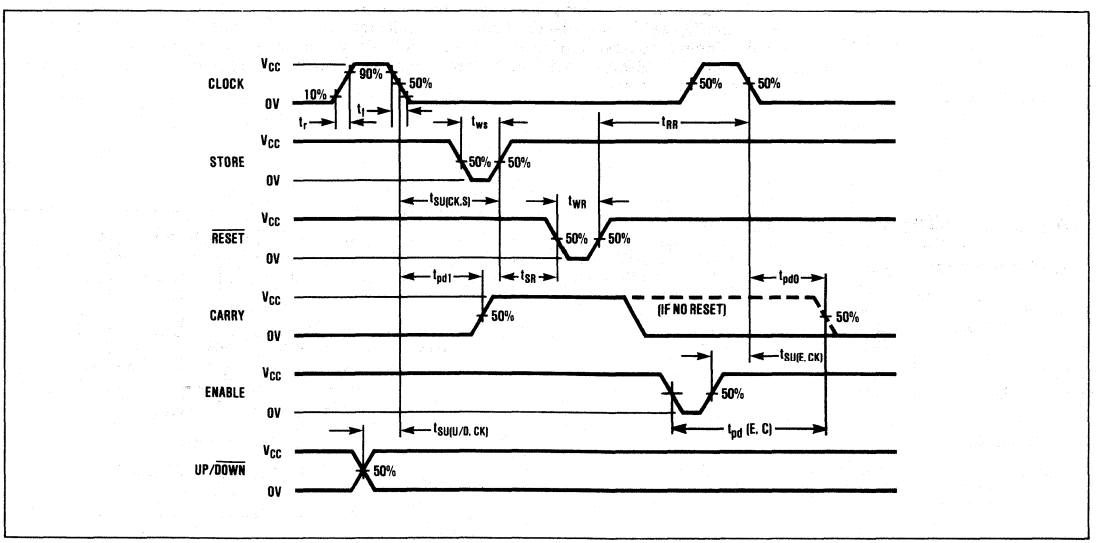
AC ELECTRICAL CHARACTERISTICS

T_j = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Clock to Carry	t_{pd0} , t_{pd1}	V_{CC}= 5.0V (Note 2)		600	800	ns
Maximum Clock Frequency	f_{CLK}	V_{CC}= 5.0V	2	3		MHz
Clock Input Rise/Fall Time	t_r , t_f	V_{CC}= 5.0V			No Limit	
Reset Pulse Width	t_{WR}	V_{CC}= 5.0V	180	50		ns
Store Pulse Width	t_{WS}	V_{CC}= 5.0V	150	50		ns
Clock to Store Set-Up Time	$t_{SU(CK, S)}$	V_{CC}= 5.0V	500	120		ns
Store to Reset Wait Time	t_{SR}	V_{CC}= 5.0V	280	170		ns
Enable to Clock Set-Up Time	$t_{SU(E, CK)}$	V_{CC}= 5.0V (Note 3)	600	400		ns
Reset Removal	t_{RR}	V_{CC}= 5.0V	50	0		ns
Up/Down to Clock Set-Up Time	$t_{SU(U/D, CK)}$	V_{CC}= 5.0V (Note 4)	600	400		ns
Backplane Output Frequency	f_{BP}	Pin 36 Floating, V_{CC}= 5.0V		85		Hz
Input Capacitance	C_{IN}	Logic Inputs (Note 1)		5		pF
Segment Rise/Fall Time	t_{rfs}	C_{Load}= 200 pF		0.5		μS
Backplane Rise/Fall Time	t_{rfb}	C_{Load}= 5000 pF		1.5		μS
Oscillator Frequency	f_{OSC}	Pin 36 Floating, V_{CC}= 5.0V		11		kHz
Propagation Delay Enable to Carry	t_{pd}(E, C)	V_{CC} = 5.0V		450		ns

Note 1: Does not apply to backplane and oscillator pins. Does apply to pin 30 on MM74C945.
Note 2: National's MM74C945/947 is specified at 600ns maximum.
Note 3: National's MM74C945/947 is specified at 140ns minimum.
Note 4: National's MM74C945/947 is specified at 300ns maximum.

AC Waveforms



4 Digit Up/Down Counter/Decoder/Driver

TABLE 1. PIN DESCRIPTIONS

(Pin numbers correspond to 40 lead DIP package)

PIN	FUNCTION	DESCRIPTION
1	V_{CC}	Positive power supply
2-4 6-26 37-40	Segment Outputs	These 28 pins directly drive LCD display segments. Segments A1-G1 drive the least significant digit, segments A4-G4 drive the 1000s digit.
5	BACKPLANE	The backplane pin is both an input and an output. As an output it drives the LCD backplane with an internally generated backplane signal. The backplane pin is an input when the slave mode is selected by grounding pin 36, Oscillator.
27	UP/$\overline{\text{DOWN}}$	This input controls the direction of counting. When high, counter counts up, when low, down.
28	CARRY	The CARRY output goes high when the ENABLE input is high and the counter is at 9999 counting up or at 0000 counting down. When the ENABLE input is low CARRY is low. This output may be used to ripple or synchronously cascade counters.
29	SELECT	When high, counter contents displayed. When low, latch contents displayed. MM74C945 only.
30	BLANKING	When high, entire display is blanked. MM74C945 only.
29	LZB IN	The MM74C947 displays leading zeroes when this pin is grounded. Connecting this pin to V_{CC} enables leading zero blanking. The entire display will be blanked if this pin is high, the counter is at 0000, and the oscillator pin is grounded. If the oscillator pin is floating, the least significant digit A1-G1 will not blank. MM74C947 only.
30	LZB OUT	This output allows the proper blanking of cascaded counters. The LZB OUT goes high when all digits are blanked. MM74C947 only.
31	ENABLE	When this input is low, the counter is inhibited and the CARRY output will be low. When this input is high, the counter is enabled.
32	CLOCK	Every negative-going transition at the CLOCK input clocks the counter. This input has a Schmitt trigger to prevent multiple clocking with slow rate-of-fall inputs.
33	$\overline{\text{RESET}}$	A low level at this input will reset the counter to 0000. This input is inactive when high.
34	STORE	When the STORE input is low, the latches are transparent and the counter contents are displayed. When this input is high, the data is latched.
35	GROUND	The negative power supply input.
36	OSCILLATOR	When this pin is left floating, the chip oscillator will free-run at approximately 11kHz. Connecting an external capacitor between this pin and either power supply will lower the oscillator frequency as shown in the Typical Characteristics graphs. The oscillator may be overdriven but care must be taken to avoid swinging too close to ground. Grounding this pin puts the chip into the backplane slave mode making pin 5, BACKPLANE, into an input, and on the MM74C947 allowing the least significant digit to leading zero blank.

TABLE 1. TYPICAL LCD DISPLAYS

MANUFACTURER	PART NUMBER	DIGIT HEIGHT	NUMBER OF DIGITS
Epson (213) 534-0360	LD-H7924 LD-H7916 LD-K7994	0.350″ 0.500″ 0.700″	4½ 4 4
LXD (216) 292-3300	44D3F-85 44D3F-45	0.800″ 0.400″	4½ 4½
Hamlin (414) 648-2361	3909 3912	0.400″ 0.800″	4½ 4½
AND (415) 347-9916	FE0202W-DU FE0206W-DU	0.500″ 0.400″	4 4½

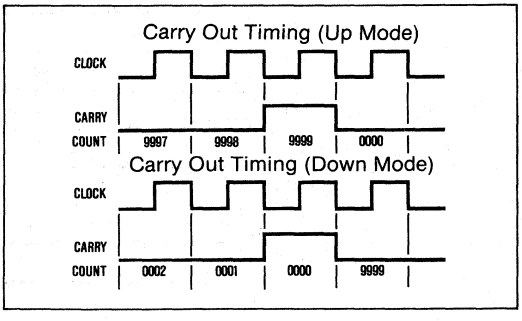


Figure 1. Carry Timing

4 Digit Up/Down Counter/Decoder/Driver

Applications Information

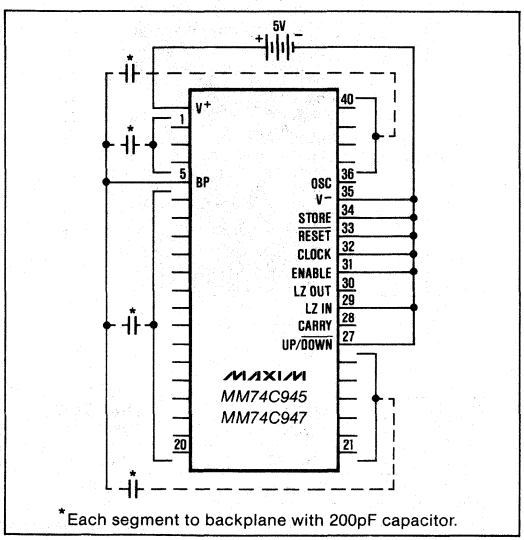
Display Drive Circuitry Description

The MM74C945 and MM74C947 have 28 segment outputs and a backplane input-output which directly drive a 4-digit seven-segment LCD display. The segment and backplane drivers are designed to provide matched rise and fall times which eliminates any DC component of the display signals maximizing display life.

The backplane driver may be disabled by connecting the oscillator pin to ground. In this mode, the backplane pin becomes an input, and the display waveforms will be synchronized with the signal applied to the pin. Several chips may be ganged in this manner, allowing the use of single-backplane displays with four, eight, twelve, etc. digits where one four-digit counter drives the backplane and the rest are slaved to it.

On the MM74C947, which implements leading zero blanking, the oscillator pin also controls the blanking of the least significant digit; when the oscillator pin is open (backplane master) the least significant digit will not blank, and when the oscillator pin is grounded, the entire display will blank when the latch contents of all four digits are zero and the Leading Zero Blanking input is high. In order to cascade counters and have leading zero blanking operate correctly, the least-significant counter should be the backplane master, with the other counters as slaves.

An on-board oscillator and divider chain generate the backplane and segment timing. The oscillator typically runs at 11kHz resulting in a backplane frequency of 85Hz. The oscillator may be slowed by connecting a capacitor between the oscillator pin and either power supply, or the oscillator pin may be overdriven by an external signal. When overdriving the oscillator, ensure that the input waveform does not swing close to ground to avoid putting the device into backplane slave mode. See VIH(osc) and VIL(osc) specifications.



*Each segment to backplane with 200pF capacitor.

Figure 2. Test Circuit

Counter Circuitry Description

The MM74C945/7 are synchronous four-decade up/down counters. A high level on the UP/DOWN input causes the counter to count up, while a low level at this input causes the counter to count down. The counter indexes on the negative-going edge of the CLOCK input. The CARRY output will be high for one clock period when the counter is at 9999 in up mode or 0000 in down mode. On the Maxim devices, the CARRY output will not go high if the ENABLE input is low. This ensures that synchronous cascading does not allow the higher-order digits to count incorrectly as can occur with the original manufacturer's device when the low-order counter ENABLE input is low and the counter is at 9999 up or 0000 down. As shown in the applications figures, the CARRY output allows synchronous or ripple cascading.

The $\overline{\text{RESET}}$ and ENABLE inputs are provided to allow these counters to perform frequency and period measurements. The counter is forced to 0000 when $\overline{\text{RESET}}$ is taken low, and the counter (including the CARRY output) is disabled when the ENABLE input is taken low.

The counter outputs are latched. The latches are transparent and the display will follow the counter when the STORE input is low. The latches store the counter outputs when the STORE input is taken high.

On the MM74C945 the SELECT input allows the counter or latch to be selected for display. When the SELECT input is high, the counter contents are displayed, and when low, the latch contents are displayed. The BLANKING input on the MM74C945 blanks the entire display when taken high. The MM74C945 does not implement leading zero blanking.

On the MM74C947 the latch contents are always displayed, but the decoders include leading zero blanking circuitry and two pins to allow cascaded counters to leading zero blank properly. When the LZB IN pin is low, leading zero blanking is inhibited. When the LZB IN is high, the device will blank leading zeros except for the least-significant digit when the oscillator pin is open (backplane master). When the oscillator pin is grounded (backplane slave) the device will blank all digits when in 0000, and the LZB OUT will go high.

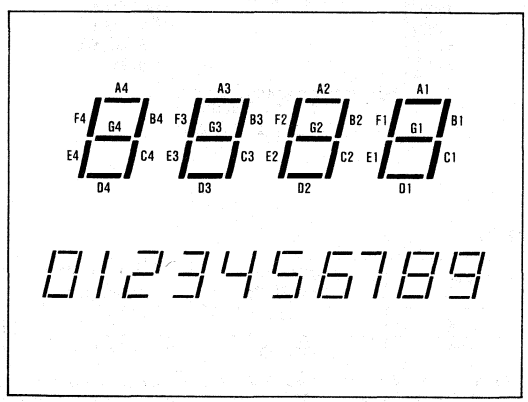
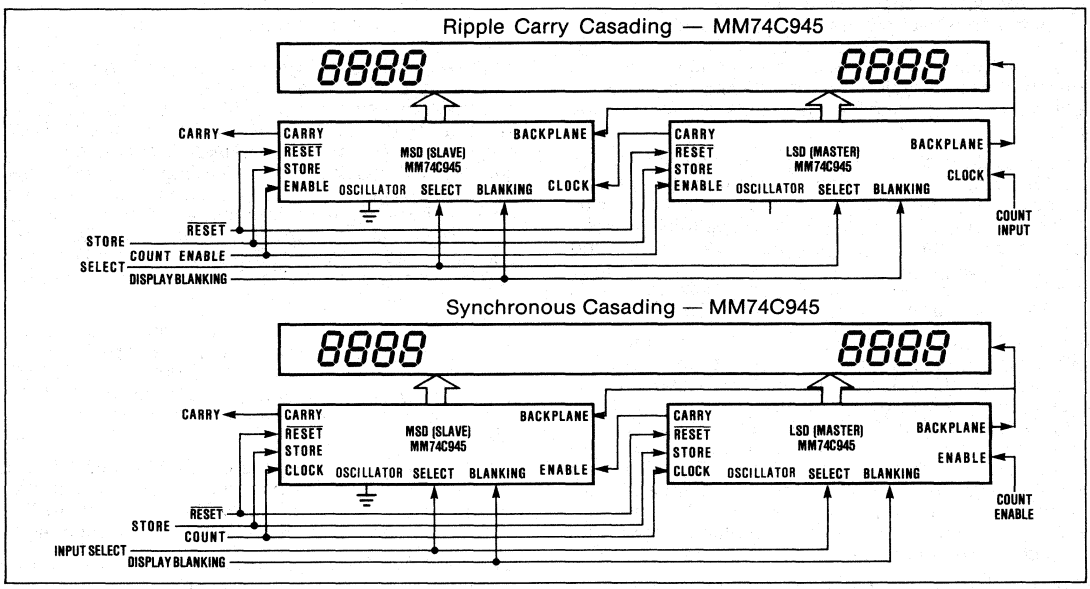


Figure 5. Segment Assignment and Display Font

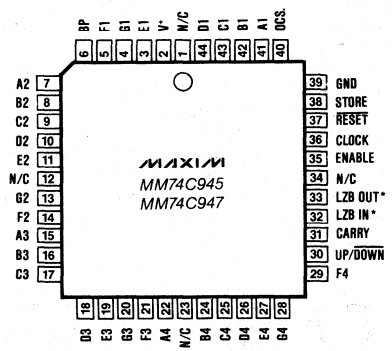
7

4 Digit Up/Down Counter/Decoder/Driver

Typical Applications



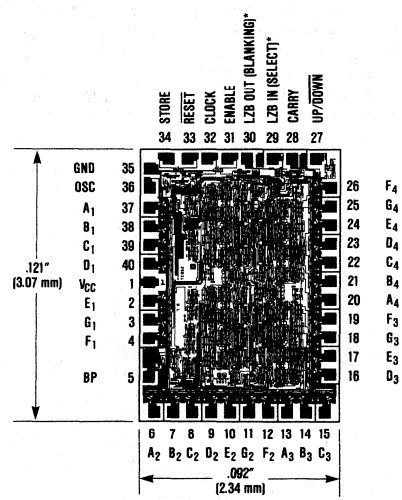
Pin Configuration



***Note:**

PIN #	MM74C945 FUNCTION	MM74C947 FUNCTION
32	Select	LZB IN
33	Blanking	LZB OUT

Chip Topography



***Note:**

PIN #	MM74C945 FUNCTION	MM74C947 FUNCTION
29	Select	LZB IN
30	Blanking	LZB OUT

Timers/Counters

Counters and Timers

Part Number	Description	Maximum Count	Output	Speed (MHz max)	Supply Voltage	Supply Current	Features	Page No.
ICM7217	4 Digit Up/Down	9999	C.A. LED	2	4.5V to 5.5V	350mA typ	Equals and Zero outputs, counter preset and pre-determining register set by thumb-wheel switches	7-33
ICM7217A	4 Digit Up/Down	9999	C.C. LED	2	4.5V to 5.5V	100mA typ		7-33
ICM7217B	4 Digit Up/Down	5959	C.A. LED	2	4.5V to 5.5V	200mA typ		7-33
ICM7217C	4 Digit Up/Down	5959	C.C. LED	2	4.5V to 5.5V	100mA typ		7-33
ICM7224	4-1/2 Digit	19,999	LCD	15	3V to 6V	25μA max		7-53
ICM7225	4-1/2 Digit	19,999	C.A. LED	15	3V to 6V	25μA max		7-53
ICM7240	8 Bit Binary	1-255	open drain	15	2V to 16V	500μA max	RC oscillator or ext. clock	8-1
ICM7242	Fixed 8 Bit	128/256	CMOS	15	2V to 16V	500μA max	Programmable Time outs	8-1
ICM7250	2 Digit BCD	1-99	open drain	15	2V to 16V	500μA max	RC oscillator or ext. clock	8-1
ICM7260	2 Digit Timer	1-59	open drain	15	2V to 16V	500μA max	RC oscillator or ext. clock	8-1
ICM7555	CMOS 555 Timer		CMOS	0.5	2V to 16.5V	250μA max		8-9
ICM7556	CMOS 556 Timer		CMOS	0.5	2V to 16.5V	500μA max		8-9
MM74C945	4 Digit Up/Down	9,999	LCD	3	3V to 6V	60μA max		7-61
MM74C947	4 Digit Up/Down	9,999	LCD	3	3V to 6V	60μA max		7-61

NOTE:
C.A. LED = Common Anode LED Display
C.C. LED = Common Cathode LED Display

LCD and LED Display Drivers

Part Number	Input Formula	Display Formats	4-Digit	8-Digit	10-Digit	4-Char	5-Char	LCD	LED	Page No.
MAX7231	6-bit Parallel	Hex, BCD, or Code B, plus 16 annunciators		X				X		7-1
MAX7232	Bit Serial	Hex, BCD, or Code B, plus 20 annunciators			X			X		7-1
MAX7233	6-bit Parallel	Upper Case ASCII				X		X		7-1
MAX7234	Bit Serial	Upper Case ASCII					X	X		7-1
ICM7211	μP and Muxed 4-bit	Hex, BCD and Code B	X					X		7-17
ICM7212	μP and Muxed 4-bit	Hex, BCD and Code B	X						X	7-17
ICM7218/ ICM7228	8-bit Parallel	Hex, BCD, Code B, plus No Decode		X					X	7-41

MAXIM

Fixed And Programmable Timer/Counters

General Description

The Maxim ICM7240/50/60 are programmable timer/counters and the Maxim ICM7242 is a fixed timer/counter. They require only 120μA of supply current, while generating delays from microseconds to days. Each device combines a counter with an internal oscillator whose period is controlled by an external resistor and capacitor. The oscillator can be inhibited and an external clock applied to the TB I/O terminal. The programmable counters in the ICM7240/50/60 can be programmed using thumbwheel switches, jumpers, and analog switches.

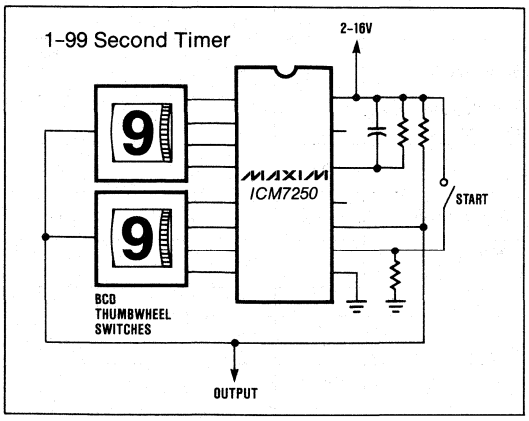
The ICM7240 has an 8 bit programmable counter and can generate time delays from 1 to 255 RC time constants. The ICM7250 has a two digit programmable BCD counter and can generate time delays from 1 to 99 RC time constants. The ICM7260 is used for "real time" applications and has a modulo 60 programmable divider, producing time delays from 1 to 59 RC time constants. The ICM7242 has an 8 bit fixed counter and can generate a time delay of 1 and 128 RC time constants. These four devices are easily cascaded and can operate in either astable or monostable configurations, using the on-chip control flip-flop with Trigger and Reset inputs.

Applications

The ICM7240/42/50/60 family is suitable for a wide variety of timing and control applications.

- ON/OFF Delay Timers
- Batch Timer/Sequencers
- Cycle Timers
- Programmable Timers
- Frequency Synthesizers
- Ultra-Long Time Delay Generators

Typical Operating Circuit



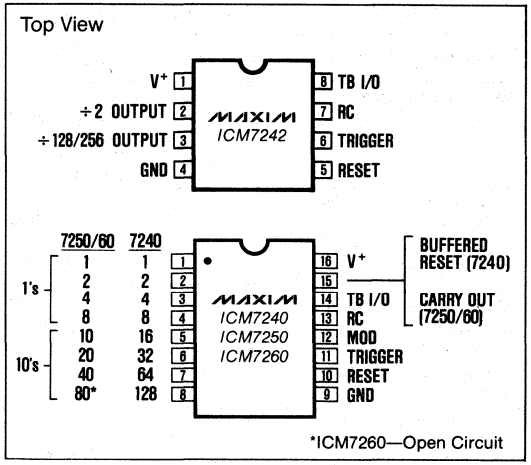
Features

- **Improved Second Source! (See 3rd page for "Maxim Advantage™.")**
- **Low Supply Current: 120μA**
- **Timing from μs to Days**
- **Shutdown Current less than 10μA**
- **Programmable Fixed Count**
- **Cascadable for Long Range Timing**
- **Monostable or Astable Operation**
- **Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7240IPE	-20°C to +85°C	16 Lead PLASTIC DIP
ICM7240IJE	-20°C to +85°C	16 Lead CERDIP
ICM7240C/D	0°C to +70°C	Dice
ICM7242IPA	0°C to +85°C	8 Lead PLASTIC DIP
ICM7242IJA	-20°C to +85°C	8 Lead CERDIP
ICM7242C/D	0°C to +70°C	Dice
ICM7250IPE	-20°C to +85°C	16 Lead PLASTIC
ICM7250IJE	-20°C to +85°C	16 Lead CERDIP
ICM7250C/D	0°C to +70°C	Dice
ICM7260IPE	-20°C to +85°C	16 Lead PLASTIC
ICM7260IJE	-20°C to +85°C	16 Lead CERDIP
ICM7260C/D	0°C to +70°C	Dice

Pin Configuration



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Fixed and Programmable Timer/Counters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Input Voltage (Note 1)
  ICM7240/50/60,
    pins 10,11,12,13,14 ..... (Gnd-0.3V) to (V^+ +0.3V)
  ICM7242
    pins 5,6,7,8 ..... (Gnd-0.3V) to (V^+ +0.3V)
Output Voltage
  ICM7240/50/60
    pins 1,2,3,4,5,6,7,8 ..... (Gnd-0.3V) to +18V
    pins 14,15 ..... (Gnd-0.3V) to (V^+ 0.3V)
Output Voltage
  ICM7242
    pins 2,3,8 ..... (Gnd-0.3V) to (V^+0.3V)
Maximum Continuous Output
  Current (each output) 50mA
Power Dissipation 200mW
  Derate at -2mW/°C above 25°C.
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: Due to the SCR structure inherent in the CMOS process, connecting any terminal (except pins 1 through 8 on the ICM7240/50/60) to voltages greater than V^+ or less than Ground may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources be applied to the device before the supply is established. In multiple supply systems, the supply to ICM7240/42/50/60 should be turned on first. Pins 1 through 8 in the ICM7240/50/60 are open drain devices and are rated to withstand 18Volts with respect to ground (pin 9).

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+=+5V, T_A=+25°C, R=10kΩ, C=0.1μF, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current 7240,50,60 7242	I^+	Reset Operating, R = 10kΩ, C = 0.1μF Operating, R = 1MΩ, C = 0.1μF TB Inhibited, RC Connected to GND Operating, R = 10kΩ, C = 0.1μF Operating, R = 1MΩ, C = 0.1μF TB Inhibited, RC Connected to GND		125 300 120 125 340 220 225	 700 500 800 600 	μA μA μA μA μA μA μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	Δf/ΔT	(Exclusive of RC Drift)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 1 mA I_{SINK} = 3.2 mA	3.5	4.2 0.25	 0.6	V V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Mod Voltage Level 7240/50/60	V_{MOD}	V^+ = 5V V^+ = 15V		3.5 11.0		V V
Trigger Input Voltage	V_{TRIG}	V^+ = 5V V^+ = 15V		1.6 3.5	2.0 4.5	V V
Reset Input Voltage	V_{RST}	V^+ = 5V V^+ = 15V		1.3 2.7	2.0 4.0	V V
Max Count Toggle Rate 7240, 7242	f_t	V = 2V V = 5V V = 15V Counter/Divider Mode 50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND	2	1 6 13		MHz MHz MHz
Max Counter Toggle Rate, 7250, 7260	f_t	V^+ = 5V (Counter/Divider Mode)	1.5	5		MHz
Max Count Toggle Rate 7240, 7250, 7260	f_t	Programmed Timer — Divider Mode			100	kHz
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output V^+ = 5V, I_{OUT} = 3.2 mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	V^+ = 5V, per Output			1	μA
Output Sourcing Current 7242	I_{SOURCE}	V^+ = 5V Terminals 2 & 3, V_{OUT} = 1V		300		μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \leq 5.5V$ $V^+ \leq 16V$			22M 22M	Ω Ω

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983, 1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The Electrical Characteristics Table along with the descriptive excerpts from the manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Fixed And Programmable Timer/Counters

- ♦ Synchronous High Speed Operation
- ♦ No False Clocking
- ♦ Increased Toggle Rate
- ♦ Supply Current Guaranteed Over Temperature
- ♦ Standby Current Less Than 10μA
- ♦ Significantly Improved ESD Protection (Note 1)
- ♦ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: These devices conform to the Absolute Maximum ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS: *Specifications below satisfy or exceed all "tested" parameters on adjacent page.*

(V^+=+5V, T_A=+25°C, Test circuit: R=10kΩ, C=0.1μF, unless otherwise specified).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	**Reset, $-20°C \le T_A \le +85°C$** **Operating, R = 10kΩ, C = 0.1μF, T_A = 25°C** **$-20°C \le T_A \le +85°C$** **Operating, R = 1MΩ, C = 0.1μF (Note 2)** **TB Inhibited, RC Connected to GND** **$-20°C \le T_A \le +85°C$**		**125** **300** **120** **10**	**700** **700** **800** **500** **10**	**μA** **μA** **μA** **μA** **μA**
Timing Accuracy		V^+ = +5V, R = 10kΩ, C = 0.1μF		5		%
RC Oscillator Frequency Temperature Drift	Δf/ΔT	(Exclusive of RC Drift)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 1 mA I_{SINK} = 3.2 mA	3.5	4.2 0.25	 0.6	V V
Time Base Output Leakage Current	I_{TBLK}	**RC = Ground**			**5**	**μA**
Timebase Input Voltage	V_{IL} V_{IH}		 **3.5**		**0.8**	**V** **V**
Mod Voltage Level 7240,50,60	V_{MOD}	V^+ = 5V V^+ = 15V		4.0 12		V V
Trigger Input Voltage	V_{TRIG}	**V^+ = 5V** **V^+ = 15V**	**0.8** **0.8**	**1.6** **3.5**	**2.0** **4.5**	**V** **V**
Reset Input Voltage	V_{RST}	**V^+ = 5V** **V^+ = 15V**	**0.8** **0.8**	**1.3** **2.7**	**2.0** **4.0**	**V** **V**
Trigger/Reset Input Current	I_{TRIG} I_{RESET}	$-20°C \le T_A \le +85°C$		0.1	10	μA
Max Count Toggle Rate 7240, 7242 7250, 7260	f_t	**V^+ = 2V Fixed Counter/** **V^+ = 5V Divider Mode** **V^+ = 15V** **50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND**	**3**	**1** **8** **15**		**MHz** **MHz** **MHz**
Max Count Toggle Rate 7240, 7250, 7260	f_t	**Programmable Divide Mode (Note 2)**	**200**			**kHz**
Carry Out Source **Source Output Current** **Sink Output Current**	I_{COH}	 **$V_{OH} = V^+ - 1V$** **V_{OL} = +0.4 Volts**	 **300** **3.2**			 **μA** **mA**
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output V^+ = +5V, I_{SINK} = 3.2 mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	V^+ = +5V, per Output			1	μA
Output Sourcing Current 7242	I_{SOURCE}	**V^+ = +5V terminals 2,8,3** **$V_{OUT} = V^+ - 1V$**	**300**			**μA**
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \le 5.5V$ $V^+ \le 16V$	1k 1k		22M 22M	Ω Ω
RC Input Leakage	I_{RC}	**RC = 2.5V**			**10**	**nA**

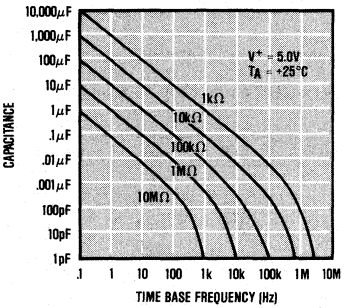
Note 1: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883C Method 3015.2 Test Circuit).

Note 2: Parameter is Q.A. sample tested.

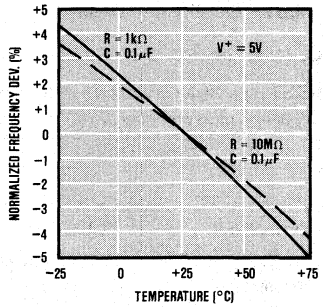
Fixed And Programmable Timer/Counters

Typical Operating Characteristics

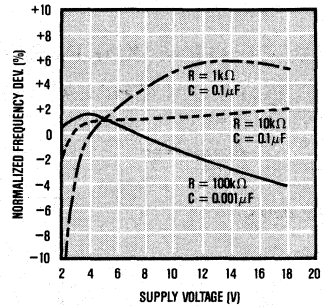
RC OSCILLATOR FREQUENCY vs. R AND C



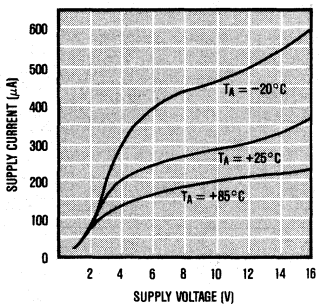
NORMALIZED FREQUENCY vs. TEMPERATURE



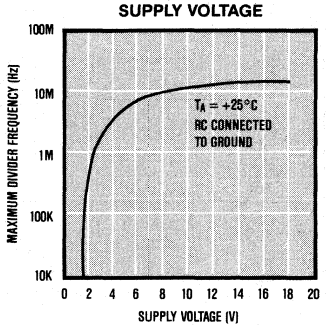
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



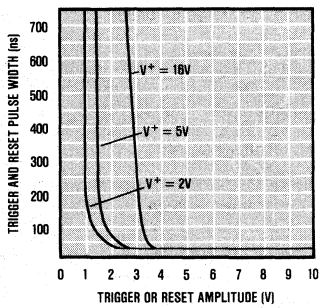
SUPPLY CURRENT vs. SUPPLY VOLTAGE OVER TEMPERATURE



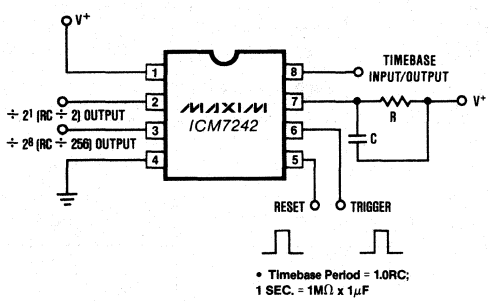
MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



MINIMUM RESET AND TRIGGER PULSE WIDTH vs. AMPLITUDE

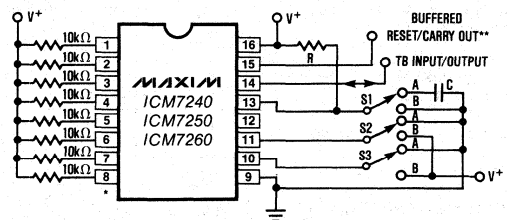


Test Circuits



Note: Outputs ÷ 2^1 and ÷ 2^8 are inverters and have active pullups.

ICM7240/50/60



S1—A = RC Run
B = T. B. Input Run

S2—A = Inactive
B = Trigger

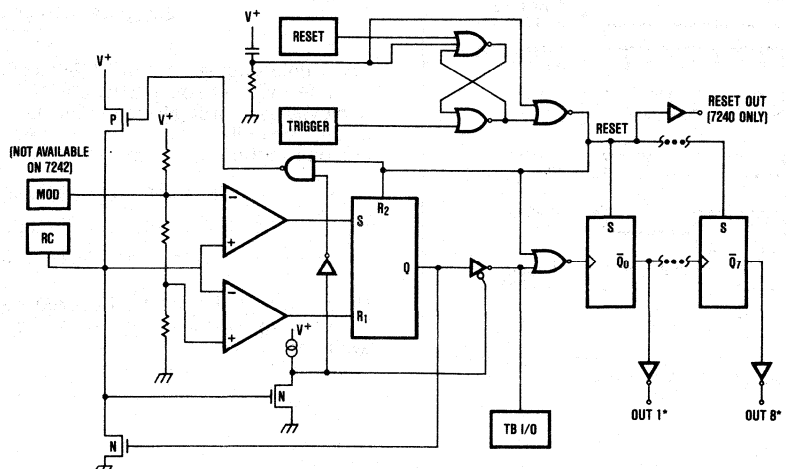
S3—A = Inactive
B = Reset

Note: S1-B inhibits the timebase section, allowing terminal 14 to become the counter input.
***Note:** Terminal 8 is open circuit for 7260.
****Note:** Terminal 15 is open circuit for 7250/60 devices.

Table 1. PIN DESCRIPTIONS

PIN NAME	PIN # ICM7240/50/60	PIN # ICM7242	DESCRIPTION
V^+	16	1	Positive power supply pin.
GND	9	4	Ground
RC	13	7	RC timing node. If this pin is grounded, the TB I/O pin is an external clock input. An external resistor and capacitor connected to this pin sets the frequency of the internal oscillator to 1/RC.
Trigger	11	6	The Trigger input sets the internal control flip-flop to the Run state. If the counter is reset and TB I/O is low, a high on Trigger will clock the counter to the all 0s count and counting will begin. If the counter is reset and TB I/O is high, a high level on Trigger will only set the control flip-flop. The counter will clock to the all 0s count on the next falling edge of TB I/O, provided the control flip-flop is set.
Reset	10	5	A high input on Reset while Trigger is low will reset the counter, force all counter outputs high, and stop the counter by resetting the control flip-flop. The Reset input has no effect if Trigger is high.
TB I/O	14	8	The TB I/O pin is an external clock input if the RC pin is grounded. If RC is not grounded the TB I/O pin is the timebase oscillator output. The Maxim TB I/O output is fully buffered and can drive up to 1000pF of capacitance.
Carry Out	15 (ICM 7250/60 only)	—	Carry goes high during the last 10 counts—50 through 59 in the ICM 7260, 90 through 99 in the ICM7250. To cascade two ICM 7250/60s, drive the TB I/O pin of one ICM7250/60 with the Carry Out of the other. (Use the ÷ 128 output to cascade ICM7240 and ICM7242.)
Buffered Reset	15	—	Buffered output of the Reset input of the control flip-flop. (Maxim ICM7240 only)
Counter Outputs	1-8		The ICM7240/50/60 outputs are open drain n-channel outputs which sink current when on and are open circuits when off. These outputs are TTL and CMOS compatible if a pullup resistor is connected to V^+.
Counter Outputs	—	2,3	The ICM7242 outputs are logic outputs which both sink and source currents. The ICM7242 outputs are both TTL and CMOS compatible and do not require pullups. The ÷ 2 output is a square wave at ½ the frequency of the onboard oscillator or external timebase. The ÷ 128/256 output is a square wave with a period 256 times the oscillator or external timebase period. This pin goes high 128 clock cycles after the counter is triggered.
MOD	12	—	Similar to the Control input of an ICM7555, this pin is connected to the resistor string that sets the oscillator thresholds. The internal resistor divider drives the Modulation (MOD) pin to 80% of V^+. Varying the MOD voltage will adjust the oscillator frequency.

Block Diagram



*ICM7240, 7250, 7260 have open drain outputs

Fixed And Programmable Timer/Counters

Circuit Description

The timing cycle is controlled by the internal control flip-flop. This set-reset flip-flop is set to the Run state by a high level on the Trigger input. A high level on the Reset input puts the control flip-flop into the Reset state, provided Trigger is low. Trigger overrides Reset: if both Trigger and Reset are high the control flip-flop is set to the Run state.

When the control flip-flop is set to the run state the counter is set to all 0s (all outputs low), the timebase input is also enabled, and the counter will increment with each negative-going edge at TB I/O.

A high level on the Reset input while Trigger is low resets the control flip-flop. The flip-flop resets the counter forcing all the counter outputs high, inhibiting the counter from being incremented, and unless in the external timebase mode, turns on the internal pullup connected to the RC pin.

The RC oscillator period is set by an external resistor and capacitor. The external resistor charges the capacitor to 80% of V^+. This voltage is detected at the RC terminal, TB I/O goes low, the counter increments one count, and the internal discharge transistor rapidly discharges the capacitor to 45% of V^+. When the capacitor voltage goes below 45% of V^+ the internal discharge transistor turns off, TB I/O goes high, and the external capacitor again starts to charge through the external resistor. The period of each oscillator cycle is 1.0 RC.

In many applications, one or more of the counter outputs can be used to reset the counter after a programmed count is completed. With no outputs connected back to the Reset pin, the circuit operates in the astable (free running) mode.

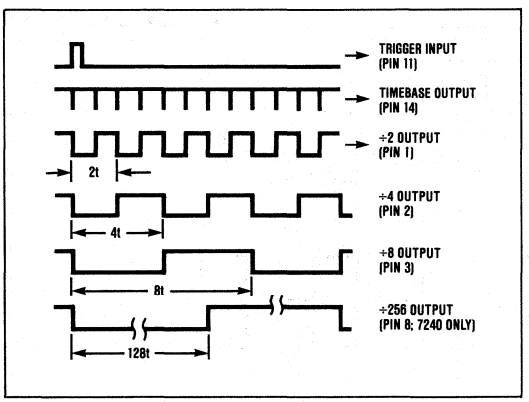
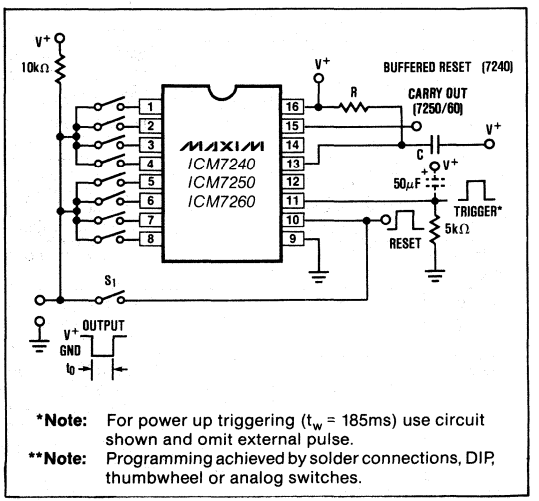


Figure 1. Timing Diagram for ICM7240/50/60.

Applications

Programmable Time Delay

Figure 2 shows a basic programmable time delay. When the circuit is triggered all outputs go low. When the programmed count is reached, the Reset input is pulled high by the 10kΩ resistor, resetting the counter. The programming can be achieved by using either mechanical switches such as thumbwheel or DIP switches, or analog switches such as the CD4016 and CD4066.



**Note: For power up triggering (t_w = 185ms) use circuit shown and omit external pulse.

**Note: Programming achieved by solder connections, DIP, thumbwheel or analog switches.

Figure 2. Generalized Circuit for Timing Applications (Switch S_1 open for astable operation, closed for monostable operation)

Output Count Programming (ICM7240/50/60)

The counter outputs on the ICM7240/50/60 are open-drain-channel FETs, enabling a "wired-OR" connection to be achieved by shorting together the desired outputs with a common pull-up resistor. In this way, the timing cycle can be programmed from:

1RC to 255RC (ICM7240)
1RC to 99RC (ICM7250)
1RC to 59RC (ICM7260)

Programming the ICM7240/50/60 can achieved by hard wiring, DIP switches, or standard thumbwheel switches.

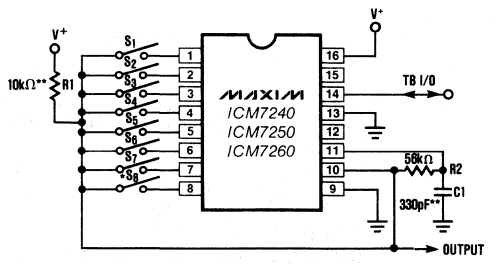
ICM7242 Counter Outputs

The ICM7242 is a non-programmable timer/counter. The outputs on the ICM7242 are inverters which both source and sink current, unlike the open drain N-channel outputs of the ICM7240/50/60 which only sink current. The ICM7242 output inverters eliminate the need for external pull-up resistors.

Outputs on pins 2 and 3 are ÷2 and ÷2^8 respectively. To use the 8 bit counter without the timebase, connect pin 7 (RC) to ground and drive pin 8 (TB I/O) with an external timebase. For monostable applications connect the ÷2^8 output to the reset pin.

Programmable Divider

With the addition of an RC network betweeen the Reset and Trigger inputs, the circuit of Figure 3 becomes a programmable divider. The output period is N times the oscillator (or external input) period, where N is the number programmed into the thumbwheel switches. The 56kΩ and 30pF RC network drives the Trigger high approximately 7μs after Reset goes high, retriggering the counter and starting the cycle again. For high speed operation the capacitor should be reduced to 39pF and the 10kΩ pullup resistor reduced to 2.2kΩ.



* **Note:** S_2 not used on ICM7260.
****Note:** For high-speed operation replace resistor R1 with 2.2 kΩ and capacitor C1 with 39pF.

Figure 3. Programming the Counter Section of the ICM7240/50/60

Competitive Comparison

Maxim's ICM7240/42/50/60 devices are upwardly compatible with Intersil's devices. The counters used in Maxim's parts are synchronous versus the ripple-type used in Intersil's parts. In the programmable divider mode, the maximum frequency of operation is limited by the propagation delay across the counter and the reset delay of the flip-flop. These delays must be less than one half the timebase period, for reliable operation.

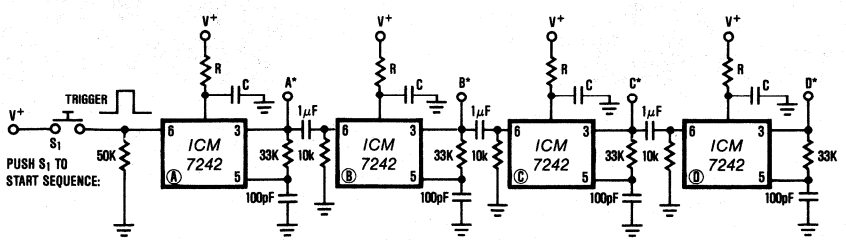
Maxim's ICM7240 has a Buffered Reset Output on pin 15 versus a No Connection on Intersil's part. This output is a buffered output from the reset line for the counters contained within the ICM7240, so that when the device is being used in the programmable divider mode, the output can be used as the divider count output.

When Maxim's devices are operated with the time-base inhibited (RC pin grounded) and the counter is reset, the supply current for the Maxim part is guaranteed to be no more than 10μA versus a possible 8mA at +5Volts and 20mA at +16Volts for the Intersil part.

The TB I/O output has significantly improved drive capability and can drive up to 1,000pF of load capacitance versus 50pf for the Intersil part. Maxim's devices are also less sensitive than Intersil's to the rate of change of the input waveform at TB I/O when in the external clock mode. This reduces the possibility of false triggering on slow falling clock waveforms.

Sequence Timer

Figure 4 shows how to cascade multiple counters to perform more complex control functions.



***Note:** Select RC values to desired "ON time" for each ICM7242.

Figure 4. Sequence Timer Using ICM7242

Fixed And Programmable Timer/Counters

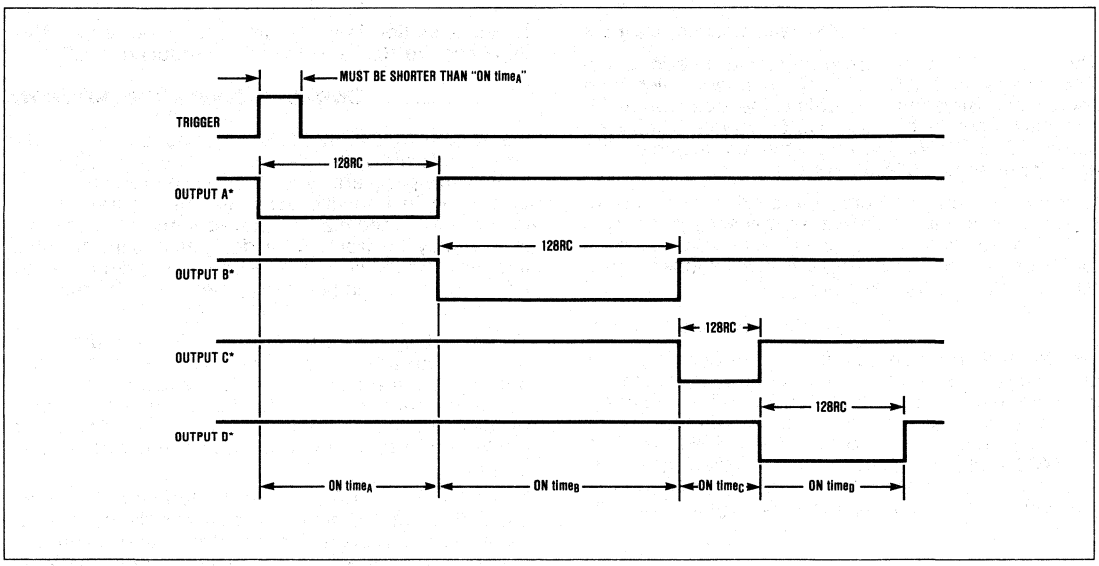
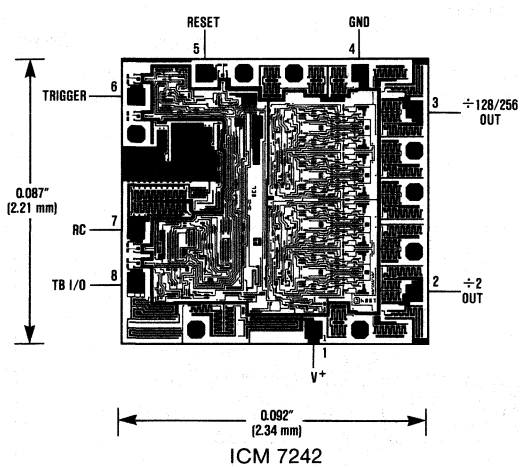
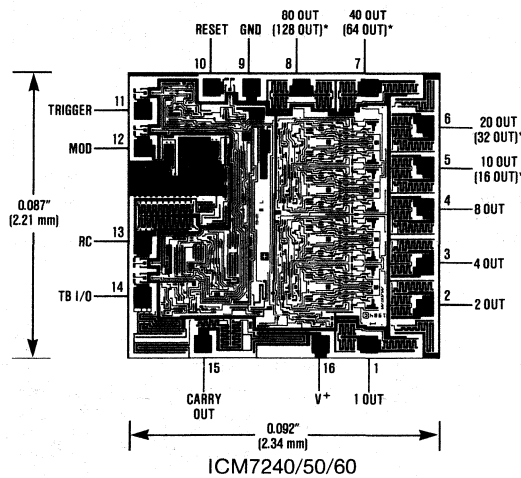


Figure 5. Timing Diagram for Sequence Timer of Figure 4.

Chip Topography



ICM 7242



ICM7240/50/60

***Note:** Pin descriptions in parentheses refer to ICM7240.*

General Description

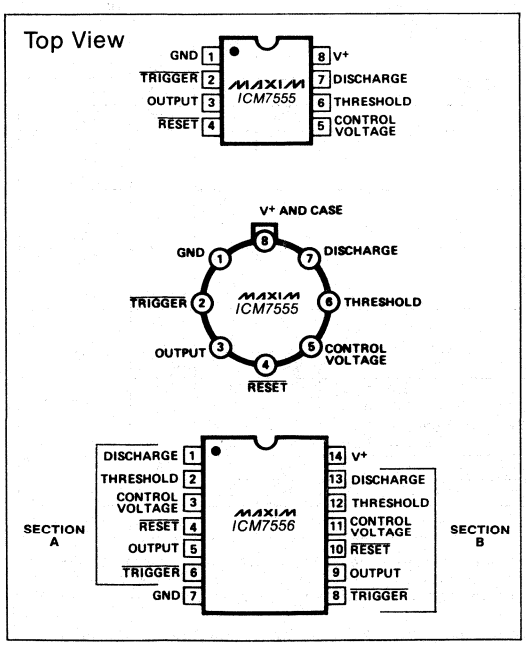
The Maxim ICM7555 and ICM7556 are respectively single and dual general purpose RC timers capable of generating accurate time delays or frequencies. The primary feature is an extremely low supply current, making this device ideal for battery-powered systems. Additional features include low THRESHOLD, TRIGGER, and RESET currents, a wide operating supply voltage range, and improved performance at high frequencies.

These CMOS low-power devices offer significant performance advantages over the standard 555 and 556 bipolar timers. Low-power consumption, combined with the virtually non-existent current spike during output transitions, make these timers the optimal solution in many applications.

Applications

Pulse Generator	Pulse Position Modulation
Precision Timing	Sequential Timing
Time Delay Generation	Missing Pulse Detector
Pulse Width Modulation	

Pin Configuration



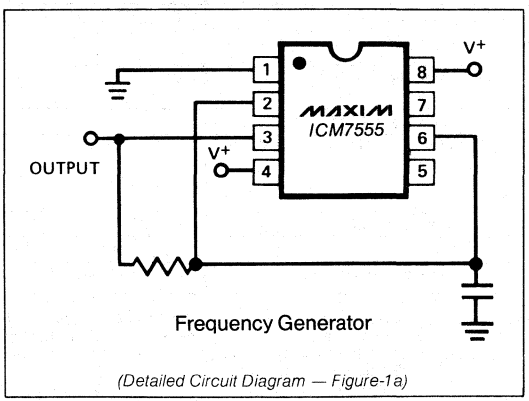
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Wide Supply Voltage Range: 2-18V**
- **No Crowbarring of Supply During Output Transition**
- **Adjustable Duty Cycle**
- **Low THRESHOLD, TRIGGER and RESET Curents**
- **TTL Compatible**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7555IPA	-20°C to +85°C	8 Lead Plastic DIP
ICM7555IJA	-20°C to +85°C	8 Lead CERDIP
ICM7555ITV	-20°C to +85°C	TO-99 Can
ICM7555MJA	-55°C to +125°C	8 Lead CERDIP
ICM7555MTV	-55°C to +125°C	TO-99 Can
ICM7555ISA	-20°C to +85°C	8 Lead Small Outline
ICM7555/D	0°C to +70°C	Dice
ICM7556IPD	-20°C to +85°C	14 Lead Plastic DIP
ICM7556MJD	-55°C to +125°C	14 Lead CERDIP
ICM7556ISD	-20°C to +85°C	14 Lead Small Outline
ICM7556/D	0°C to +70°C	Dice

Typical Operating Circuit



(Detailed Circuit Diagram — Figure-1a)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

General Purpose Timers

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... +18 Volts
Input Voltage TRIGGER
Control Voltage THRESHOLD <V+ + 0.3V to ≥ − 0.3V
RESET

Output Current 100mA
Power Dissipation[2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Operating Temperature Range
ICM7555IJA (Maxim) ..... −20°C to +85°C
ICM7555ISA (Maxim) ..... −20°C to +85°C
ICM7555IPA ..... −20°C to +85°C
ICM7555ITV ..... −20°C to +85°C
ICM7556IPD ..... −20°C to +85°C
ICM7555MTV ..... −55°C to +125°C
ICM7556MJD ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 60 Seconds) ..... +300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +2 to +15 volts; T_A = 25°C, Unless Noted)

PARAMETER	SYMBOL	TEST CONDITIONS			VALUE MIN	VALUE TYP	VALUE MAX	UNITS
Supply Voltage	V^+	−20°C ≤ T_A ≤ +70°C			2		18	V
		−55°C ≤ T_A ≤ +125°C			3		16	V
Supply Current[3]	I^+	ICM7555	V^+ = 2V			60	200	µA
			V^+ = 18V			120	300	µA
		ICM7556	V^+ = 2V			120	400	µA
			V^+ = 18V			240	600	µA
Timing Error		R_A, R_B = 1k to 100k, C = 0.1µF	5V ≤ V^+ ≤ 15V					
Initial Accuracy		Note 4				2.0	5.0	%
Drift with Temperature		Note 4	V^+ = 5V			50		ppm/°C
			V^+ = 10V			75		
			V^+ = 15V			100		
Drift with Supply Voltage		V^+ = 5V				1.0	3.0	%/V
Threshold Voltage	V_{TH}		V^+ = 5V		0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}		V^+ = 5V		0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	V^+ = 18V				50		pA
		V^+ = 5V				10		pA
		V^+ = 2V				1		pA
Threshold Current	I_{TH}	V^+ = 18V				50		pA
		V^+ = 5V				10		pA
		V^+ = 2V				1		pA
Reset Current	I_{RST}	V_{RESET} = Ground	V^+ = 18V			100		pA
			V^+ = 5V			20		pA
			V^+ = 2V			2		pA
Reset Voltage	V_{RST}	V^+ = 18V			0.4	0.7	1.0	V
		V^+ = 2V			0.4	0.7	1.0	V
Control Voltage Lead	V_{CV}		V^+ = 5V		0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo	V^+ = 18V	I_{SINK} = 3.2mA		0.1	0.4	V
			V^+ = 5V	I_{SINK} = 3.2mA		0.15	0.4	V
		Output Hi	V^+ = 18V	I_{SOURCE} = 1.0mA	17.25	17.8		V
			V^+ = 5V	I_{SOURCE} = 1.0mA	4.0	4.5		V
Rise Time of Output	t_r	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Fall Time of Output	t_f	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Guaranteed Max Osc Freq	f_{max}	Astable Operation			500			kHz

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V^- −0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

Note 2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).

Note 3: The supply current value is essentially independent of the TRIGGER, THRESHOLD and RESET voltages.

Note 4: Parameter is not 100% tested. Majority of all units meet this specification.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

General Purpose Timers

- **Lower Supply Current**
- **Increased Output Source Current**
- **Guaranteed THRESHOLD, TRIGGER and RESET Input Currents**
- **Guaranteed Discharge Output Voltage**
- **Supply Current Guaranteed Over Temperature**
- **Significantly Improved ESD Protection (Note 6)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +2 to +15 volts; T_A = 25°C, unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V^+	−20°C ≤ T_A ≤ +85°C −55°C ≤ T_A ≤ +125°C	2 3		16.5 16	V V
Supply Current (Note 3)	I^+	**ICM 7555** V^+ = 2-16.5V; T_A = +25°C V^+ = 5V; T_A = +25°C V^+ = 5V; -20°C ≤ T_A ≤ +85°C V^+ = 5V; -55°C ≤ T_A ≤ +125°C		30	250 120 250 300	µA µA µA µA
		ICM 7556 V^+ = 2-16.5V; T_A = +25°C V^+ = 5V; T_A = +25°C V^+ = 5V; -20°C ≤ T_A ≤ +85°C V^+ = 5V; -55°C ≤ T_A ≤ +125°C		60	500 240 500 600	µA µA µA µA
Timing Error (Note 4) Initial Accuracy (Note 5) Drift with Temperature Drift with Supply Voltage		Circuit of figure 1(b); $R_A = R_B$ = 100kΩ, C = 0.1µF, V^+ = 5V V^+ = 5V V^+ = 10V V^+ = 15V V^+ = 5V		 2.0 50 75 100 1.0	 5.0 3.0	 % ppm/°C ppm/°C ppm/°C %/V
Threshold Voltage	V_{TH}	V^+ = 5V	0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}	V^+ = 5V	0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	V^+ = 16.5V V^+ = 5V V^+ = 2V		50 10 1	500	pA pA pA
Threshold Current	I_{TH}	V^+ = 16.5V V^+ = 5V V^+ = 2V		50 10 1	500	pA pA pA
Reset Current	I_{RST}	V_{RESET} = Ground V^+ = 16.5V V^+ = 5V V^+ = 2V		100 20 2	500	pA pA pA
Reset Voltage	V_{RST}	V^+ = 16.5V V^+ = 2V	0.4 0.4	0.7 0.7	1.2 1.2	V V
Control Voltage	V_{CV}	V^+ = 5V	0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo V^+ = 16.5V I_{SINK} = 3.2mA V^+ = 5V I_{SINK} = 3.2mA **Output Hi** V^+ = 16.5V I_{SOURCE} = 2.0mA V^+ = 5V I_{SOURCE} = 2.0mA	 17.25 4.0	0.1 0.15 17.8 4.5	0.4 0.4	V V V V
Discharge Output Voltage	V_{DIS}	V^+ = 5V, I_{DIS} = 3.2mA		0.1	0.4	V
Rise Time of Output (Note 4)	t_r	R_L = 10MΩ C_L = 10pF V^+ = 5V	35	40	75	ns
Fall Time of Output (Note 4)	t_f	R_L = 10MΩ C_L = 10pF V^+ = 5V	35	40	75	ns
Guaranteed Max Osc. Freq. (Note 4)	f_{max}	Astable Operation	500			kHz

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V^- −0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

Note 2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).

Note 3: The supply current value is essentially independent of the TRIGGER, THRESHOLD AND RESET voltages.

Note 4: Parameter is not 100% tested. Majority of all units meet this specification.

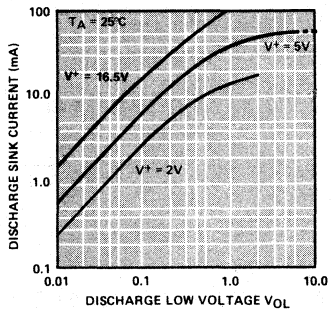
Note 5: Deviation from f = 1.46/(R_A + 2 R_B)C, V^+ = 5V.

Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)

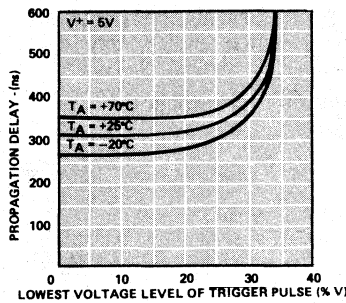
General Purpose Timers

Typical Operating Characteristics

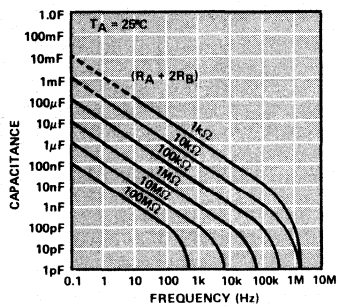
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



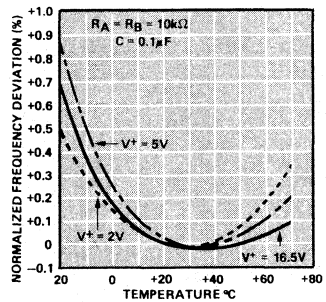
PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



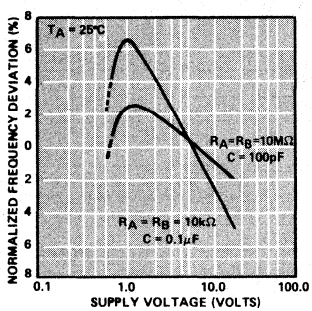
FREE RUNNING FREQUENCY AS A FUNCTION OF R_A, R_B AND C



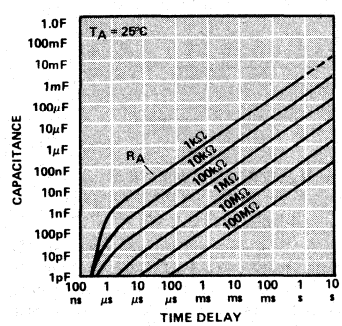
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

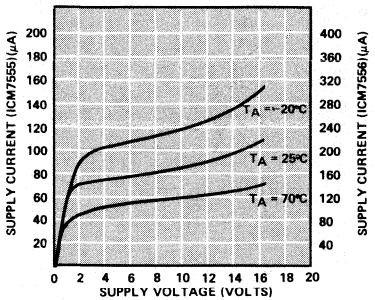


TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF R_A AND C

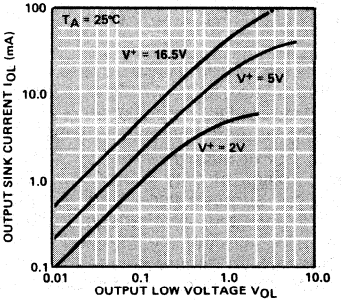


Typical Operating Characteristics

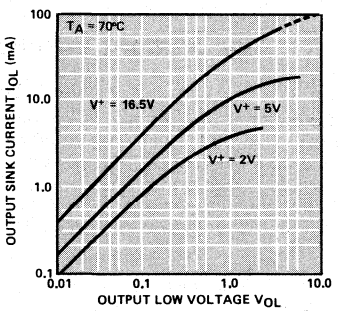
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



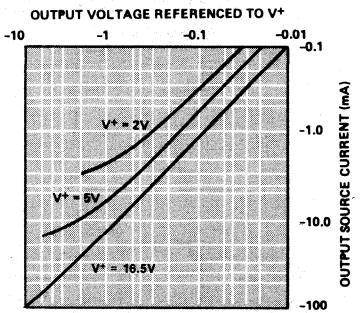
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



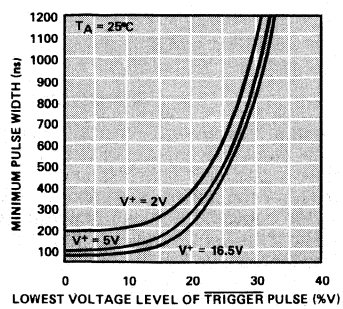
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



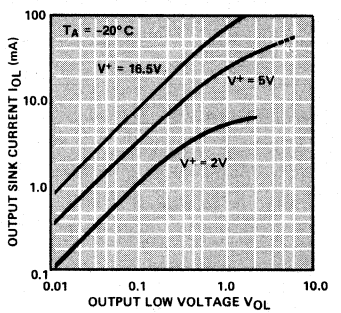
OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



8

General Purpose Timers

Detailed Description

Both the ICM7555 timer and the ICM7556 dual timer can be configured for either astable or monostable operation. In the astable mode the free running frequency and the duty cycle are controlled by two external resistors and one capacitor. Similarly, the pulse width in the monostable mode is precisely controlled by one external resistor and capacitor.

The external component count is decreased when replacing a bipolar timer with the ICM7555 or ICM7556. The bipolar devices produce large crowbar currents in the output driver. To compensate for this spike, a capacitor is used to decouple the power supply lines. The CMOS timers produce supply spikes of only 2-3mA vs. 300-400mA (Bipolar), therefore supply decoupling is typically not needed. This current spike comparison is illustrated in Figure 3. Another component is eliminated at the control voltage pin. These CMOS timers, due to the high impedance inputs of the comparators, do not require decoupling capacitors on the control voltage pin.

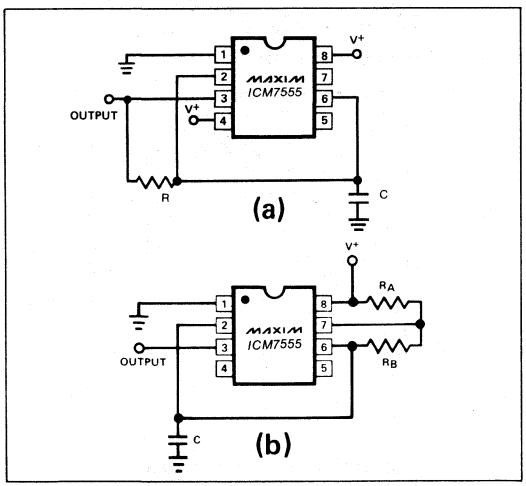


Figure 1. Maxim ICM7555 used in two different astable configurations.

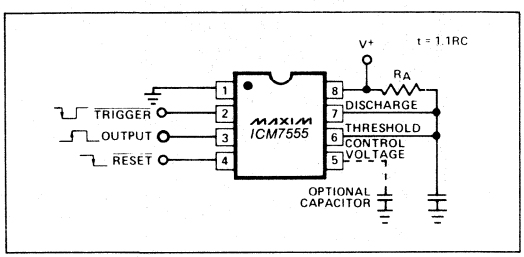


Figure 2. Maxim ICM7555 in a monostable operation.

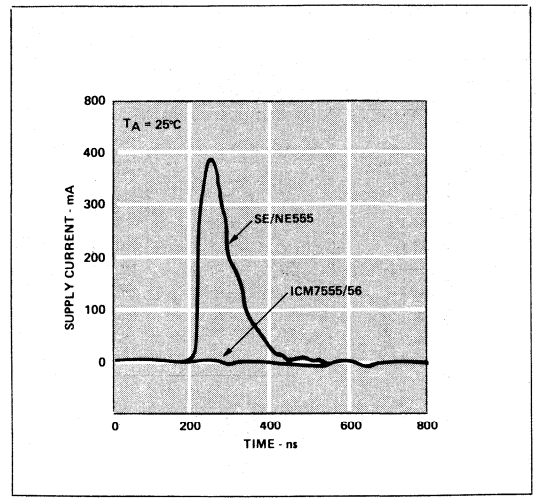


Figure 3. Supply current transient compared with a standard bipolar 555 during an output transition.

Applications Information

Astable Operation

We recommend either of the two astable circuit configurations illustrated in Figure 1. The circuit in (1a) provides a 50% duty cycle output using one timing resistor and capacitor. The oscillator waveform across the capacitor is symmetrical and triangular, swinging from ⅓ to ⅔ of the supply voltage. The frequency generated is defined by:

$$f = \frac{1}{1.4\,RC}$$

The circuit in (1b) provides a means of varying the duty cycle of the oscillator. The frequency is defined by:

$$f = \frac{1.46}{(R_A + 2R_B)C}$$

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

Monostable Operation

The circuit diagram in Figure 2 illustrates monostable operation. In this mode the timer acts as a one shot. Initially the external capacitor is held discharged by the discharge output. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the capacitor begins to charge exponentially through R_A. The device resets after the voltage across the capacitor reaches ⅔(V^+).

$$t_{output} = -\ln(⅓)R_AC = 1.1\,R_AC$$

Reset

The reset function is significantly improved over the standard bipolar 555 and 556 in that it controls only the internal flip-flop, which in turn simultaneously controls the state of the Output and Discharge pins. This avoids the multiple threshold problems sometimes encountered with slow-falling edges of the bipolar devices. This input is designed to have essentially the same trip voltage as the standard bipolar devices (0.6 to 0.7V). At all supply voltages this input maintains an extremely high impedance.

Control Voltage

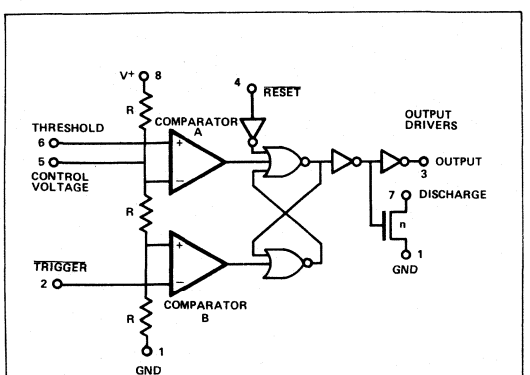
The control voltage regulates the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators. This pin can be used for frequency modulation in the astable mode. By varying the applied voltage to the control voltage pin, delay times can be changed in the monostable mode.

Power Supply Considerations

Since the $\overline{\text{TRIGGER}}$, THRESHOLD and Discharge leakage currents are very low, high impedance timing components may be used, keeping total system supply current at a minimum.

Output Drive Capability

The CMOS output stage is capable of driving most logic families including CMOS and TTL. The ICM7555 and ICM7556 will drive at least two standard TTL loads at a supply voltage of 4.5V or greater. When driving CMOS, the output swing at all supply voltage levels will equal the supply voltage.



This block diagram reduces the circuitry down to its simplest equivalent components.
R = 100kΩ, ±20% typ.

Figure 4. Block diagram of ICM7555.

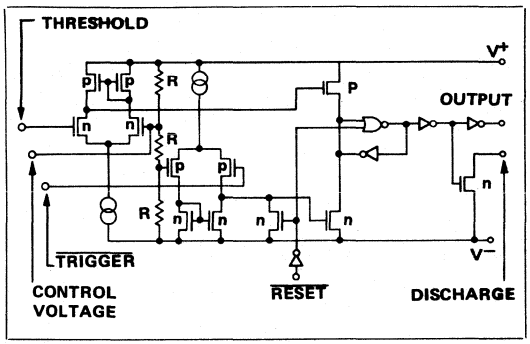


Figure 5. Equivalent circuit.

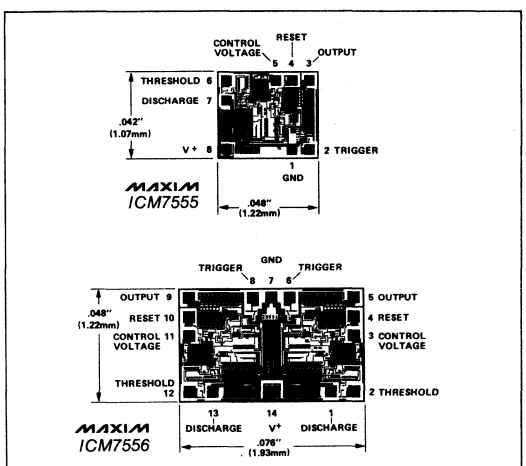
Function Table

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	$< \frac{1}{3} V^+$	Irrelevant	High	Off
High	$> \frac{1}{3} V^+$	$> \frac{2}{3} V^+$	Low	On
High	$> \frac{1}{3} V^+$	$< \frac{2}{3} V^+$	As previously established	

†Voltages levels shown are nominal.

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs. $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Chip Topographies



8

MAXIM

Interface

RS-232 Line Drivers/Receivers

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Components	Low Power Shutdown/ TTL 3-State	Comments	Page No.
MAX230	+5V	5	0	4 capacitors	Yes/No	Needs only +5V	9-1
MAX231	+5V and +7.5V to 13.2V	2	2	2 capacitors	No/No	For 9V battery or +5V and +12V	9-1
MAX232	+5V	2	2	4 capacitors	No/No	Needs only +5V	9-1
MAX233	+5V	2	2	None	No/No	Needs only +5V,	9-1
MAX234	+5V	4	0	4 capacitors	No/No	Needs only +5V	9-1
MAX235	+5V	5	5	None	Yes/Yes	Needs only +5V	9-1
MAX236	+5V	4	3	4 capacitors	Yes/Yes	Needs only +5V	9-1
MAX237	+5V	5	3	4 capacitors	No/No	Needs only +5V	9-1
MAX238	+5V	4	4	4 capacitors	No/No	Needs only +5V	9-1
MAX239	+5V and +7.5V to 13.2V	3	5	2 capacitors	Yes/No	For 9V battery or +5V and +12V.	9-1
MAX240	+5V	5	5	4	Yes/Yes	Needs only +5V	9-1
MAX241	+5V	4	5	4	Yes/Yes	Needs only +5V	9-1

MAXIM

+5V Powered RS-232 Drivers/Receivers

General Description

Maxim's family of line drivers/receivers are intended for all RS-232 and V.28/V.24 communications interfaces, and in particular, for those applications where ±12V is not available. The MAX230, MAX236, MAX240 and MAX241 are particularly useful in battery powered systems since their low power shutdown mode reduces power dissipation to less than 5μW. The MAX233 and MAX235 use no external components and are recommended for applications where printed circuit board space is critical.

All members of the family except the MAX231 and MAX239 need only a single +5V supply for operation. The RS-232 drivers/receivers have on-board charge pump voltage converters which convert the +5V input power to the ±10V needed to generate the RS-232 output levels. The MAX231 and MAX239, designed to operate from +5V and +12V, contain a +12V to -12V charge pump voltage converter.

Since nearly all RS-232 applications need both line drivers and receivers, the family includes both receivers and drivers in one package. The wide variety of RS-232 applications require differing numbers of drivers and receivers. Maxim offers a wide selection of RS-232 driver/receiver combinations in order to minimize the package count (see table below).

Both the receivers and the line drivers (transmitters) meet all EIA RS-232C and CCITT V.28 specifications.

Features

- **Operates from Single 5V Power Supply (+5V and +12V — MAX231 and MAX239)**
- **Meets All RS-232C and V.28 Specifications**
- **Multiple Drivers and Receivers**
- **Onboard DC-DC Converters**
- **±9V Output Swing with +5V Supply**
- **Low Power Shutdown — <1μA (typ)**
- **3-State TTL/CMOS Receiver Outputs**
- **±30V Receiver Input Levels**

Applications

Computers
Peripherals
Modems
Printers
Instruments

Selection Table

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Components	Low Power Shutdown /TTL 3-State	No. of Pins
MAX230	+5V	5	0	4 capacitors	Yes/No	20
MAX231	+5V and +7.5V to 13.2V	2	2	2 capacitors	No/No	14
MAX232	+5V	2	2	4 capacitors	No/No	16
MAX233	+5V	2	2	None	No/No	20
MAX234	+5V	4	0	4 capacitors	No/No	16
MAX235	+5V	5	5	None	Yes/Yes	24
MAX236	+5V	4	3	4 capacitors	Yes/Yes	24
MAX237	+5V	5	3	4 capacitors	No/No	24
MAX238	+5V	4	4	4 capacitors	No/No	24
MAX239	+5V and +7.5V to 13.2V	3	5	2 capacitors	No/Yes	24
MAX240	+5V	5	5	4 capacitors	Yes/Yes	44 (Flatpak)
MAX241	+5V	4	5	4 capacitors	Yes/Yes	28 (Small Outline)

*Patent Pending

+5V Powered RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V^+ ..... (V_{CC} - 0.3V) to +14V
V^- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3 to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V^+ + 0.3V) to (V^- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)

Short Circuit Duration
T_{OUT} ..... continuous
Power Dissipation
CERDIP 675mW
(derate 9.5mW/°C above +70°C)
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline (SO) 375mW
(derate 7mW/°C above +70°C)
Lead Temperature (soldering 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX232, 234, 236, 237, 238, 240, 241 V_{CC} = 5V ± 10%; MAX233, 235 V_{CC} = 5V ± 5%; MAX231, 239 V_{CC} = 5V ± 10%, V^+ = 7.5V to 13.2V; T_A = Operating Temperature Range, Figures 3-14, unless otherwise noted.)

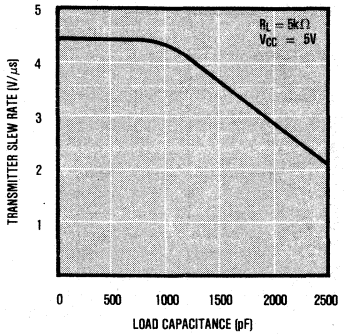
PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Swing	All Transmitter Outputs loaded with 3kΩ to Ground		±5	±9		V
V_{CC} Power Supply Current	No load, T_A = +25°C			5	10	mA
	MAX231, MAX239			0.4	1	
V^+ Power Supply Current	No load, MAX231 and MAX239 only	MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	Figure 1, T_A = +25°C			1	10	µA
Input Logic Threshold Low	T_{IN}, $\overline{EN}$, Shutdown				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	$\overline{EN}$, Shutdown		2.4			
Logic Pullup Current	T_{IN} = 0V			15	200	µA
RS-232 Input Voltage Operating Range			-30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V, T_A = +25°C (MAX231, 239 V^+ = 0V)		0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V, T_A = +25°C (MAX231, 239 V^+ = 12V)			1.7	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231-233, I_{OUT} = 3.2mA)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5			V
TTL/CMOS Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}			0.05	±10	µA
Output Enable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, 241			400		ns
Output Disable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, 241			250		ns
Propagation Delay	RS-232 to TTL			0.5		µs
Instantaneous Slew Rate	C_L = 10pF, R_L = 3-7kΩ T_A = +25°C (Note 1)				30	V/µs
Transition Region Slew Rate	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V			3		V/µs
Output Resistance	V_{CC} = V^+ = V^- = 0V, V_{OUT} = ±2V		300			Ω
RS-232 Output Short Circuit Current				±10		mA

Note 1: Sample tested.

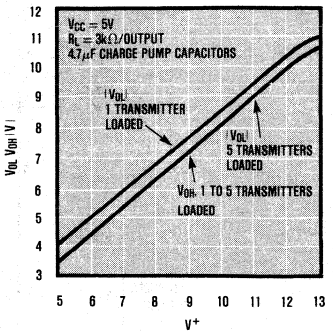
+5V Powered RS-232 Drivers/Receivers

Typical Operating Characteristics

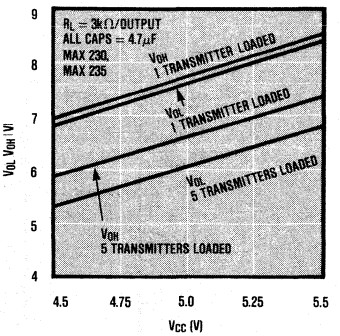
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



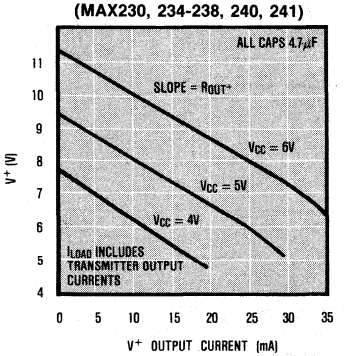
MAX239 TRANSMITTER OUTPUT VOLTAGE vs. V+ VOLTAGE



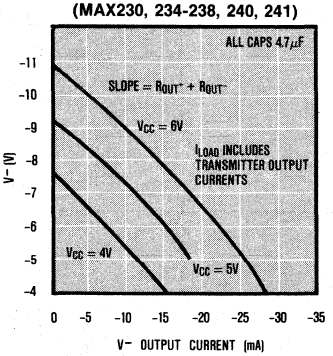
TRANSMITTER OUTPUT VOLTAGE vs. VCC VOLTAGE



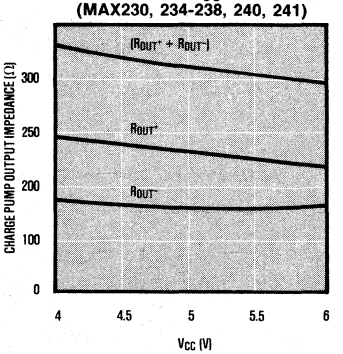
V+ SUPPLY VOLTAGE vs. LOAD CURRENT (MAX230, 234-238, 240, 241)



V- SUPPLY VOLTAGE vs. LOAD CURRENT (MAX230, 234-238, 240, 241)



CHARGE PUMP OUTPUT IMPEDANCE vs. VCC (MAX230, 234-238, 240, 241)



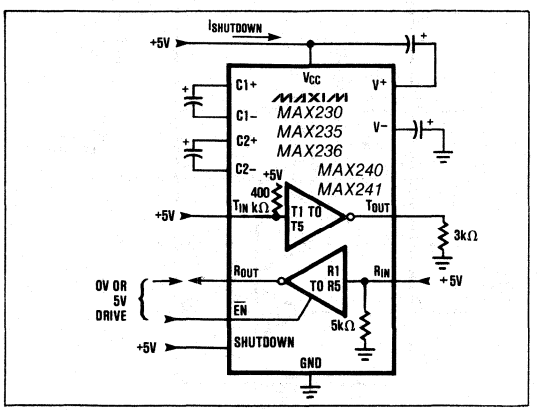


Figure 1. Shutdown Current Test Circuit

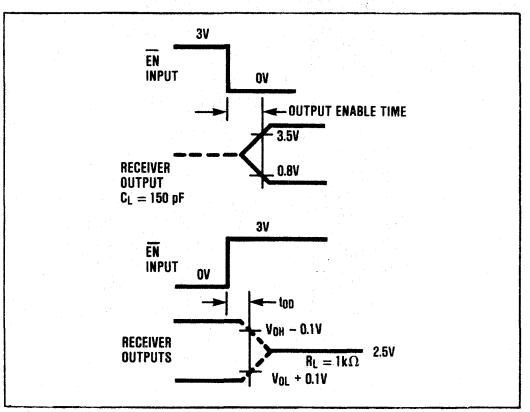
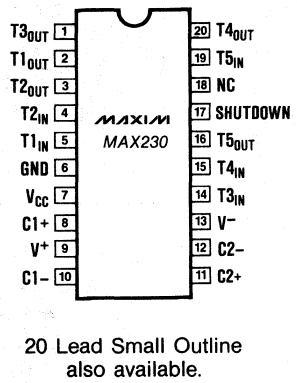


Figure 2. Receiver Output Enable and Disable Timing

+5V Powered RS-232 Drivers/Receivers



20 Lead Small Outline
also available.

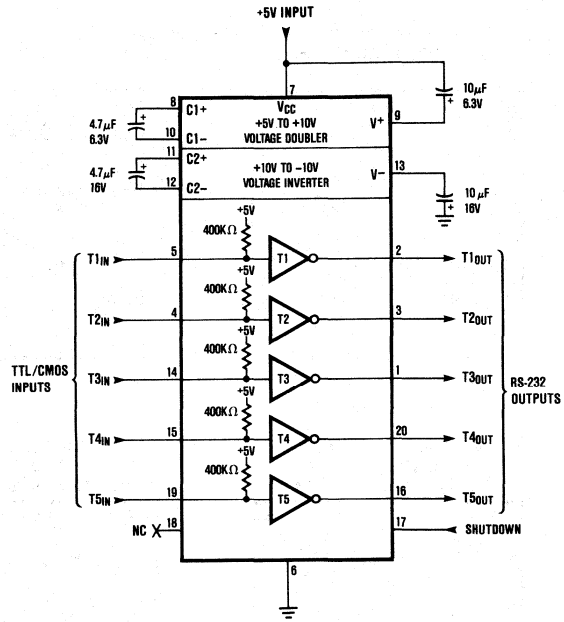
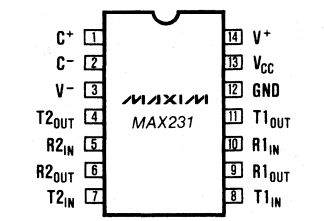
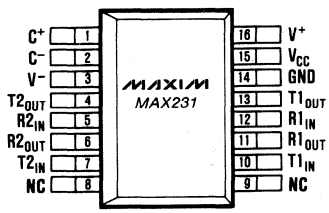


Figure 3. MAX230 Typical Operating Circuit



14 Lead Plastic DIP



16 Lead Small Outline

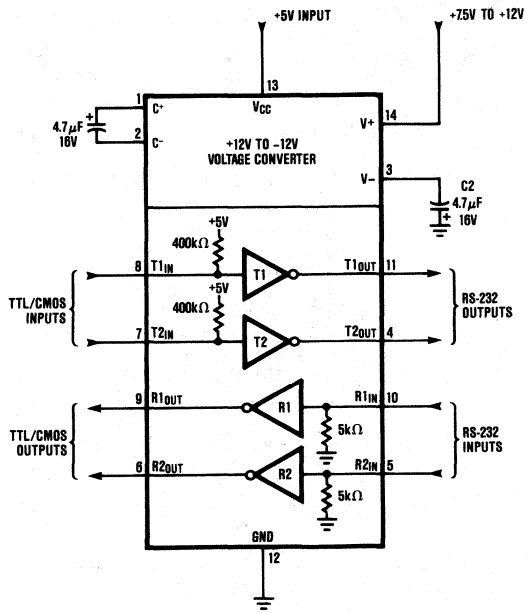
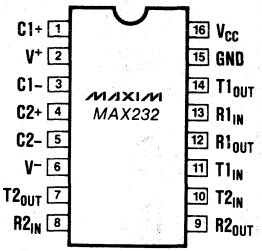


Figure 4. MAX231 Typical Operating Circuit



16 Lead Small Outline
also available.

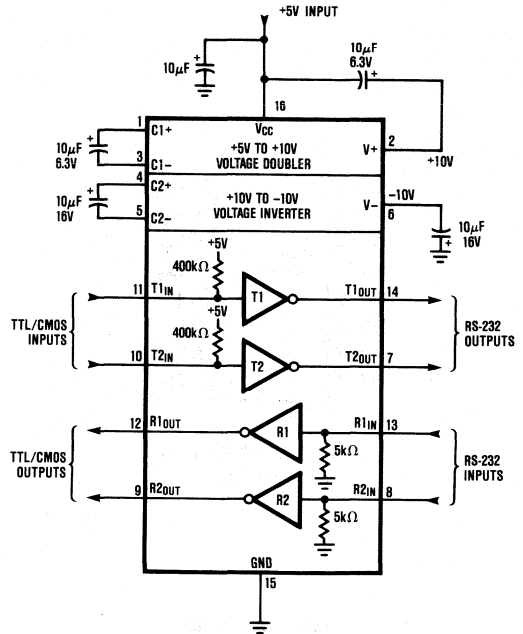
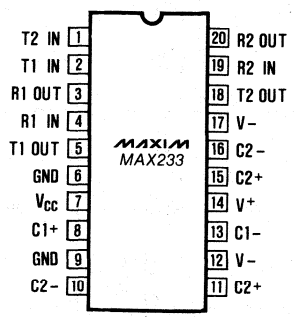


Figure 5. MAX232 Typical Operating Circuit



Small Outline Not Available

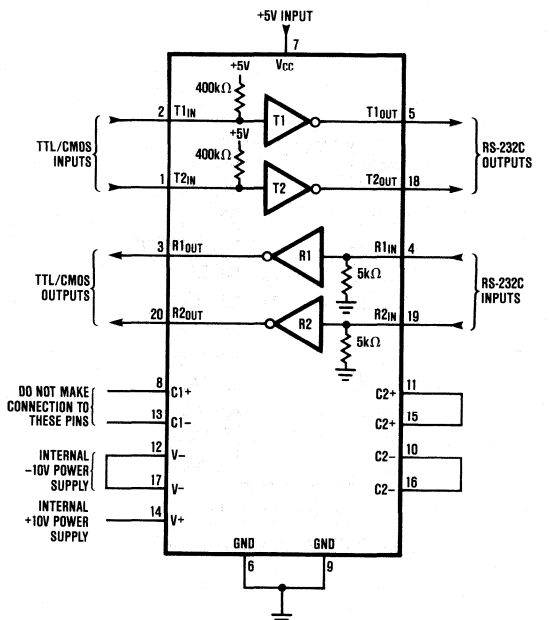
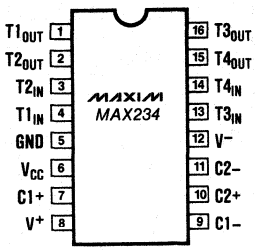


Figure 6. MAX233 Typical Operating Circuit

+5V Powered RS-232 Drivers/Receivers



16 Lead Small Outline
also available.

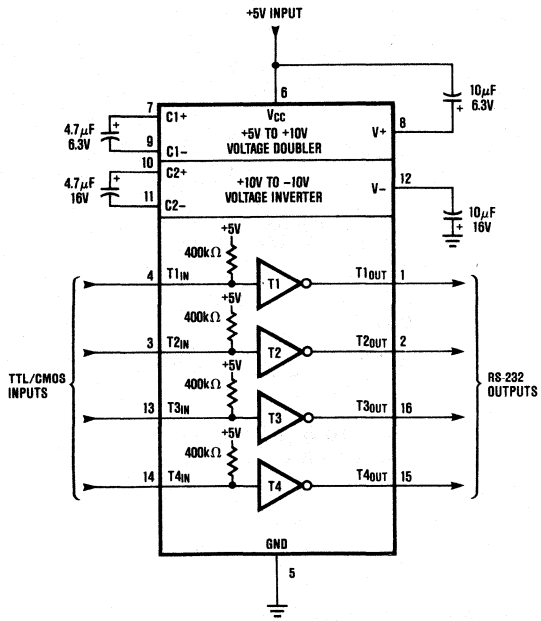
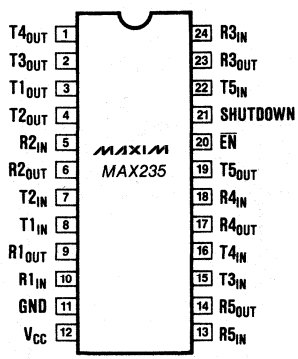


Figure 7. MAX234 Typical Operating Circuit



0.600" Wide Package Only

Small Outline Not Available

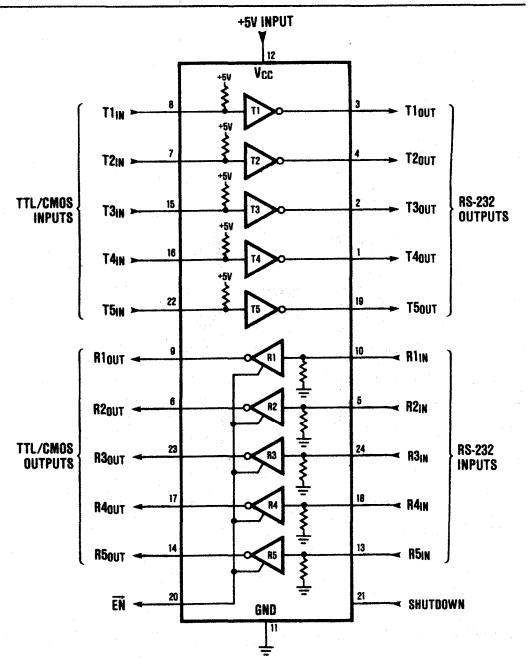
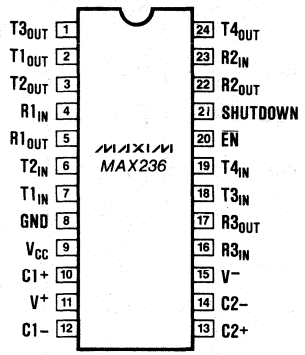


Figure 8. MAX235 Typical Operating Circuit



24 Lead Small Outline
also available.

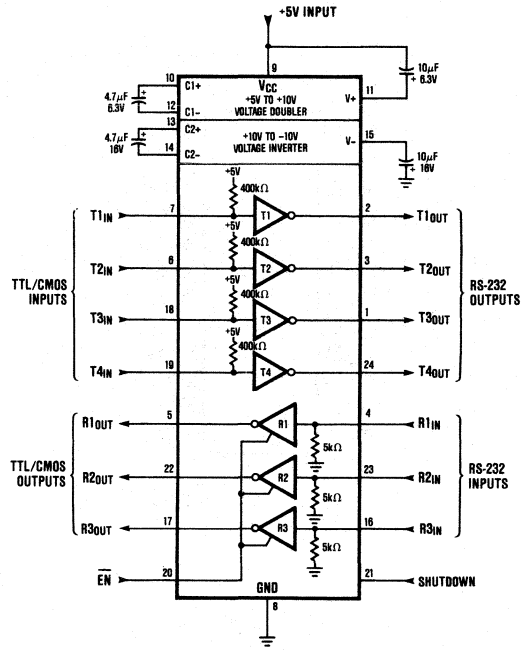
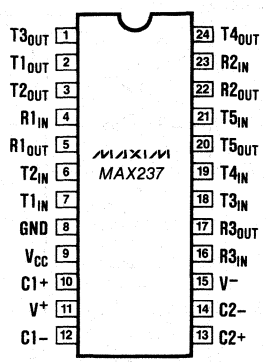


Figure 9. MAX236 Typical Operating Circuit



24 Lead Small Outline
also available.

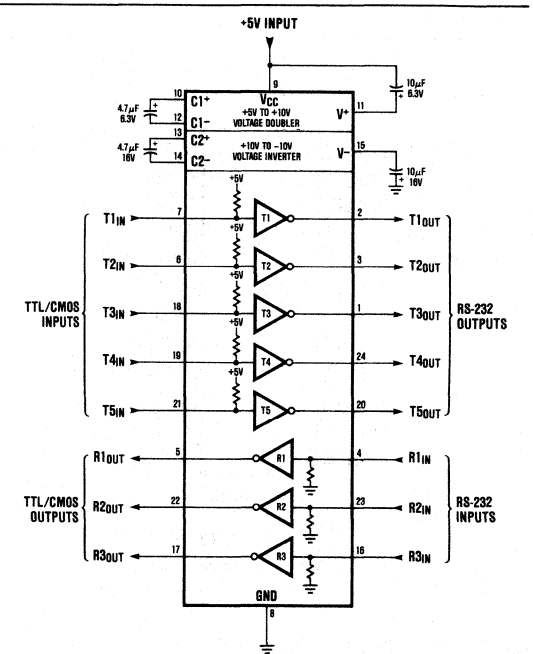
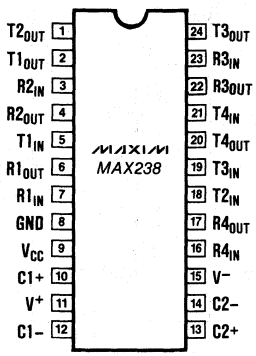


Figure 10. MAX237 Typical Operating Circuit

+5V Powered RS-232 Drivers/Receivers



24 Lead Small Outline
also available.

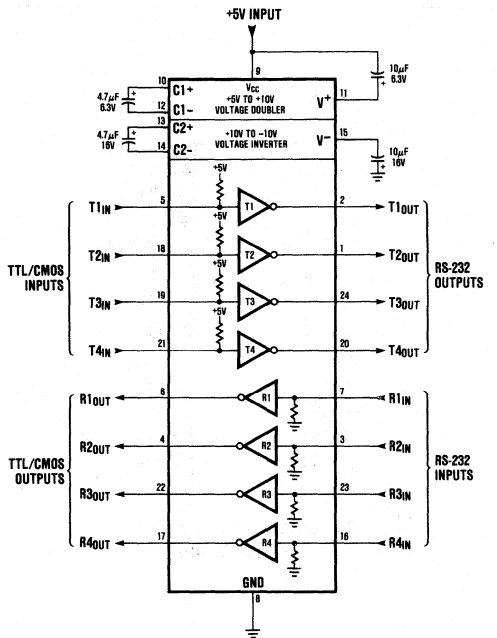
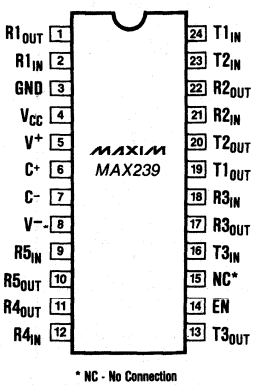


Figure 11. MAX238 Typical Operating Circuit



24 Lead Small Outline
also available.

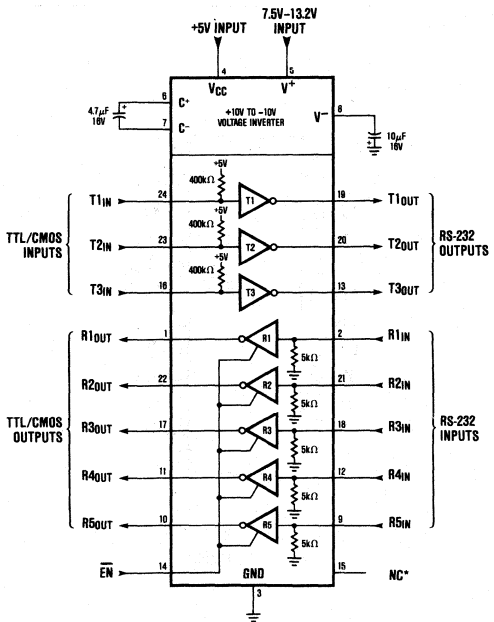
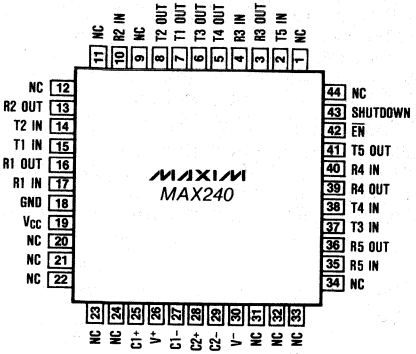


Figure 12. MAX239 Typical Operating Circuit



44 Lead Plastic Flatpak Only

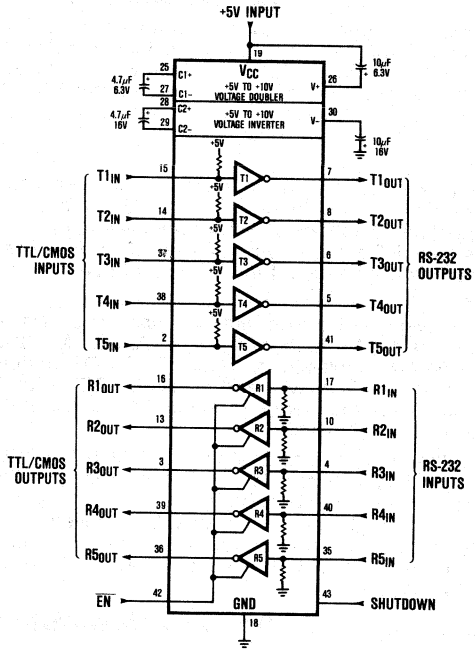
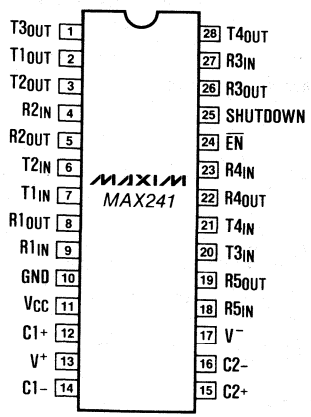


Figure 13. MAX240 Typical Operating Circuit.



28 Lead Wide Small Outline Only

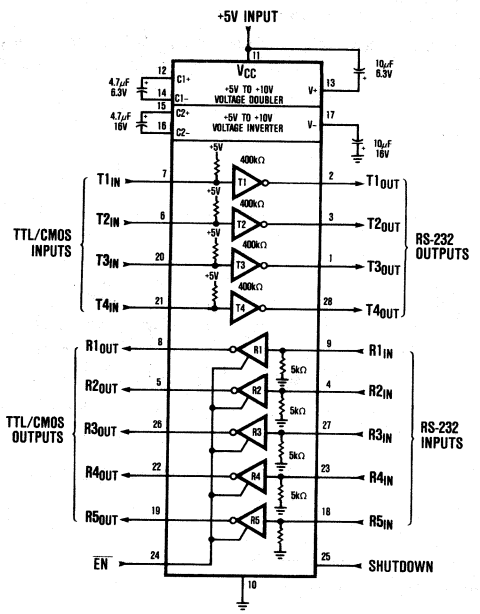


Figure 14. MAX241 Typical Operating Circuit.

+5V Powered RS-232 Drivers/Receivers

Typical Applications

Figures 3 through 14 show typical applications. The capacitor values are non-critical. Reducing the capacitors C1 and C2 to 1μF will slightly increase the impedance of the charge pump, lowering the RS-232 driver output voltages by about 100mV. Lower values of C3 and C4 increase the ripple on the V^+ and V^- outputs.

If the power supply input to the device has a very fast rate-of-rise (as would occur if a PCB were to be plugged into a card cage with power already on), use the simple RC filter shown in Figure 15. This bypass network is not needed if the V_{CC} rate-of-rise is below 1V/μs.

All receivers and drivers are inverting. The $\overline{EN}$able control of the MAX235, MAX236, MAX239, MAX240 and MAX241 enables the receiver TTL/CMOS outputs when it is at a low level, and places the TTL/CMOS outputs of the receivers into a high impedance state when it is a high level.

When the Shutdown control of the MAX230, MAX235, MAX236, MAX240 and MAX241 is at a logic 1 the charge pump is turned off, the receiver outputs are put into the high impedance state, V^+ is pulled down to V_{CC}, V^- is pulled up to ground, and the transmitter outputs are disabled. The supply current drops to less than 10μA.

Detailed Description

The following sections provide supplementary information for those designers with non-standard applications and for those with interest in the internal operation of the devices.

The devices consist of 3 sections: the transmitters, the receivers, and the charge pump DC-DC voltage converter.

+5V to ±10V Dual Charge Pump Voltage Converter

All but the MAX231 and MAX239 convert +5V to ±10V. This conversion is performed by two charge pump voltage converters. The first uses capacitor C1 to double the +5V to +10V, storing the +10V on the V^+ output filter capacitor, C3. The second charge pump voltage converter uses capacitor C2 to invert the +10V to -10V, storing the -10V on the V^- output filter capacitor, C4. The equivalent circuit of the charge pump section is shown in Figure 16.

A small amount of power may be drawn from the +10V (V^+) and -10V (V^-) outputs to power external circuitry. The typical characteristics graphs show the typical output voltage vs. load current characteristics.

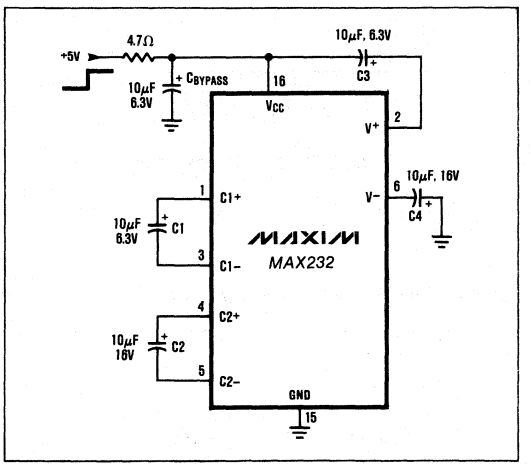


Figure 15. Protection from High $\frac{dV}{dT}$

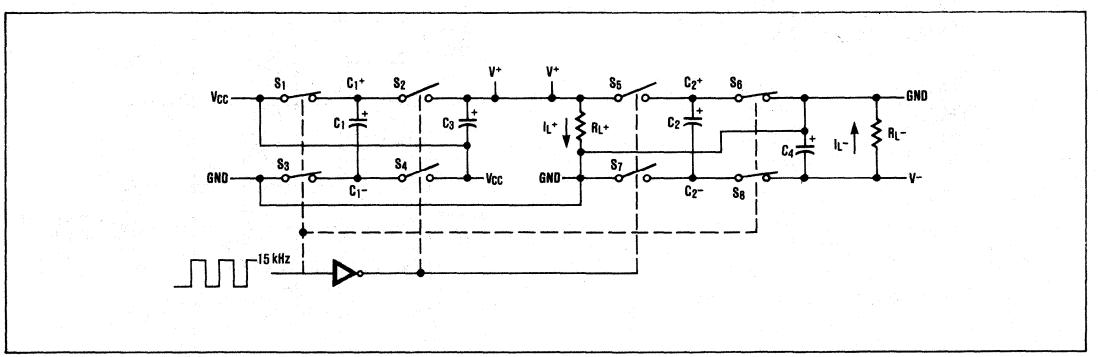


Figure 16. Charge Pump Diagram.

For applications needing only the +5V to ±10V charge pump voltage converter, the MAX680 is available.

The capacitor values for C1 through C4 are non-critical. At the 15kHz typical switching frequency of the voltage converter, a 1μF capacitor has approximately 10Ω impedance, and replacing the 4.7μF and 10μF capacitors shown in the typical applications with 1μF for C1 and C2 will increase the output impedance of the V^+ output by about 10Ω and the output impedance of V^- by about 20Ω. Lowering the value of C3 and C4 increases the ripple on the V^+ and V^- outputs. Where operation to the upper temperature limit is not required, or V_{CC} will not go below 4.75V, C1 and C2 can be 1μF, and C3 and C4 can be 1μF per output channel (1μF if one transmitter is used, 5μF if five transmitters are used).

There are parasitic diodes which become forward biased if V^+ goes below V_{CC} or V^- goes above ground. When in the shutdown mode (MAX230, MAX235, MAX236, MAX240 and MAX241 only), V^+ is internally connected to V_{CC} by a 1kΩ pulldown, and V^- is internally connected to ground via a 1kΩ pullup.

The MAX233 and MAX235 contain all charge pump components, including the capacitors, and operate with NO external components.

The MAX231 and MAX239 include only the V^+ to V^- charge pump, and are intended for applications which have a +5V supply and either a +12V ± 10% supply or a 7.5V to 13.2V battery voltage. When operating with V^+ greater than 8.0V, both capacitors can be 1μF.

Driver (Transmitter) Section

The transmitters or line drivers are inverting level translators which convert the CMOS or TTL input levels to RS-232 or V.28 voltage levels. With +5V V_{CC}, the typical output voltage swing is ±9V when loaded with the nominal 5kΩ input resistance of an RS-232 receiver. The output swing is guaranteed to meet the RS-232/V.28 specification of ±5V minimum output swing under the worst case conditions of all transmitters driving the 3kΩ minimum allowable load impedance, V_{CC} = 4.5V, and maximum operating ambient temperature. The open circuit output voltage swing is from (V^+ - 0.6V) to V^-.

The input thresholds are both CMOS and TTL compatible, with a logic threshold of about 25% of V_{CC}. The inputs of unused drivers sections can be left unconnected; an internal 400kΩ input pullup resistor to V_{CC} will pull the inputs high, forcing the unused transmitter outputs low. The input pullup resistors source about 12μA, and the driver inputs should be driven high or open circuited to minimize power supply current in the shutdown mode.

When in the low power shutdown mode, the driver outputs are turned off and their leakage current is less than 1μA with the driver output pulled to ground. The driver output leakage remains less than 1μA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ. As required by the RS232 and V.28, the slew rate is limited to less than 30V/μs. This limits the maximum usable baud rate to 19,200 baud.

Receiver Section

All but the MAX230 and MAX234 contain RS-232/V.28 receivers. These receivers convert the ±5V to ±15V RS-232 signals to 5V TTL/CMOS outputs. Since the RS-232C/V.28 specifications define a voltage level greater than +3V as a 0, the receivers are inverting. Maxim has set the guaranteed input thresholds of the receivers to 0.8V minimum and 2.4V maximum, which are significantly tighter than the -3.0V minimum and +3.0V maximum required by the RS-232 and V.28 specifications. This allows the receivers to respond both to RS-232/V.28 levels and TTL level inputs. The receivers are protected against input overvoltage up to ±30V.

The 0.8V guaranteed lower threshold is important to ensure that the receivers will have a logic 1 output if the receiver is not being driven because the equipment containing the line driver is turned off or disconnected, or if the connecting cable has an open circuit or short circuit. In other words, the receiver implements Type 1 interpretation of fault conditions (§7 of V.28, §2.5 of RS-232C). While a 0V or even a -3V receiver threshold would be acceptable for the data lines, these lower thresholds would not give proper indication on the control lines such as DTR and DSR. The receivers, on the other hand, have a full 0.8V noise margin for detecting the power-down or cable-disconnected states.

The receivers have a hysteresis of approximately 0.5V, with a minimum guaranteed hysteresis of 200mV. This aids in obtaining clean output transitions, even with slow rise and fall time input signals with moderate amounts of noise and ringing. The propagation delays of the receivers are 350ns for negative-going input signals, and 650ns for positive-going input signals (see Typical Characteristics graphs).

The MAX239 has a receiver 3-state control line, and the MAX235, MAX236, MAX240 and MAX241 have both a receiver 3-state control line and a low power shutdown control. The receiver TTL/CMOS outputs are in a high impedance 3-state mode whenever the 3-state $\overline{\text{EN}}$able line is high, and are also high impedance whenever the Shutdown control line is high.

+5V Powered RS-232 Drivers/Receivers

Review of EIA Standard RS-232-C and CCITT Recommendations V.28 and V.24

The most common serial interface between electronic equipment is the "RS232" interface. This serial interface has been found to be particularly useful for the interface between units made by different manufacturers since the voltage levels are defined by the EIA Standard RS-232-C and CCITT Recommendation V.28. The RS-232 specification also contains signal circuit definitions and connector pin assignments, while CCITT circuit definitions are contained in a separate document, Recommendation V.24. Originally intended to interface modems to computers and terminals, these standards have many signals which are not used for computer-to-computer or computer-to-peripheral communication.

Serial interfaces can be used with a variety of transmission formats. The most popular by far is the asynchronous format, generally at one of the standard baud rates of 300, 600, 1200, etc. The maximum recommended baud rate for RS-232 and V.28 is 20,000 baud, and the fastest commonly used baud rate is 19,200 baud. Asynchronous serial links use a variety of combinations of the number of data bits, what type (if any) of parity bit, and the number of stop bits. A typical combination is 7 data bits, even parity, and 1 stop bit.

RS232/V.28 physical links are also suitable for synchronous transmission protocols. These higher level protocols often use the standard RS-232C/V.28 voltage levels. Note that one type of physical link (such as RS-232/V.28 voltage levels) can be used for a variety of higher level protocols. Table 2 summarizes the voltage levels and other requirements of V.28 and RS-232.

Comparison of RS-232C/V.28 with other Standards

The other two most common serial interface specifications are the EIA RS423 and RS422/RS485 (CCITT recommendations V.10 and V.11). While the RS-232 or V.28/V.24 interface is the most common interface for communication between equipment made by different manufacturers, the RS423/V.10 interface and RS422/V.11 interfaces can operate at higher baud rates. In addition, the RS485 interface can be used for low cost local area networks.

The RS423 and V.10 interfaces are unbalanced or "single-ended" interfaces which use a differential receiver. This standard is intended for data signaling rates up to 100 kbit/s (100 kilobaud). It achieves this higher baud rate through more precise requirements on the waveshape of the transmitters and through the use of differential receivers to compensate for ground potential variations beween the transmitting and receiving equipment. With certain limitations, this interface is compatible with RS-232 and V.28. The limitations are:

1) less than 20,000 baud rate,
2) maximum cable lengths determined by RS-232 performance,
3) RS423/V.10 DTE and DCE signal return paths must be connected to the the RS232/V.28 signal ground,
4) the RS-232 transmitter output voltages must be limited to ±12V, or additional protection must be provided for the RS423/V.10 receivers, and
5) not all RS232/V.28 receivers will show proper power-off detection of V.10 transmitter outputs.

Maxim's MAX230 and MAX232-MAX238, MAX240 and MAX241 meet restrictions 4 and 5 over the entire range of recommended operating conditions. The MAX231 and MAX239 meet restrictions 4 and 5 provided that the V^+ voltage is 12.5V or less.

The RS422, RS485, and V.11 interfaces are balanced double-current interchanges suitable for baud rates up to 10 Mbit/s. These interfaces are not compatible with RS-232 or V.28 voltage levels.

Application Hints

Operation at High Baud Rates

V.28 states that "the time required for the signal to pass through the transition region during a change in state shall not exceed 1 millisecond or 3 percent of the nominal element period on the interchange circuit, whichever is less." RS-232C allows the transition time to be 4 percent of the duration of a signal element. At 19,200 baud, the "nominal element period" is approximately 50μs, of which 3 percent is 1.5μs. Since the transition region is from -3V to +3V, this means the V.28 slew rate would ideally be faster than 6V/1.5μs = 4V/μs at 19.2 kbaud and 2V/μs at 9600 baud. The RS-232 requirement is equivalent to 3V/μs at 19.2 kbaud, 1.5V/μs at 9600 baud, etc. The slew rate of the MAX230 series devices is about 3V/μs with the maximum recommended load of 2500pF. In practice, the effect of less than optimum slew rate is a distortion of the recovered data, where the 1's and 0's no longer have equal width. This distortion generally has negligible effect and the devices can be reliably used for 19.2 kbaud serial links when the cable capacitance is kept below 2500pF. With very low capacitance loading, the MAX230 and MAX234-239, MAX240 and MAX241 may even be used at 38.4 kbaud, since the typical slew rate is 5V/μs when loaded with 500pF in parallel with 5kΩ. Under no circumstance will the

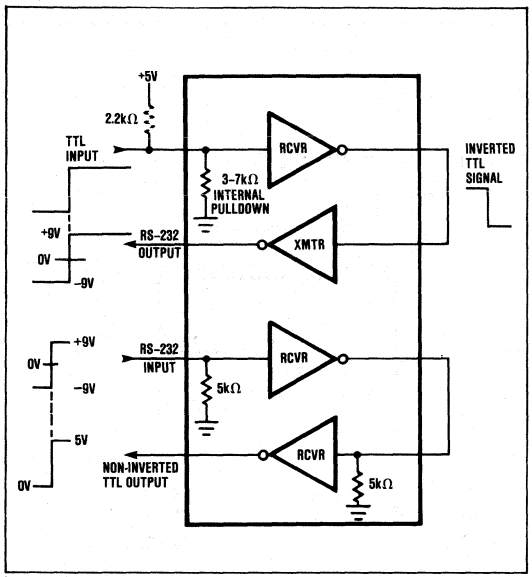


Figure 17. Non-inverting RS-232 Transmitters and Receivers.

slew rate exceed the RS-232/V.28 maximum spec of 30V/μs and, unlike the 1488 driver, no external compensation capacitors are needed under any load condition.

Driving Long Cables

The RS-232 standard states that "The use of short cables (each less than approximately 50 feet or 15 meters) is recommended; however, longer cables are permissible, provided that the load capacitance . . . does not exceed 2500pF."

Baud rate and cable length can be traded off: use lower baud rates for long cables, use short cables if high baud rates are desired. For both long cables and high baud rates, use RS422/V.11. The maximum cable length for a given baud rate is determined by several factors, including the capacitance per meter of cable, the slew rate of the driver under high capacitive loading, the receiver threshold and hysteresis, and the acceptable bit error rate. The receivers have 0.5V of hysteresis, and the drivers are designed such that the slew rate reduction caused by capacitive loading is minimized (see Typical Characteristics).

Non-Inverting Drivers and Receivers

Occasionally a non-inverting driver or receiver is needed instead of the inverting drivers and receivers of the family. Simply use one of the receivers as a TTL/CMOS inverter to get the desired operation (Figure 17). If the logic output driving the receiver input has less than 1mA of output source capability, then add the 2.2kΩ pullup resistor.

The receiver TTL outputs can directly drive the input of another receiver to form a non-inverting RS-232 receiver.

Protection for Shorts to ±15V Supplies

All driver outputs except on the MAX231, MAX232 and MAX233 are protected against short circuits to ±15V, which is the maximum allowable loaded output voltage of an RS-232/V.28 transmitter. The MAX231, MAX232, and MAX233 can be protected against short circuits to ±15V power supplies by the addition of a series 220Ω resistor in each output. This protection is not needed to protect against short circuits to most RS-232 transmitters such as the 1488, since they have an internal short circuit current limit of 12mA.

The power dissipation of the MAX230 and MAX234-MAX239, MAX240 and MAX241 is about 200mW with all transmitters shorted to ±15V.

Isolated RS-232 Interfaces

RS-232 and V.28 specifications require a common ground connection between the two units communicating via the RS-232/V.28 interface. In some cases, there may be large differences in ground potential between the two units, and in other cases it may be desired to avoid ground loop currents by isolating the two grounds. In other cases, a computer or control system must be protected against accidental connection of the RS-232/V.28 signal lines to 110/220VAC power lines. Figure 18 shows a circuit with this isolation. The power for the MAX233 is generated by a MAX635 DC-DC converter. When the MAX635 regulates point "A" to -5V, the isolated output at point "B" will be semi-regulated to +5V. The two optocouplers maintain isolation between the system ground and the RS-232 ground while transferring the data across the isolation barrier. While this circuit will not withstand 110VAC between the RS-232 ground and either the receiver or transmitter lines, the voltage difference between the two grounds is only limited by the optocoupler and DC-DC converter transformer breakdown ratings.

+5V Powered RS-232 Drivers/Receivers

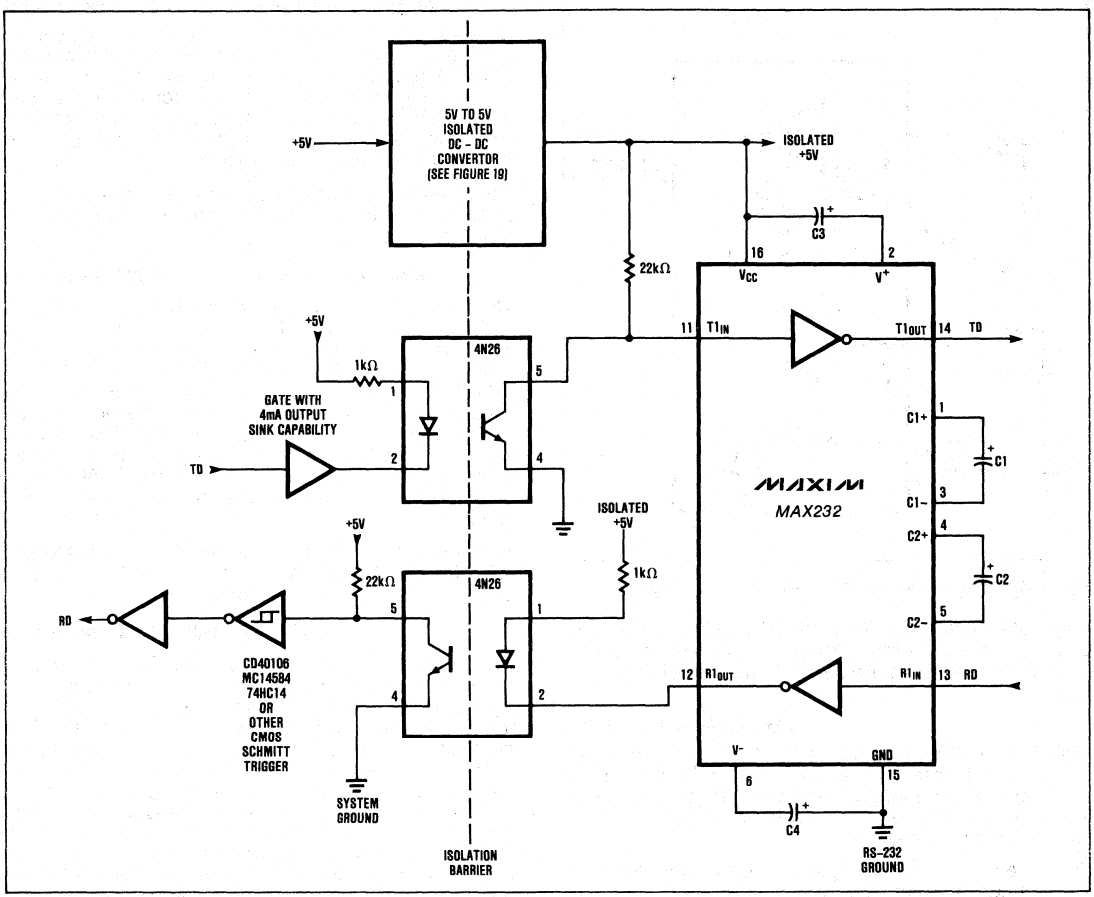


Figure 18. Optically isolated RS-232 Interface.

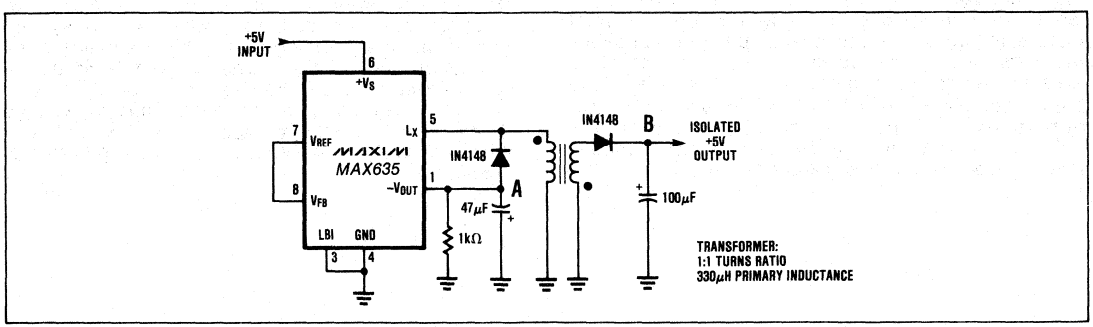


Figure 19. +5V Isolated Power Supply For Optically Isolated RS-232 Interface.

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX230		**0.3" Wide**
MAX230CPP	0°C to +70°C	20 Lead Plastic DIP
MAX230CWP	0°C to +70°C	20 Lead Wide S.O.
MAX230C/D	0°C to +70°C	Dice
MAX230EPP	-40°C to +85°C	20 Lead Plastic DIP
MAX230EWP	-40°C to +85°C	20 Lead Wide S.O.
MAX230EJP	-40°C to +85°C	20 Lead CERDIP
MAX230MJP	-55°C to +125°C	20 Lead CERDIP
MAX231		**0.3" Wide**
MAX231CPD	0°C to +70°C	14 Lead Plastic DIP
MAX231CWE	0°C to +70°C	16 Lead Wide S.O.
MAX231C/D	0°C to +70°C	Dice
MAX231EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX231EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX231EJD	-40°C to +85°C	14 Lead CERDIP
MAX231MJD	-55°C to +125°C	14 Lead CERDIP
MAX232		**0.3" Wide**
MAX232CPE	0°C to +70°C	16 Lead Plastic DIP
MAX232CWE	0°C to +70°C	16 Lead Wide S.O.
MAX232C/D	0°C to +70°C	Dice
MAX232EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX232EJE	-40°C to +85°C	16 Lead CERDIP
MAX232EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX232MJE	-55°C to +125°C	16 Lead CERDIP
MAX233		**0.3" Wide**
MAX233CPP	0°C to +70°C	20 Lead Plastic DIP
MAX233EPP	-40°C to +85°C	20 Lead Plastic DIP
MAX234		**0.3" Wide**
MAX234CPE	0°C to +70°C	16 Lead Plastic DIP
MAX234CWE	0°C to +70°C	16 Lead Wide S.O.
MAX234C/D	0°C to +70°C	Dice
MAX234EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX234EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX234EJE	-40°C to +85°C	16 Lead CERDIP
MAX234MJE	-55°C to +125°C	16 Lead CERDIP
MAX235		**0.6" Wide**
MAX235CPG	0°C to +70°C	24 Lead Plastic DIP*
MAX235EPG	-40°C to +85°C	24 Lead Plastic DIP*
MAX235EDG	-40°C to +85°C	24 Lead Ceramic*
MAX235MDG	-55°C to +125°C	24 Lead Ceramic*

** = 0.600" package*

PART	TEMP. RANGE	PACKAGE
MAX236		**0.3" Wide**
MAX236CNG	0°C to +70°C	24 Lead Plastic DIP
MAX236CWG	0°C to +70°C	24 Lead Wide S.O.
MAX236C/D	0°C to +70°C	Dice
MAX236ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX236EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX236ERG	-40°C to +85°C	24 Lead CERDIP
MAX236MRG	-55°C to +125°C	24 Lead CERDIP
MAX237		**0.3" Wide**
MAX237CNG	0°C to +70°C	24 Lead Plastic DIP
MAX237CWG	0°C to +70°C	24 Lead Wide S.O.
MAX237C/D	0°C to +70°C	Dice
MAX237ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX237EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX237ERG	-40°C to +85°C	24 Lead CERDIP
MAX237MRG	-55°C to +125°C	24 Lead CERDIP
MAX238		**0.3" Wide**
MAX238CNG	0°C to +70°C	24 Lead Plastic DIP
MAX238CWG	0°C to +70°C	24 Lead Wide S.O.
MAX238C/D	0°C to +70°C	Dice
MAX238ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX238EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX238ERG	-40°C to +85°C	24 Lead CERDIP
MAX238MRG	-55°C to +125°C	24 Lead CERDIP
MAX239		**0.3" Wide**
MAX239CNG	0°C to +70°C	24 Lead Plastic DIP
MAX239CWG	0°C to +70°C	24 Lead Wide S.O.
MAX239C/D	0°C to +70°C	Dice
MAX239ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX239EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX239ERG	-40°C to +85°C	24 Lead CERDIP
MAX239MRG	-55°C to +125°C	24 Lead CERDIP
MAX240		**Flatpak**
MAX240CMH	0°C to +70°C	44 Lead Flatpak
MAX240EMH	-40°C to +85°C	44 Lead Flatpak
MAX241		**0.3" Wide**
MAX241CWI	0°C to +70°C	28 Lead Wide S.O.
MAX241EWI	-40°C to +85°C	28 Lead Wide S.O.

+5V Powered RS-232 Drivers/Receivers

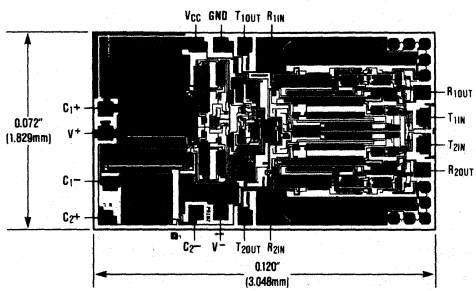
Table 1. Circuits Commonly Used for RS-232C and V.24 Asynchronous Interfaces

PIN	CIRCUIT	
1	Protective Ground	Connect to Earth Ground
2	Transmit Data (TD)	Data from DTE
3	Receive Data (RD)	Data from DCE
4	Request To Send (RTS)	Handshake from DTE
5	Clear to Send (CTS)	Handshake from DCE
6	Data Set ready (DSR)	Handshake from DCE
7	Signal Ground	Reference Point for Signals
8	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
11	Printer Busy Signal	Handshake from Printer
20	Data Terminal Ready	Handshake from DTE
22	Ring Indicator	Handshake from DCE

Table 2. Summary of RS-232C and V.28 Electrical Specifications

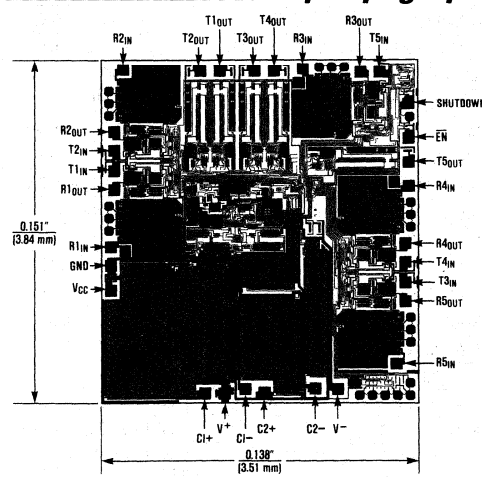
PARAMETER	SPECIFICATION	COMMENTS
Driver Output Voltage		
0 level	+5V to +15V	With 3-7kΩ load
1 level	-5V to -15V	With 3-7kΩ load
Max. output	±25V Max.	No Load
Receiver Input Thresholds (data and clock signals)		
0 level	+3V to +25V	
1 level	-3V to -25V	
Receiver Thresholds RTS, DSR, DTR		
On level	+3V to +25V	
Off level	Open Circuit or -3V to -25V	Detects Power Off Condition at Driver
Receiver Input Resistance	3kΩ to 7kΩ	
Driver Output Resistance, power off condition	300Ω Min.	$V_{OUT} < \pm 2V$
Driver Slew Rate	30V/μs Max.	$3k\Omega < R_L < 7k\Omega$; $0pF < C_L < 2500pF$
Signalling Rate	Up to 20kbits/sec.	
Cable Length	50'/15 m. Recommended Max. Length	Longer cables permissible, if $C_{LOAD} \leq 2500pF$

Chip Topography



MAX231, MAX232 and MAX233

Note: Connect substrate to V^+.



MAX230 and MAX234-239, MAX240, MAX241

Notes:
1. Shutdown pin of MAX234, MAX237, MAX238, MAX239, MAX240 and MAX241 are internally connected to ground.
2. Connect substrate to V^+.

Switched Capacitor Filters

Switched Capacitor Filters

Part Number	Description	Analog Frequency Range	Features	Page No.
MAX260	Universal Filter	0.01Hz to 7.5kHz	Microprocessor Interface	10-1
MAX261	Universal Filter	0.40Hz to 57.0kHz	Microprocessor Interface	10-1
MAX262	Universal Filter	1.0Hz to 140.0kHz	Microprocessor Interface	10-1
MAX263	Universal Filter	0.4Hz to 57.0kHz	Pin Strap Interface	10-25
MAX264	Universal Filter	1.0Hz to 140.0kHz	Pin Strap Interface	10-25
MAX265	Universal Filter	0.4Hz to 57.0kHz	Resistor and Pin Strap Interface	10-47
MAX266	Universal Filter	1.0Hz to 140.0kHz	Resistor and Pin Strap Interface	10-47
MAX267	Bandpass Filter	0.4Hz to 57.0kHz	Pin Strap Interface	10-25
MAX268	Bandpass Filter	1.0Hz to 140.0kHz	Pin Strap Interface	10-25
MF10	Universal 2nd Order Filter	0.1Hz to 30.0kHz	Resistor Programmed	10-49

MAXIM

Microprocessor Programmable Universal Active Filters

General Description

The MAX260/261/262 CMOS dual second-order universal switched-capacitor active filters allow microprocessor control of precise filter functions. No external components are required for a variety of bandpass, lowpass, highpass, notch and allpass configurations. Each device contains two second-order filter sections which place center frequency, Q, and filter operating mode under programmed control.

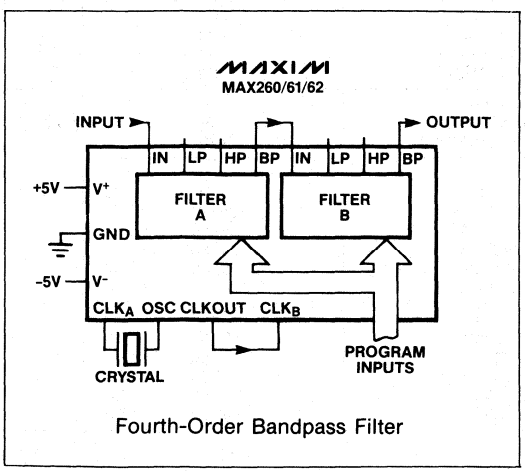
An input clock, along with a 6-bit f_0 program input, determine the filter's center or corner frequency without affecting other filter parameters. The filter Q is also programmed independently. Separate clock inputs for each filter section operate with either a crystal, RC network, or external clock generator.

The MAX260 has superior offset and DC specifications than the MAX261 and MAX262 and a center frequency (f_0) range of 7.5kHz. The MAX261 handles center frequencies to 57kHz while the MAX262 extends the center frequency range to 140kHz by employing lower clock-to-f_0 ratios. All devices are available in 24-pin DIP and small outline packages in commercial, extended, and military temperature ranges.

Applications

- μP Tuned Filters
- Anti-Aliasing Filters
- Digital Signal Processing
- Adaptive Filters
- Signal Analysis
- Phase-Locked Loops

Functional Diagram



Fourth-Order Bandpass Filter

Features

- ◆ **Filter Design Software Available**
- ◆ **Microprocessor Interface**
- ◆ **64-Step Center Frequency Control**
- ◆ **128-Step Q Control**
- ◆ **Independent Q and f_0 Programming**
- ◆ **Guaranteed Clock to f_0 Ratio—1% (A grade)**
- ◆ **75kHz f_0 Range (MAX262)**
- ◆ **Single +5V and ±5V Operation**

Ordering Information

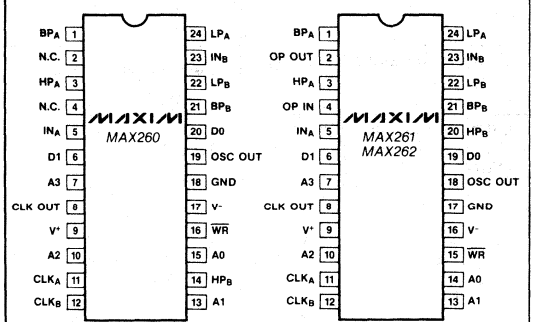
PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX260ACNG	0°C to +70°C	Plastic DIP	1%
MAX260BCNG	0°C to +70°C	Plastic DIP	2%
MAX260AENG	-40°C to +85°C	Plastic DIP	1%
MAX260BENG	-40°C to +85°C	Plastic DIP	2%
MAX260ACWG	0°C to +70°C	Wide SO	1%
MAX260BCWG	0°C to +70°C	Wide SO	2%
MAX260AMRG	-55°C to +125°C	CERDIP	1%
MAX260BMRG	-55°C to +125°C	CERDIP	2%
MAX261ACNG	0°C to +70°C	Plastic DIP	1%

** All devices—24-pin packages 0.3" wide packages*

Ordering Information Continued on Last Page

Pin Configuration

Top View



Microprocessor Programmable Universal Active Filters

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage, any pin ..... V^--0.3V to V^++0.3V
Input Current, any pin ..... ±50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above 70°C) ... 660mW
  CERDIP (derate 12.5mW/°C above 70°C) 1000mW
  Wide SO (derate 11.8mW/°C above 70°C) 944mW

Operating Temperature
  MAX260/261/262XCXG ..... 0°C to +70°C
  MAX260/261/262XEXG ..... -40°C to +85°C
  MAX260/261/262XMXG ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V 350kHz for the MAX260 and 1.5MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				See Table 1		
Maximum Clock Frequency				See Table 1		
f_{CLK}/f_0 Ratio Error (Note 1)	$T_A = T_{MIN}$ to T_{MAX}	MAX260A		±0.2	±1.0	%
		MAX260B		±0.2	±2.0	
		MAX261/62A		±0.2	±1.0	
		MAX261/62B		±0.2	±2.0	
f_0 Temperature Coefficient				-5		ppm/°C
Q Accuracy (deviation from ideal continuous filter) (Note 2)	$T_A = T_{MIN}$ to T_{MAX}					%
	Q = 0.5 to 16	MAX260A		±1	±5	
	Q = 0.5 to 16	MAX260B		±1	±10	
	Q = 32	MAX260A		±2	±10	
	Q = 32	MAX260B		±2	±15	
	Q = 64	MAX260A		±4	±15	
	Q = 64	MAX260B		±4	±22	
	Q = 0.5 to 16	MAX261/62A		±1	±5	
	Q = 0.5 to 16	MAX261/62B		±1	±10	
	Q = 32	MAX261/62A		±2	±10	
	Q = 32	MAX261/62B		±2	±15	
	Q = 64	MAX261/62A		±4	±15	
	Q = 64	MAX261/62B		±4	±22	
Q Temperature Coefficient				±20		ppm/°C
DC Lowpass Gain Accuracy		MAX260A		±0.1	±0.2	dB
		MAX260B		±0.1	±0.3	
		MAX261/62A		±0.1	±0.25	
		MAX261/62B		±0.1	±0.5	
Gain Temperature Coefficient	Lowpass (at D.C.)	MAX260		-5		ppm/°C
		MAX261/62		-5		
	Bandpass (at f_0)	MAX260/61/62		+20		
Offset Voltage At Filter Outputs—LP, BP, HP (Note 3)	$T_A = T_{MIN}$ to T_{MAX}, Q = 4 Mode 1					V
		MAX260A		±0.05	±0.25	
		MAX260B		±0.15	±0.45	
		MAX261A		±0.40	±0.90	
		MAX261B		±0.80	±1.60	
		MAX262A		±0.40	±0.90	
		MAX262B		±0.80	±1.60	
	Mode 3	MAX260A		±0.075	±0.30	
		MAX260B		±0.075	±0.50	
		MAX261A		±0.50	±1.00	
		MAX261B		±0.90	±1.60	
		MAX262A		±0.50	±1.00	
		MAX262B		±0.90	±1.60	
Offset Voltage Temperature Coefficient	f_{CLK}/f_0 = 100.53, Q = 4 $T_A = T_{MIN}$ to T_{MAX}			±0.75		mV/°C

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V 350kHz for the MAX260 and 1.5MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Feedthrough				±4		mV
Crosstalk				-70		dB
Wideband Noise (Note 4)	Q = 1, 2nd-Order, LP/BP 4th-Order LP (Fig. 26) 4th-Order BP (Fig. 24)			See Typ. Oper. Char. 90 100		μV_{RMS}
Harmonic Distortion at f_0	Q = 4, V_{IN} = 1.5V_{PP}			-57		dB
Supply Voltage Range	T_A = T_{MIN} to T_{MAX}		±2.37	±5	±6.3	V
Power Supply Current (Note 5)	T_A = T_{MIN} to T_{MAX} CMOS Level Logic Inputs	MAX260 MAX261 MAX262		15 16 16	20 20 20	mA
Shutdown Supply Current	$Q0_A$-$Q6_A$ = all 0, CMOS Level Logic Inputs (Note 5)			1.5		mA
INTERNAL AMPLIFIERS						
Output Signal Swing (Note 6)	T_A = T_{MIN} to T_{MAX}, 10kΩ load			±4.75		V
Output Short Circuit Current	Source Sink			50 2		mA
Power Supply Rejection Ratio	0Hz to 10kHz			-70		dB
Gain Bandwidth Product				2.5		MHz
Slew Rate				6		V/μs

ELECTRICAL CHARACTERISTICS (for V± = ±2.5V ±5%)

V^+ = +2.37V, V^- = -2.37V, CLK_A = CLK_B = ±2.5V 250kHz for the MAX260 and 1MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				(Note 7)		
Maximum Clock Frequency				(Note 7)		
f_{CLK}/f_0 Ratio Error (Notes 1, 8)	Q = 8	MAX26XA MAX26XB		±0.1 ±0.1	1 2	%
Q Accuracy (deviation from ideal continuous filter) (Notes 2, 8)	Q = 8 f_{CLK}/f_0 = 199.49 f_{CLK}/f_0 = 199.49 f_{CLK}/f_0 = 139.80	 MAX260A MAX260B MAX261A MAX261B MAX262A MAX262B		 ±2 ±2 ±2 ±2 ±2 ±2	 ±5 ±10 ±5 ±10 ±5 ±10	%
Output Signal Swing	All Outputs (Note 6)			±2		V
Power Supply Current	CMOS Level Logic Inputs (Note 5)			7		mA
Shutdown Current	CMOS Level Logic Inputs (Note 5)			0.35		mA

Note 1: f_{CLK}/f_0 accuracy is tested at 100.53, 103.67, 106.81, 113.1, 125.66, 150.8, and 199.49 on the MAX260/61, and at 40.84, 43.98, 47.12, 53.41, 65.97, 91.11, and 139.8 on the MAX262.

Note 2: Q accuracy tested at Q = 0.5, 1, 2, 4, 8, 16, 32, and 64. Q of 32 and 64 tested at 1/2 stated clock frequency.

Note 3: The Offset Voltage is specified for the entire filter. Offset is virtually independent of Q and f_{CLK}/f_0 ratio setting. The test clock frequency for Mode 3 is 175kHz for the MAX260 and 750kHz for the MAX261/262.

Note 4: Output noise is measured with an RC output smoothing filter at 4 × f_0 to remove clock feedthrough.

Note 5: TTL logic levels are: HIGH = 2.4V, LOW = 0.8V. CMOS logic levels are: HIGH = 5V, LOW = 0V. Power supply current is typically 4mA higher with TTL logic and clock input levels.

Note 6: On the MAX260 only, the HP output signal swing is typically 0.75V less than the LP or BP outputs.

Note 7: At ±2.5V supplies, the f_0 range and maximum clock frequency are typically 75% of values listed in Table 1.

Note 8: f_{CLK}/f_0 and Q accuracy are a function of the accuracy of internal capacitor ratios. No increase in error is expected at ±2.5V as compared to ±5V however these parameters are only tested to the extent indicated by the MIN or MAX limits.

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INTERFACE SPECIFICATIONS (Note 9)

(V^+ = +5V, V^+ = -5V, T_A = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{WR}$ Pulse Width	t_{WR}		250	150		ns
Address Setup	t_{AS}		25			ns
Address Hold	t_{AH}		0			ns
Data Setup	t_{DS}		100	50		ns
Data Hold	t_{DH}		10	0		ns
Logic Input High	V_{IH}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B $T_A = T_{MIN}$ to T_{MAX}	2.4			V
Logic Input Low	V_{IL}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B $T_A = T_{MIN}$ to T_{MAX}			0.8	V
Input Leakage Current	I_{IN}	$\overline{WR}$, D0-D1, A0-A3, CLK_B CLK_A $T_A = T_{MIN}$ to T_{MAX}		6	10 60	µA
Input Capacitance	C_{IN}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B			15	pF

Note 9: Interface timing specifications are guaranteed by design and are not subject to test.

Pin Description

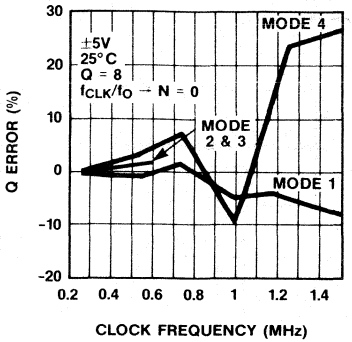
MAX260 PIN #	MAX261/2 PIN #	NAME	FUNCTION
9	9	V^+	Positive supply voltage
17	16	V^-	Negative supply voltage
18	17	GND	Analog Ground. Connect to the system ground for dual supply operation or mid-supply for single supply operation. GND should be well bypassed in single supply applications.
11	11	CLK_A	Input to the oscillator and clock input to section A. This clock is internally divided by 2.
12	12	CLK_B	Clock input to filter B. This clock is internally divided by 2.
8	8	CLK OUT	Clock Output for crystal and R-C oscillator operation
19	18	OSC OUT	Connects to crystal or R-C for self clocked operation

MAX260 PIN #	MAX261/2 PIN #	NAME	FUNCTION
5,23	5,23	IN_A,IN_B	Filter inputs
1,21	1,21	BP_A,BP_B	Bandpass outputs
24,22	24,22	LP_A,LP_B	Lowpass outputs
3,14	3,20	HP_A,HP_B	Highpass/Notch/Allpass outputs
16	15	$\overline{WR}$	Write Enable input
15,13, 10,7	14,13, 10,7	A0,A1 A2,A3	Address inputs for f_0 and Q input data locations
20,6	19,6	D0,D1	Data inputs for f_0 and Q programming
	2	OP OUT	Output of uncommitted op-amp on MAX261/62 only. Pin 2 is a no-connect on the MAX260
	4	OP IN	Inverting input of uncommitted op-amp on MAX261/62 only (Non-inverting input is internally connected to ground). Pin 4 is a no-connect on the MAX260.

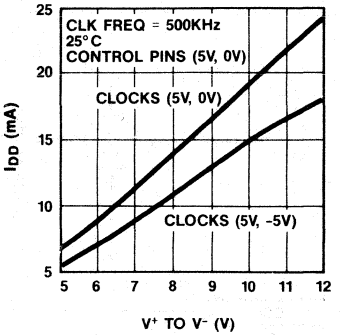
Microprocessor Programmable Universal Active Filters

Typical Operating Characteristics

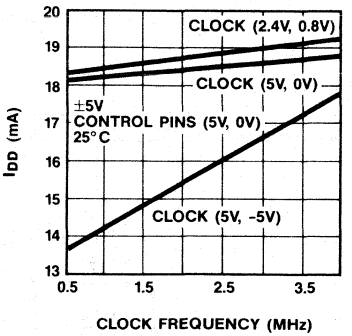
Q ERROR vs CLOCK FREQUENCY MAX260



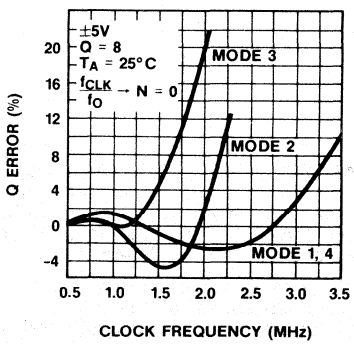
I_{DD} vs POWER SUPPLY VOLTAGE



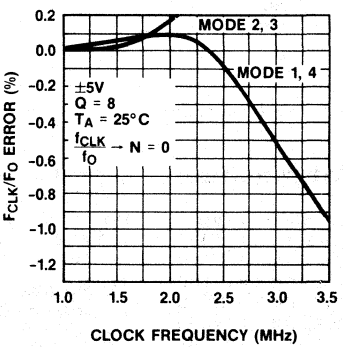
I_{DD} vs CLOCK FREQUENCY



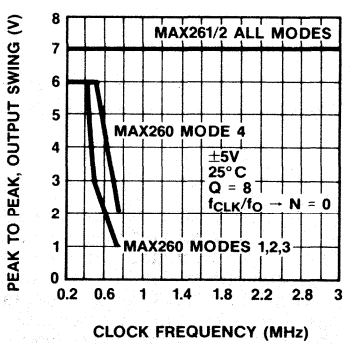
Q ERROR vs CLOCK FREQUENCY MAX261/2



F_{CLK}/F_O ERROR vs CLOCK FREQUENCY MAX261/2



OUTPUT SIGNAL SWING vs CLOCK FREQUENCY



Wideband RMS Noise (db ref. to 2.47V_{RMS}, 7V_{p-p}) **±5V Supplies**

	Mode	Q = 1			Q = 8			Q = 64		
		LP	BP	HP/AP/N	LP	BP	HP/AP/N	LP	BP	HP/AP/N
MAX261/2	1	-84	-90	-84	-80	-82	-85	-72	-73	-85
	2	-88	-90	-88	-84	-82	-84	-77	-73	-76
	3	-84	-90	-88	-80	-82	-82	-73	-73	-74
	4	-83	-89	-84	-79	-81	-85	-71	-73	-85
MAX260	1	-87	-89	-86	-81	-81	-86	-73	-73	-86
	2	-89	-88	-85	-83	-80	-82	-75	-72	-74
	3	-87	-88	-85	-80	-82	-80	-71	-72	-72
	4	-87	-88	-86	-81	-80	-86	-71	-72	-86

Notes:
1. f_{CLK} = 1 MHz for MAX261/2, f_{CLK} = 350kHz for MAX260
2. f_{CLK}/f_0 ratio programmed at N = 63 (see Table 2)
3. Clock feedthrough is removed with an RC lowpass at $4f_0$, i.e. R = 3.9kΩ, C = 2000pF for MAX261.

Noise Spectral Distribution
(MAX261, f_{CLK} = 1 MHz, dB ref. to 2.47V_{RMS}, 7V_{p-p})

Measurement Bandwidth	Q=1	Q=8	Q=64
Wideband	-84	-80	-72
3 KHz	-87	-87	-86
C Message Weighted	-93	-93	-93

10

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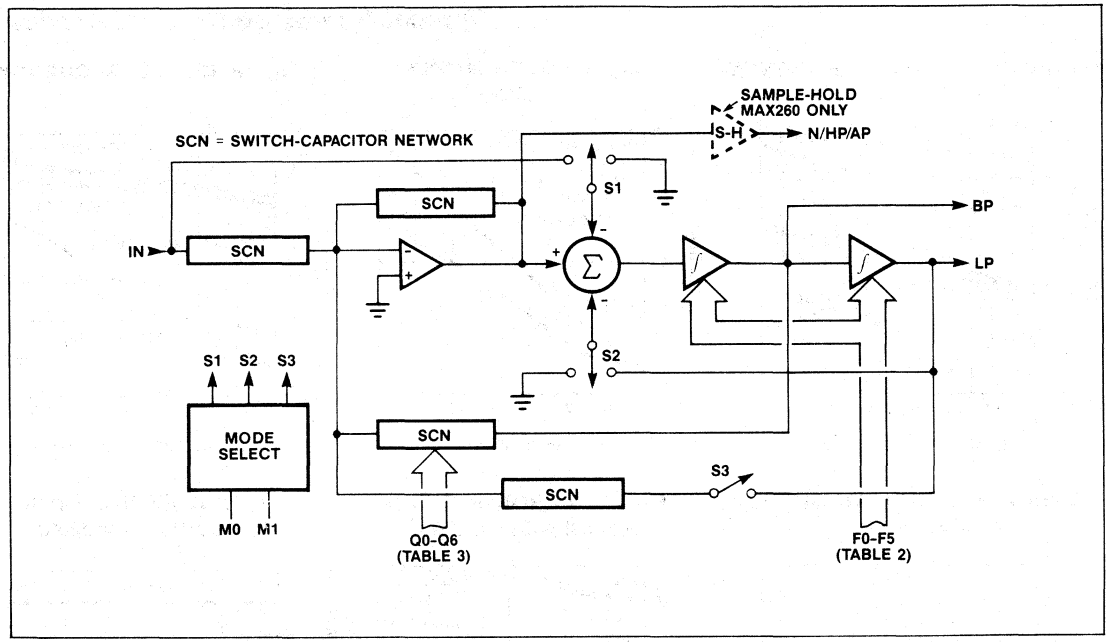

Figure 1. Filter Block Diagram (One Second-Order Section)

Introduction

Each MAX260/61/62 contains two second-order switched-capacitor active filters. Figure 1 shows the filter's state variable topology, employed with two cascaded integrators and one summing amplifier. The MAX261 and MAX262 also contain an uncommitted amplifier. On-chip switches and capacitors provide feedback to control each filter section's f_0 and Q. Internal capacitor ratios are primarily responsible for the accuracy of these parameters. Although these switched-capacitor networks (SCN) are in fact sampled systems, their behavior very closely matches that of continuous filters, such as RC active filters. The ratio of the clock frequency to the filter center frequency (f_{CLK}/f_0) is kept large so that ideal second-order state-variable response is maintained.

The MAX262 uses a lower range of sampling (f_{CLK}/f_0) ratios than the MAX260 or MAX261 to allow higher operating f_0 frequencies and signal bandwidths. These reduced sample rates result in somewhat more deviation from ideal continuous filter parameters than with the MAX260/61. However, these differences can be compensated using Figure 20 (See "Applications Hints") or Maxim's filter design software.

The MAX260 employs auto-zero circuitry not included in the MAX261 or 262. This provides improved DC characteristics, and improved low frequency performance at the expense of high end f_0 and signal bandwidth. The N/HP/AP outputs of the MAX260 are internally sample-and-held, as a result of its auto-zero operation. Signal swing at this output is somewhat reduced as a result (MAX260 only). See Table 1 for bandwidth comparisons of the three filters.

Maxim also provides design programs which aid in converting filter response specifications into the f_0 and Q program codes used by the MAX260 series devices. This software also precompensates f_0 and Q when low sample rates are used.

It is important to note that in all MAX260 series filters, the filter's internal sample rate is one half the input clock rate (CLK_A or CLK_B) due to an internal division by two. All clock related data, tables, and other discussions in this data sheet refer to the frequency at the CLK_A or CLK_B input, i.e. twice the internal sample rate, unless specifically stated otherwise.

Quick Look Design Procedure

The MAX260, MAX261 and MAX262, with Maxim's filter design software, greatly simplifies the design procedures for many active filters. Most designs can be realized using a three step process described in this section. If the design software is not used, or if the filter complexity is beyond the scope of this section, refer to the remainder of this data sheet for more detailed applications and design information.

```
100  AB$="FILTER A " : GOSUB 150 : REM GET DATA FOR SECTION A
110  ADD = 0 : GOSUB 220 : REM WRITE DATA TO THE PRINTER PORT
120  AB$="FILTER B " : GOSUB 150 : REM GET DATA FOR B
130  ADD = 32 : GOSUB 220 : REM WRITE DATA TO PRINTER PORT
140  GOTO 100
150  PRINT "MODE (1 to 4, see Table 5) "; AB$; : INPUT M
160  IF M<1 OR M>4 THEN GOTO 150
170  PRINT "CLOCK RATIO (0 to 63, N of Table 2) "; AB$; : INPUT F
180  IF F<0 OR F>63 THEN GOTO 170
190  PRINT "Q (0 to 127, N of Table 3) "; AB$; : INPUT Q
200  IF Q<0 OR Q>127 THEN GOTO 190 ELSE : PRINT
210  RETURN
220  LPRINT CHR$(ADD+M-1); : ADD = ADD+4
230  FOR I = 1 TO 3
240  X=(ADD + (F - 4*INT(F/4))) : LPRINT CHR$(X);
250  F=INT(F/4) : ADD = ADD + 4
260  NEXT I
270  FOR I = 1 TO 4
280  X=(ADD + (Q - 4*INT(Q/4))) : LPRINT CHR$(X);
290  Q=INT(Q/4) :: ADD = ADD + 4
300  NEXT I
310  RETURN
```

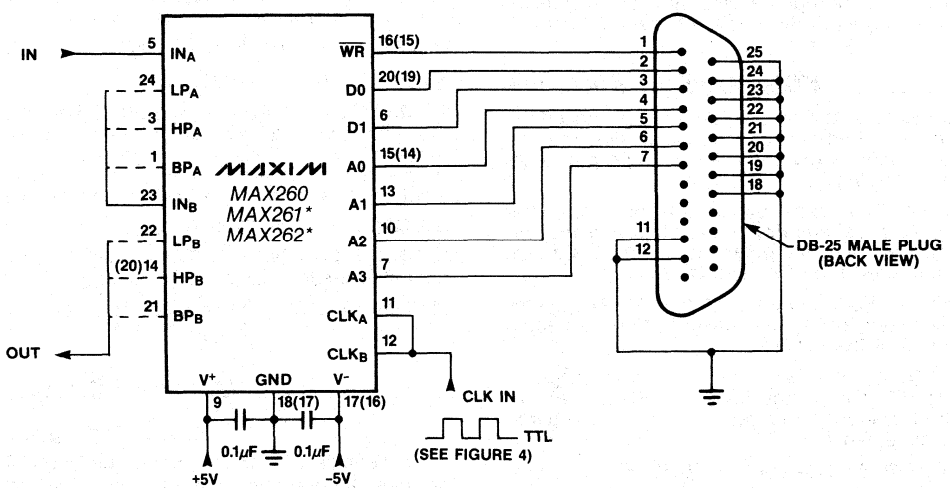

Figure 2. Basic Program and Hardware Connections to Parallel Printer Port for "Quick Look" Using a Personal Computer.

Step 1—Filter Design

Start with the program "PZ" to determine what type of filter is needed. This helps determine the type (Butterworth, Chebyshev, etc.) and the number of poles for the optimum choice. The program also plots the frequency response and calculates the pole/zero (f_0) and Q values for each second-order section. Each MAX260/61/62 contains two second-order sections and devices may be cascaded for higher order filters.

Step 2—Generate Programming Coefficients

Starting with the f_0 and Q values obtained in Step 1, use the program "MPP" to generate the digital coefficients which program each second-order section's f_0 and Q. The program displays values for "N" ("N = __ for f_0" and "N = __ for Q"). N is the decimal equivalent of the binary code that sets the filter section's f_0 or Q. These are the same "N"s that are listed in Tables 2 and 3.

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An input clock frequency and filter "Mode" must also be selected in this step, however if a specific clock rate is not selected, "GEN" will pick one. With regard to mode selection, Mode 1 is the most convenient choice for most bandpass and lowpass filters. Exceptions are elliptic bandpass and lowpass filters which require Mode 3. Highpass filters also use Mode 3, while allpass filters use Mode 4. For further information regarding these filter modes see "Filter Operating Modes" in this data sheet.

Step 3—Loading the Filter

When the N values for the f_0 and Q of each second-order filter section are determined, the filter can then be programmed and operated. What follows is a convenient method of programming the filter and evaluating a design if a personal computer is available.

A short Basic program loads data into the MAX260/261/262 via the personal computer's parallel printer port. The program asks for the filter Mode as well as the N values for the f_0 and Q of each section. These coefficients are then loaded into the filter in the form of ASCII characters. This program may be used with or without Maxim's other filter design software. The program and the appropriate hardware connections for a Centronics type printer port are shown in Figure 2.

Filter Design Software

Maxim provides software programs to help speed the transition from frequency response design requirements to working hardware. A series of programs are available, including:

Program PZ. Given the requirements, such as center frequency, Q, passband ripple, and stopband attenuation, PZ will calculate the pole frequencies, Q's, zeros, and the number of stages needed.

Program MPP. For programmed filters, MPP computes the input codes to use and describes the expected performance of the design.

Program FR. When a design of one or more stages is completed, FR checks the final cascaded assembly. The output frequency response can be compared with that expected from PZ.

Program PR.BAS Allows a MAX260/61/62 to be programmed via a personal computer. The Mode, f_0, and Q of each section are typed in, and the proper codes are sent to the filter via the computer's parallel printer port. This program is also provided in Figure 2.

Other design programs are also included for use with other Maxim filter products.

Other Filter Products

Maxim has developed a number of other filter products in addition to the MAX260, MAX261 and MAX262:

PIN PROGRAMMABLE ACTIVE FILTERS—A dual second-order universal filter that needs no external components. A Microprocessor interface is not required.

MAX263	0.4Hz to 30kHz f_0 range
MAX264	1Hz to 75kHz f_0 range

RESISTOR AND PIN PROGRAMMABLE FILTERS—A dual second-order universal filter where f_0 adjustment beyond pin-programmable resolution employs external resistors.

MAX265	0.4Hz to 30kHz f_0 range. Includes two uncommitted op-amps.
MAX266	1Hz to 75kHz f_0 range. Includes two uncommitted op-amps.
MF10	Industry Standard. Resistor Programmed Only

PIN PROGRAMMABLE BANDPASS FILTERS—A dual second-order bandpass that needs no external components. A Microprocessor interface is not required.

MAX267	0.4Hz to 30kHz f_0 range
MAX268	1Hz to 75kHz f_0 range

PROGRAMMABLE ANTI-ALIAS FILTER—A programmable dual second-order continuous (not switched) lowpass filter. No clock noise is generated. Designed for use as an anti-alias filter in front of, or as a smoothing filter following, any sampled filter or system.

MAX270	1kHz to 25kHz Cutoff Frequency Range

5th ORDER LOW PASS FILTER—Features zero offset and drift errors for designs requiring high DC accuracy.

MAX280, LT1062	0.1Hz to 20kHz Cutoff Frequency Range

Detailed Description

f_0 and Q Programming

Figure 3 shows a block diagram of the MAX260. Each 2nd-order filter section has its own clock input and independent f_0 and Q control. The actual center frequency is a function of the filter's clock rate, 6-bit f_0 control word (see Table 2), and operating Mode. The Q of each section is also set by a separate programmed input (see Table 3). This way each half of a MAX260/61/62 is tuned independently so that complex filter polynomials can be realized. Equations which convert program code numbers to f_{CLK}/f_0 and Q values are listed in the notes beneath Tables 2 and 3.

Table 1. Typical Clock and Center Frequency Limits

PART	Q	MODE	f_{CLK}	f_0
MAX260	1	1	1Hz-400kHz	0.01Hz-4.0kHz
	1	2	1Hz-425kHz	0.01Hz-6.0kHz
	1	3	1Hz-500kHz	0.01Hz-5.0kHz
	1	4	1Hz-400kHz	0.01Hz-4.0kHz
	8	1	1Hz-500kHz	0.01Hz-5.0kHz
	8	2	1Hz-700kHz	0.01Hz-10.0kHz
	8	3	1Hz-700kHz	0.01Hz-5.0kHz
	8	4	1Hz-600kHz	0.01Hz-4.0kHz
	64	1	1Hz-750kHz	0.01Hz-7.5kHz
	90	2	1Hz-500kHz	0.01Hz-7.0kHz
	64	3	1Hz-400kHz	0.01Hz-4.0kHz
	64	4	1Hz-750kHz	0.01Hz-7.5kHz
MAX261	1	1	40Hz-4.0MHz	0.4Hz-40kHz
	1	2	40Hz-4.0MHz	0.5Hz-57kHz
	1	3	40Hz-4.0MHz	0.4Hz-40kHz
	1	4	40Hz-4.0MHz	0.4Hz-40kHz
	8	1	40Hz-2.7MHz	0.4Hz-27kHz
	8	2	40Hz-2.1MHz	0.5Hz-30kHz

PART	Q	MODE	f_{CLK}	f_0
MAX261	8	3	40Hz-1.7MHz	0.4Hz-17kHz
	8	4	40Hz-2.7MHz	0.4Hz-27kHz
	64	1	40Hz-2.0MHz	0.4Hz-20kHz
	90	2	40Hz-1.2MHz	0.4Hz-18kHz
	64	3	40Hz-1.2MHz	0.4Hz-12kHz
	64	4	40Hz-2.0MHz	0.4Hz-20kHz
MAX262	1	1	40Hz-4.0MHz	1.0Hz-100kHz
	1	2	40Hz-4.0MHz	1.4Hz-140kHz
	1	3	40Hz-4.0MHz	1.0Hz-100kHz
	1	4	40Hz-4.0MHz	1.0Hz-100kHz
	8	1	40Hz-2.5MHz	1.0Hz-60kHz
	8	2	40Hz-1.4MHz	1.4Hz-50kHz
	8	3	40Hz-1.4MHz	1.0Hz-35kHz
	8	4	40Hz-2.5MHz	1.0Hz-60kHz
	64	1	40Hz-1.5MHz	1.0Hz-37kHz
	90	2	40Hz-0.9MHz	1.4Hz-32kHz
	64	3	40Hz-0.9MHz	1.0Hz-22kHz
	64	4	40Hz-1.5MHz	1.0Hz-37kHz

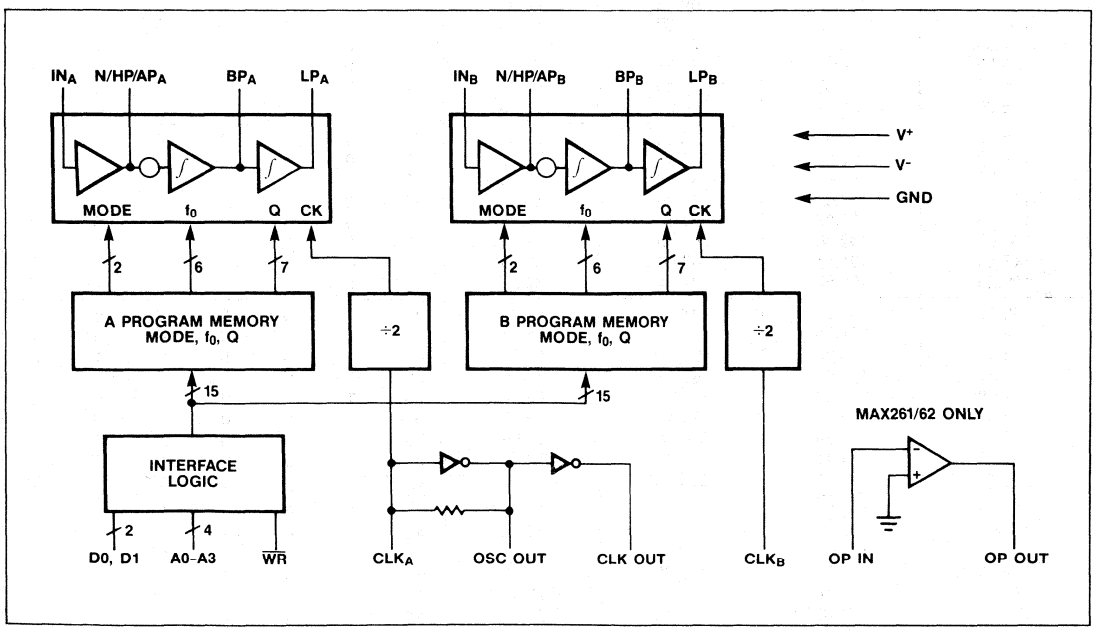

Figure 3. MAX260/61/62 Block Diagram

Microprocessor Programmable Universal Active Filters

Table 2. f_{CLK}/f_0 Program Selection Table

f_{CLK}/f_0 RATIO				PROGRAM CODE						
MAX260/61		MAX262								
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F5	F4	F3	F2	F1	F0
100.53	71.09	40.84	28.88	0	0	0	0	0	0	0
102.10	72.20	42.41	29.99	1	0	0	0	0	0	1
103.67	73.31	43.98	31.10	2	0	0	0	0	1	0
105.24	74.42	45.55	32.21	3	0	0	0	0	1	1
106.81	75.53	47.12	33.32	4	0	0	0	1	0	0
108.38	76.64	48.69	34.43	5	0	0	0	1	0	1
109.96	77.75	50.27	35.54	6	0	0	0	1	1	0
111.53	78.86	51.84	36.65	7	0	0	0	1	1	1
113.10	79.97	53.41	37.76	8	0	0	1	0	0	0
114.67	81.08	54.98	38.87	9	0	0	1	0	0	1
116.24	82.19	56.55	39.99	10	0	0	1	0	1	0
117.81	83.30	58.12	41.10	11	0	0	1	0	1	1
119.38	84.42	59.69	42.21	12	0	0	1	1	0	0
120.95	85.53	61.26	43.32	13	0	0	1	1	0	1
122.52	86.64	62.83	44.43	14	0	0	1	1	1	0
124.09	87.75	64.40	45.54	15	0	0	1	1	1	1
125.66	88.86	65.97	46.65	16	0	1	0	0	0	0
127.23	89.97	67.54	47.76	17	0	1	0	0	0	1
128.81	91.80	69.12	48.87	18	0	1	0	0	1	0
130.38	92.19	70.69	49.98	19	0	1	0	0	1	1
131.95	93.30	72.26	51.10	20	0	1	0	1	0	0
133.52	94.41	73.83	52.20	21	0	1	0	1	0	1
135.08	95.52	75.40	53.31	22	0	1	0	1	1	0
136.66	96.63	76.97	54.43	23	0	1	0	1	1	1
138.23	97.74	78.53	55.54	24	0	1	1	0	0	0
139.80	98.86	80.11	56.65	25	0	1	1	0	0	1
141.37	99.97	81.68	57.76	26	0	1	1	0	1	0
142.94	101.08	83.25	58.87	27	0	1	1	0	1	1
144.51	102.89	84.82	59.98	28	0	1	1	1	0	0
146.08	103.30	86.39	61.09	29	0	1	1	1	0	1
147.65	104.41	87.96	62.20	30	0	1	1	1	1	0
149.23	105.52	89.54	63.31	31	0	1	1	1	1	1
150.80	106.63	91.11	64.42	32	1	0	0	0	0	0
152.37	107.74	92.68	65.53	33	1	0	0	0	0	1
153.98	108.85	94.25	66.64	34	1	0	0	0	1	0
155.51	109.96	95.82	67.75	35	1	0	0	0	1	1
157.08	111.07	97.39	68.86	36	1	0	0	1	0	0
158.65	112.18	98.96	69.98	37	1	0	0	1	0	1
160.22	113.29	100.53	71.09	38	1	0	0	1	1	0
161.79	114.41	102.10	72.20	39	1	0	0	1	1	1
163.36	115.52	102.67	73.31	40	1	0	1	0	0	0
164.93	116.63	105.24	74.42	41	1	0	1	0	0	1
166.50	117.74	106.81	75.53	42	1	0	1	0	1	0
168.08	118.85	108.38	76.64	43	1	0	1	0	1	1
169.65	119.96	109.96	77.75	44	1	0	1	1	0	0
171.22	121.07	111.53	78.86	45	1	0	1	1	0	1
172.79	122.18	113.10	79.97	46	1	0	1	1	1	0
174.36	123.29	114.66	81.08	47	1	0	1	1	1	1

Table 2. f_{CLK}/f_0 Program Selection Table (Continued)

f_{CLK}/f_0 RATIO				PROGRAM CODE						
MAX260/61		MAX262								
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F5	F4	F3	F2	F1	F0
175.93	124.40	116.24	82.19	48	1	1	0	0	0	0
177.50	125.51	117.81	83.30	49	1	1	0	0	0	1
179.07	126.62	119.38	84.41	50	1	1	0	0	1	0
180.64	127.73	120.95	85.53	51	1	1	0	0	1	1
182.21	128.84	122.52	86.64	52	1	1	0	1	0	0
183.78	129.96	124.09	87.75	53	1	1	0	1	0	1
185.35	131.07	125.66	88.86	54	1	1	0	1	1	0
186.92	132.18	127.23	89.97	55	1	1	0	1	1	1
188.49	133.29	128.81	91.08	56	1	1	1	0	0	0
190.07	134.40	130.38	92.19	57	1	1	1	0	0	1
191.64	135.51	131.95	93.30	58	1	1	1	0	1	0
193.21	136.62	133.52	94.41	59	1	1	1	0	1	1
194.78	137.73	135.09	95.52	60	1	1	1	1	0	0
196.35	138.84	136.66	96.63	61	1	1	1	1	0	1
197.92	139.95	138.23	97.74	62	1	1	1	1	1	0
199.49	141.06	139.80	98.85	63	1	1	1	1	1	1

Notes: 1) For the MAX260/61, $f_{CLK}/f_0 = (64 + N)\pi/2$ in Mode 1, 3, and 4, where N varies from 0 to 63.
2) For the MAX262, $f_{CLK}/f_0 = (26 + N)\pi/2$ in Mode 1, 3, and 4, where N varies 0 to 63.
3) In Mode 2, all f_{CLK}/f_0 ratios are divided by $\sqrt{2}$. The functions are then:
MAX260/61 $f_{CLK}/f_0 = 1.11072\ (64 + N)$, MAX262 $f_{CLK}/f_0 = 1.11072\ (26 + N)$

Table 3. Q Program Selection Table

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.500*	0.707*	0*	0	0	0	0	0	0	0
0.504	0.713	1	0	0	0	0	0	0	1
0.508	0.718	2	0	0	0	0	0	1	0
0.512	0.724	3	0	0	0	0	0	1	1
0.516	0.730	4	0	0	0	0	1	0	0
0.520	0.736	5	0	0	0	0	1	0	1
0.525	0.742	6	0	0	0	0	1	1	0
0.529	0.748	7	0	0	0	0	1	1	1
0.533	0.754	8	0	0	0	1	0	0	0
0.538	0.761	9	0	0	0	1	0	0	1
0.542	0.767	10	0	0	0	1	0	1	0
0.547	0.774	11	0	0	0	1	0	1	1
0.552	0.780	12	0	0	0	1	1	0	0
0.556	0.787	13	0	0	0	1	1	0	1
0.561	0.794	14	0	0	0	1	1	1	0
0.566	0.801	15	0	0	0	1	1	1	1
0.571	0.808	16	0	0	1	0	0	0	0
0.577	0.815	17	0	0	1	0	0	0	1
0.582	0.823	18	0	0	1	0	0	1	0
0.587	0.830	19	0	0	1	0	0	1	1
0.593	0.838	20	0	0	1	0	1	0	0
0.598	0.846	21	0	0	1	0	1	0	1
0.604	0.854	22	0	0	1	0	1	1	0
0.609	0.862	23	0	0	1	0	1	1	1

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.615	0.870	24	0	0	1	1	0	0	0
0.621	0.879	25	0	0	1	1	0	0	1
0.627	0.887	26	0	0	1	1	0	1	0
0.634	0.896	27	0	0	1	1	0	1	1
0.640	0.905	28	0	0	1	1	1	0	0
0.646	0.914	29	0	0	1	1	1	0	1
0.653	0.924	30	0	0	1	1	1	1	0
0.660	0.933	31	0	0	1	1	1	1	1
0.667	0.943	32	0	1	0	0	0	0	0
0.674	0.953	33	0	1	0	0	0	0	1
0.681	0.963	34	0	1	0	0	0	1	0
0.688	0.973	35	0	1	0	0	0	1	1
0.696	0.984	36	0	1	0	0	1	0	0
0.703	0.995	37	0	1	0	0	1	0	1
0.711	1.01	38	0	1	0	0	1	1	0
0.719	1.02	39	0	1	0	0	1	1	1
0.727	1.03	40	0	1	0	1	0	0	0
0.736	1.04	41	0	1	0	1	0	0	1
0.744	1.05	42	0	1	0	1	0	1	0
0.753	1.06	43	0	1	0	1	0	1	1
0.762	1.08	44	0	1	0	1	1	0	0
0.771	1.09	45	0	1	0	1	1	0	1
0.780	1.10	46	0	1	0	1	1	1	0
0.790	1.12	47	0	1	0	1	1	1	1

Notes: 4) * Writing all 0s into Q0A-Q6A on Filter A activates a low power shutdown mode. BOTH filter sections are deactivated. Therefore this Q value is only achievable in filter B.

Microprocessor Programmable Universal Active Filters

Table 3. Q Program Selection Table (Continued)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.800	1.13	48	0	1	1	0	0	0	0
0.810	1.15	49	0	1	1	0	0	0	1
0.821	1.16	50	0	1	1	0	0	1	0
0.831	1.18	51	0	1	1	0	0	1	1
0.842	1.19	52	0	1	1	0	1	0	0
0.853	1.21	53	0	1	1	0	1	0	1
0.865	1.22	54	0	1	1	0	1	1	0
0.877	1.24	55	0	1	1	0	1	1	1
0.889	1.26	56	0	1	1	1	0	0	0
0.901	1.27	57	0	1	1	1	0	0	1
0.914	1.29	58	0	1	1	1	0	1	0
0.928	1.31	59	0	1	1	1	0	1	1
0.941	1.33	60	0	1	1	1	1	0	0
0.955	1.35	61	0	1	1	1	1	0	1
0.969	1.37	62	0	1	1	1	1	1	0
0.985	1.39	63	0	1	1	1	1	1	1
1.00	1.41	64	1	0	0	0	0	0	0
1.02	1.44	65	1	0	0	0	0	0	1
1.03	1.46	66	1	0	0	0	0	1	0
1.05	1.48	67	1	0	0	0	0	1	1
1.07	1.51	68	1	0	0	0	1	0	0
1.08	1.53	69	1	0	0	0	1	0	1
1.10	1.56	70	1	0	0	0	1	1	0
1.12	1.59	71	1	0	0	0	1	1	1
1.14	1.62	72	1	0	0	1	0	0	0
1.16	1.65	73	1	0	0	1	0	0	1
1.19	1.68	74	1	0	0	1	0	1	0
1.21	1.71	75	1	0	0	1	0	1	1
1.23	1.74	76	1	0	0	1	1	0	0
1.25	1.77	77	1	0	0	1	1	0	1
1.28	1.81	78	1	0	0	1	1	1	0
1.31	1.85	79	1	0	0	1	1	1	1
1.33	1.89	80	1	0	1	0	0	0	0
1.36	1.93	81	1	0	1	0	0	0	1
1.39	1.97	82	1	0	1	0	0	1	0
1.42	2.01	83	1	0	1	0	0	1	1
1.45	2.06	84	1	0	1	0	1	0	0
1.49	2.10	85	1	0	1	0	1	0	1
1.52	2.16	86	1	0	1	0	1	1	0
1.56	2.21	87	1	0	1	0	1	1	1

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
1.60	2.26	88	1	0	1	1	0	0	0
1.64	2.32	89	1	0	1	1	0	0	1
1.68	2.40	90	1	0	1	1	0	1	0
1.73	2.45	91	1	0	1	1	0	1	1
1.78	2.51	92	1	0	1	1	1	0	0
1.83	2.59	93	1	0	1	1	1	0	1
1.88	2.66	94	1	0	1	1	1	1	0
1.94	2.74	95	1	0	1	1	1	1	1
2.00	2.83	96	1	1	0	0	0	0	0
2.06	2.92	97	1	1	0	0	0	0	1
2.13	3.02	98	1	1	0	0	0	1	0
2.21	3.12	99	1	1	0	0	0	1	1
2.29	3.23	100	1	1	0	0	1	0	0
2.37	3.35	101	1	1	0	0	1	0	1
2.46	3.48	102	1	1	0	0	1	1	0
2.56	3.62	103	1	1	0	0	1	1	1
2.67	3.77	104	1	1	0	1	0	0	0
2.78	3.96	105	1	1	0	1	0	0	1
2.91	4.11	106	1	1	0	1	0	1	0
3.05	4.31	107	1	1	0	1	0	1	1
3.20	4.53	108	1	1	0	1	1	0	0
3.37	4.76	109	1	1	0	1	1	0	1
3.56	5.03	110	1	1	0	1	1	1	0
3.76	5.32	111	1	1	0	1	1	1	1
4.00	5.66	112	1	1	1	0	0	0	0
4.27	6.03	113	1	1	1	0	0	0	1
4.57	6.46	114	1	1	1	0	0	1	0
4.92	6.96	115	1	1	1	0	0	1	1
5.33	7.54	116	1	1	1	0	1	0	0
5.82	8.23	117	1	1	1	0	1	0	1
6.40	9.05	118	1	1	1	0	1	1	0
7.11	10.1	119	1	1	1	0	1	1	1
8.00	11.3	120	1	1	1	1	0	0	0
9.14	12.9	121	1	1	1	1	0	0	1
10.7	15.1	122	1	1	1	1	0	1	0
12.8	18.1	123	1	1	1	1	0	1	1
16.0	22.6	124	1	1	1	1	1	0	0
21.3	30.2	125	1	1	1	1	1	0	1
32.0	45.3	126	1	1	1	1	1	1	0
64.0	90.5	127	1	1	1	1	1	1	1

Notes: 5) In Modes 1, 3, and 4: Q = 64/(128-N)

6) In Mode 2, the listed Q values are those of Mode 1 multiplied by $\sqrt{2}$. Then Q = 90.51/(128-N)

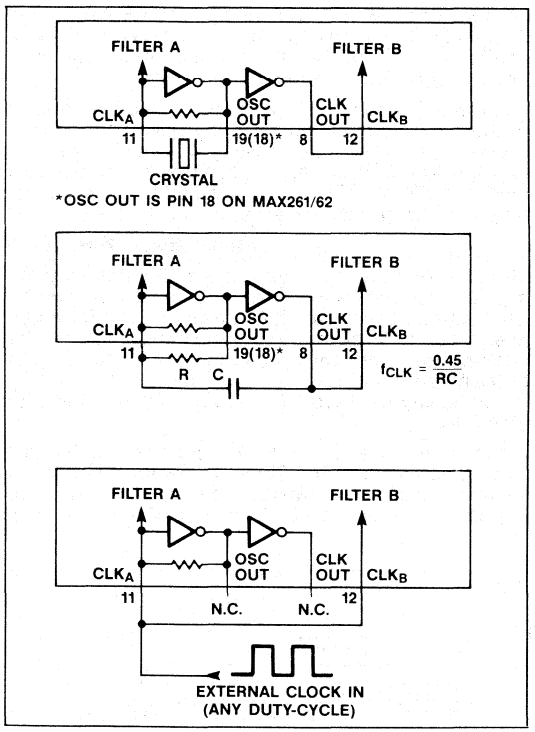

Figure 4. Clock Input Connections

Oscillator and Clock Inputs

The clock circuitry of the MAX260/61/62 can operate with a crystal, resistor-capacitor (RC) network, or an external clock generator as shown in Figure 4. If an RC oscillator is used, the clock rate, f_{CLK}, nominally equals 0.45/RC.

The duty cycle of the clock at CLK_A and CLK_B is unimportant because the input is internally divided by two to generate the sampling clock for each filter section. It is important to note that this internal division also halves the sample rate when considering aliasing and other sampled system phenomenon.

Microprocessor Interface

f_0, Q, and Mode selection data is stored in an internal program memory. The memory contents are updated by writing to addresses selected by A0-A3. D0 and D1 are the data inputs. A map of the memory locations is shown in Table 4. Data is stored in the selected address on the rising edge of $\overline{WR}$. Address and data inputs are TTL and CMOS compatible when the filter is powered from ±5 volts. With other power supply voltages, CMOS logic levels should be used. Interface timing is shown in Figure 5. Note: Clock inputs CLK_A and CLK_B have no relation to the digital interface. They control the switched-capacitor filter sample rate only.

Some noise may be generated on the filter outputs by transitions at the logic inputs. If this is objectionable, the digital lines should be buffered from the device by logic gates as shown in Figure 6.

Table 4. Program Address Locations

DATA BIT		ADDRESS				LOCATION
D0	D1	A3	A2	A1	A0	
FILTER A						
$M0_A$	$M1_A$	0	0	0	0	0
$F0_A$	$F1_A$	0	0	0	1	1
$F2_A$	$F3_A$	0	0	1	0	2
$F4_A$	$F5_A$	0	0	1	1	3
$Q0_A$	$Q1_A$	0	1	0	0	4
$Q2_A$	$Q3_A$	0	1	0	1	5
$Q4_A$	$Q5_A$	0	1	1	0	6
$Q6_A$		0	1	1	1	7
FILTER B						
$M0_B$	$M1_B$	1	0	0	0	8
$F0_B$	$F1_B$	1	0	0	1	9
$F2_B$	$F3_B$	1	0	1	0	10
$F4_B$	$F5_B$	1	0	1	1	11
$Q0_B$	$Q1_B$	1	1	0	0	12
$Q2_B$	$Q3_B$	1	1	0	1	13
$Q4_B$	$Q5_B$	1	1	1	0	14
$Q6_B$		1	1	1	1	15

Note: Writing 0 into $Q0_A$-$Q6_A$ (address locations 4-7) on Filter A activates shutdown mode. BOTH filter sections deactivate.

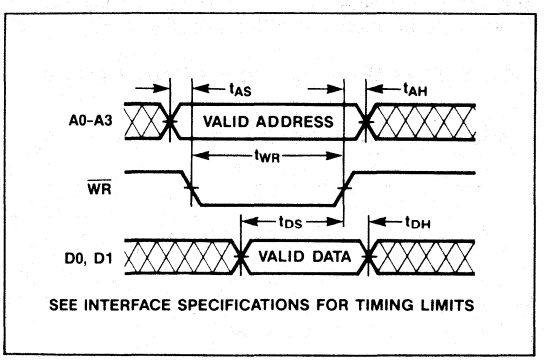

Figure 5. Interface Timing

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Microprocessor Programmable Universal Active Filters

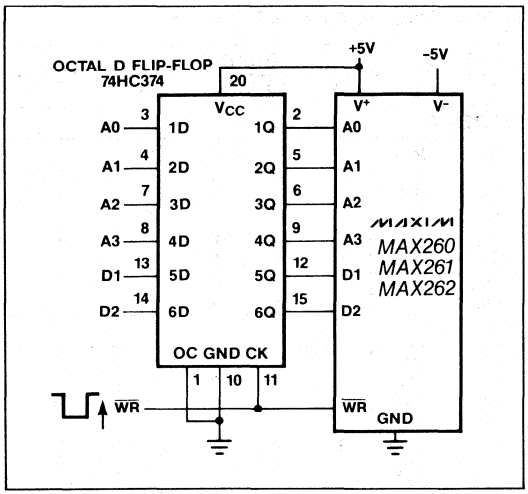

Figure 6. Buffering/Latching Logic Inputs

Shutdown Mode

The MAX260/61/62 enters a shutdown/standby mode when all zeroes are written to the Q addresses of filter A ($Q0_A$-$Q6_A$). When shut down, power consumption with ±5V supplies typically drops to 10mW. When reactivating the filter after shutdown, allow 2ms to return to full operation.

Filter Operating Modes

There are several ways in which the summing amplifier and integrators in each MAX260/61/62 filter section can be configured. The four most versatile interconnections (modes) are selected by writing to inputs M0 and M1 (See Tables 4 and 5). These modes use no external components. A fifth mode, 3A, makes use of an additional op-amp (included in the MAX261 and 262) and external resistors but uses the same internal configuration, and is selected with the same programming code, as Mode 3.

Figures 7 through 11 show symbolic representations of the MAX260 filter modes. Only one second-order section is shown in each case. The A and B sections of one MAX260/61/62 can be programmed for different modes if desired. The f_0, f_N (notch), Q, and various output gains in each case are shown in Table 5.

Filter Mode Selection

MODE 1 (Figure 7) is useful when implementing all-pole lowpass and bandpass filters such as Butterworth, Chebyshev, Bessel, etc.. It can also be used for notch filters, but only second-order notches because the relative pole and zero locations are fixed. Higher order notch filters require more latitude in f_0 and f_N, which is why they are more easily implemented with Mode 3A.

Mode 1, along with Mode 4, supports the highest clock frequencies (See Table 1) because the input summing amplifier is outside the filter's resonant loop (Figure 7). The gain of the lowpass and notch outputs

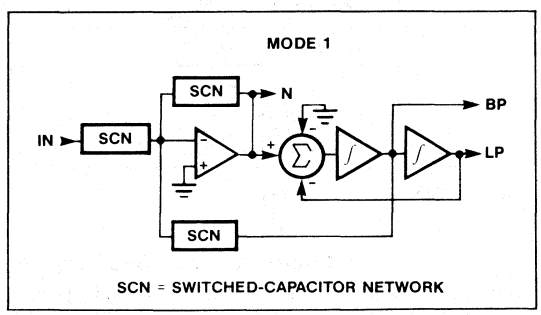

Figure 7. Filter Mode 1: Second-Order Bandpass, Lowpass and Notch

Table 5. Filter Modes for Second-Order Functions

MODE	M1, M0	FILTER FUNCTIONS	f_0	Q	f_N	H_{OLP}	H_{OBP}	H_{ON1} ($f \rightarrow 0$)	H_{ON2} ($f \rightarrow f_{CLK}/4$)	OTHER
1	0, 0	LP, BP, N	SEE TABLE 2	SEE TABLE 3	f_0	-1	-Q	-1	-1	
2	0, 1	LP, BP, N			$f_0\sqrt{2}$	-0.5	$-Q/\sqrt{2}$	-0.5	-1	
3	1, 0	LP, BP, HP				-1	-Q			$H_{OHP} = -1$
3A	1, 0	LP, BP, HP, N			$f_0\sqrt{\frac{R_H}{R_L}}$	-1	-Q	$+\frac{R_G}{R_L}$	$+\frac{R_G}{R_H}$	$H_{OHP} = -1$
4	1, 1	LP, BP, AP				-2	-2Q			$H_{OAP} = -1$ $f_Z = f_0$, $Q_Z = Q$

Notes: f_0 = Center Frequency
f_N = Notch Frequency
H_{OLP} = Lowpass Gain at DC
H_{OBP} = Bandpass Gain at f_0
H_{OHP} = Highpass Gain as f approaches $f_{CLK}/4$
H_{ON1} = Notch Gain as f approaches DC
H_{ON2} = Notch Gain as f approaches $f_{CLK}/4$
H_{OAP} = Allpass Gain
f_Z, Q_Z = f and Q of Complex Pole Pair

is 1, while the bandpass gain at the center frequency is Q. For bandpass gains other than Q, the filter input or output can be scaled by a resistive divider or op-amp.

MODE 2 (Figure 8) is used for all-pole lowpass and bandpass filters. Key advantages compared to Mode 1 are higher available Qs (See Table 3) and lower output noise. Mode 2's available f_{CLK}/f_0 ratios are $\sqrt{2}$ less than with Mode 1 (See Table 2) so a wider overall range of f_0s can be selected from a single clock when both modes are used together. This is demonstrated in the Wide Passband Chebyshev Bandpass design example.

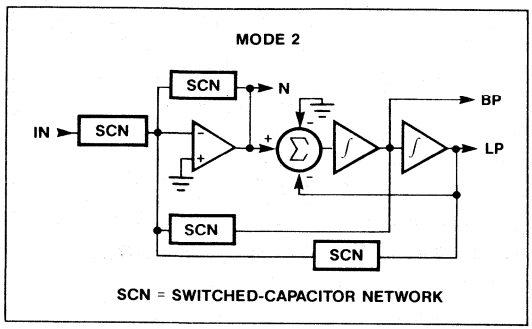

Figure 8. Filter Mode 2: Second-Order Bandpass, Lowpass and Notch

MODE 3 (Figure 9) is the only mode which produces high-pass filters. The maximum clock frequency is somewhat less than with MODE 1 (See Table 1).

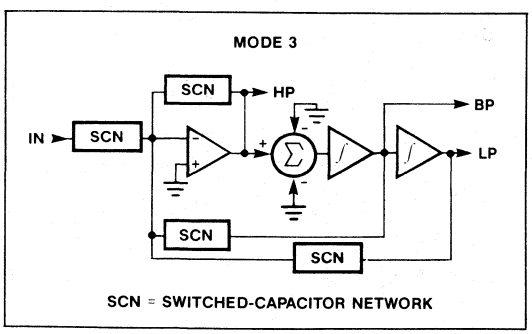

Figure 9. Filter Mode 3: Second-Order Bandpass, Lowpass and Highpass

MODE 3A (Figure 10) uses a separate op-amp to sum the highpass and lowpass outputs of Mode 3, creating a separate notch output. This output allows the notch to be set independently of f_0 by adjusting the op-amp's feedback resistor ratio (R_H, R_L). R_H, R_L, and R_G are external resistors. Because the notch can be independently set, Mode 3A is also useful when designing pole-zero filters such as elliptics.

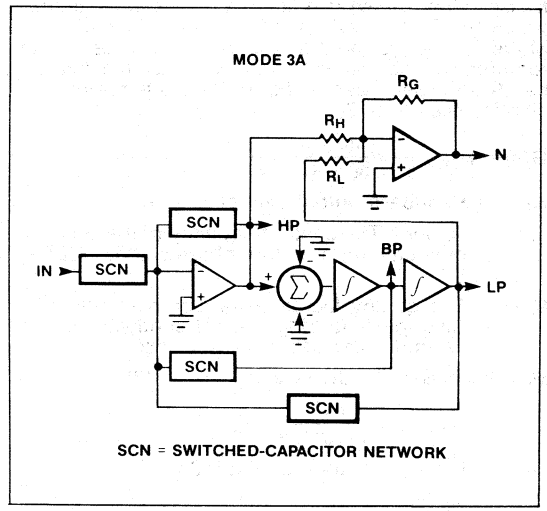

Figure 10. Filter Mode 3A: Second-Order Bandpass, Lowpass, Highpass and Notch. For elliptic LP, BP, HP and Notch, the N output is used

MODE 4 (Figure 11) is the only mode that provides an allpass output. This is useful when implementing group delay equalization. In addition to this, Mode 4 can also be used in all pole lowpass and bandpass filters. Along with Mode 1, it is the fastest operating mode for the filter, although the gains are different than in Mode 1. When the allpass function is used, note that some amplitude peaking occurs (approximately 0.3dB when Q = 8) at f_0. Also note that f_0 and Q sampling errors are highest in Mode 4 (See Figure 20).

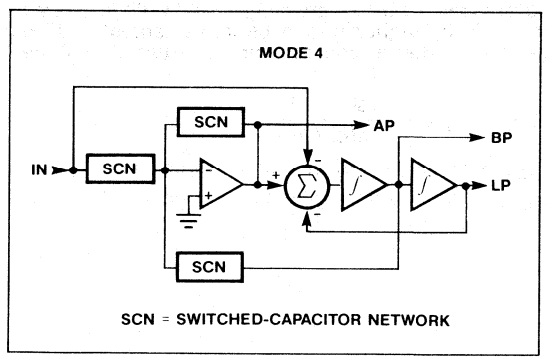

Figure 11. Filter Mode 4: Second-Order Bandpass, Lowpass and Allpass

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Description of Filter Functions

BANDPASS (Figure 12)

For all pole bandpass and lowpass filters (Butterworth, Bessel, Chebyshev) use Mode 1 if possible. If appropriate f_{CLK}/f_0 or Q values are not available in Mode 1, Mode 2 may provide a selection that is closer to the required values. Mode 1 however has the highest bandwidth (See Table 1). For pole-zero filters such as elliptics see Mode 3A.

$$G(s) = H_{OBP} \frac{s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Bandpass output gain at $\omega = \omega_o$

f_0 = $\omega_o/2\pi$ = The center frequency of the complex pole pair. Input-output phase shift is -180° at f_0.

Q = The quality factor of the complex pole pair. Also the ratio of f_0 to -3dB bandwidth of the second-order bandpass response.

LOWPASS See Bandpass text. (Figure 13)

$$G(s) = H_{OLP} \frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = Lowpass output gain at DC

f_0 = $\omega_0/2\pi$

HIGHPASS (Figure 14)

Mode 3 is the only mode with a highpass output. It will work for all pole filter types such as Butterworth, Bessel and Chebyshev. Use mode 3A for filters employing both poles and zeros such as elliptics.

$$G(s) = H_{OHP} \frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = Highpass output gain as f approaches $f_{CLK}/4$

f_0 = $\omega_0/2\pi$

NOTCH (Figure 15)

Mode 3A is recommended for multi-pole notch filters. In 2nd order filters, Mode 1 can also be used. The advantages of Mode 1 are higher bandwidth compared to mode 3 (Higher f_N can be implemented) and no need for external components as required in Mode 3A.

$$G(s) = H_{ON2} \frac{s^2 + \omega_n^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = Notch output gain as f approaches $f_{CLK}/4$

H_{ON1} = Notch output gain as f approaches DC

f_n = $\omega_n/2\pi$

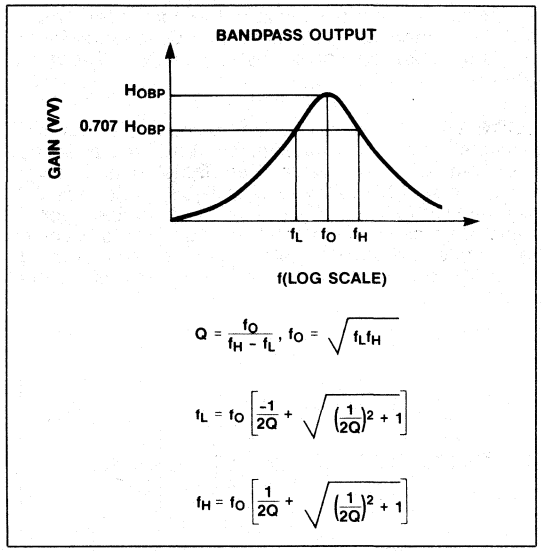

Figure 12. Second-Order Bandpass Characteristics

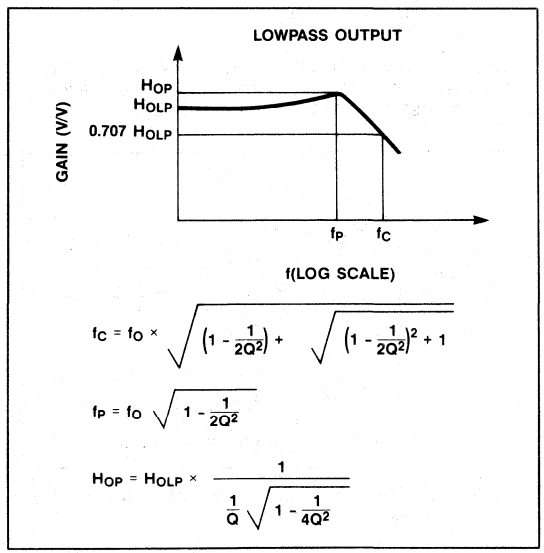

Figure 13. Second-Order Lowpass Characteristics

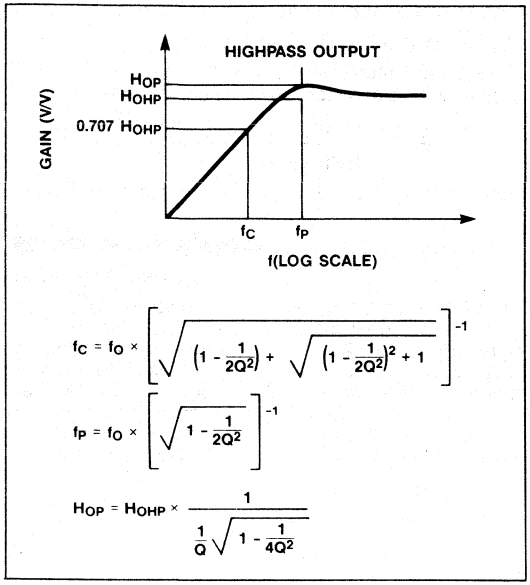

Figure 14. Second-Order Highpass Characteristics

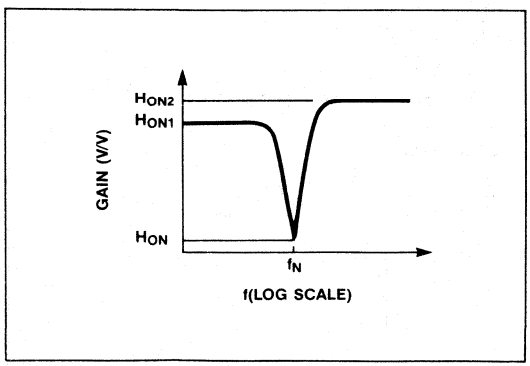

Figure 15. Second-Order Notch Characteristics

ALL PASS

Mode 4 is the only configuration in which an allpass function can be realized.

$$G(s) = H_{OAP} \frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = All pass output gain for DC < f < $f_{CLK}/4$

$f_0 = \omega_0/2\pi$

Filter Design Procedure

The procedure for most filter designs is to first convert the required frequency response specifications to f_0s and Qs for the appropriate number of second-order sections that implement the filter. This can be done by using design equations or tables in available literature, or can be conveniently calculated using Maxim's filter design software. Once the f_0 and Qs have been found, the next step is to turn them into the digital program coefficients required by the MAX260/61/62. An operating Mode and clock frequency (or clock/center frequency ratio) must also be selected.

Next, if the sample rate ($f_{CLK}/2$) is low enough to cause significant errors, the selected f_0s and Qs should be corrected to account for sampling effects by using Figure 20 or Maxim's design software. In most cases, the sampling errors are small enough to require no correction, i.e. less than 1%. In any case, with or without correction, the required f_0s and Qs can then be selected from Tables 2 and 3. Maxim's filter design software can also perform this last step. The desired f_0s and Qs are stated, and the appropriate digital coefficients are supplied.

Cascading Filters

In some designs, such as very narrow band filters, several second-order sections with identical center frequency may be cascaded. The total Q of the resultant filter is:

$$\text{Total } Q_T = \frac{Q}{\sqrt{(2^{1/N} - 1)}}$$

Q is the Q of each individual filter section, and N is the number of sections. In Table 6, the total Q and bandwidth are listed for up to five identical second-order sections. B is the bandwidth of each section.

Table 6. Cascading Identical Bandpass Filter Sections

Total Sections	Total B.W.	Total Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Note: B = individual stage bandwidth, Q = individual stage Q.

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In high order bandpass filters, stages with different f_0s and Qs are also often cascaded. When this happens the overall filter gain at the bandpass center frequency is not simply the product of the individual gains because f_0, the frequency where each section's gain is specified, is different for each second-order section. The gain of each section at the cascaded filter's center frequency must be determined to obtain the total gain.

For all-pole filters the gain, $H(f_0)$, at each second-order section's f_0 is divided by an adjustment factor, G, to obtain that section's gain, $H(f_{0BP})$, at the overall center frequency:

$$H_1(f_{0BP}) = H(f_{01})/G_1 = \text{Section 1's Gain at } f_{0BP}$$

$$G_1 = \frac{Q_1[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1}$$

where $F_1 = f_{01}/f_{OBP}$

G_1, Q_1, and f_{01} are the gain adjustment factor, Q, and f_0 for the first of the cascaded second-order sections. The gain of the other sections (2, 3 etc.) at f_{0BP} is determined the same way. The overall gain is:

$$H(f_{0BP}) = H_1(f_{0BP}) \times H_2(f_{0BP}) \times \text{etc.}$$

For cascaded filters with zeros (f_Z) such as elliptics, the gain adjustment factor for each stage is:

$$G_1 = \frac{Q_1[F_{Z1}^2 - F_1^2]\,[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1^2(F_{Z1}^2 - 1)}$$

where $F_{1Z} = f_{Z1}/f_{0BP}$, and F_1 is the same as above.

Application Hints

Power Supplies

The MAX260/61/62 can be operated with a variety of power supply configurations including +5V to +12V single supply, or ±2.5V to ±5V dual supplies. When a single supply is used, V^- is connected to system ground and the filter's GND pin should be biased at $V^+/2$. The input signal is then either capacitively coupled to the filter input or biased to $V^+/2$. Figure 16 shows circuit connections for single supply operation.

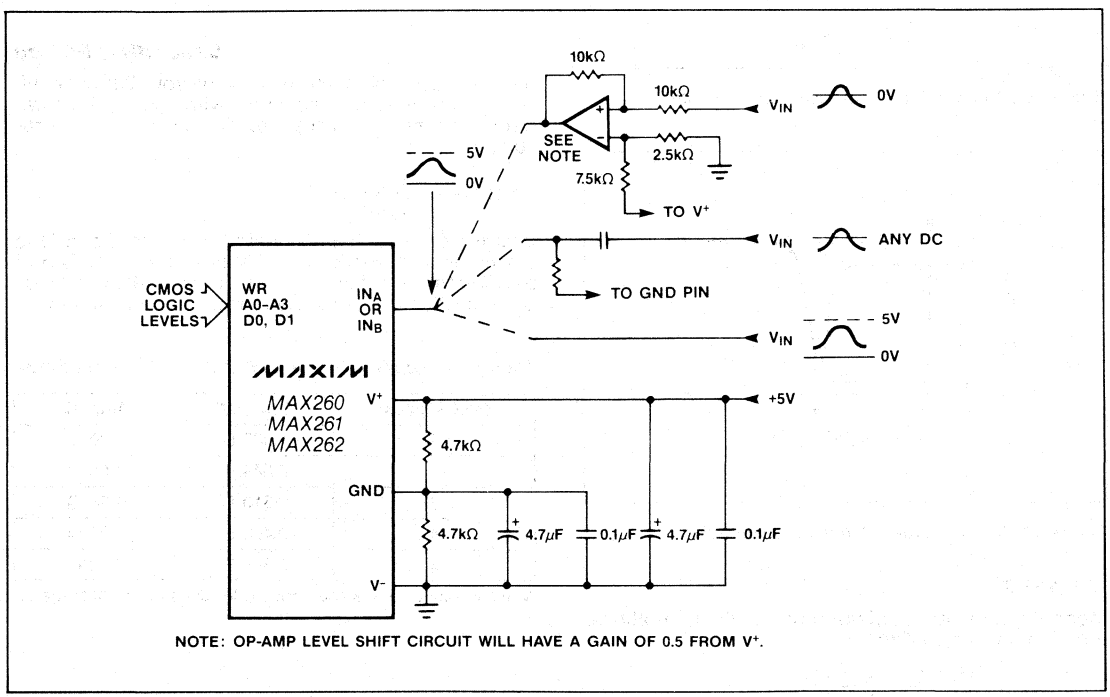

Figure 16. Power Supply and Input Connections for Single Supply Operation

When power supplies other than ±5V are used, CMOS input logic levels (HIGH = V^+, LOW = GND or V^-) are required for $\overline{WR}$, D0-D1, A0-A3, CLK_A and CLK_B. With ±5V supplies, either TTL or CMOS levels can be used. Note however that power consumption at ±5V is reduced if CLK_A and CLK_B are driven with ±5V, rather than TTL or 0 to 5V levels. Operation with +5V or ±2.5V power lowers power consumption but also reduces bandwidth by approximately 25% compared to +12V or ±5V supplies.

Best performance is achieved if V^+ and V^- are bypassed to ground with 4.7µF electrolytic (Tantalum is preferred.) and 0.1µF ceramic capacitors. These should be located as close to the supply pins as possible. The lead length of the bypass capacitors should be shortest at the V^+ and V^- pins. When using a single supply V^+ and GND should be bypassed to V^- as shown in Figure 16.

Output Swing and Clipping

MAX260/61/62 outputs are designed to drive 10kΩ loads. For the MAX261 and MAX262, all filter outputs swing to within 0.15V of each supply rail with a 10kΩ load. In the MAX260 only, an internal sample-hold circuit reduces voltage swing at the N/HP/AP output compared to LP and BP. N/HP/AP therefore swings to within 1V (10kΩ load) of either rail on the MAX260.

To ensure that the outputs are not driven beyond their maximum range (output clipping), the peak amplitude response, individual section gains (H_{OBP}, H_{OLP}, H_{OHP}), input signal level, and filter offset voltages must be carefully considered. It is especially important to check UNUSED outputs for clipping (i.e. the lowpass output in a bandpass hookup) because overload at ANY filter stage severely distorts the overall response. The maximum signal swing with ±4.75V supplies and a 1.0V filter offset is approximately ±3.5V.

For example lets assume a fourth-order lowpass filter is being implemented with a Q of 2 using Mode 1. With a single 5V supply (i.e. ±2.5V with respect to chip GND) the maximum output signal is ±2V (w.r.t. GND). Since in Mode 1 the maximum signal is Q times the input signal, the input should not exceed ±(2/Q)V, or ±1V in this case.

Clock Feedthrough and Noise

Typical wideband noise for MAX260 series devices is $0.5mV_{pp}$ from DC to 100kHz. The noise is virtually independent of clock frequency. In multistage filters, the section with the highest Q should be placed first for lower output noise.

The output waveform of the MAX260 series and other switched capacitor filters appears as a sampled signal with stepping or "staircasing" of the output waveform occurring at the internal sample rate ($f_{CLK}/2$). This stepping, if objectionable, can be removed by adding a single pole RC filter. With no input signal, clock related feedthrough is approximately $8mV_{pp}$. This can also be attenuated with an RC smoothing filter as shown with the MAX261 in Figure 17.

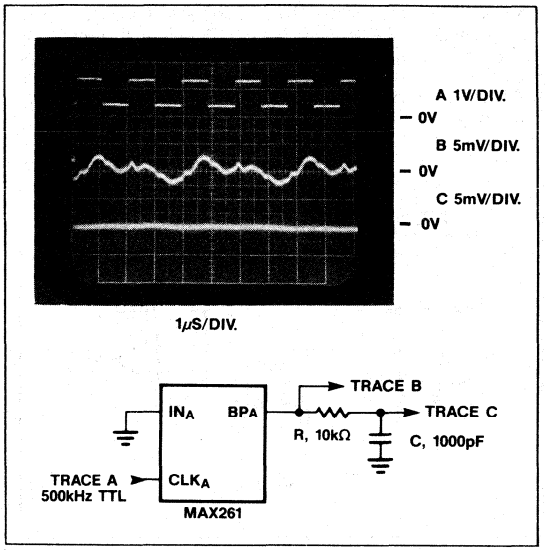

Figure 17. MAX261 Bandpass Output Clock Noise

Some noise also may be generated at the filter outputs by transitions at the logic inputs. If this is objectionable, the digital lines should be buffered from the device by logic gates as shown in Figure 6.

Input Impedance

The input to each filter is the switched capacitor circuit shown in Figure 18. In the MAX260, the input capacitor charges to the input voltage V_{IN} during the first half clock cycle. During the second half-cycle its charge is transferred to the feedback capacitor. The resultant input impedance can be approximated by:

$$R_{IN} = 1/(C_{IN}f_{CLK}/2) = 2/(C_{IN}f_{CLK}).$$

C_{IN} is around 12pF, hence for a clock frequency of 500kHz, R_{IN} = 333kΩ. The input also has about 5pF of fixed capacitance to ground.

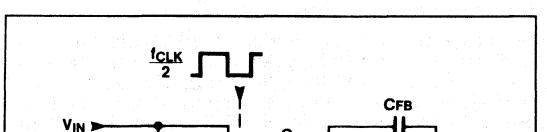

Figure 18. MAX260 Input Model

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The MAX261/262 input structure is shown in Figure 19. Here C_A = 12pF and C_B = 0.016pF and only C_B is switched, so the input resistance is 750 times larger compared to the MAX260 (R_{IN} = 250MΩ). The MAX261/62 has a fixed capacitance of approximately 5pF to ground.

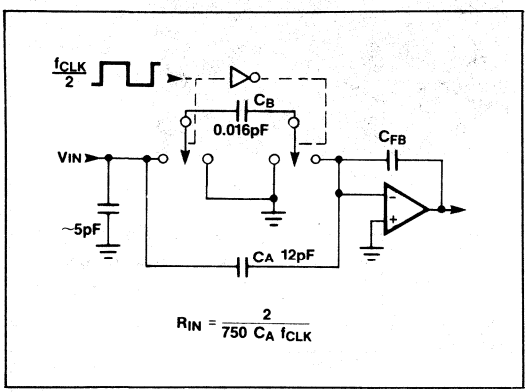


Figure 19. MAX261/262 Input Model

f_0 and Q at Low Sample Rates

When low f_{CLK}/f_0 ratios and low Q settings are selected, deviation from ideal continuous filter response may be noticeable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Figure 20 quantifies these differences. Since the errors are predictable, the graphs can be used to correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX260 series devices and in fact occur with all types of sampled filters. Consequently, these corrections can be applied to other switched-capacitor filters. In the majority of cases, the errors are not significant, i.e. less than 1%, and correction is not needed. However, the MAX262 does employ a lower range of f_{CLK}/f_0 ratios than the MAX260 or MAX261 and is more prone to sampling errors as the tables show.

Maxim's filter design software applies the previous corrections automatically as a function of desired f_{CLK}/f_0, and Q. Therefore, Figure 20 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

The data plotted in Figure 20 applies for Modes 1 and 3. When using Figure 20 for Mode 4, the f_0 error obtained from the graph should be multiplied by 1.5 and the Q error should be multiplied by 3.0. In Mode 2 the value of f_{CLK}/f_0 should be multiplied by $\sqrt{2}$ and the programmed Q should be divided by $\sqrt{2}$ before using the graphs.

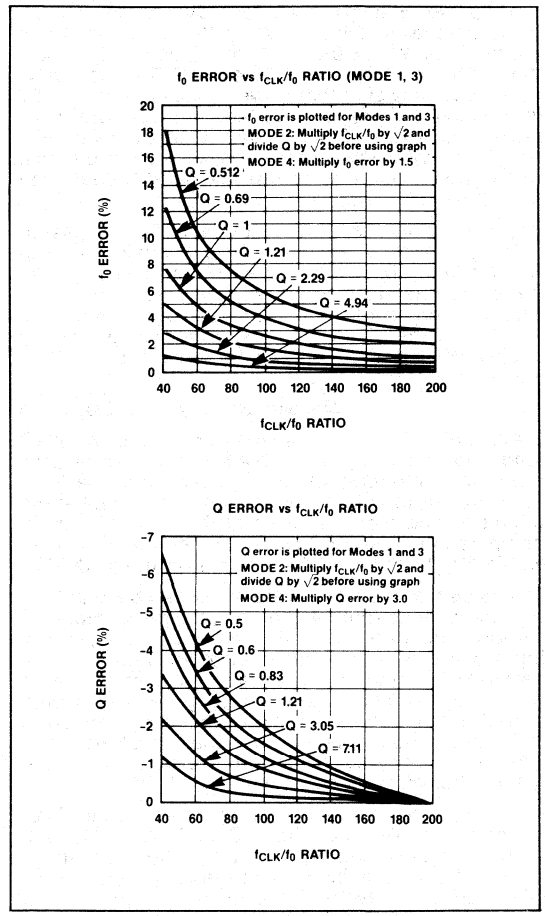


Figure 20. Sampling Errors in f_{CLK}/f_0 and Q at Low f_{CLK}/f_0 and Q Settings

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, (f_{CLK} = 200kHz) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Remember that with the MAX260 series filters, the nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

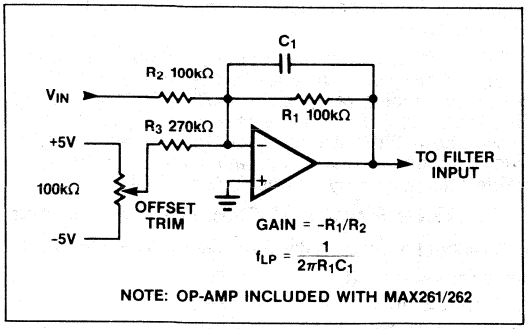
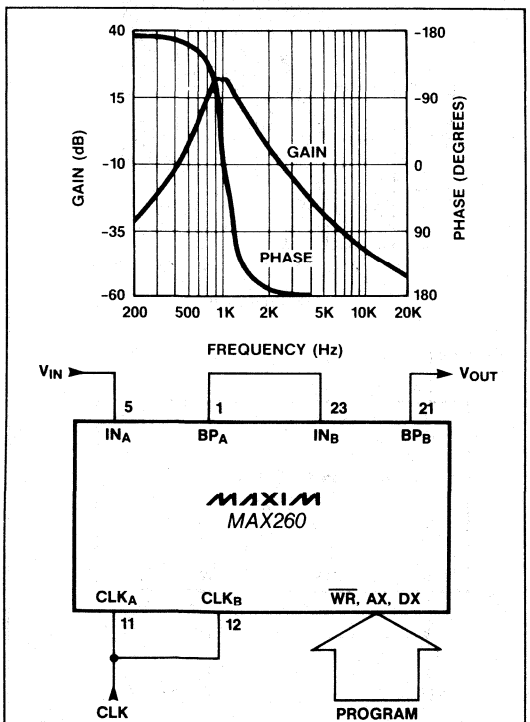


Figure 21. Circuit for DC Offset Adjustment

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can cause aliasing. In many cases the input signal itself may be band limited and require no special anti-alias filtering. The wideband MAX262 uses lower f_{CLK}/f_0 ratios than the MAX260/61 and for this reason is more likely to require input filtering than the MAX260 or MAX261.



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
150kHz	1	N = 42	N = 23	N = 119	N = 119

Figure 22. Fourth-Order Chebyshev Bandpass Filter

Trimming DC Offset

The DC offset voltage at the LP or Notch output can be adjusted with the circuit in Figure 21. This circuit also uses the input op-amp to implement a single pole anti-alias filter. Note that the total offset will generally be less in multistage filters than when only one section is used since each offset is typically negative and each section inverts. When the HP or BP outputs are used, the offset can be removed with capacitor coupling.

Design Examples

Fourth-Order Chebyshev Bandpass Filter

Figure 22 shows both halves of a MAX260 cascaded to form a fourth-order Chebyshev bandpass filter. The desired parameters are:

Center frequency (f_0)	= 1 kHz
Pass bandwidth	= 200 Hz
Stop Bandwidth	= 600 Hz
Max. passband ripple	= 0.5 dB
Min. stopband Attenuation	= 15 dB

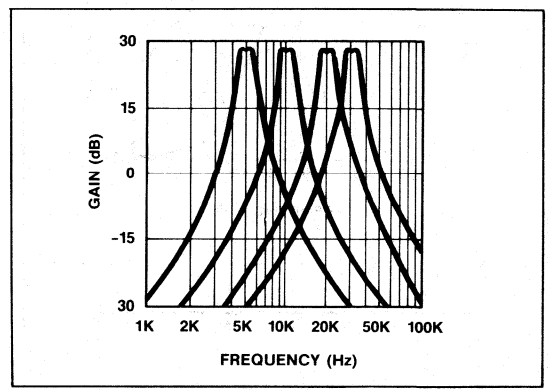


Figure 23. MAX261 Fourth-Order Chebyshev Bandpass Using Coefficients of Figure 22.)

From the above parameters, the order (number of poles), and the f_0 and Q of each section can be determined. Such a derivation is beyond the scope of this data sheet, however there are a number of sources which provide design data for this procedure. These include look-up tables, design texts and computer programs. Design software is available from Maxim to provide comprehensive solutions for most popular filter configurations. The A and B section parameters for the above filter are:

f_{0A} = 904 Hz f_{0B} = 1106 Hz
Q_A = 7.05 Q_B = 7.05

Microprocessor Programmable Universal Active Filters

To implement this filter, both halves operate in Mode 1 and use the same clock. See selection Tables 2 and 3. The programmed parameters are:

$CLK_A = CLK_B = 150$ kHz
$f_{CLK}/f_{0A} = 166.50$ (Mode 1, N=42), actual $f_{0A} = 902.4$Hz
$f_{CLK}/f_{0B} = 136.66$ (Mode 1, N=23), actual $f_{0B} = 1099.7$Hz
$Q_A = Q_B = 7.11$ (Mode 1, N=119)

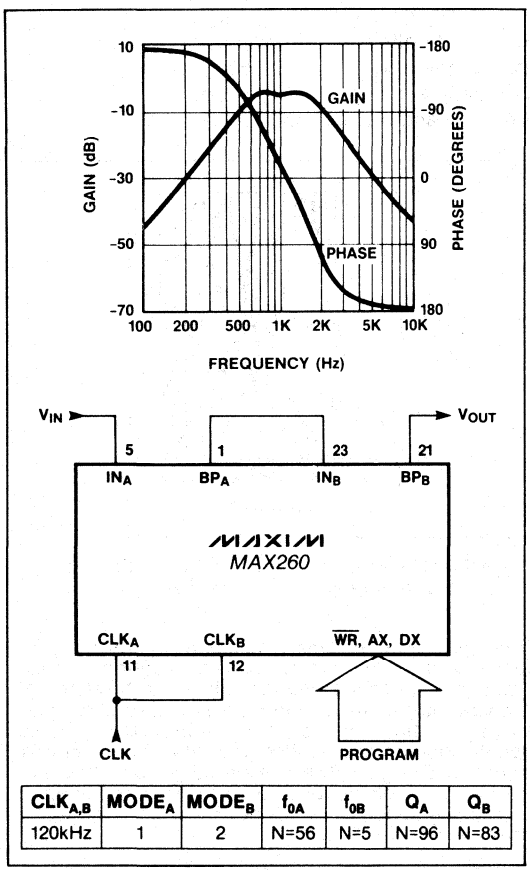
Sampling errors are very small at this f_{CLK}/f_0 ratio so the actual realized Q is very close to 7.05 (See Figure 20 or Filter Program MPP). Often the realized Q will not be exactly the target value at high Qs because programming resolution lowers as Q increases. This doesn't affect most filter designs, since 3-digit Q accuracy is practically never required, and a Q resolution of 1 is provided up to Qs of 10. The overall filter gain at f_0 is 16.4V/V or 24.3dB (See Cascading Filters section). If another gain is required, amplification or attenuation must be added at the input, output, or between stages.

In Figure 23, a series of response curves are shown for the above configuration using a MAX261 with clock frequencies ranging from 750kHz to 4MHz (f_0 from 500Hz to 30kHz). Note that the rightmost curve shows about 2dB of gain peaking compared to the lower frequency curves, indicating the upper limit of usable filter accuracy at this Q (See Table 1)

Wide Passband Chebyshev Bandpass

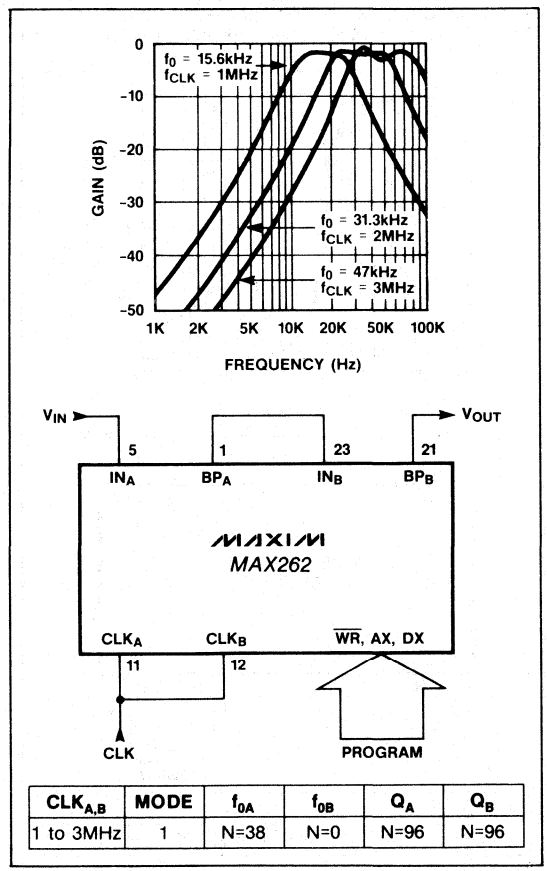
In this example (Figure 24) the desired parameters are:

Center frequency (f_0)	= 1 kHz
Pass bandwidth	= 1 kHz
Stop bandwidth	= 3 kHz
Max passband ripple	= 1 dB
Min stopband Attenuation	= 20 dB



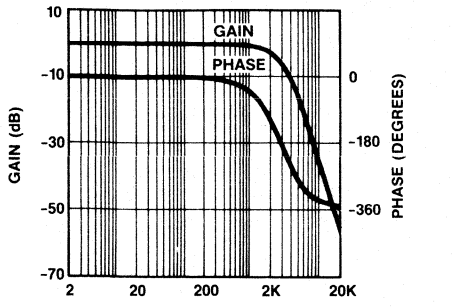
$CLK_{A,B}$	$MODE_A$	$MODE_B$	f_{0A}	f_{0B}	Q_A	Q_B
120kHz	1	2	N=56	N=5	N=96	N=83

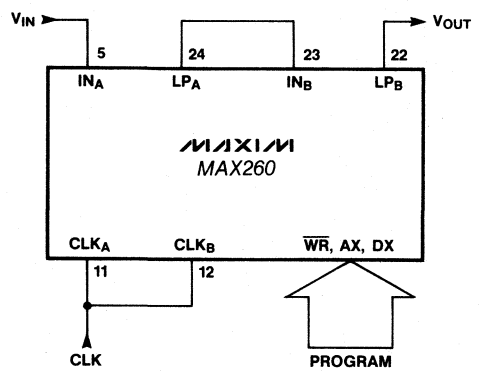
Figure 24. Wide Passband Chebyshev Bandpass Filter



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
1 to 3MHz	1	N=38	N=0	N=96	N=96

Figure 25. High Frequency Chebyshev Bandpass Filter





$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400KHz	1	N = 22	N = 25	N = 79	N = 11

Figure 26. Fourth-Order Butterworth Lowpass

From the above parameters, we use either lookup tables, design texts or Maxim's filter design programs to generate the order (number of poles), and the f_0 and Q of each second-order section. The A and B parameters are:

f_{0A} = 639 Hz f_{0B} = 1564 Hz
Q_A = 2.01 Q_B = 2.01

To implement this filter, section A operates in Mode 1 and section B uses Mode 2 to provide a wider overall range of f_{CLK}/f_0 ratios. This way one clock frequency can drive both sections A and B. See selection Tables 2 and 3.

$CLK_A = CLK_B$ = 120 kHz
f_{CLK}/f_{0A} = 188.49 (Mode 1, N=56), actual f_{0A} = 636.6 Hz
f_{CLK}/f_{0B} = 76.64 (Mode 2, N=5), actual f_{0B} = 156.5 Hz
Q_A = 2.000 (Mode 1, N=96), Q_B = 2.01 (Mode 2, N=83)

The overall passband gain at f_0 will be 0.64V/V or -3.9dB.

High Frequency Chebyshev Bandpass

The same Chebyshev response shape shown in Figure 24 is implemented at higher frequencies with a MAX262 in Figure 25. The curves show plots for center frequencies of 15.6kHz, 31.3kHz, and 47kHz. Not only is this faster than the MAX260 implementation but Mode 1 can be used in both halves of the MAX262 for this filter because the range of available f_{CLK}/f_0 ratios is wider with the MAX262 than the MAX260.

Fourth-Order Butterworth Lowpass

Figure 26 shows a fourth-order Butterworth lowpass with a cutoff frequency of 3kHz. Section A and B of a MAX260 are cascaded. The f_0 and Q parameters for each section are:

f_{0A} = 3kHz f_{0B} = 3kHz
Q_A = 1.307 Q_B = 0.541

Mode 1 and a 400kHz clock are used. Because of low Q values, the sampling errors of Figure 20 begin to look significant in this case. From the graphs, using f_{CLK}/f_0 ratio near 133, f_0A will be about 4% high, f_0B will be 1.5% high. Q_A will be -1.2% low, and Q_B will be -0.5% low. If these errors are not a problem, the corrections can be ignored. They are included here for best possible accuracy:

$CLK_A = CLK_B$ = 400 kHz
f_{CLK}/f_{0A} = 135.08 (N=22), f_{0B} = 2961 Hz (-1.3% correction)
f_{CLK}/f_{0B} = 139.80 (N=25), f_{0A} = 2861 Hz (-4.6% correction)
Q_A = 1.306 (N=79, Q resolution prevents +0.5% correction)
Q_B = 0.547 (N=11, +1.1% correction)

Measured wideband noise for this filter is 123μV RMS. If Mode 2 were used, the noise would be 87μV RMS. For lower noise with either Mode the first section should have the highest Q (Section A in this example).

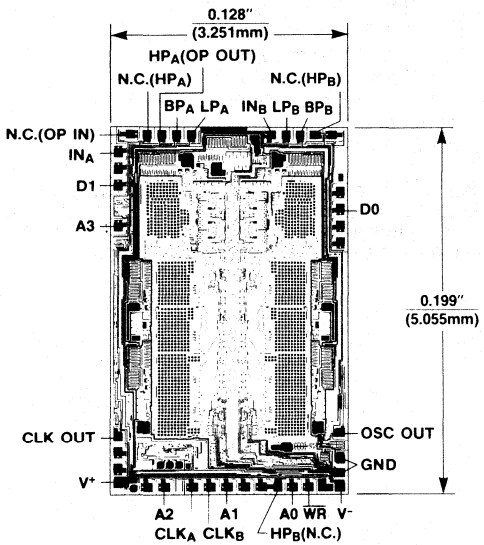
Microprocessor Programmable Universal Active Filters

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX261BCNG	0°C to +70°C	Plastic DIP	2%
MAX261AENG	-40°C to +85°C	Plastic DIP	1%
MAX261BENG	-40°C to +85°C	Plastic DIP	2%
MAX261ACWG	0°C to +70°C	Wide SO	1%
MAX261BCWG	0°C to +70°C	Wide SO	2%
MAX261AMRG	-55°C to +125°C	CERDIP	1%
MAX261BMRG	-55°C to +125°C	CERDIP	2%
MAX262ACNG	0°C to +70°C	Plastic DIP	1%
MAX262BCNG	0°C to +70°C	Plastic DIP	2%
MAX262AENG	-40°C to +85°C	Plastic DIP	1%
MAX262BENG	-40°C to +85°C	Plastic DIP	2%
MAX262ACWG	0°C to +70°C	Wide SO	1%
MAX262BCWG	0°C to +70°C	Wide SO	2%
MAX262AMRG	-55°C to +125°C	CERDIP	1%
MAX262BMRG	-55°C to +125°C	CERDIP	2%

** All devices—24-pin 0.3" wide packages*

Chip Topography



NOTE: LABELS IN PARENTHESES ( ) ARE FOR MAX261/62 ONLY

MAXIM
Pin Programmable Universal and Bandpass Filters

General Description

The MAX263/264 and MAX267/268 CMOS switched-capacitor active filters are designed for precision filtering applications. Center frequency, Q, and operating mode are all selected via pin-strapped inputs. The MAX263/264 uses no external components for a variety of bandpass, lowpass, highpass, notch and allpass filters. The MAX267/268 is dedicated to bandpass applications and includes an uncommitted op-amp. Two second-order filter sections are included in both devices.

An input clock and a 5-bit programming input precisely set the filter center/corner frequency. Q is also programmed from 0.5 to 64. Separate clock inputs for each filter half operate with either an external clock or a crystal.

The MAX263 and 267 operate with center frequencies up to 57kHz while the MAX264 and 268 extend the f_0 range to 140kHz by employing lower f_{CLK}/f_0 ratios. The MAX263/264 is supplied in 28 pin wide DIP and small outline packages while the MAX267/268 is supplied in 24 pin narrow DIP and wide SO packages. All devices are available in commercial, extended, and military temperature ranges.

Applications

Sonar and Avionics Instruments

Anti-Aliasing Filters

Digital Signal Processing

Vibration and Audio Analysis

Matched Tracking Filters

Features

- ◆ **Filter Design Software Available**
- ◆ **32-Step Center Frequency Control**
- ◆ **128-Step Q Control**
- ◆ **Independent Q and f_0 Programming**
- ◆ **Guaranteed Clock to f_0 Ratio—1% (A grade)**
- ◆ **75kHz f_0 Range (MAX264/268)**
- ◆ **Single +5V and ±5V Operation**

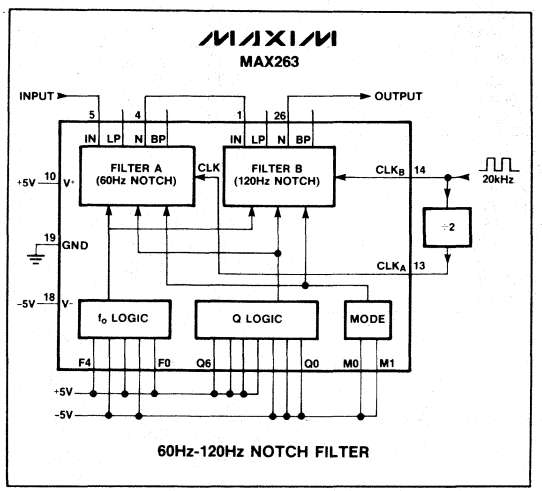
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX263ACPI	0°C to +70°C	Plastic DIP	1%
MAX263BCPI	0°C to +70°C	Plastic DIP	2%
MAX263AEPI	-40°C to +85°C	Plastic DIP	1%
MAX263BEPI	-40°C to +85°C	Plastic DIP	2%
MAX263ACWI	0°C to +70°C	Wide SO	1%
MAX263BCWI	0°C to +70°C	Wide SO	2%
MAX263AMJI	-55°C to +125°C	CERDIP	1%
MAX263BMJI	-55°C to +125°C	CERDIP	2%
MAX264ACPI	0°C to +70°C	Plastic DIP	1%
MAX264BCPI	0°C to +70°C	Plastic DIP	2%

(Ordering Information continued on last page.)

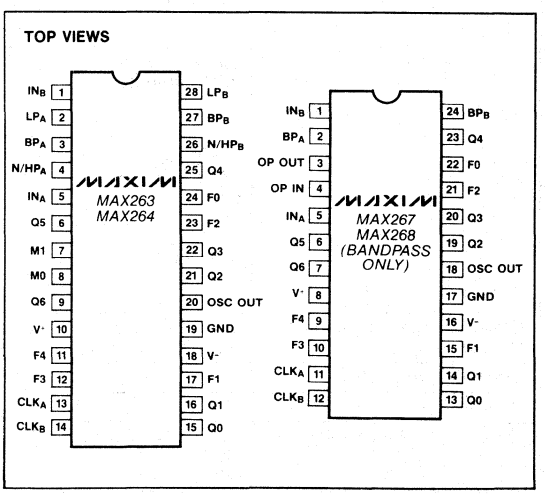
* *MAX263/264 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" wide SO (Small Outline).*
MAX267/268 packages are 24-pin 0.3" wide DIP and 24-pin 0.3" wide SO (Small Outline).

Typical Application



60Hz-120Hz NOTCH FILTER

Pin Configuration



Pin Programmable Universal and Bandpass Filters

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage, any pin ..... V^--0.3V to V^++0.3V
Input Current, any pin ..... ±50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above 70°C) ... 660mW
  CERDIP (derate 12.5mW/°C above 70°C) 1000mW
  Wide SO (derate 11.8mW/°C above 70°C) 944mW

Operating Temperature
  MAX26XXCXX ..... 0°C to +70°C
  MAX26XXEXX ..... -40°C to +85°C
  MAX26XXMXX ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V, 1.5MHz, f_{CLK}/f_0 = 197.92 for MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, "1" = V^+ and "0" = V^- on F and Q inputs, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				See Table 1		
Maximum Clock Frequency				See Table 1		
f_{CLK}/f_0 Ratio Error (Note 1)	T_A = T_{MIN} to T_{MAX}	MAX26XA MAX26XB		±0.2 ±0.2	±1.0 ±2.0	%
f_0 Temperature Coefficient				-5		ppm/°C
Q Accuracy (deviation from ideal continuous filter) (Note 2)	T_A = T_{MIN} to T_{MAX} Q = 0.5 to 16 Q = 0.5 to 16 Q = 32 Q = 32 Q = 64 Q = 64	 MAX26XA MAX26XB MAX26XA MAX26XB MAX26XA MAX26XB		 ±1 ±1 ±2 ±2 ±4 ±4	 ±6 ±10 ±10 ±15 ±15 ±22	%
Q Temperature Coefficient				±20		ppm/°C
DC Lowpass Gain Accuracy		MAX263/4A MAX263/4B		±0.1 ±0.1	±0.25 ±0.5	dB
Gain Temperature Coefficient	Lowpass (at D.C.) Bandpass (at f_0)			-5 +20		ppm/°C
Output Offset Voltage (Note 3)	T_A = T_{MIN} to T_{MAX}, Q = 4 Mode 1 BP Output	 MAX263/67A MAX263/67B MAX264/68A MAX264/68B		 ±0.05 ±0.05 ±0.05 ±0.05	 ±0.20 ±0.30 ±0.20 ±0.30	V
	Mode 1 LP,N Outputs	MAX263A MAX263B MAX264A MAX264B		±0.40 ±0.80 ±0.40 ±0.80	±0.90 ±1.60 ±0.90 ±1.60	
	Mode 3 BP, HP Outputs	MAX263A MAX263B MAX264A MAX264B		±0.10 ±0.10 ±0.10 ±0.10	±0.20 ±0.30 ±0.20 ±0.30	
	Mode 3 LP Output	MAX263A MAX263B MAX264A MAX264B		±0.50 ±0.90 ±0.50 ±0.90	±1.00 ±1.60 ±1.00 ±1.60	
Offset Voltage Temperature Coefficient	f_{CLK}/f_0 = 100.53, Q = 4 T_A = T_{MIN} to T_{MAX}			±0.75		mV/°C
Clock Feedthrough				±4		mV
Crosstalk				-70		dB
Wideband Noise (Note 4)	Q = 1, 2nd-Order, LP/BP 4th-Order LP 4th-Order BP			See Typ. Oper. Char. 90 100		μV_{RMS}

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V, 1.5MHz, f_{CLK}/f_0 = 197.92 for MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, "1" = V^+ and "0" = V^- on F and Q inputs, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Harmonic Distortion at f_0	Q = 4, V_{IN} = 1.5V_{PP}			-57		dB
Supply Voltage Range	T_A = T_{MIN} to T_{MAX}		±2.37	±5	±6.3	V
Power Supply Current (Note 5)	T_A = T_{MIN} to T_{MAX}	MAX263/67 MAX264/68		14 14	20 20	mA
Shutdown Supply Current (Note 5)	Q0-Q6 = all 0			2.5		mA
f_0, Q Programming Inputs	T_A = T_{MIN} to T_{MAX}, F0-F4, Q0-Q6 High Threshold Low Threshold		V^+–0.5		 V^-+0.5	V
Clock Inputs	T_A = T_{MIN} to T_{MAX}, CLK_A, CLK_B High Threshold Low Threshold		2.4		 0.8	V
Input Leakage Current	T_A = T_{MIN} to T_{MAX} CLK_B = V^+ or V^- CLK_A = V^+ or V^- M0, M1, F0-F4, Q0-Q6 = V^+–0.5V or V^-+0.5V M0, M1, F0-F4, Q0-Q6 = V^+ or V^-			 6 20 5	10 60 200	µA
INTERNAL AMPLIFIERS						
Output Signal Swing	T_A = T_{MIN} to T_{MAX}, 10kΩ load			±4.75		V
Output Short Circuit Current	Source Sink			50 2		mA
Power Supply Rejection Ratio	0Hz to 10kHz			-70		dB
Gain Bandwidth Product				2.5		MHz
Slew Rate				6		V/µs

ELECTRICAL CHARACTERISTICS (for V± = ±2.5V ±5%)

(V^+ = +2.37V, V^- = -2.37V, CLK_A = CLK_B = ±2.5V 1MHz f_{CLK}/f_0 = 197.92 for the MAX263/67 and 138.23 for MAX264/68, Filter Mode 1, T_A = +25°C unless otherwise noted.)

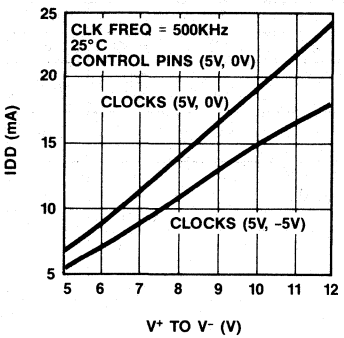
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				(Note 6)		
Maximum Clock Frequency				(Note 6)		
f_{CLK}/f_0 Ratio Error (Notes 1, 7)	Q = 8	MAX26XA MAX26XB		±0.1 ±0.1	±1 ±2	%
Q Accuracy (deviation from ideal continuous filter) (Notes 2, 7)	Q = 8 f_{CLK}/f_0 = 197.92 f_{CLK}/f_0 = 138.23	 MAX263/67A MAX263/67B MAX264/68A MAX264/68B		 ±2 ±2 ±2 ±2	 ±5 ±10 ±5 ±10	%
Output Signal Swing	All Outputs			±2		V
Power Supply Current				7		mA
Shutdown Current				0.45		mA

Note 1: f_{CLK}/f_0 accuracy is tested at 100.53, 103.67, 106.81, 113.1, 125.66, 150.8, and 197.92 on the MAX263/67, and at 40.84, 43.98, 47.12, 53.41, 65.97, 91.11, and 138.23 on the MAX264/68.
Note 2: Q accuracy tested at Q = 0.5, 1, 2, 4, 8, 16, 32, and 64. Q of 32 and 64 tested at 1/2 stated clock frequency.
Note 3: The Offset Voltage is specified for the entire filter. Offset is virtually independent of Q and f_{CLK}/f_0 ratio setting. The test clock frequency for Mode 3 is 750kHz.
Note 4: Output noise is measured with an RC output smoothing filter at 4 × f_0 to remove clock feedthrough.
Note 5: TTL logic levels are: HIGH = 2.4V, LOW = 0.8V. Power supply current is typically 4mA higher with TTL clock input levels.
Note 6: At ±2.5V supplies, the f_0 range and maximum clock frequency are typically 75% of values listed in Table 1.
Note 7: f_{CLK}/f_0 and Q accuracy are a function of the accuracy of internal capacitor ratios. No increase in error is expected at ±2.5V as compared to ±5V however these parameters are only tested to the extent indicated by the MIN or MAX limits.

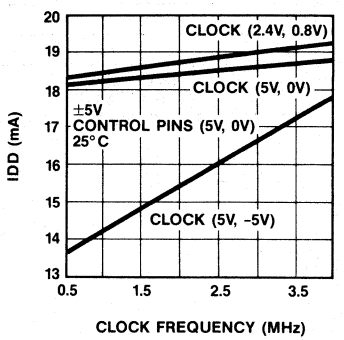
Pin Programmable Universal and Bandpass Filters

Typical Operating Characteristics

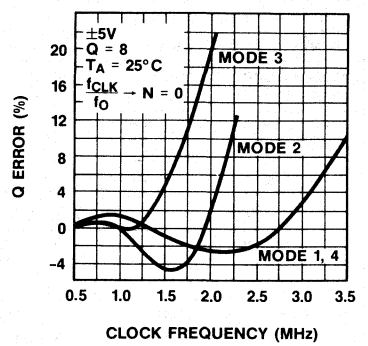
IDD vs POWER SUPPLY VOLTAGE



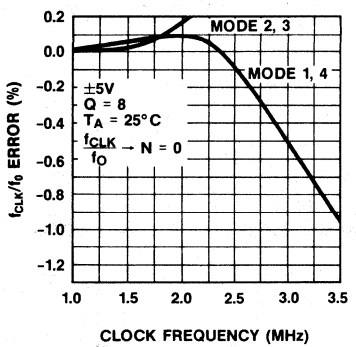
IDD vs CLOCK FREQUENCY



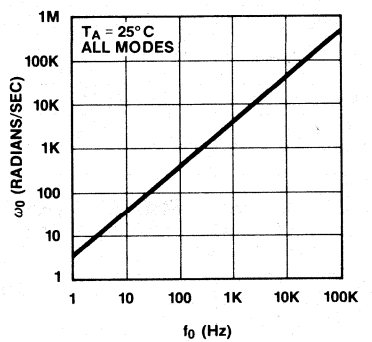
Q vs CLOCK FREQUENCY



f_{CLK}/f_0 vs CLOCK FREQUENCY



ω_0 vs f_0



Wideband RMS Noise (db ref. to 2.47V_{RMS}, 7V_{p-p}), ±5V Operation

Mode	Q = 1			Q = 8			Q = 64		
	LP	BP	HP/AP/N	LP	BP	HP/AP/N	LP	BP	HP/AP/N
1	-84	-90	-84	-80	-82	-85	-72	-73	-85
2	-88	-90	-88	-84	-82	-84	-77	-73	-76
3	-84	-90	-88	-80	-82	-82	-73	-73	-74
4	-83	-89	-84	-79	-81	-85	-71	-73	-85

Notes:
1. f_{CLK} = 1MHz
2. f_{CLK}/f_0 ratio programmed at N = 31 (see Table 2)
3. Clock feedthrough is removed with an RC lowpass at $4f_0$, i.e. R = 3.9kΩ, C = 2000pF for MAX263.

Noise Spectral Distribution
(MAX263/67, f_{CLK} = 1 MHz, dB ref. to 2.47V_{RMS}, 7V_{p-p})

Measurement Bandwidth	Q=1	Q=8	Q=64
Wideband	-84	-80	-72
3kHz	-87	-87	-86
C Message Weighted	-93	-93	-93

Pin Description

MAX263 MAX264 PIN #	MAX267 MAX268 PIN #	NAME	FUNCTION
10	8	V^+	Positive supply voltage
18	16	V^-	Negative supply voltage
19	17	GND	Analog Ground. Connect to the system ground for dual supply operation or mid-supply for single supply operation. GND should be well bypassed in single supply applications.
13	11	CLK_A	Input to the oscillator and clock input to section A. This clock is internally divided by 2.
14	12	CLK_B	Clock input to filter B. This clock is internally divided by 2.
20	18	OSC OUT	Connects to crystal for self clocked operation
5, 1	5, 1	IN_A, IN_B	Filter inputs
3, 27	2, 24	BP_A, BP_B	Bandpass outputs
2, 28		LP_A, LP_B	Lowpass outputs (MAX263/264 only)
4, 26		HP_A, HP_B	Highpass/Notch/Allpass outputs (MAX263/264 only)
8, 7		M0, M1	Mode select inputs (MAX267/268 are fixed in Mode 1)
24, 17, 23 12, 11	22, 15, 21 10, 9	F0-F4	Clock/center frequency ratio (f_{CLK}/f_0) programming inputs
15, 16, 21 22, 25, 6 9	13, 14, 19 20, 23, 6 7	Q0-Q6	Q programming inputs
	4	OP IN	Inverting input of uncommitted op-amp on MAX267/268 only. Noninverting input is internally connected to ground.
	3	OP OUT	Output of uncommitted op-amp on MAX267/268 only.

Pin Programmable Universal and Bandpass Filters

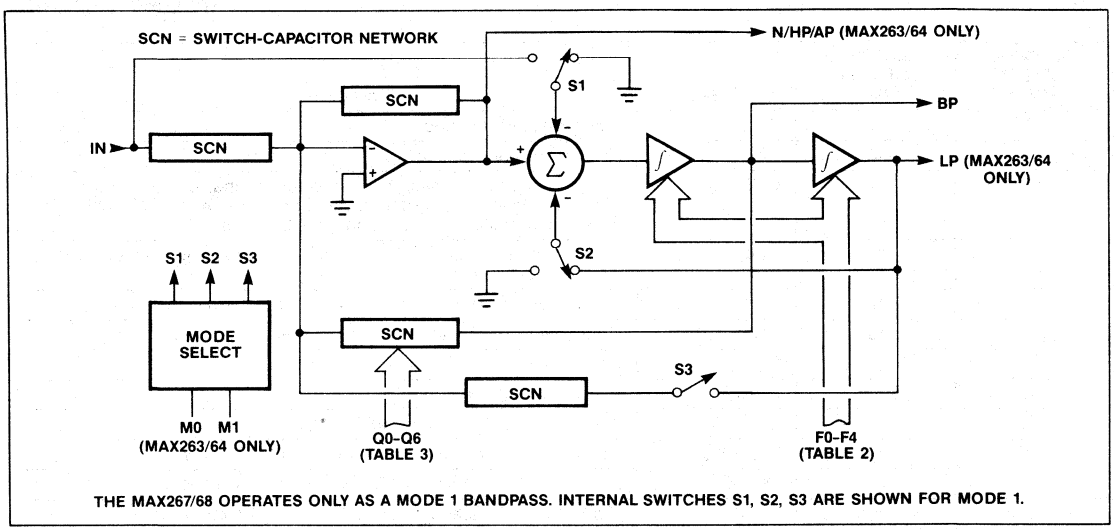


Figure 1. Filter Block Diagram (One Second-Order Section)

Introduction

Each MAX26X device contains two second-order filters. In Figure 1, a block diagram of the state variable topology employed in one filter section shows how on-chip switched capacitor networks provide adjustable feedback to control f_0 and Q. Shared programming inputs require that both halves of the filter be set for the same f_{CLK}/f_0 ratio and Q. In the MAX263 and MAX264 universal filters, switches S1-S3 are controlled by inputs M0 and M1 to set the filter operating mode. The MAX267/68 bandpass filter operates only in Mode 1.

The MAX264/68 uses a lower range of sampling (f_{CLK}/f_0) ratios than the MAX263/67 to allow higher signal bandwidths and a wider programming range. The reduced f_{CLK}/f_0 ratios result in somewhat more deviation from ideal continuous filter parameters than with the MAX263/67, however these differences can be compensated using Figure 17 (See "Applications Hints") or Maxim's filter design software.

The second-order sections in the MAX263/64/67/68 are identical and may be used as matched dual tracking filters, or can be cascaded to form higher-order filters. They can also be combined with external resistors and amplifiers for multiple feedback all-pole bandpass filters.

In all MAX26X series filters, the internal sample rate is one half the input clock rate (CLK_A or CLK_B) due to an internal division by two. All clock related data, tables, and other discussions in this data sheet refer to the frequency at the CLK_A or CLK_B input, i.e. twice the internal sample rate, unless specifically stated otherwise.

Quick Look Design Procedure

MAX26X series filters, with Maxim's filter design software, greatly simplify the design procedure for many active filters. Most designs can be realized using the steps in this section. If the filter software is not used, or if the complexity is beyond the scope of this section, refer to the remainder of this data sheet for more detailed application information.

Step 1—Filter Design

Starting with the design program "PZ", determine what type of filter is needed. PZ helps determine the type (Butterworth, Chebyshev, etc.) and the number of poles for the optimum choice. The program also plots the frequency response and calculates the pole/zero (f_0) and Q values for each second-order section. Each MAX26X contains two such sections and devices may be cascaded for higher order filters.

An alternate technique for bandpass filters uses multiple feedback (see Figure 13). If this is employed, the filter design program "BP" should be used instead of PZ and Step 2 is not used.

Step 2—Generate Programming Coefficients

If multiple feedback is not used, start with the f_0 and Q values obtained with PZ in Step 1 and use the program "MPP" to generate the digital program codes for f_{CLK}/f_0 and Q. MPP displays "N" values for f_0 and Q where N is the decimal equivalent of the binary pin-program codes. These are listed in Tables 2 and 3.

An input clock and filter "Mode" must also be selected in this step, however, if a specific clock rate is not selected, "MPP" will pick one. With regard to mode selection, Mode 1 (only possible mode for MAX267/68) is the most convenient choice for most bandpass and lowpass filters except for elliptics which require Mode 3. Highpass filters also use Mode 3, while allpass filters require Mode 4. For details regarding mode selection see "Filter Operating Modes". When a clock frequency (or frequencies) is selected and the programming codes for f_{CLK}/f_0 and Q are determined, the filter can then be programmed and operated.

Filter Design Software

Maxim provides software programs to help speed the transition from frequency response design requirements to working hardware. A series of programs are available, including:

Program PZ. Given the requirements, such as center frequency, Q, passband ripple, and stopband attenuation, PZ will calculate the pole frequencies, Q's, zeros, and the number of stages needed.

Program MPP. For programmed filters, MPP computes the input codes to use and describes the expected performance of the design.

Program BP. In the special case of bandpass filters, an alternate mode of operation is the "Multiple Feedback Technique". BP calculates the resistor values and the bandpass frequency response for this mode. An advantage of multiple feedback is that identical programming and one clock frequency can be used for all stages.

Program FR. When a design of one or more stages is completed, FR checks the final cascaded assembly. The output frequency response can be compared with that expected from PZ.

Detailed Description

f_0 and Q Programming

Figure 2 shows a block diagram of a complete filter. Each 2nd-order filter section has its own clock input, however, package pin limitations require that f_0, Q, and Mode control be shared by both sections. The actual center frequency is a function of the filter's clock rate, 5-bit f_0 control word (see Table 2), and operating Mode.

For some filter designs, the MAX263/64/67/68 may require separate clocks for each second-order section since separate programming inputs are not provided. Such designs may be implemented with different clock inputs, or, in the case of bandpass filters, by using multiple feedback and one clock (see "Description of Filter Functions"). When implementing two or more matched filters, however, the programming restrictions are easily overcome and one clock can still be used as demonstrated by the design example in Figure 21. Another alternative is to use the MAX260/261/262 microprocessor programmed filters or the MAX265/266 resistor programmed filters which allow independent programming of each filter section. Refer to the device data sheets for further details on those products.

Pin Programmable Universal and Bandpass Filters

Table 1. Typical Clock and Center Frequency Limits (MAX267/268 are operated in Mode 1 only.)

PART	Q	MODE	f_{CLK}	f_0
MAX263/ 267	1	1	40Hz-4.0MHz	0.4Hz-40kHz
	1	2	40Hz-4.0MHz	0.5Hz-57kHz
	1	3	40Hz-4.0MHz	0.4Hz-40kHz
	1	4	40Hz-4.0MHz	0.4Hz-40kHz
	8	1	40Hz-2.7MHz	0.4Hz-27kHz
	8	2	40Hz-2.1MHz	0.5Hz-30kHz
	8	3	40Hz-1.7MHz	0.4Hz-17kHz
	8	4	40Hz-2.7MHz	0.4Hz-27kHz
	64	1	40Hz-2.0MHz	0.4Hz-20kHz
	90	2	40Hz-1.2MHz	0.4Hz-18kHz
	64	3	40Hz-1.2MHz	0.4Hz-12kHz
	64	4	40Hz-2.0MHz	0.4Hz-20kHz

PART	Q	MODE	f_{CLK}	f_0
MAX264/ 268	1	1	40Hz-4.0MHz	1.0Hz-100kHz
	1	2	40Hz-4.0MHz	1.4Hz-140kHz
	1	3	40Hz-4.0MHz	1.0Hz-100kHz
	1	4	40Hz-4.0MHz	1.0Hz-100kHz
	8	1	40Hz-2.5MHz	1.0Hz-60kHz
	8	2	40Hz-1.4MHz	1.4Hz-50kHz
	8	3	40Hz-1.4MHz	1.0Hz-35kHz
	8	4	40Hz-2.5MHz	1.0Hz-60kHz
	64	1	40Hz-1.5MHz	1.0Hz-37kHz
	90	2	40Hz-0.9MHz	1.4Hz-32kHz
	64	3	40Hz-0.9MHz	1.0Hz-22kHz
	64	4	40Hz-1.5MHz	1.0Hz-37kHz

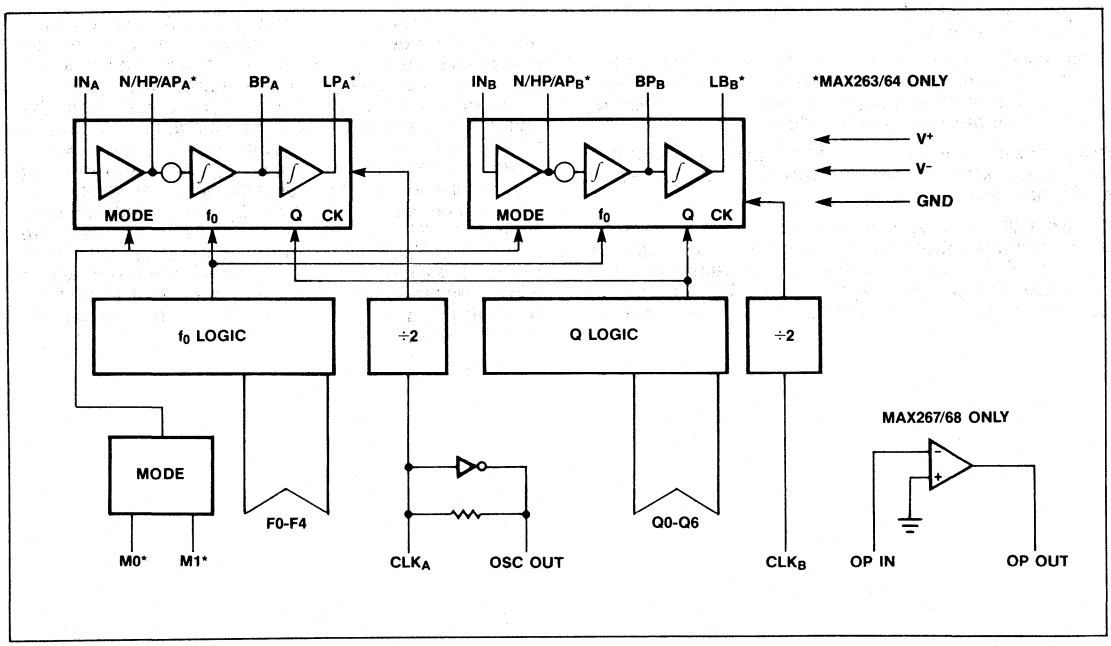


Figure 2. MAX263/264/267/268 Block Diagram

Table 2. f_{CLK}/f_0 Program Selection Table

f_{CLK}/f_0 RATIO				PROGRAM CODE					
MAX263/67		MAX264/68							
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F4	F3	F2	F1	F0
100.53	71.09	40.84	28.88	0	0	0	0	0	0
103.67	73.31	43.98	31.10	1	0	0	0	0	1
106.81	75.53	47.12	33.32	2	0	0	0	1	0
109.96	77.75	50.27	35.54	3	0	0	0	1	1
113.10	79.97	53.41	37.76	4	0	0	1	0	0
116.24	82.19	56.55	39.99	5	0	0	1	0	1
119.38	84.42	59.69	42.21	6	0	0	1	1	0
122.52	86.64	62.83	44.43	7	0	0	1	1	1
125.66	88.86	65.97	46.65	8	0	1	0	0	0
128.81	91.80	69.12	48.87	9	0	1	0	0	1
131.95	93.30	72.26	51.10	10	0	1	0	1	0
135.08	95.52	75.40	53.31	11	0	1	0	1	1
138.23	97.74	78.53	55.54	12	0	1	1	0	0
141.37	99.97	81.68	57.76	13	0	1	1	0	1
144.51	102.89	84.82	59.98	14	0	1	1	1	0
147.65	104.41	87.96	62.20	15	0	1	1	1	1
150.80	106.63	91.11	64.42	16	1	0	0	0	0
153.98	108.85	94.25	66.64	17	1	0	0	0	1
157.08	111.07	97.39	68.86	18	1	0	0	1	0
160.22	113.29	100.53	71.09	19	1	0	0	1	1
163.36	115.52	102.67	73.31	20	1	0	1	0	0
166.50	117.74	106.81	75.53	21	1	0	1	0	1
169.65	119.96	109.96	77.75	22	1	0	1	1	0
172.79	122.18	113.10	79.97	23	1	0	1	1	1
175.93	124.40	116.24	82.19	24	1	1	0	0	0
179.07	126.62	119.38	84.81	25	1	1	0	0	1
182.21	128.84	122.52	86.64	26	1	1	0	1	0
185.35	131.07	125.66	88.86	27	1	1	0	1	1
188.49	133.29	128.81	91.08	28	1	1	1	0	0
191.64	135.51	131.95	93.30	29	1	1	1	0	1
194.78	137.73	135.09	95.52	30	1	1	1	1	0
197.92	139.95	138.23	97.74	31	1	1	1	1	1

Notes: 1) For the MAX263/67, $f_{CLK}/f_0 = \pi(N+32)$ in Mode 1, 3, and 4, where N varies form 0 to 31.
2) For the MAX264/68, $f_{CLK}/f_0 = \pi(N+13)$ in Mode 1, 3, and 4, where N varies 0 to 31.
3) In Mode 2, all f_{CLK}/f_0 ratios are divided by $\sqrt{2}$.

Pin Programmable Universal and Bandpass Filters

Table 3. Q Program Selection Table (Continued on following page)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Note 4	Note 4	0	0	0	0	0	0	0	0
0.504	0.713	1	0	0	0	0	0	0	1
0.508	0.718	2	0	0	0	0	0	1	0
0.512	0.724	3	0	0	0	0	0	1	1
0.516	0.730	4	0	0	0	0	1	0	0
0.520	0.736	5	0	0	0	0	1	0	1
0.525	0.742	6	0	0	0	0	1	1	0
0.529	0.748	7	0	0	0	0	1	1	1
0.533	0.754	8	0	0	0	1	0	0	0
0.538	0.761	9	0	0	0	1	0	0	1
0.542	0.767	10	0	0	0	1	0	1	0
0.547	0.774	11	0	0	0	1	0	1	1
0.552	0.780	12	0	0	0	1	1	0	0
0.556	0.787	13	0	0	0	1	1	0	1
0.561	0.794	14	0	0	0	1	1	1	0
0.566	0.801	15	0	0	0	1	1	1	1
0.571	0.808	16	0	0	1	0	0	0	0
0.577	0.815	17	0	0	1	0	0	0	1
0.582	0.823	18	0	0	1	0	0	1	0
0.587	0.830	19	0	0	1	0	0	1	1
0.593	0.838	20	0	0	1	0	1	0	0
0.598	0.846	21	0	0	1	0	1	0	1
0.604	0.854	22	0	0	1	0	1	1	0
0.609	0.862	23	0	0	1	0	1	1	1
0.615	0.870	24	0	0	1	1	0	0	0
0.621	0.879	25	0	0	1	1	0	0	1
0.627	0.887	26	0	0	1	1	0	1	0
0.634	0.896	27	0	0	1	1	0	1	1
0.640	0.905	28	0	0	1	1	1	0	0
0.646	0.914	29	0	0	1	1	1	0	1
0.653	0.924	30	0	0	1	1	1	1	0
0.660	0.933	31	0	0	1	1	1	1	1
0.667	0.943	32	0	1	0	0	0	0	0
0.674	0.953	33	0	1	0	0	0	0	1
0.681	0.963	34	0	1	0	0	0	1	0
0.688	0.973	35	0	1	0	0	0	1	1
0.696	0.984	36	0	1	0	0	1	0	0
0.703	0.995	37	0	1	0	0	1	0	1
0.711	1.01	38	0	1	0	0	1	1	0
0.719	1.02	39	0	1	0	0	1	1	1
0.727	1.03	40	0	1	0	1	0	0	0
0.736	1.04	41	0	1	0	1	0	0	1
0.744	1.05	42	0	1	0	1	0	1	0
0.753	1.06	43	0	1	0	1	0	1	1
0.762	1.08	44	0	1	0	1	1	0	0
0.771	1.09	45	0	1	0	1	1	0	1
0.780	1.10	46	0	1	0	1	1	1	0
0.790	1.12	47	0	1	0	1	1	1	1
0.800	1.13	48	0	1	1	0	0	0	0
0.810	1.15	49	0	1	1	0	0	0	1
0.821	1.16	50	0	1	1	0	0	1	0
0.831	1.18	51	0	1	1	0	0	1	1
0.842	1.19	52	0	1	1	0	1	0	0
0.853	1.21	53	0	1	1	0	1	0	1
0.865	1.22	54	0	1	1	0	1	1	0
0.877	1.24	55	0	1	1	0	1	1	1
0.889	1.26	56	0	1	1	1	0	0	0
0.901	1.27	57	0	1	1	1	0	0	1
0.914	1.29	58	0	1	1	1	0	1	0
0.928	1.31	59	0	1	1	1	0	1	1
0.941	1.33	60	0	1	1	1	1	0	0
0.955	1.35	61	0	1	1	1	1	0	1
0.969	1.37	62	0	1	1	1	1	1	0
0.985	1.39	63	0	1	1	1	1	1	1
1.00	1.41	64	1	0	0	0	0	0	0
1.02	1.44	65	1	0	0	0	0	0	1
1.03	1.46	66	1	0	0	0	0	1	0
1.05	1.48	67	1	0	0	0	0	1	1
1.07	1.51	68	1	0	0	0	1	0	0
1.08	1.53	69	1	0	0	0	1	0	1
1.10	1.56	70	1	0	0	0	1	1	0
1.12	1.59	71	1	0	0	0	1	1	1
1.14	1.62	72	1	0	0	1	0	0	0
1.16	1.65	73	1	0	0	1	0	0	1
1.19	1.68	74	1	0	0	1	0	1	0
1.21	1.71	75	1	0	0	1	0	1	1
1.23	1.74	76	1	0	0	1	1	0	0
1.25	1.77	77	1	0	0	1	1	0	1
1.28	1.81	78	1	0	0	1	1	1	0
1.31	1.85	79	1	0	0	1	1	1	1
1.33	1.89	80	1	0	1	0	0	0	0
1.36	1.93	81	1	0	1	0	0	0	1
1.39	1.97	82	1	0	1	0	0	1	0
1.42	2.01	83	1	0	1	0	0	1	1
1.45	2.06	84	1	0	1	0	1	0	0
1.49	2.10	85	1	0	1	0	1	0	1
1.52	2.16	86	1	0	1	0	1	1	0
1.56	2.21	87	1	0	1	0	1	1	1
1.60	2.26	88	1	0	1	1	0	0	0
1.64	2.32	89	1	0	1	1	0	0	1
1.68	2.40	90	1	0	1	1	0	1	0
1.73	2.45	91	1	0	1	1	0	1	1
1.78	2.51	92	1	0	1	1	1	0	0
1.83	2.59	93	1	0	1	1	1	0	1
1.88	2.66	94	1	0	1	1	1	1	0
1.94	2.74	95	1	0	1	1	1	1	1

Notes: 4) Writing all 0s into Q0-Q6 activates a low power shutdown mode. BOTH filter sections are deactivated.

Table 3. Q Program Selection Table (Continued)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
2.00	2.83	96	1	1	0	0	0	0	0
2.06	2.92	97	1	1	0	0	0	0	1
2.13	3.02	98	1	1	0	0	0	1	0
2.21	3.12	99	1	1	0	0	0	1	1
2.29	3.23	100	1	1	0	0	1	0	0
2.37	3.35	101	1	1	0	0	1	0	1
2.46	3.48	102	1	1	0	0	1	1	0
2.56	3.62	103	1	1	0	0	1	1	1
2.67	3.77	104	1	1	0	1	0	0	0
2.78	3.96	105	1	1	0	1	0	0	1
2.91	4.11	106	1	1	0	1	0	1	0
3.05	4.31	107	1	1	0	1	0	1	1
3.20	4.53	108	1	1	0	1	1	0	0
3.37	4.76	109	1	1	0	1	1	0	1
3.56	5.03	110	1	1	0	1	1	1	0
3.76	5.32	111	1	1	0	1	1	1	1

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
4.00	5.66	112	1	1	1	0	0	0	0
4.27	6.03	113	1	1	1	0	0	0	1
4.57	6.46	114	1	1	1	0	0	1	0
4.92	6.96	115	1	1	1	0	0	1	1
5.33	7.54	116	1	1	1	0	1	0	0
5.82	8.23	117	1	1	1	0	1	0	1
6.40	9.05	118	1	1	1	0	1	1	0
7.11	10.1	119	1	1	1	0	1	1	1
8.00	11.3	120	1	1	1	1	0	0	0
9.14	12.9	121	1	1	1	1	0	0	1
10.7	15.1	122	1	1	1	1	0	1	0
12.8	18.1	123	1	1	1	1	0	1	1
16.0	22.6	124	1	1	1	1	1	0	0
21.3	30.2	125	1	1	1	1	1	0	1
32.0	45.3	126	1	1	1	1	1	1	0
64.0	90.5	127	1	1	1	1	1	1	1

Notes: 5) In Modes 1, 3, and 4: Q = 64/(128-N)
6) In Mode 2, the listed Q values are those of Mode 1 multiplied by $\sqrt{2}$. Then Q = 90.51/(128-N)

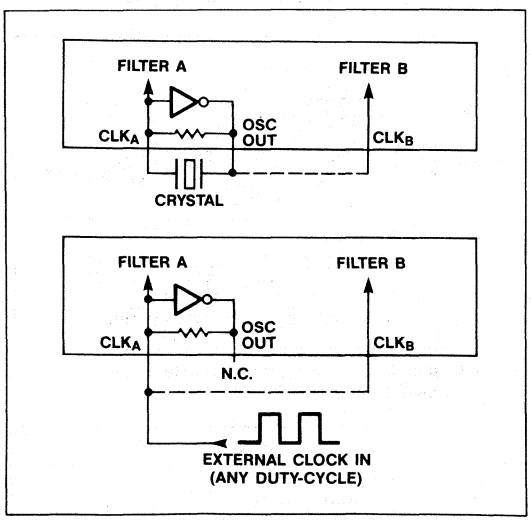


Figure 3. Clock Input Connections

Oscillator and Clock Inputs

The clock circuitry of the MAX263/64/67/68 can operate with a crystal or an external clock generator as shown in Figure 3. The duty cycle of the clock at CLK_A and CLK_B is unimportant because the input is internally divided by two to generate the sampling clock for each filter section. It is important to note that this internal division also halves the sample rate when considering aliasing and other sampled system phenomenon.

Shutdown Mode

The filter enters a shutdown mode when all Q inputs, Q0-Q6, are tied low. When shut down, power consumption with ±5V supplies typically drops to 25mW. When reactivating the filter after shutdown, allow 2ms to return to full operation.

Filter Operating Modes (MAX263/264 Only)

The MAX263/264's filter sections can be configured in four basic "Modes" as selected by inputs M0 and M1 (see Table 4). The MAX267/68 operates only in Mode 1. A fifth mode, 3A, uses an external op amp and resistors but is selected the same way and uses the same internal configuration as Mode 3.

Figures 4 through 8 show symbolic representations of the MAX263/64 filter modes. Only one second-order section is shown in each case, however the f_0, Q, and Mode select inputs are common to both halves of the IC. The f_0, f_N (notch), Q, and various output gains for each mode are shown in Table 4.

Filter Mode Selection

All operating modes listed in this section can be used with the MAX263/64. The MAX267/28 bandpass filter operates only in Mode 1.

MODE 1 (Figure 4) is useful when implementing all-pole lowpass and bandpass filters such as Butterworth, Chebyshev, Bessel, etc.. It can also be used for notch filters, but only second-order notches because the relative pole and zero locations are fixed. Higher order notch filters require more latitude in f_0 and f_N, which is why they are more easily implemented with Mode 3A.

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Table 4. Filter Modes for Second-Order Functions—MAX263/264 (MAX267/268 = MODE 1, BP only)

MODE	M1, M0	FILTER FUNCTIONS	f_0	Q	f_N	H_{OLP}	H_{OBP}	H_{ON1} ($f \rightarrow 0$)	H_{ON2} ($f \rightarrow f_{CLK}/4$)	OTHER
1	0, 0	LP, BP, N	SEE TABLE 2	SEE TABLE 3	f_0	-1	-Q	-1	-1	
2	0, 1	LP, BP, N			$f_0\sqrt{2}$	-0.5	$-Q/\sqrt{2}$	-0.5	-1	
3	1, 0	LP, BP, HP				-1	-Q			$H_{OHP} = -1$
3A	1, 0	LP, BP, HP, N			$f_0\sqrt{\frac{R_H}{R_L}}$	-1	-Q	$+\frac{R_G}{R_L}$	$+\frac{R_G}{R_H}$	$H_{OHP} = -1$
4	1, 1	LP, BP, AP				-2	-2Q			$H_{OAP} = -1$ $f_Z = f_0$, $Q_Z = Q$

Notes: f_0 = Center Frequency
f_N = Notch Frequency
H_{OLP} = Lowpass Gain at DC
H_{OBP} = Bandpass Gain at f_0
H_{OHP} = Highpass Gain as f approaches $f_{CLK}/4$
H_{ON1} = Notch Gain as f approaches DC
H_{ON2} = Notch Gain as f approaches $f_{CLK}/4$
H_{OAP} = Allpass Gain
f_Z, Q_Z = f and Q of Complex Pole Pair

Mode 1, along with Mode 4, supports the highest clock frequencies (see Table 1) because the input summing amplifier is outside the filter's resonant loop (Figure 4). The gain of the lowpass and notch outputs is 1, while the bandpass gain at the center frequency is Q. For bandpass gains other than Q, the filter input or output can be scaled by a resistive divider or op amp. In multiple feedback filters, the gain is set by the feedback resistors.

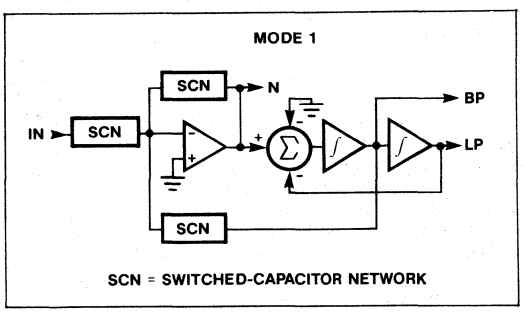

Figure 4. Filter Mode 1: Second-Order Bandpass, Lowpass and Notch

MODE 2 (Figure 5) is used for all-pole lowpass and bandpass filters. Key advantages compared to Mode 1 are higher available Qs (see Table 3) and lower output noise. Mode 2's available f_{CLK}/f_0 ratios are $\sqrt{2}$ less than with Mode 1 (see Table 2) so a wider overall range of f_0s can be selected from a single clock when both modes are used together.

MODE 3 (Figure 6) is the only mode which produces high-pass filters. The maximum clock frequency is somewhat less than with Mode 1 (see Table 1).

MODE 3A (Figure 7) uses a separate op amp to sum the highpass and lowpass outputs of Mode 3, creating a separate notch output. This output allows the notch to be set independently of f_0 by adjusting the op amp's feedback resistor ratio (R_H, R_L). R_H, R_L, and R_G are external resistors. Because the notch can be independently set, Mode 3A is also useful when designing pole-zero filters such as elliptics.

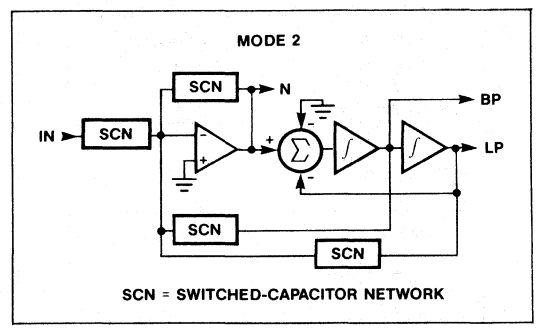

Figure 5. Filter Mode 2: Second-Order Bandpass, Lowpass and Notch

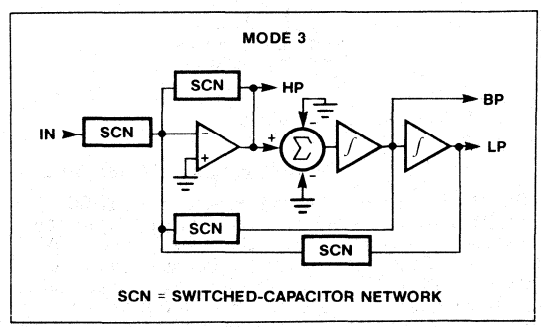

Figure 6. Filter Mode 3: Second-Order Bandpass, Lowpass and Highpass

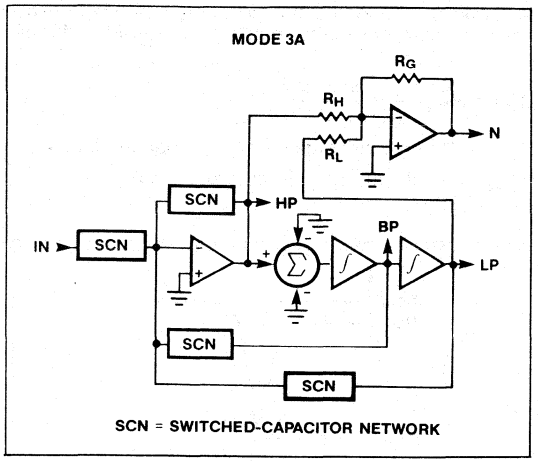

Figure 7. Filter Mode 3A: Second-Order Bandpass, Lowpass, Highpass and Notch. For elliptic LP, BP, HP and Notch, the N output is used.

MODE 4 (Figure 8) is the only mode that provides an allpass output. This is useful when implementing group delay equalization. In addition to this, Mode 4 can also be used in all pole lowpass and bandpass filters. Along with Mode 1, it is the fastest operating mode for the filter, although the gains are different than in Mode 1. When the allpass function is used, note that some amplitude peaking occurs (approximately 0.3dB when Q = 8) at f_0. Also note that f_0 and Q sampling errors are highest in Mode 4 (see Figure 17).

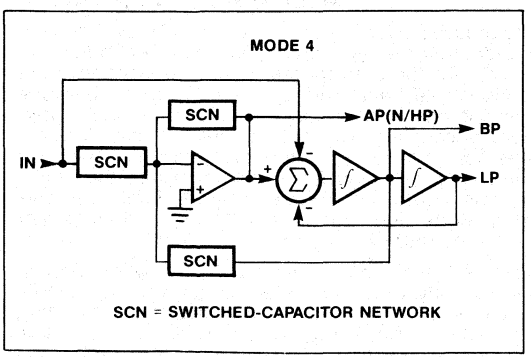

Figure 8. Filter Mode 4: Second-Order Bandpass, Lowpass and Allpass

Description of Filter Functions

The MAX263/64 performs all filter functions listed in this section. The MAX267/68 operates only as a bandpass filter.

BANDPASS (Figure 9)

For all pole bandpass and lowpass filters (Butterworth, Bessel, Chebyshev) use Mode 1 if possible. If appropriate f_{CLK}/f_0 or Q values are not available in Mode 1, Mode 2 may provide a selection that is closer to the required values. Mode 1 however has the highest bandwidth (see Table 1). For pole-zero filters such as elliptics see Mode 3A.

$$G(s) = H_{OBP}\frac{s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OBP} = Bandpass output gain at $\omega = \omega_o$

f_0 = $\omega_o/2\pi$ = The center frequency of the complex pole pair. Input-output phase shift is -180° at f_0.

Q = The quality factor of the complex pole pair. Also the ratio of f_0 to -3dB bandwidth of the second-order bandpass response.

LOWPASS See Bandpass text. (Figure 10)

$$G(s) = H_{OLP}\frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OLP} = Lowpass output gain at DC

f_0 = $\omega_0/2\pi$

HIGHPASS (Figure 11)

Mode 3 is the only mode with a highpass output. It will work for all pole filter types such as Butterworth, Bessel and Chebyshev. Use mode 3A for filters employing both poles and zeros such as elliptics.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OHP} = Highpass output gain as f approaches $f_{CLK}/4$

f_0 = $\omega_0/2\pi$

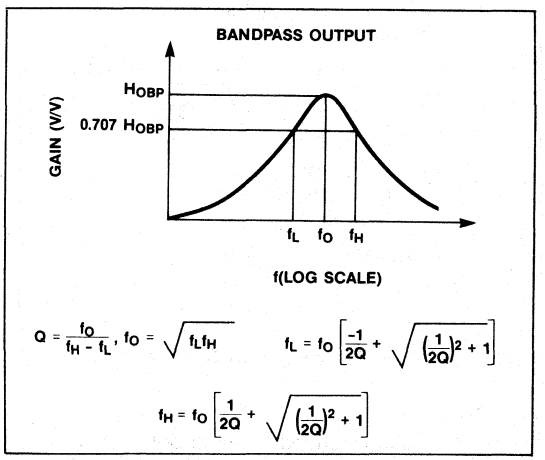

Figure 9. Second-Order Bandpass Characteristics

Pin Programmable Universal and Bandpass Filters

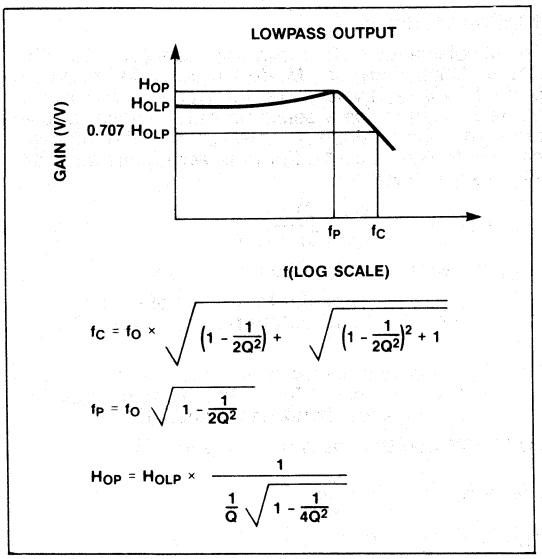

Figure 10. Second-Order Lowpass Characteristics

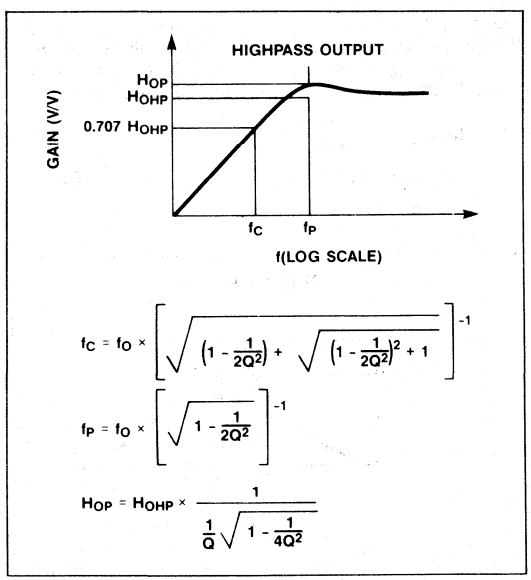

Figure 11. Second-Order Highpass Characteristics

NOTCH (Figure 12)

Mode 3A is recommended for multi-pole notch filters. In 2nd order filters, Mode 1 can also be used. The advantages of Mode 1 are higher bandwidth compared to mode 3 (Higher f_N can be implemented) and no need for external components as required in Mode 3A.

$$G(s) = H_{ON2} \frac{s^2 + \omega_n^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{ON2} = Notch output gain as f approaches $f_{CLK}/4$

H_{ON1} = Notch output gain as f approaches DC

$f_n = \omega_n/2\pi$

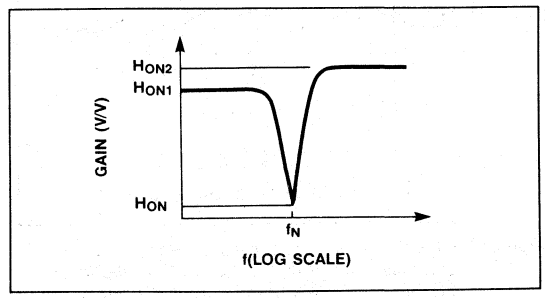

Figure 12. Second-Order Notch Characteristics

ALL PASS

Mode 4 is the only configuration in which an allpass function can be realized.

$$G(s) = H_{OAP} \frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = All pass output gain for DC < f < $f_{CLK}/4$

$f_0 = \omega_0/2\pi$

Filter Design Procedure

The procedure for most filter designs is to first convert the required frequency response specifications to f_0s and Qs for the appropriate number of second-order sections that implement the filter. This can be done by using design equations or tables in available literature, or can be conveniently calculated using Maxim's filter design software. Once the f_0 and Qs have been found, the next step is to turn them into the digital program coefficients required by the filter. An operating Mode and clock frequency (or clock/center frequency ratio) must also be selected.

Next, if the sample rate ($f_{CLK}/2$) is low enough to cause significant errors, the selected f_0s and Qs should be corrected to account for sampling effects by using Figure 17 or Maxim's design software. In most cases, the sampling errors are small enough to require no correction, i.e. less than 1%. In any case, with or without correction, the required f_0s and Qs can then be selected from Tables 2 and 3. Maxim's filter design software can also perform this last step. The desired f_0s and Qs are stated, and the appropriate digital coefficients are supplied.

Pin Programmable Universal and Bandpass Filters

Multiple Feedback Bandpass Filters

An alternate implementation of all-pole bandpass filters (i.e. Butterworth, Chebyshev) requires only one clock and common programming for all second-order sections. This can be useful with MAX26X pin-programmed filters since the two second-order halves must be programmed with the same f_{CLK}/f_0 ratio and Q (although they may use different clocks).

As shown in Figure 13, external resistors connect the outputs of cascaded filter sections to a summing op-amp at the input. Since each 2nd-order section inverts (gain = -Q) the output from odd numbered sections (except for the first) must be inverted before being fed back as in the 8th-order example in Figure 13. The MAX267/68 has an on-chip amplifier for this purpose but the MAX263/64 requires external op-amp(s).

In multiple feedback filters, the bandpass response is a function of the clock, f_{CLK}/f_0 ratio, Q, and feedback resistor ratios. In Table 5, constants for calculating resistor ratios in common bandpass configurations are listed. Maxim's filter design program "BP" also selects resistors for multiple feedback bandpass designs. A 4th-order design example (Figure 13) best illustrates how Table 5 is used.

Multiple Feedback Example

Requirements: 4th-order Chebyshev with 1 dB passband ripple, f_0 = 10kHz, and bandwidth (BW) = 2kHz.

1) The overall filter Q is $Q_F = f_0/BW = 10kHz/2kHz = 5$
2) From Table 5: $K_Q = 1.8219$
3) The Q of each 2nd-order selection is $Q_R = Q_F \times K_Q = 5 \times 1.8219 = 9.09$
4) R_F is selected, 10kΩ is a convenient value.
5) $R_2 = K_2 R_F (Q_R/2)^2 = 1.5039 \times 10k \times (9.109/2)^2 = 312k$
   In higher order filters, the general equation is: $R_N = K_N R_F (Q_R/2)^N$
6) R_0 sets the overall gain, A: $R_0 = K_0 R_F (Q_R/2)^2/A$, so for a gain of 1: $R_0 = 1.0930 \times 10k \times (9.109/2)^2/1 = 226.8k$. In higher order filters the general equation is $R_0 = K_0 R_F (Q_R/2)^M$ where M = (order of filter)/2.
7) The filter f_0 can be programmed using a wide range of clock frequencies and f_{CLK}/f_0 ratios. If f_{CLK} = 1MHz, then f_{CLK}/f_0 = 100 (code 00000 = 100.53) results in f_0 = 10kHz.
8) A 2.5pF to 10pF capacitor may be required across R_2 to prevent response peaking.

Cascading Filters

In some designs, such as very narrow band filters, several second-order sections with identical center frequency may be cascaded without multiple feedback. The total Q of the resultant filter is:

$$\text{Total } Q_T = \frac{Q}{\sqrt{(2^{1/N} - 1)}}$$

Q is the Q of each individual filter section, and N is the number of sections. In Table 5, the total Q and

Table 5. Multiple Feedback Bandpass Filter Constants

TYPE (RIPPLE)	ORDER	K0	K2	K3	K4	KQ
Butterworth	4	2.0000	4.0000			1.4142
(3.0 dB)	6	2.3704	2.6667	9.1429		1.5000
	8	2.9142	2.000	5.8284	14.315	1.5307
Chebyshev	4	1.6983	2.9512			0.8430
(0.1 dB)	6	1.3183	1.2137	4.5125		1.5473
	8	0.7986	0.5782	1.8809	2.0343	2.2176
Chebyshev	4	1.5757	2.5998			1.0378
(0.2 dB)	6	1.1128	0.9894	3.7271		1.8413
	8	0.5891	0.4551	1.4954	1.3309	2.6057
Chebyshev	4	1.3405	2.0161			1.4029
(0.5 dB)	6	0.8143	0.6897	2.6447		2.3944
	8	0.3389	0.3040	1.0114	0.6365	3.3406
Chebyshev	4	1.0930	1.5039			1.8219
(1.0 dB)	6	0.5822	0.4756	1.8475		3.0354
	8	0.1869	0.2038	0.6840	0.3002	4.1981
Chebyshev	4	0.9192	1.1934			2.1688
(1.5 dB)	6	0.4515	0.3616	1.4145		3.5705
Chebyshev	4	0.7850	0.9767			2.4881
(2.0 dB)	6	0.3641	0.2878	1.1308		4.0660
Chebyshev	4	0.6769	0.8148			2.7962
(2.5 dB)	6	0.3005	0.2353	0.9275		4.5462
Chebyshev	4	0.5875	0.6886			3.1013
(3.0 dB)	6	0.2519	0.1959	0.7739		5.0231

Pin Programmable Universal and Bandpass Filters

Table 6. Cascading Identical Bandpass Filter Sections

Total Sections	Total B.W.	Total Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Note: B = individual stage bandwidth, Q = individual stage Q.

bandwidth are listed for up to five identical second-order sections. B is the bandwidth of each section.

In high order bandpass filters that do not use multiple feedback, stages with different f_0s and Qs may also be cascaded. When this happens the overall filter gain at the bandpass center frequency is not simply the product of the individual gains because f_0s, the frequency where each section's gain is specified, is different for each second-order section. The gain of each section at the cascaded filter's center frequency must be determined to obtain the total gain.

For all-pole filters the gain, $H(f_0)$, at each second-order section's f_0 is divided by an adjustment factor, G, to obtain that section's gain, $H(f_{0BP})$, at the overall center frequency:

$H_1(f_{0BP}) = H(f_{01})/G_1$ = Section 1's Gain at f_{0BP}

$$G_1 = \frac{Q_1[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1}$$

where $F_1 = f_{01}/f_{0BP}$

G_1, Q_1, and f_{01} are the gain adjustment factor, Q, and f_0 for the first of the cascaded second-order sections. The gain of the other sections (2, 3 etc.) at f_{0BP} is determined the same way. The overall gain is:

$H(f_{0BP}) = H_1(f_{0BP}) \times H_2(f_{0BP}) \times$ etc.

For cascaded filters with zeros (f_Z) such as elliptics, the gain adjustment factor for each stage is:

$$G_1 = \frac{Q_1[F_{Z1}^2 - F_1^2]\ [(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1^2(F_{Z1}^2 - 1)}$$

where $F_{Z1} = f_{Z1}/f_{0BP}$, and F_1 is the same as above.

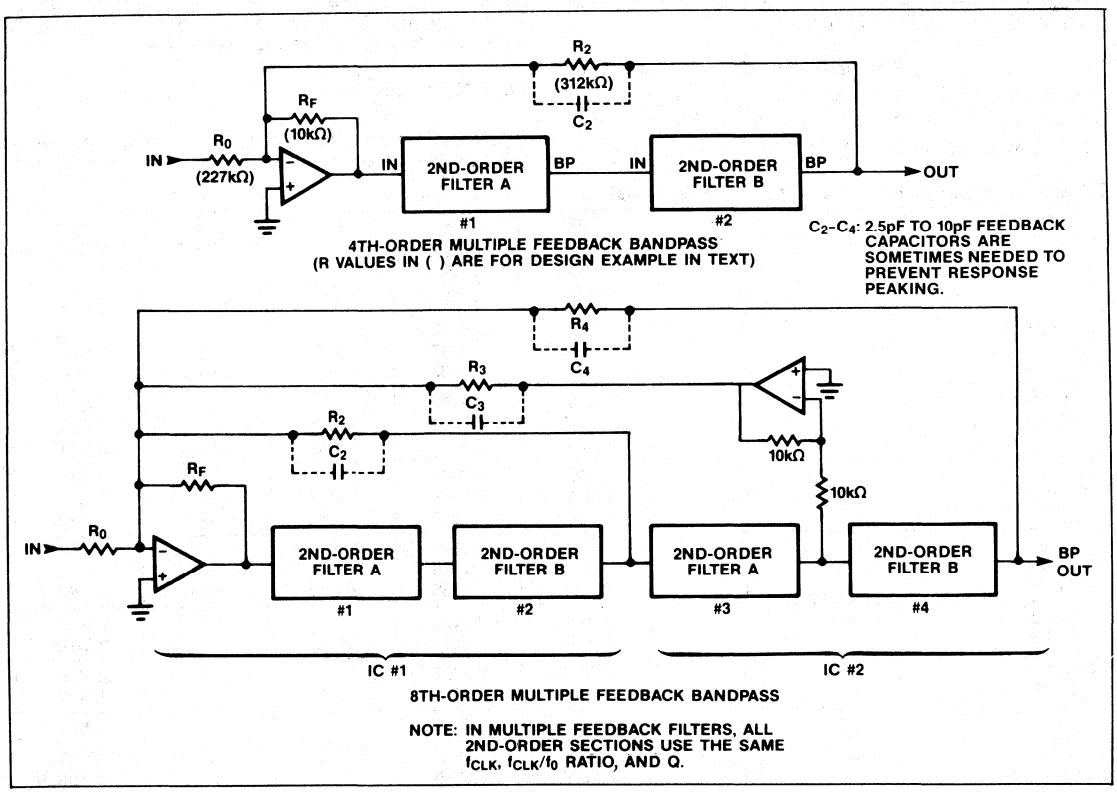

Figure 13. Multiple Feedback Bandpass Block Diagram (See Text for R Values)

Application Hints

Power Supplies

The MAX263/64/67/68 can be operated with a variety of power supply configurations including +5V to +12V single supply, or ±2.5V to ±6V dual supplies. When a single supply is used, V^- is connected to system ground and the filter's GND pin should be biased at $V^+/2$. The input signal is then either capacitively coupled to the filter input or biased to $V^+/2$. Figure 14 shows circuit connections for single supply operation.

Power consumption at ±5V is reduced if CLK_A and CLK_B are driven with ±5V, rather than TTL or 0 to 5V levels. Operation with +5V or ±2.5V power lowers power consumption but also reduces bandwidth by approximately 25% compared to +12V or ±5V supplies.

Best performance is achieved if V^+ and V^- are bypassed to ground with 4.7µF electrolytic (Tantalum is preferred.) and 0.1µF ceramic capacitors. These should be located as close to the supply pins as possible. The lead length of the bypass capacitors should be shortest at the V^+ and V^- pins. When using a single supply V^+ and GND should be bypassed to V^- as shown in Figure 14.

Output Swing and Clipping

MAX26X outputs are designed to swing to within 0.15V of each supply rail with a 10kΩ load.

To ensure that the outputs are not driven beyond their maximum range (output clipping), the peak amplitude response, individual section gains (H_{OBP}, H_{OLP}, H_{OHP}), input signal level, and filter offset voltages must be carefully considered. It is especially important to check UNUSED outputs for clipping (i.e. the lowpass output in a bandpass hookup) because overload at ANY filter stage severely distorts the overall response. The maximum signal swing with ±4.75V supplies and a 1.0V filter offset is approximately ±3.5V.

For example lets assume a fourth-order lowpass filter is being implemented with a Q of 2 using Mode 1. With a single 5V supply (i.e. ±2.5V with respect to chip GND) the maximum output signal is ±2V (w.r.t. GND). Since in Mode 1 the maximum signal is Q times the input signal, the input should not exceed ±(2/Q)V, or ±1V in this case.

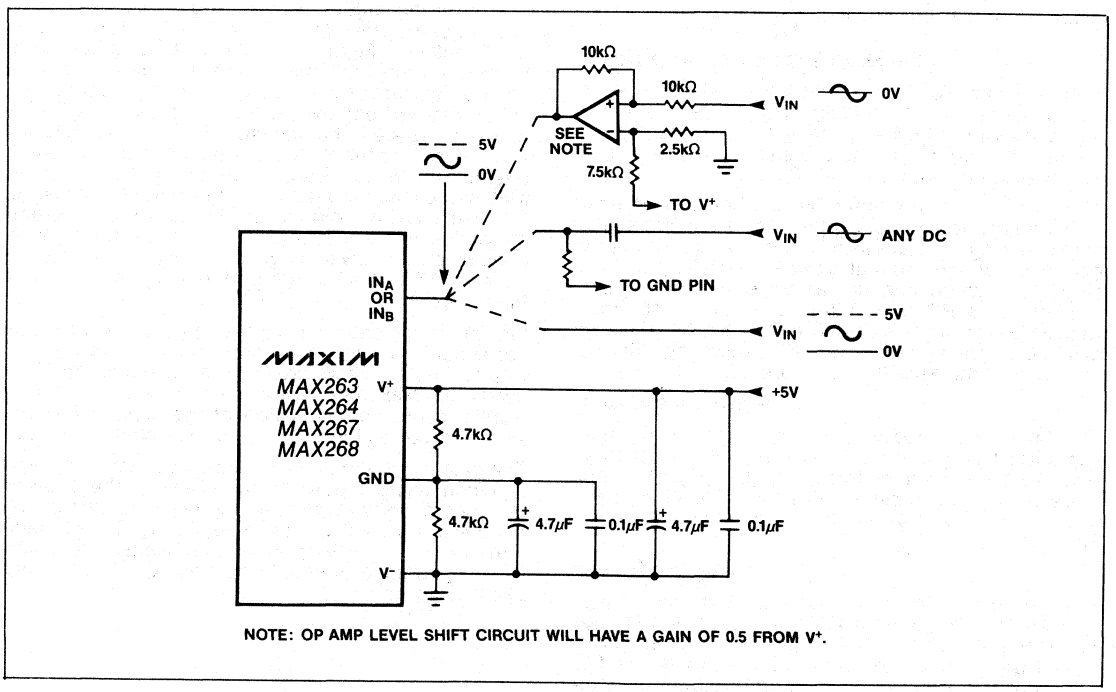

Figure 14. Power Supply and Input Connections for Single Supply Operation

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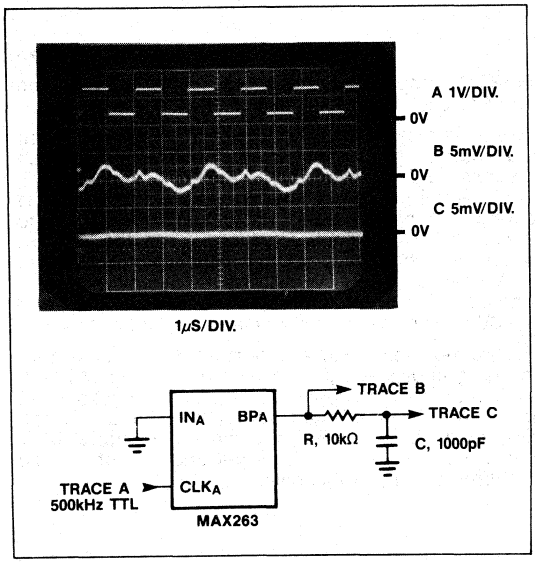


Figure 15. MAX263 Bandpass Output Clock Noise

Clock Feedthrough and Noise

Typical wideband noise for MAX26X series devices is $0.5mV_{pp}$ from DC to 100kHz. The noise is virtually independent of clock frequency. In multistage filters, the section with the highest Q should be placed first for lower output noise.

The output waveform of the MAX26X series and other switched capacitor filters appears as a sampled signal with stepping or "staircasing" of the output waveform occurring at the internal sample rate ($f_{CLK}/2$). This stepping, if objectionable, can be removed by adding a single pole RC filter. With no input signal, clock related feedthrough is approximately $8mV_{pp}$. This can also be attenuated with an RC smoothing filter as shown with the MAX263 in Figure 15.

Input Impedance

The filter input model is shown in Figure 16. Input capacitor C_A is shunted by C_B which is switched at one half the input clock frequency ($F_{CLK}/2$). The input impedance is described by: $R_{IN} = 2/(C_A \times f_{CLK})$. There is also a fixed stray capacitance of about 5pF to ground.

Digital Inputs

Filter programming is accomplished by tying input pins M0, M1, F0-F4, and Q0-Q6 to high or low voltage levels, typically V^+ and V^-. Inputs are not internally pulled up or down so these inputs must not be left unconnected. Input thresholds are guaranteed to be no higher than $V^+ -0.5V$ and no lower than $V^- +0.5V$. If pull-up resistors are used with switches at the programming inputs as might be the case in prototype breadboards, the pull-up resistors should be no more than 3.3kΩ.

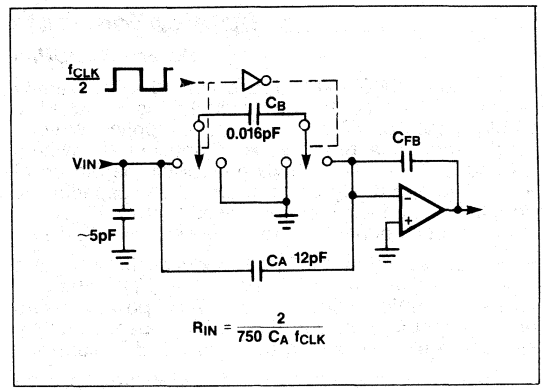


Figure 16. MAX263/64/67/68 Input Model

f_0 and Q at Low Sample Rates

When low f_{CLK}/f_0 ratios and low Q settings are selected, deviation from ideal continuous filter response may be noticeable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Figure 17 quantifies these differences. Since the errors are predictable, the graphs can be used to correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX26X series devices and in fact occur with all sampled filters. Consequently, these corrections can be applied to other switched-capacitor filters. In the majority of cases, the errors are not significant, i.e. less than 1%, and correction is not needed. However, the MAX264/68 does employ a lower range of f_{CLK}/f_0 ratios than the MAX263/67 and is more prone to sampling errors as the tables show.

Maxim's filter design software applies the previous corrections automatically as a function of desired f_{CLK}/f_0, and Q. Therefore, Figure 17 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

The data plotted in Figure 17 applies for Modes 1 and 3. When using Figure 17 for Mode 4, the f_0 error obtained from the graph should be multiplied by 1.5 and the Q error should be multiplied by 3.0. In Mode 2 the value of f_{CLK}/f_0 should be multiplied by $\sqrt{2}$ and the programmed Q should be divided by $\sqrt{2}$ before using the graphs.

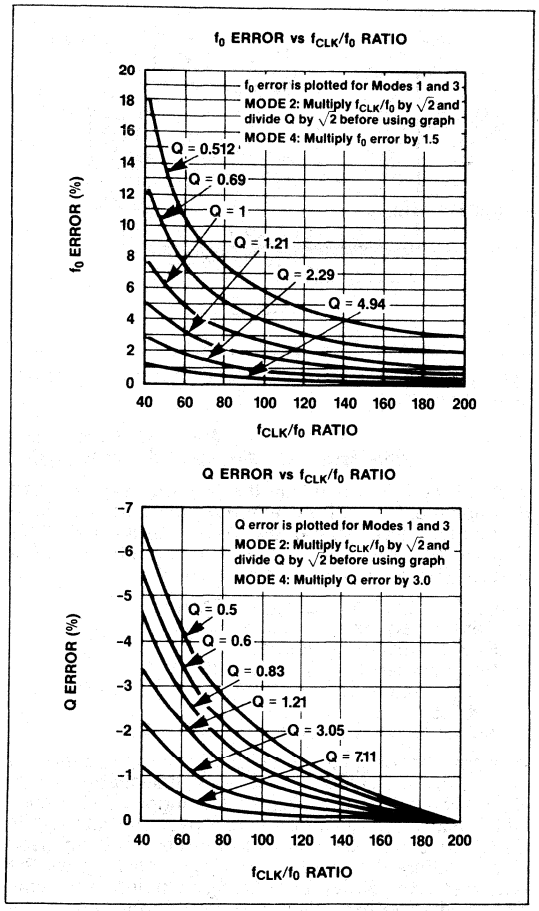


Figure 17. Sampling Errors in f_{CLK}/f_0 and Q at Low f_{CLK}/f_0 and Q Settings

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, (f_{CLK} = 200kHz) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Remember that with the MAX26X series filters, the nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can cause aliasing. In many cases the input signal itself may be band limited and require no special anti-alias filtering. The wideband MAX264/68 uses lower f_{CLK}/f_0 ratios than the MAX263/67 and for this reason is more likely to require input filtering than the MAX263 or MAX267.

Trimming DC Offset

The DC offset voltage at the LP or Notch output can be adjusted with the circuit in Figure 18. This circuit also uses the input op-amp to implement a single pole anti-alias filter. Note that the total offset will generally be less in multistage filters than when only one section is used since each offset is typically negative and each section inverts. When the HP or BP outputs are used, the offset can be removed with capacitor coupling.

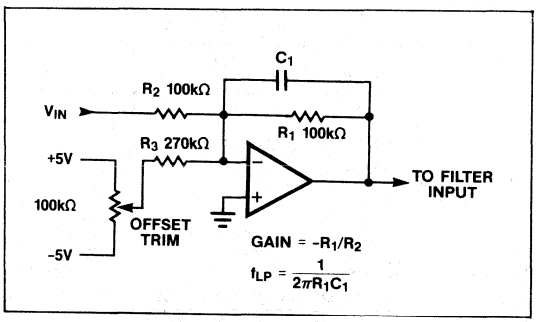


Figure 18. Circuit for DC Offset Adjustment

Design Examples

4th-Order Multiple Feedback Bandpass—MAX268

In Figure 19, a pin-programmed MAX268 operates as a 4th-order 50kHz Chebyshev bandpass. The specifications are:

Center frequency (f_0) = 50kHz
Pass bandwidth = 10kHz
Max. passband ripple = 0.1dB
Gain at center freq. = 1V/V

Two identical 2nd-order sections and the internal op amp are used with multiple feedback. The general form is as in Figure 13. Maxim's design program, BP, generates the programming codes and feedback resistor values. With a 2.5MHz crystal clock the realized parameters are:

Center frequency = 50.305kHz
Pass Bandwidth = 10.07kHz
Programmed f_{CLK}/f_0 ratio = 50.27 (N = 3)
Programmed Q = 4.27 (N = 113)
(desired Q = 4.215)
Actual Q (with error correction) = 4.21
Resistors: R_2 = 131kΩ, R_0 = 75kΩ, R_F = 10kΩ

Pin Programmable Universal and Bandpass Filters

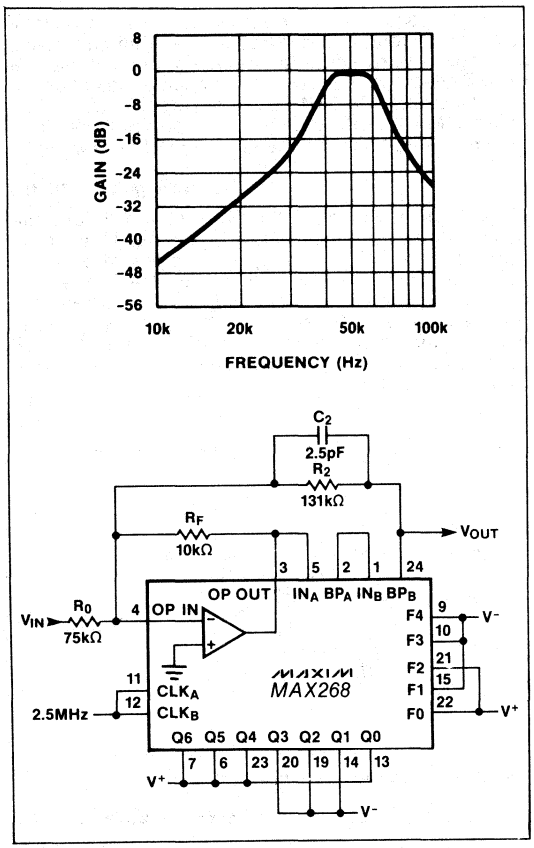


Figure 19. 4th-Order 50kHz Chebyshev Bandpass Using Multiple Feedback

Other clock rates and f_{CLK}/f_0 ratios can be chosen to implement the same filter, but larger f_{CLK}/f_0 ratios provide performance closer to the ideal. Capacitor C_2 may be needed to prevent response peaking at the passband edge. In this example C_2 = 2.5pF.

Multiple feedback can also be extended to 8th-order designs while still using one clock by adding a second MAX268 and 2 additional feedback resistors. These can also be calculated with the design program, BP. Note that for filter order above 4, the feedback signal from odd filter sections is inverted before it is summed (see Figure 13).

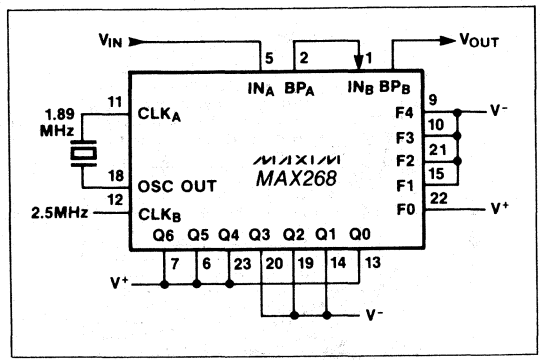


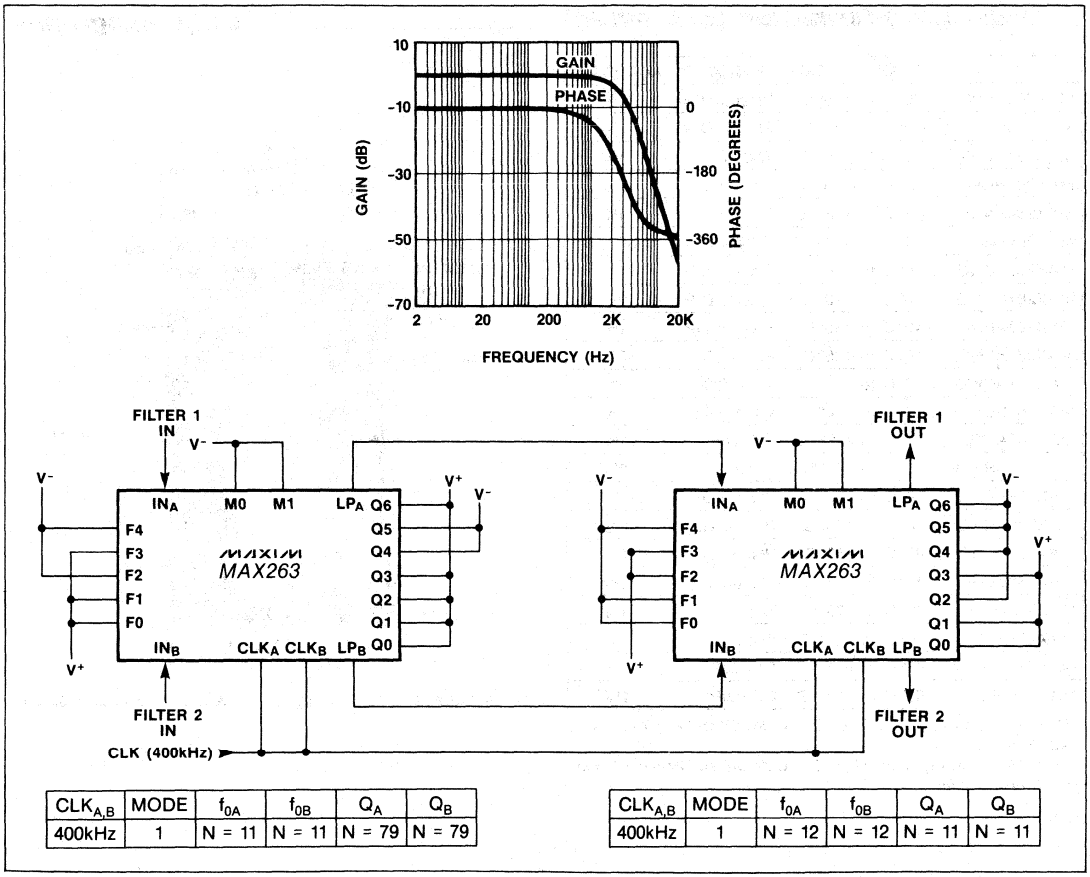
Figure 20. 4th-Order 50kHz Chebyshev Bandpass Using No External Resistors

4th-Order Bandpass (No Multiple Feedback)—MAX268

Without multiple feedback, the previous example can be implemented with no external components, however separate clocks are required for CLK_A and CLK_B (Figure 20). The target specifications are the same as before. The realized parameters are now:

CLK_A = 1.89MHz, CLK_B = 2.5MHz
Center frequency = 50kHz
Pass bandwidth = 10kHz
Programmed f_{CLK}/f_0 ratio = 43.98 (N = 1)
Programmed Q = 4.27 (N = 113) (desired Q = 4.215)
Actual Q (with error correction) = 4.2

With the chosen f_{CLK}/f_0 ratio, a crystal may be used at CLK_A while a divided system clock, if available (2.5, 5, 10, or 20MHz), drives CLK_B. This is suggested because CLK_A has internal circuitry to drive a crystal while CLK_B does not. Other clock sources may be used with a different programmed f_{CLK}/f_0 as long as the ratio between CLK_A and CLK_B remains the same as above. Another advantage of this circuit is that higher center frequencies can be achieved relative to equivalent multiple feedback designs because lower Q sections are used compared to multiple feedback.



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400kHz	1	N = 11	N = 11	N = 79	N = 79

$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
400kHz	1	N = 12	N = 12	N = 11	N = 11

Figure 21. Dual Tracking 3kHz 4th-Order Lowpass

Dual 4th-Order Tracking Lowpass—MAX263

In Figure 21, two Butterworth lowpass filters are set up to accurately track each other. By "splitting" two MAX263s only one clock is needed. The specifications are:

Cutoff frequency = 3kHz
$f_{0A} = f_{0B}$ = 3kHz
Q_A = 1.307, Q_B = 0.541

These values can be programmed directly into the filter. However, since the Qs are low, sampling errors may be large enough to deserve attention. From Figure 17, if f_{CLK}/f_0 is near 130 (f_{CLK} is 400kHz), f_{0A} and f_{0B} will be about 4% and 1.5% high respectively. Q_A and Q_B will be 1.2% and 0.5% low. These errors may not be large enough to worry about but are corrected here (within the programming resolution of the MAX263) by the filter design programs PZ and MPP. f_{0A} and f_{0B} are programmed to different values (N_A = 11, N_B = 12) for this reason.

Mode 1, $CLK_A = CLK_B$ = 400kHz
f_{CLK}/f_{0A} = 135.08, N = 11
(target f_{0A} = 2961Hz, actual = 3008Hz)
f_{CLK}/f_{0B} = 138.23, N = 12
(target f_{0B} = 2894Hz, actual = 3015Hz)
Q_A = 1.31, N = 79 (actual Q_A = 1.30)
Q_B = 0.547, N = 11 (actual Q_A = 0.542)

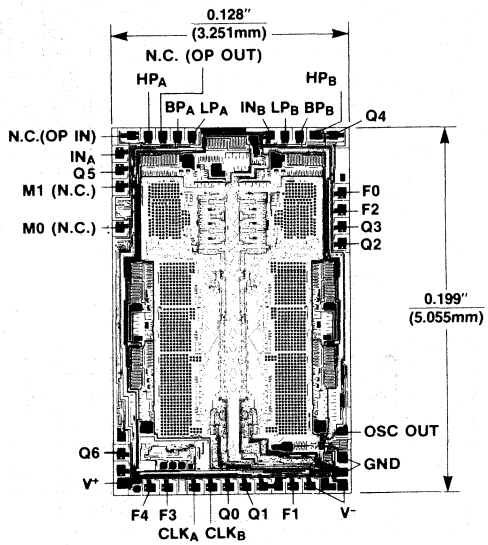
Pin Programmable Universal and Bandpass Filters

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX264AEPI	-40°C to +85°C	Plastic DIP	1%
MAX264BEPI	-40°C to +85°C	Plastic DIP	2%
MAX264ACWI	0°C to +70°C	Wide SO	1%
MAX264BCWI	0°C to +70°C	Wide SO	2%
MAX264AMJI	-55°C to +125°C	CERDIP	1%
MAX264MBJI	-55°C to +125°C	CERDIP	2%
MAX267ACNG	0°C to +70°C	Plastic DIP	1%
MAX267BCNG	0°C to +70°C	Plastic DIP	2%
MAX267AENG	-40°C to +85°C	Plastic DIP	1%
MAX267BENG	-40°C to +85°C	Plastic DIP	2%
MAX267ACWG	0°C to +70°C	Wide SO	1%
MAX267BCWG	0°C to +70°C	Wide SO	2%
MAX267AMRG	-55°C to +125°C	CERDIP	1%
MAX267BMRG	-55°C to +125°C	CERDIP	2%
MAX268ACNG	0°C to +70°C	Plastic DIP	1%
MAX268BCNG	0°C to +70°C	Plastic DIP	2%
MAX268AENG	-40°C to +85°C	Plastic DIP	1%
MAX268BENG	-40°C to +85°C	Plastic DIP	2%
MAX268ACWG	0°C to +70°C	Wide SO	1%
MAX268BCWG	0°C to +70°C	Wide SO	2%
MAX268AMRG	-55°C to +125°C	CERDIP	1%
MAX268BMRG	-55°C to +125°C	CERDIP	2%

** MAX263/264 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" wide SO (Small Outline).*
MAX267/268 packages are 24-pin 0.3" wide DIP and 24-pin 0.3" wide SO (Small Outline).

Chip Topography



NOTE: LABELS IN PARENTHESES ( ) ARE FOR MAX 267/268 ONLY

MAXIM

Resistor/Pin Programmed Universal Active Filters

General Description

The MAX265 and MAX266 switched-capacitor active filters are designed for precision filtering applications. Each contains two independent, second-order building blocks which can be configured as a lowpass, highpass, bandpass, notch or allpass filter by adding a few external resistors. Any of the classical filter configurations (Butterworth, Chebyshev, elliptic, etc.) can be built. Two uncommitted op amps are included on chip.

Separate clock input pins are provided for both second-order filter blocks. The clock source can be either a crystal or external clock input. The center or cutoff frequency (f_{CLK}/f_0 ratio) is set by a 6-bit pin-strapped programming input and with resistors.

The MAX265 operates with center frequencies up to 40kHz and while the MAX266 operates with f_0s to 140kHz by employing a lower range of f_{CLK}/f_0 ratios. The filters operate with supplies ranging from ±2.37V to ±6.3V as well as a single +5V power. The MAX265/266 is supplied in 28-pin wide DIP and small outline packages. All devices are available in commercial, extended, and military temperature ranges.

Applications

Sonar and Avionics Instruments

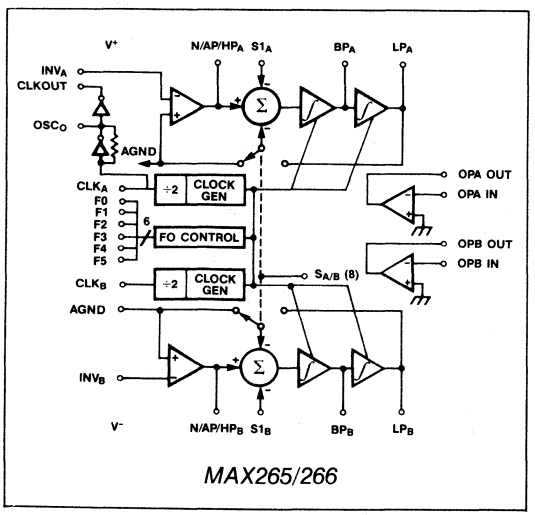
Anti-Aliasing Filters

Digital Signal Processing

Vibration and Audio Analysis

Telecommunications Test Equipment

Block Diagram



MAX265/266

Features

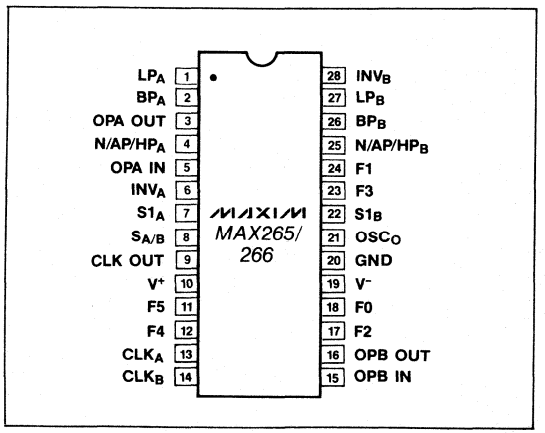
- ◆ Filter Design Software
- ◆ 64-Step Frequency Control
- ◆ Resistor Adjustment of Frequency
- ◆ 140kHz Center Frequency Range (MAX266)
- ◆ Single +5V and ±5V Operation

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX265ACPI	0°C to +70°C	Plastic DIP	1%
MAX265BCPI	0°C to +70°C	Plastic DIP	2%
MAX265AEPI	-40°C to +85°C	Plastic DIP	1%
MAX265BEPI	-40°C to +85°C	Plastic DIP	2%
MAX265ACWI	0°C to +70°C	Wide SO	1%
MAX265BCWI	0°C to +70°C	Wide SO	2%
MAX265AMJI	-55°C to +125°C	CERDIP	1%
MAX265BMJI	-55°C to +125°C	CERDIP	2%
MAX266ACPI	0°C to +70°C	Plastic DIP	1%
MAX266BCPI	0°C to +70°C	Plastic DIP	2%
MAX266AEPI	-40°C to +85°C	Plastic DIP	1%
MAX266BEPI	-40°C to +85°C	Plastic DIP	2%
MAX266ACWI	0°C to +70°C	Wide SO	1%
MAX266BCWI	0°C to +70°C	Wide SO	2%
MAX266AMJI	-55°C to +125°C	CERDIP	1%
MAX266BMJI	-55°C to +125°C	CERDIP	2%

* *MAX265/266 packages are 28-pin 0.6" wide DIP and 28-pin 0.3" Wide SO (Small Outline).*

Pin Configuration



MAXIM

Dual Universal Switched Capacitor Filter

General Description

The MF10 is a dual 2nd order, switched capacitor, state variable filter. Each of the two filter sections uses two switched capacitor integrators and an op amp to generate a second order function. The location of the poles (and thus the center frequency and Q) is determined by the frequency of an external clock and 2 to 4 external resistors. No external capacitors are used.

Each of the two filter sections of the MF10 can generate all standard 2nd order functions: bandpass, lowpass, highpass, notch (band-reject), complex zeroes and allpass functions. Three of these functions are simultaneously available. The frequency of the 2nd order poles is accurate to ±0.2% and the Q is accurate to within 2%.

Fourth order filters can be made by cascading the two 2nd order filter sections of the MF10, and higher order filters can easily be made by cascading more MF10s. The excellent accuracy and stability of MF10 based filters eliminates the complex, costly tuning normally required in the production of high order (multipole) filters. Design equations for Butterworth, Bessel, Chebyshev, and Cauer (Elliptic) filters are provided.

Features

- **No External Capacitors Required**
- **Low Sensitivity to External Component Variation**
- **Excellent Frequency and Q Stability**
- **Easily Cascaded for Multipole Filters**
- **Filter Frequency Set by External Clock Frequency**
- **0.2% Clock to Center Frequency Ratio Accuracy**
- **Highpass, Lowpass, Bandpass, Notch, and Allpass Filter Functions.**
- **Up to 3 Simultaneous Filter Function Outputs**
- **Up to 30kHz Operation**
- **Easy to use—Design Directly from the Data Sheet**
- **Monolithic, Low Power CMOS Design**

Applications

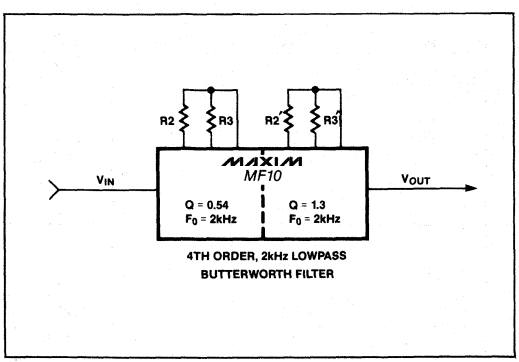
This versatile device is used for a wide range of filtering applications such as:

Tunable active filters
Multi-pole filters
Anti-aliasing filters
Adaptive Filtering
Phase locked loops
Signal Processing/ Conditioning

Ordering Information

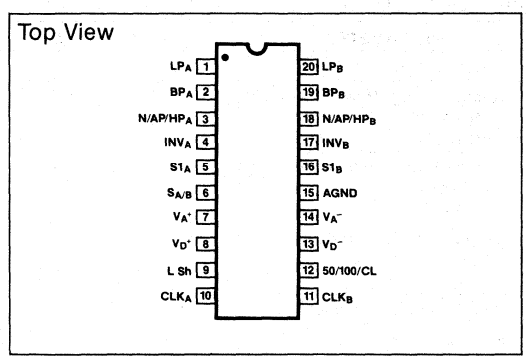
PART	TEMP. RANGE	PACKAGE
MF10BD	0°C to +70°C	20 Lead CERDIP
MF10BN	0°C to +70°C	20 Lead Plastic DIP
MF10CD	0°C to +70°C	20 Lead CERDIP
MF10CN	0°C to +70°C	20 Lead Plastic DIP

Typical Operating Circuit



4TH ORDER, 2kHz LOWPASS BUTTERWORTH FILTER

Pin Configuration



Dual Universal Switched Capacitor Filter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 14V
Power Dissipation 500mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Complete Filter)

(V_S = ±5V, T_A = +25°C)

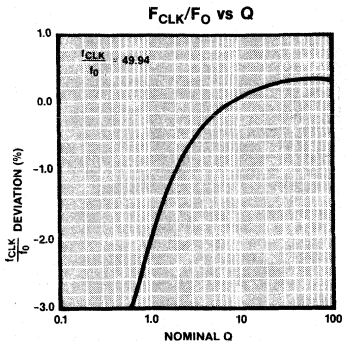
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_o \times Q \leq 200$ kHz	20	30		kHz
Clock to Center Frequency Ratio, f_{CLK}/f_o					
MF10BN	Pin 12 High, Q = 10		49.94 ± 0.2%	±0.6%	
MF10CN	$f_o \times Q \leq$ 50kHz, Mode 1		49.94 ± 0.2%	±1.5%	
MF10BN	Pin 12 at Mid Supplies		99.35 ± 0.2%	±0.6%	
MF10CN	Q = 10, $f_o \times Q \leq$ 50kHz, Mode 1		99.35 ± 0.2%	±1.5%	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)	$f_o \times Q \leq$ 50kHz $f_o \leq$ 5kHz, Mode 1		±2%	±6%	
f_o Temperature Coefficient	Pin 12 High (~50:1) Pin 12 Mid Supplies (~100:1) $f_o \times Q \leq$ 100kHz, Mode 1 External Clock Temperature Independent		±10 ±100		ppm/°C ppm/°C
Q Temperature Coefficient	$f_o \times Q \leq$ 100kHz, Q Setting Resistors Temperature Independent		±500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 10kΩ		±1	±2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			7	10	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps)

(V_S = ±5V, T_A = +25°C)

PARAMETER	CONDITIONS	MIN	Typ	MAX	UNITS
Supply Voltage		±4	±5		V
Voltage Swing (Pins 1, 2, 19, 20)	R_L = 5kΩ				
MF10BN		±4.0	±4.1		V
MF10CN		±3.8	±3.9		V
Voltage Swing (Pins 3 and 18)	R_L = 3.5kΩ				
MF10BN		±4.0	±4.1		V
MF10CN		±3.8	±3.9		V
Output short Circuit Current					
Source			3		mA
Sink			1.5		mA
Gain Bandwidth Product			2.5		MHz
Slew Rate			7		V/μS

Dual Universal Switched Capacitor Filter



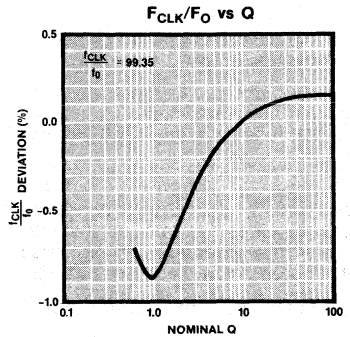


Table 1. PIN DESCRIPTION

PIN NAME	PIN NUMBER Filter A	PIN NUMBER Section B	DESCRIPTION
LP	1	20	These are the lowpass, bandpass, and notch/allpass/highpass outputs of each 2nd order section. The LP and BP outputs can typically sink 1mA and source 3mA. The N/AP/HP output can typically sink 1.5mA and source 3mA.
BP	2	19	
N/AP/HP	3	18	
INV	4	17	INV is the inverting input of the summing op amp of each filter.
S1	5	16	This is an alternate signal input pin used in modes 1A, 4, 5 and 6B. This pin must be driven with a low source impedance.
$S_{A/B}$	6		The $S_{A/B}$ input controls a switch connecting one of the inputs of the filter's 2nd summer — either to analog ground ($S_{A/B}$ low) or to the low pass output ($S_{A/B}$ high). The $S_{A/B}$ input controls the configuration of both sections of the MF10.
V_A^+	7		Analog and digital positive supply inputs.
V_D^+	8		These pins are internally connected through the MF10's substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source.
LSh	9		Level shift pin. This pin controls the digital input threshold level of the clock inputs, CLK_A and CLK_B. With the level shift pin at 0V and with ±5V power supplies, the clock inputs are TTL compatible. With the level shift pin connected to V_D^- the clock input thresholds are approximately 2V above V_D^-.

PIN NAME	PIN NUMBER Filter A	PIN NUMBER Section B	DESCRIPTION
CLK	10	11	Clock inputs for each switched capacitor building block. The duty cycle should be close to 50% to allow the op amps the maximum time to settle, particularly when the clock frequency is above 200kHz.
50/100/CL	12		This three-level input pin selects one of three MF10 operating conditions. When the 50/100/CL pin is connected to V_D^+ the ratio between clock frequency and center frequency is 50:1. With this pin at mid supplies (i.e., analog ground with dual supplies) the clock frequency to center frequency ratio is 100:1. Tying the pin low activates a simple current limiting circuitry which halts normal filtering operation and reduces the supply current by 70%.
V_D^-	13		Analog and digital negative supply inputs. These pins are internally connected. V_A^- and V_D^- should be derived from the same power supply source.
V_A^-	14		
AGND	15		Analog Ground. This pin should be connected to the system ground for dual supply operation or driven to mid supply for single supply operation. The non-inverting inputs of the filter op amps are internally connected to the AGND pin, therefore AGND should be well bypassed.

Dual Universal Switched Capacitor Filter

Definition of Terms

f_{CLK}: The frequency applied to the switched capacitor filter external clock input.

f_0: The center frequency of the second order complex pole pair, f_0, is determined by measuring the peak response frequency at the bandpass output.

Q: "Quality factor", or Q, is the ratio of f_0 to the -3dB bandwidth of the second order bandpass filter. Q also determines the amount of amplitude peaking at the lowpass and highpass outputs, but is not measured at these outputs.

H_{OBP}: The gain in V/V of the bandpass output at $f=f_0$. See Figure 1.

H_{OLP}: The gain in V/V of the lowpass output as $f \rightarrow 0Hz$, See Figure 2.

H_{OHP}: The gain in V/V of the highpass output at $f = f_{CLK}/2$. See Figure 3.

Q_Z: The quality factor of the 2nd order function complex zero pair, if any.

f_z: The center frequency of the 2nd order complex zero pair. If f_z is different from f_0, and Q_Z is high, f_z can be observed as a notch frequency at the allpass output.

f_{notch}: The frequency of minimum amplitude response at the notch output.

H_{OCZ1}: The complex zero output gain as $f \rightarrow 0Hz$.

H_{OCZ2}: The complex zero output gain at $f = f_{CLK}/2$.

H_{ON1}: The notch output gain as $f \rightarrow 0Hz$.

H_{ON2}: The notch output gain at $f = f_{CLK}/2$.

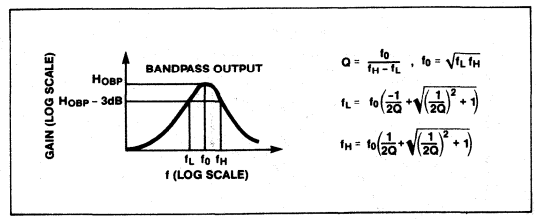


Figure 1. Bandpass Filter Terminology

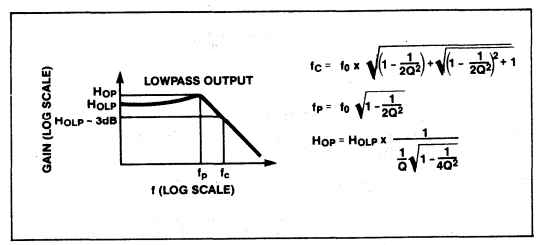


Figure 2. Lowpass Filter Terminology

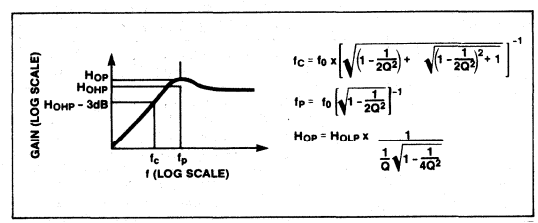


Figure 3. Highpass Filter Terminology

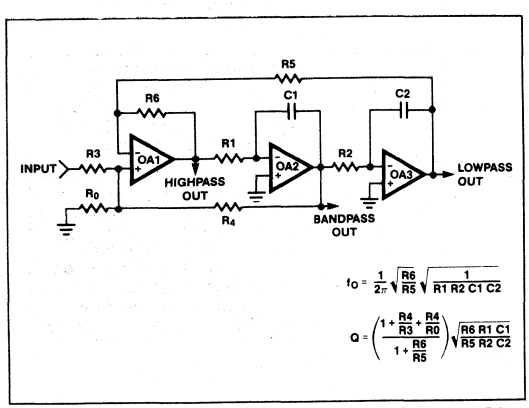


Figure 5. The Universal State Variable 2nd Order Active Filter Using RC Integrators

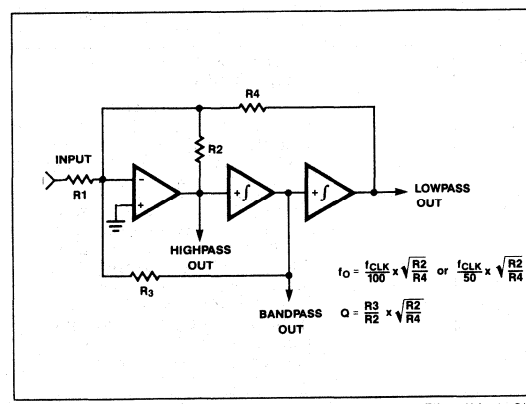


Figure 6. MF10 Universal State Variable 2nd Order Active Filter (Mode 3)

Dual Universal Switched Capacitor Filter

General Description

The MF10 is a switched capacitor (sampled data) filter. While the time domain approach most accurately describes the MF10's transfer functions, time domain calculations are cumbersome and most circuit designers are more familiar with the frequency domain approach used in designing RC active filters. Fortunately, the MF10 closely emulates RC active filters when the sampling frequency is much higher than the frequency band of interest. The operation of the MF10 can then be described in terms of the frequency domain with reasonable accuracy. Specifically, each of the two sections of an MF10 can be treated as a second order state variable filter. The similarity between the MF10 and the classic state variable filter allows the use of the extensive literature available on the design of 2nd order state variable filters.

The RC second order state variable filter (Figure 5) requires 3 op amps, 7 resistors, and 2 capacitors. This filter lacks the frequency stability and tunability of the MF10 switched capacitor filter. The MF10 excels in these areas because the center frequency of a switched capacitor filter is determined by the frequency of the clock, which, if crystal controlled, can achieve a stability of a few parts per million over the entire operating temperature range. Having the center frequency controlled by an external digital clock frequency also simplifies tuning of the filter since it is easier to accurately control a variable modulo divider than it is to precisely vary the time constant of an RC integrator.

The MF10's maximum guaranteed operating clock frequency is 1MHz, corresponding to a 20kHz maximum filter center frequency with a 50:1 clock to center frequency ratio, and a 10kHz maximum center frequency with a 100:1 clock to center frequency ratio.

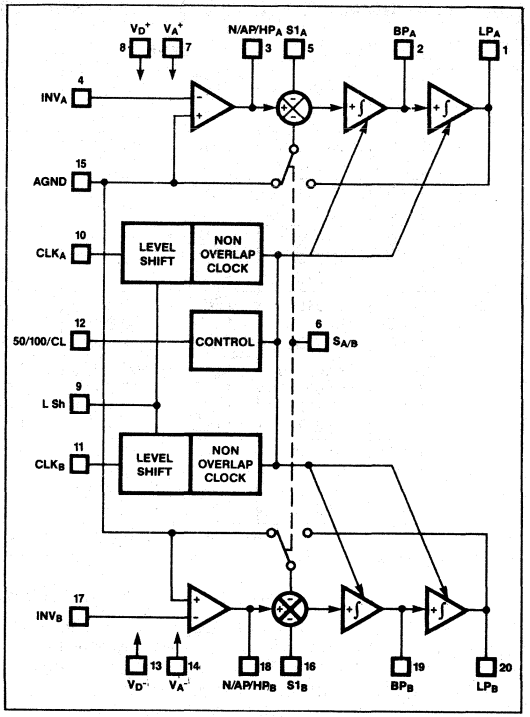


Figure 4. Block Diagram of the MF10

Filter Design

Simple 2nd Order Bandpass Filter Design

All modes except mode 6 offer a 2nd order bandpass response. The simplest circuit, mode 1A uses only two external resistors, but is limited to low Q operation by output swing limitations. Mode 1 uses three resistors and is suitable for either low or high Q bandpass functions. The center frequency of modes 1 and 1A is determined solely by the external clock frequency. Modes 2 and 3 are also suitable for bandpass filters, and are easier to implement in some applications since the center frequency is controlled by both the external clock frequency and a resistor ratio. See Table 2.

Second order bandpass filter functions are characterized by Q, center frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 2 and 3 only, determine the value of R4 using the available external clock frequency and the selected value for R2. (The center frequency of mode 1 and 1A is determined solely by the external clock frequency.)

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Table 2. MODE SELECTION

FILTER TYPE	MODE
Lowpass	1, 1A, 2, 3, 3A, 4, 5, 6A, 6B
Highpass	3, 3A, 6A
Bandpass	1, 1A, 2, 3, 3A, 4, 5
Notch	2, 3A, 5 (Complex Zero)
Allpass	4, 5

Dual Universal Switched Capacitor Filter

Table 3A. NORMALIZED LOWPASS FILTER PARAMETERS

NUMBER OF POLES	BUTTERWORTH		BESSELL		CHEBYSHEV					
					0.1dB RIPPLE		0.5dB RIPPLE		2dB RIPPLE	
	fn	Q	fn	Q	fn	Q	fn	Q	fn	Q
2	1.0	0.707	1.274	0.577	1.820	0.767	1.231	0.864	0.907	1.129
3	1.0	Real Pole	1.325	Real Pole	0.969	Real Pole	0.625	Real Pole	0.369	Real Pole
	1.0	1.000	1.450	0.691	1.300	1.341	1.069	1.706	0.941	2.552
4	1.0	0.541	1.432	0.522	0.789	0.619	0.597	0.705	0.471	0.929
	1.0	1.307	1.606	0.806	1.153	2.183	1.031	2.941	0.964	4.594
5	1.0	Real Pole	1.505	Real Pole	0.539	Real Pole	0.362	Real Pole	0.218	Real Pole
	1.0	0.618	1.559	0.564	0.797	0.915	0.690	1.178	0.627	1.775
	1.0	1.618	1.758	0.917	1.093	3.282	1.018	4.545	0.976	7.232
6	1.0	0.518	1.607	0.510	0.513	0.599	0.396	0.684	0.316	0.902
	1.0	0.707	1.692	0.611	0.834	1.332	0.768	1.810	0.730	2.844
	1.0	1.933	1.908	1.023	1.063	4.633	1.011	6.513	0.983	10.462
7	1.0	Real Pole	1.687	Real Pole	0.377	Real Pole	0.256	Real Pole	0.155	Real Pole
	1.0	0.555	1.719	0.532	0.575	0.846	0.504	1.092	0.461	1.646
	1.0	0.802	1.82	0.661	0.868	1.847	0.823	2.575	0.797	4.115
	1.0	2.247	2.053	1.126	1.045	6.233	1.008	8.842	0.987	14.280
8	1.0	0.510	1.781	0.506	0.382	0.593	0.297	0.677	0.238	0.892
	1.0	0.601	1.835	0.560	0.645	1.183	0.599	1.611	0.572	2.533
	1.0	0.900	1.956	0.711	0.894	2.453	0.861	3.466	0.842	5.584
	1.0	2.563	2.192	1.226	1.034	8.082	1.006	11.530	0.990	18.687

The normalized frequencies for the Butterworth and Bessel filters are for a -3dB frequency of 1Hz. The Chebyshev and Elliptic normalized frequencies are for filters whose amplitude response passes from the ripple band to the stopband at 1Hz.

Simple Lowpass Filter Design

Use mode 6 or 6A if a single pole lowpass filter is desired (such as the odd pole in an odd-ordered complex filter). Single pole resistor values are determined using the equations for modes 6 and 6A:

1) Select a value for R2, typically 10 to 100 kΩ.

2) Determine R3, using the selected value of R2, the available external clock frequency, and the desired cutoff frequency.

3) Determine the value of R1 to obtain the desired gain.

Modes 1 and 1A, with a fixed clock to cutoff frequency, are the simplest 2nd order lowpass configurations. Modes 2 and 3 allow tuning of the cutoff frequency by either changing the clock frequency or adjusting resistor ratios.

Second order lowpass filter functions are characterized by Q, cutoff frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 2 and 3 only, determine the value of R4 using the available external clock frequency and the selected value for R2. (The cutoff frequency of mode 1 and 1A is determined solely by the external clock frequency.)

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Simple Highpass Filter Design

Use mode 3 or 3A to implement 2nd order highpass filters and mode 6 for a single pole highpass filter.

Second order highpass filter functions are characterized by Q, cutoff frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 3 and 3A, determine the value of R4 using the available external clock frequency and the selected value for R2.

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Multi-pole Filter Design

The two 2nd order filter sections of the MF10 can be cascaded to obtain a 4th order (4 pole) filter response. Several MF10s can be cascaded to get very high order filter responses. Unlike filters based on RC time constants, MF10-based filters usually do not require tuning of each section since the Q and center frequencies are precisely controlled by the external clock frequency and the ratio of external resistors.

The information included here is for the most common types of multi-pole filters: Butterworth, Bessel, Chebyshev, and Elliptic or Cauer. The design information given is for a 1Hz lowpass filter. However this filter can be transformed to any desired filter type and frequency using the following steps:

Table 3B. CAUER OR ELLIPTICAL FILTER PARAMETERS

NUMBER OF POLES	STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 1.5, PASSBAND RIPPLE = 0.5dB				STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 2.0, PASSBAND RIPPLE = 0.5db				STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 3.0, PASSBAND RIPPLE = 0.5dB			
	F_n	Q	F_z	A_{min} (dB)	F_n	Q	F_z	A_{min} (dB)	F_n	Q	F_z	A_{min} (dB)
2	1.266	0.969	1.982	8.3	1.262	0.803	2.732	13.9	1.247	0.737	4.182	21.5
3	0.767 1.072	Real Pole 2.208	1.675	21.9	0.693 1.072	Real Pole 1.859	2.27	31.2	0.653 1.070	Real Pole 1.697	3.439	42.8
4	1.03 0.687	3.922 1.087	1.592 3.478	36.2	1.031 0.641	3.32 1.13	2.143 4.992	48.6	1.031 0.615	3.032 1.159	3.3233 7.647	64.2
5	0.426 1.016 0.759	Real Pole 6.118 1.754	1.557 2.332	50.6	0.393 1.017 0.725	Real Pole 5.193 1.723	2.089 3.251	66.1	0.375 1.017 0.705	Real Pole 4.747 1.711	3.146 5.008	85.5

1) Identify the type of transfer function (lowpass, highpass, bandpass, etc.); the type of response (Butterworth, Bessel, Chebyshev, etc.); the number of poles, and the cutoff frequency.

2) Determine the normalized lowpass filter frequency and Q of each filter section, using Table 3A or 3B.

3) If a multi-pole transfer function other than lowpass is desired, perform the filter type transformation, as described below.

4) Denormalize each filter section frequency, fn, by multiplying the fn by the actual desired cutoff or center frequency.

5) Select a mode of operation for each filter section. Mode 3 is suitable for most filters, including Bessel and Chebyshev. Butterworth filters can be implemented using either mode 3 or mode 1. Elliptical filters can be implemented using modes 2 and 3A. Modes 6 and 6A provide a single, real pole needed for odd-ordered transfer functions. Allpass and complex zeroes can be generated in modes 4 and 5.

6)Select a clock frequency. The ratio of clock frequency to center frequency can be adjusted with resistor ratios in modes 2,3,5 and 6; allowing the use of any conveniently available clock frequency that is approximately 20 to 200 times the desired cutoff or center frequency.

7) Determine the resistor values for each filter section, using the design procedures given in the sections above for simple 2nd order bandpass, lowpass and highpass filters.

Tables 3A and 3B gives the normalized filter frequency and Q for each second order section of a multi-pole filter. Filters with an odd number of poles have one entry with "real pole" in the Q column. This denotes a real pole that should be implemented using mode 6 or a simple RC section.

Lowpass to Highpass Transformation.

The cutoff frequency and Q of each lowpass section is transformed using these equations:

$$f_n(\text{highpass}) = \frac{1}{f_n(\text{lowpass})}$$

$$Q(\text{highpass}) = Q(\text{lowpass})$$

Lowpass to Bandpass Transformation.

If the ratio between the upper and lower -3dB cutoff frequencies is greater than 1.5, the best way to make the desired bandpass filter is to cascade a lowpass filter and a highpass filter. The lowpass filter's cutoff frequency should be set to the desired bandpass upper cutoff frequency, and the highpass filter's cutoff frequency should be set to the desired bandpass filter lower cutoff frequency.

For very narrowband filters, several sections with identical center frequencies can be cascaded. When identical bandpass filters are cascaded, the Q of the resultant filter is

$$Q = \frac{Q}{\sqrt{2^n - 1}}$$

where Q is the Q of each individual filter section, B is the bandwidth of each individual filter section, and n is the number of identical sections cascaded. See table 4.

Table 4. CASCADING IDENTICAL BANDPASS FILTER SECTIONS

NUMBER OF IDENTICAL BANDPASS SECTIONS	BANDWIDTH	Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

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Application Hints

1) The maximum output swing is typically to within 1V of either supply rail. Check the peak amplitude response gains, H_{OBP}, H_{OLP}, H_{OHP}, and the input signal level to ensure that the outputs will not be driven beyond their maximum output swing range. This caution particularly applies to mode 1A when used with high Q values. The section labeled "Circuit Dynamics" is included in the description of each mode to clarify the relationship between the various filter parameters and the output amplitude peaking at the filter outputs. The lower Q sections of cascaded filters should precede the sections with high Q. This reduces the possibility of output clipping.

2) The absolute values of resistors are not critical, only the ratios between resistors directly affect filter operation. The absolute values must be high enough so that the output drive currents do not approach the limits of 3mA source current and 1mA sink current. At the other extreme, resistor values should not be so high that stray leakage currents and stray capacitances have a significant effect on circuit operation.

3) Selecting 100:1 operation doubles the number of samples per output cycle, and halves the number of output steps compared to 50:1 operation. On the other hand, 50:1 allows higher frequency operation (20kHz max vs. 10kHz max), and also offers better center frequency stability (±10ppm/°C vs. ±100ppm/°C).

4) The minimum frequency of operation is limited by the rate of discharge of the internal switched capacitors. The droop rate at the output of the integrators will be approximately 0.1mV/ms. This limits the lower value of clock frequency to about 100Hz for reasonable accuracy, corresponding to a center frequency of 1Hz using the 100:1 mode.

5) For the best accuracy in setting the center frequency, use the corrections shown in the Typical Operating Characteristic graphs. These graphs aid in the correction for the slight interaction between clock frequency, Q, and center frequency.

6) As with all sampled data systems, high frequency components of the input signal above half the clock rate will be aliased. In particular, input signal components with frequencies near the clock rate will generate difference frequencies that may fall within the passband of the lowpass and bandpass filters. Since the ratio of clock frequency to center frequency is approximately 50:1 or 100:1, a simple one pole passive RC filter will be sufficient filtering in many cases. In many other cases the input signal will itself be band-limited and will not require additional filtering.

7) The $S_{A/B}$ input controls the source of feedback into the three input summer of both sections of the MF10. If your design requires that the input of one section's summer be grounded and the input to the other section's summer be connected to the lowpass output, check to see if $S_{A/B}$ can be connected to V_D^- and the lowpass output connection made via the $S1_A$ (or $S1_B$) input.

8) If large input voltage signals are applied to the filter, the DC offset voltages of the MF10 may cause output clipping. For a more detailed discussion see the section on DC Offsets.

9) For best results, the positive and negative supplies should be bypased to AGND with a 10μF tantalum and 0.1μF ceramic capacitors.

Mode 1A
Non-Inverting Bandpass, Inverting Bandpass, Lowpass.

This minimum component count configuration uses only two external resistors. The peak gain at the inverting bandpass output is equal to the Q times the input voltage, so this circuit should only be used for low Q applications. The ratio of bandpass center frequency to clock frequency is fixed at either 50:1 or 100:1, as selected by the 50/100/CL input.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1$$

$$H_{OBP1} = -\frac{R3}{R2}$$

$$H_{OBP2} = 1 \text{ (non-inverting)}$$

Circuit Dynamics

H_{OBP1} = Q (this is the reason for the low Q recommendation)

$H_{OLP\ (peak)}$ = Q x H_{OLP} (for high Qs)

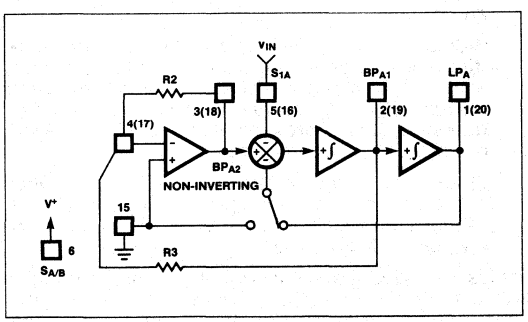


Figure 7. Mode 1A

Dual Universal Switched Capacitor Filter

Mode 1
Notch, Bandpass, and Lowpass

Like Mode 1A, f_0 is fixed at $f_{CLK}/50$ or $f_{CLK}/100$. The gain at all three outputs is inversely proportional to the value of R1; and unlike Mode 1A, high Q bandpass filters can be built without exceeding the output swing range of the bandpass output amplifier. The notch and bandpass center frequencies are identical. The notch output gain is the same above and below the notch center frequency.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_{notch} = f_0$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}(\text{as } f \rightarrow 0) = -\frac{R2}{R1}$$

$$H_{ON}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

Circuit Dynamics

$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP(peak)} = Q \times H_{OLP}$ (if the DC gain of the LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output).

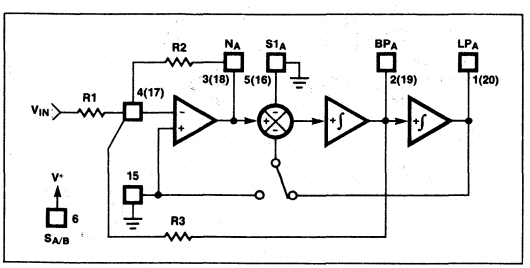


Figure 8. Mode 1

Mode 2
Notch, Bandpass, and Lowpass

The circuit of mode 2 is created by adding resistor R4 to the circuit of mode 1. This fourth resistor causes the ratio of the bandpass center frequency to clock frequency to be less than the fixed 50:1 or 100:1 ratio of mode 1. Stated another way, R4 allows the center frequency of the bandpass filter to be tuned to a higher frequency while maintaining a constant clock frequency. The notch frequency remains at $f_{CLK}/50$ or $f_{CLK}/100$, making mode 2 suitable for elliptic highpass filters, where the complex zero pair (f_{notch}) must be lower than the complex pole (f_0).

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 + \frac{R2}{R4}}$$

$$f_n = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \quad ; \quad Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

$$H_{OLP} = \frac{-\frac{R2}{R1}}{1 + \frac{R2}{R4}} \quad ; \quad H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON1}(\text{as } f \rightarrow 0) = \frac{-\frac{R2}{R1}}{1 + \frac{R2}{R4}}$$

$$H_{ON2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R_G}{R_H} \times H_{OHP}$$

Circuit Dynamics

$$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON_2}} = Q\sqrt{H_{ON_1} \times H_{ON_2}}$$

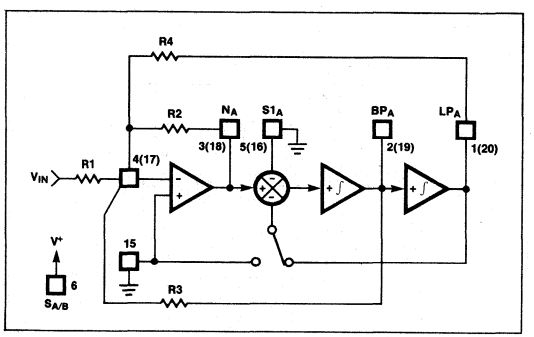


Figure 9. Mode 2

Dual Universal Switched Capacitor Filter

Mode 3
Highpass, Bandpass, and Lowpass

This mode is a sampled time (Z transform) equivalent of the classical 2nd order state variable filter. In this versatile mode, the ratio of resistors R2 and R4 can move the center frequency both above and below the $f_{CLK}/50$ and $f_{CLK}/100$ values. Mode 3 is commonly used to make multiple pole Chebyshev filters with a single clock frequency. A small (10-100pF) capacitor in parallel with R4 may be needed to avoid Q enhancement.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \quad \text{or} \quad \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

Circuit Dynamics

$$H_{OHP} = H_{OLP}\left(\frac{R2}{R4}\right)$$

$$H_{OLP(peak)} = Q \times H_{OLP}$$

$$H_{OBP} = Q\sqrt{H_{OHP} \times H_{OLP}}$$

$$H_{OHP(peak)} = Q \times H_{OHP}$$

Mode 3A
Highpass, Bandpass, Lowpass, and Notch

Similar to mode 3, this mode adds an external op amp. This op amp creates a notch output by summing the highpass and lowpass outputs of the MF10. The ratio of resistors R_H and R_L adjusts the notch frequency, while R2 and R4 adjust the bandpass center frequency. Since the notch (zero pair) frequency can be adjusted to both above and below f_0, mode 3A is suitable for both lowpass and highpass elliptic or Cauer filters. In multipole elliptic filters only one external op amp is needed. Use the inverting input of the internal op amp as the summing node for all but the final section of the filter.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}}$$

$$f_{notch} = \frac{f_{CLK}}{100} \times \sqrt{\frac{R_H}{R_L}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R_H}{R_L}}$$

$$H_{OHP} = -\frac{R2}{R1} \quad H_{OLP} = -\frac{R4}{R1} \quad H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}\ (\text{at } f = f_0) = \left|Q\left(\frac{R_G}{R_L} H_{OLP} - \frac{R_G}{R_H} H_{OLP}\right)\right|$$

$$H_{ON1}\ (\text{as } f \to 0) = \frac{R_G}{R_L} \times H_{OLP}$$

$$H_{ON2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R_G}{R_H} \times H_{OHP}$$

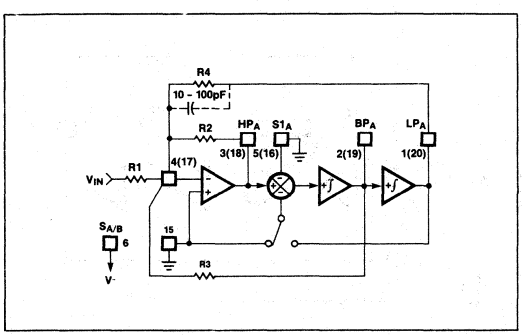


Figure 10. Mode 3

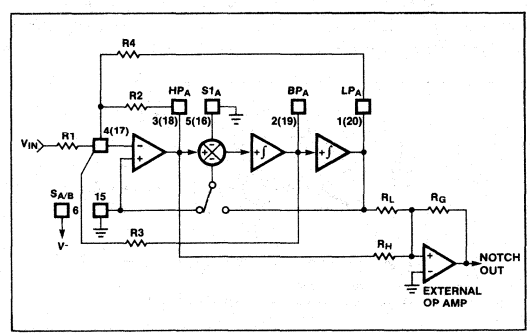


Figure 11. Mode 3A

Dual Universal Switched Capacitor Filter

Mode 4
Allpass, Bandpass, and Lowpass

Mode 4 provides an allpass output which has a nearly flat amplitude response with a phase shift that changes linearly with frequency (a constant time delay). For a flat amplitude response R2 must equal R1, fixing the allpass gain at -1.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_z (frequency of complex zero pair) = f_o

$$Q = \frac{R3}{R2}$$

Q_z (Q of complex zero pair) = $\frac{R3}{R1}$

$$H_{OAP} = -\frac{R2}{R1} = -1$$

$$H_{OLP} = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = -\left(1 + \frac{R2}{R1}\right) \times \frac{R3}{R2} = -2\frac{R3}{R2}$$

Circuit Dynamics

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q$$

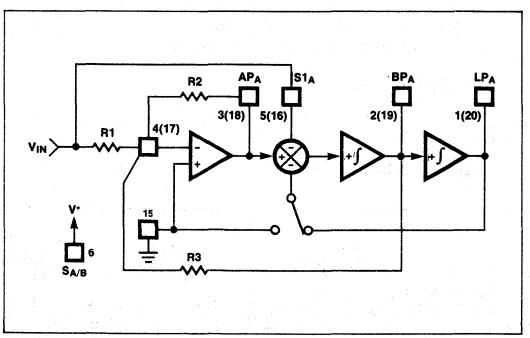


Figure 12. Mode 4

Mode 5
Complex Zero, Bandpass, and Lowpass

The addition of R4 to the circuit of mode 4 allows the independent tuning of the complex zero frequency, f_Z, and the complex pole frequency, f_0. Mode 5 can achieve a more constant allpass amplitude vs. frequency response than can be achieved with mode 4.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 + \frac{R2}{R4}}$$

$$f_z = \frac{f_{CLK}}{100} \times \sqrt{1 - \frac{R1}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 - \frac{R1}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

$$Q_z = \frac{R3}{R1} \times \sqrt{1 - \frac{R1}{R4}}$$

$$H_{OCZ1} \text{ (as } f \rightarrow 0) = \frac{R2(R4 - R1)}{R1(R2 + R4)}$$

$$H_{OCZ2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R2}{R1}$$

$$H_{OBP} = \frac{R3}{R2} \times \left(1 + \frac{R2}{R1}\right)$$

$$H_{OLP} = \frac{R4}{R1} \times \left(\frac{R2 + R1}{R2 + R4}\right)$$

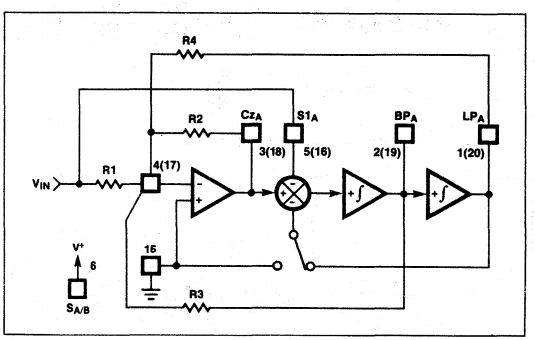


Figure 13. Mode 5

Dual Universal Switched Capacitor Filter

Mode 6A
Single Pole; Highpass and Lowpass

This circuit provides a single real pole for use in odd-ordered cascaded filters. Unlike the simple RC pole used in continuous filters, the MF10 single pole filter can be tuned by simply changing the clock frequency. The cutoff frequency is also resistor tunable.

Design Equations

$$f_c \text{ (cutoff frequency)} = \frac{f_{CLK}}{100} \times \left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50} \times \left(\frac{R2}{R3}\right)$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

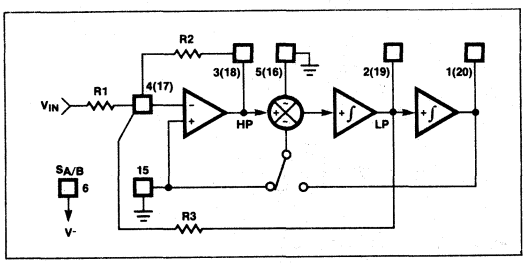


Figure 14. Mode 6A

Mode 6B
Single Lowpass Pole; Inverting and Non-Inverting

As with mode 6A, this mode is useful in implementing filters with an odd number of poles.

Design Equations

$$f_c \text{ (cutoff frequency)} = \frac{f_{CLK}}{100} \times \left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50} \times \left(\frac{R2}{R3}\right)$$

$$H_{OLP} \text{ (inverting output)} = -\frac{R3}{R2}$$

$$H_{OLP} \text{ (non-inverting output)} = +1$$

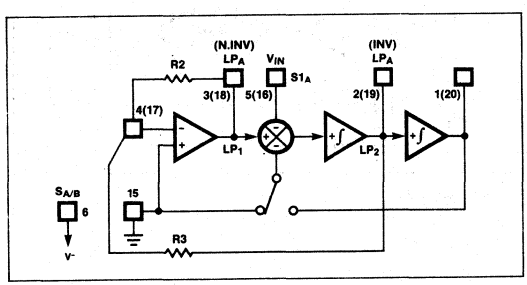


Figure 15. Mode 6B

MF10 Offsets

The MF10's switched capacitor integrators have higher equivalent input offsets than the typical RC integrator in a continuous active filter. The MF10 offsets are produced by parasitic charge injection from the switches into the integrating capacitors. These offsets are relatively independent of clock frequency and temperature. The input offset of the CMOS op amps also contribute to the overall offset error, but these offsets are small in comparison to the offsets caused by charge injection. Figure 16 shows the equivalent circuit for calculating output DC offsets.

V_{OS1} = 0 mV to ±10 mV

V_{OS2} = charge injected offset plus op amp offset
≈ -60 mV to -80 mV (50:1)

V_{OS3} = charge injected offset plus op amp offset
≈ +100 mV to +150 mV (at 50:1)

(At 100:1 the V_{OS2} and V_{OS3} are approximately doubled.)

Using the same designation for resistors as are used in Figures 7 to 15, the output offsets can be calculated as shown below.

Mode 1 and Mode 4 Output Offsets

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + |H_{OLP}|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 2 and Mode 5 Output Offsets

$$V_{OS(N)} = \left(\frac{R2}{R_p} \pm 1\right) V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

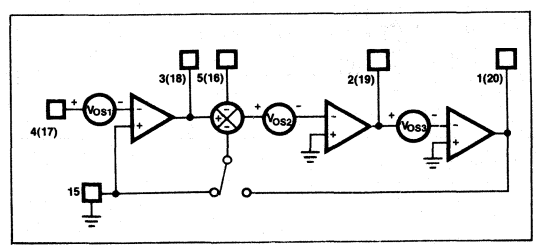


Figure 16. MF10 Offset Model

Mode 3 Output Offsets

$V_{OS(HP)} = V_{OS2}$

$V_{OS(BP)} = V_{OS3}$

$$V_{OS(LP)} = -\frac{R4}{R2} \times \left(\frac{R2}{R3} V_{OS3} + V_{OS2}\right) + \frac{R4}{R2} \times \left(1 + \frac{R2}{R_p}\right) V_{OS1}$$

$R_p = R1//R3//R4$

Mode 1A Output Offsets

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$V_{OS(INV.BP)} = V_{OS3}$

$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$

In most applications the outputs are AC coupled and the DC offsets present no problem unless large input voltages are applied to the filter.

For Mode 3 operation it should be noted that the use of small R2/R4 ratios and high Q will produce an LP output with a couple of volts DC offset and an offset adjustment should be made. Make the offset adjustment by injecting a small amount of current into the first op amp's inverting input (see Figure 17). This changes V_{OS1} but leaves the output DC offset of the integrators unchanged.

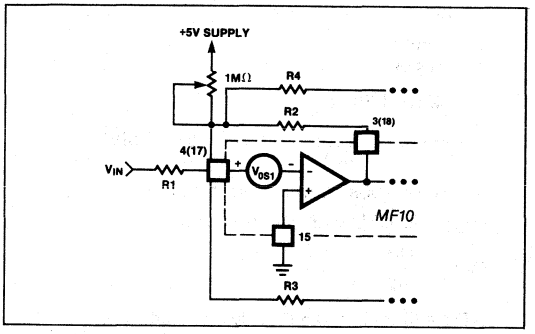


Figure 17. V_{OS} Adjustment

Application Examples

4th Order, 2kHz Lowpass Butterwoth Filter

A 4th order lowpass filter can be made by cascading the two second order filter sections of the MF10 (See Figure 18). Table 3 shows that the two sections of a Butterworth 4th order filter will have the same cutoff frequency, with one stage having a Q of 0.541 and the other stage having a Q of 1.307. Any of the modes may be used, but mode 1A uses only 2 resistors per section, and should therefore be used. The Q of both sections is low, so output clipping will not be a problem.

Using the 2nd order lowpass filter design steps shown in the Filter Design section, the resistor values for the first filter section can be calculated as follows:

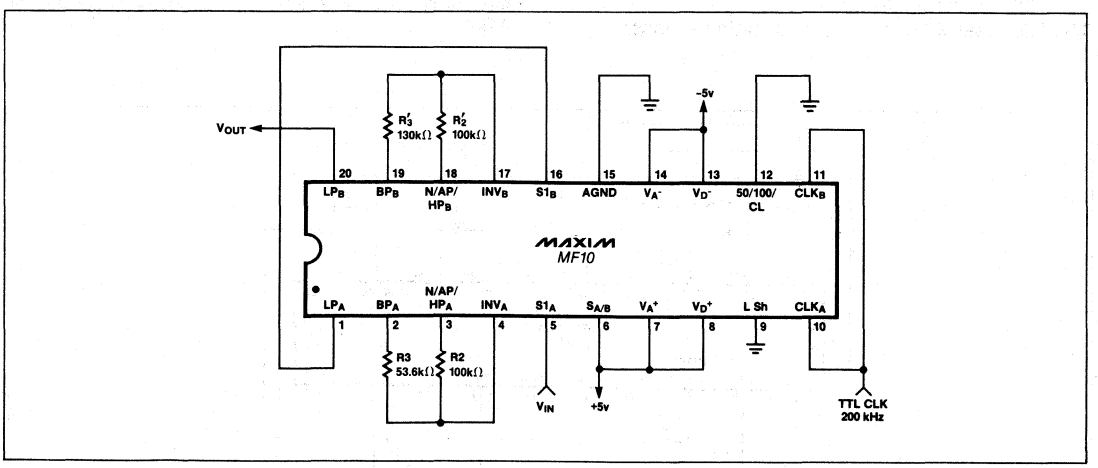


Figure 18. 4th Order, 2kHz Lowpass Butterworth Filter

Dual Universal Switched Capacitor Filter

Mode = 1A

f_0 = 2kHz
Q = 0.541

1) Let R2 be 100kΩ.

2) $f_0 = 2kHz = \frac{f_{CLK}}{100}$ (pin 12 mid-supply)

so f_{CLK} = 200kHz (pin 12 mid-supply)

f_{CLK} = 100kHz with pin 12 high.

3) $Q = \frac{R3}{R2}$;

so R3 = Q x R2 = 0.541 x 100kΩ = 54.1kΩ.

Picking the nearest 1% resistor value, R3 = 53.6 kΩ

Using similar calculations for the second filter section, R2=100kΩ and R3 = 130kΩ.

The output of the first section, LP_A (pin 1), is the input for the second stage, at $S1_B$ (pin 16). The filter output is at LP_B (pin 20). With ±5V supplies and the Level Shift pin connected to ground, the digital input threshold of the CLK inputs is about 1.6V. The CLK inputs can therefore be driven by either TTL or CMOS logic levels. The 50/100/CL pin is grounded, which selects a 100:1 ratio between the clock frequency and the lowpass cutoff frequency.

4th Order Chebyshev Lowpass Filter

Figure 19 shows a 4th order Chebyshev lowpass filter with the following specifications:

Passband Ripple = 2dB (nominal)
Cutoff Frequency = 5kHz

The filter uses a 200kHz clock for both sections.

Table 3 shows that for a 2dB ripple, 4th order Chebyshev filter the parameters of the two sections are:

f_n = 0.471 , Q = 0.929
and
f_n = 0.964 , Q = 4.594

Either mode 3 or mode 2 is suitable for this filter. The resistors for mode 2 can be calculated as follows:

1) Let R2 = 10kΩ.

2) For the first section f_n = 0.471, so for a 5kHz cutoff f_0 = 0.471 x 5kHz = 2.355kHz

Using the mode 2 equation for f_0,

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}}$$

and using 200kHz for f_{CLK}, R4 is calculated as 25.87kΩ. The closest 1% resistor value of 26.1kΩ is chosen.

3) The mode 2 formula for Q is

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

Using Q= 0.929 and the previously determined values for R2 and R4, R3 is calculated as 7.9kΩ. The closest 1% value, 7.87kΩ is used.

4) Choose R1 for the desired filter gain. In this example R1 is 10kΩ.

Repeat the above steps for the second section, with f_n = 0.964 and Q = 4.594. If R2 is chosen to be 10kΩ, the value of R4 will be 2.1kΩ and the value of R3 will be 19.1kΩ.

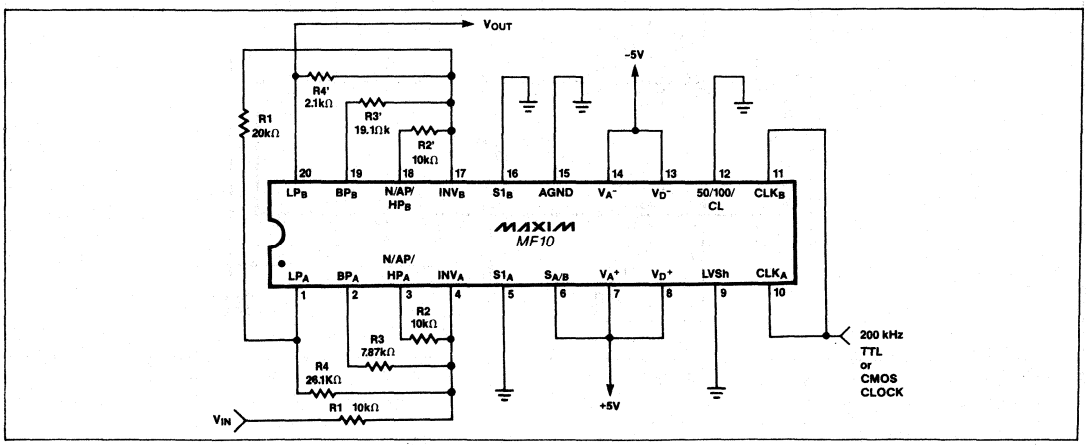


Figure 19. 4th Order Chebyshev 5kHz Lowpass Filter

Switched Capacitor Filter Fundamentals

While it is not necessary to understand the internal operation of the MF10 in order to use it, a basic understanding of switched capacitor operation may help in optimizing designs.

Figure 20 shows a standard integrator using an op amp. The time constant is determined by the passive components, R and C. When a positive input voltage is applied, the integrator output will ramp downward at a rate determined by the input voltage and the time constant, RC. This ramp has a slope of

$$\frac{\Delta V}{\Delta T} = -\frac{V_{IN}}{RC}$$

Figure 21 is a simple inverting switched capacitor integrator, where the R of the standard integrator has been replaced by a capacitor and two analog switches, S1 and S2. As S1 and S2 alternately open and close at the rate set by the clock input, first C1 is charged to the input voltage, then C1 transfers its charge into the capacitor C2. This creates a series of voltage steps on the integrator output, with each voltage step having a value of $-V_{IN}$ x C1/C2. If the value of C1 is small compared to C2, the series of steps at the integrator output approximates a ramp with the slope

$$\frac{\Delta V}{\Delta T} = -\frac{V_{IN} \times f_{CLK} \times C1}{C2}$$

where f_{CLK} is the frequency of the clock input.

This equation is similar to that of the standard integrator, but with the sampled capacitors time constant of

$$\frac{C2}{C1 \times f_{CLK}}$$

replacing the standard integrators time constant of RC. The center frequency of an RC based 2nd order state variable filter is

$$f_0 = \frac{1}{2\pi RC}$$

The center frequency of a switched capacitor 2nd order state variable filter is approximately

$$f_0 = \frac{f_{CLK} \times C1}{2\pi C2}$$

The ratio of C2/C1 in the MF10 is approximately 8 when the 50/100/CL input selects a 50:1 clock to center frequency ratio, and the ratio of C2/C1 is approximately 16 when the 50/100/CL input selects a 100:1 clock to center frequency ratio. Substituting these C2/C1 ratios in the above formula, the MF10 f_0 equation (for modes 1 and 6) results:

$$f_0 = \frac{f_{CLK}}{50} \text{ (50/100/CL Input High)}$$

or

$$f_0 = \frac{f_{CLK}}{100} \text{ (50/100/CL Input Mid-supply)}$$

The integrators used in the MF10 are non-inverting, and use the basic switching scheme of Figure 22. The switches ground one side of the input capacitor C1 when it is connected to the input; and connect the other side to ground while it is connected to the op amp's input. By changing the polarity of C1 in this manner, an additional inversion is added, and overall operation is non-inverting. This means the direction of the voltage ramp at the output of the integrator has the same polarity as V_{IN}.

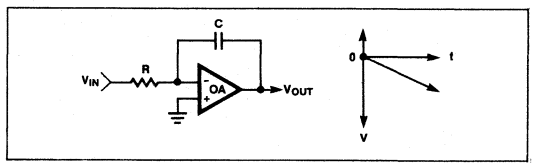


Figure 20. Typical RC integrator

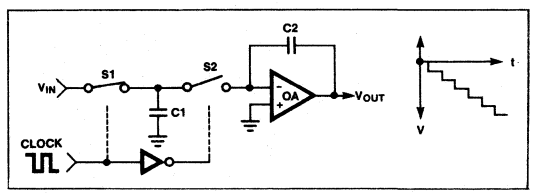


Figure 21. Simple Inverting Switched Capacitor Integrator

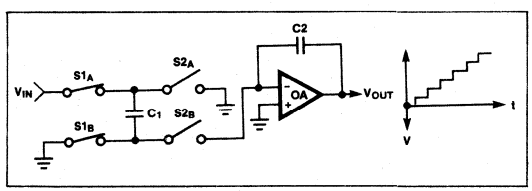
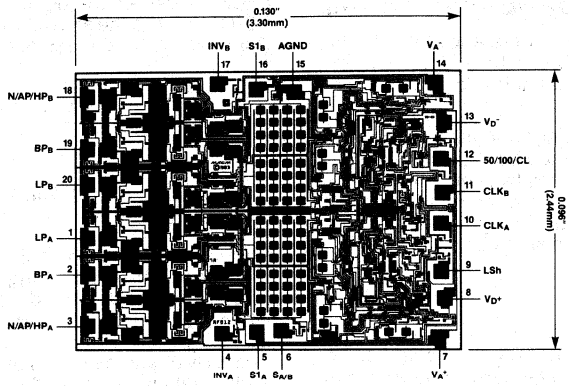


Figure 22. The Non-Inverting Integrator Used in the MF10

Dual Universal Switched Capacitor Filter

Chip Topography



Analog Multiplexers

Analog Multiplexers

Part Number	Function	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	V_{IL}/V_{IH} (V)	Analog Signal Voltage Range	Features	Page No.
MAX358	1 of 8	1500	2	1µs	0.8/2.4	-12.5V to +13.5V	Fault Protected to ±35V	11-9
MAX359	2 of 8	1500	2	1µs	0.8/2.4	-12.5V to +13.5V	Fault Protected to ±35V	11-9
DG506A	1 of 16	400	5	1µs	0.8/2.4	±15V	Industry Standard	11-21
DG507A	2 of 16	400	5	1µs	0.8/2.4	±15V	Industry Standard	11-21
DG508A	1 of 8	300	2	1µs	0.8/2.4	±15V	Industry Standard	11-27
DG509A	2 of 8	300	2	1µs	0.8/2.4	±15V	Industry Standard	11-27
HI508A	1 of 8	1500	2	1µs	0.8/2.4	-12.5V to +13.5V	Fault Protected	11-9
HI509A	2 of 8	1500	2	1µs	0.8/2.4	-12.5V to +13.5V	Fault Protected	11-9
IH5108	See MAX358							11-9
IH5208	See MAX359							11-9
IH6108	See DG508A							11-27
IH6116	See DG506A							11-21
IH6208	See DG509A							11-27
IH6216	See DG507A							11-21

Video Switching Products

Part Number	Function*	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	V_{IL}/V_{IH} (V)	Analog Signal Voltage Range	Features	Page No.
MAX310	1 of 8 Mux	250	10	1.5µs	0.8/2.4	+12/-15V	70dB Isolation at 10MHz	11-1
MAX311	2 of 8 Mux	250	10	1.5µs	0.8/2.4	+12/-15V	70dB Isolation at 10MHz	11-1
MAX453	1 of 2 Mux	Buffered Output	10	0.12µs	0.8/2.4	±2V	On-Chip Output Amp	5-29
MAX454	1 of 4 Mux	Buffered Output	10	0.12µs	0.8/2.4	±2V	On-Chip Output Amp	5-29
MAX455	1 of 8 Mux	Buffered Output	10	0.12µs	0.8/2.4	±2V	On-Chip Output Amp	5-29
IH5341	2 SPST NO	75	0.5	300	150	0.8/2.4	70dB Isolation	12-67
IH5352	4 SPST NO	75	0.5	300	150	0.8/2.4	at 10MHz	12-67

* NO – Normally Open

MAXIM
CMOS RF/Video Multiplexers

General Description

Maxim's MAX310 and MAX311 are CMOS monolithic analog multiplexer/demultiplexers designed for use with signal frequencies ranging from DC through video. The MAX310 is a 1-of-8 multiplexer while the MAX311 is for 2-of-8 (4 channel differential) applications.

A key feature of the MAX310/311 is extremely high off isolation at high frequencies. The isolation of each off channel to the output is guaranteed to be -66dB at 5MHz. The input signal range is +12V to -15V with ±15V power supplies while power consumption is typically 1.1mW.

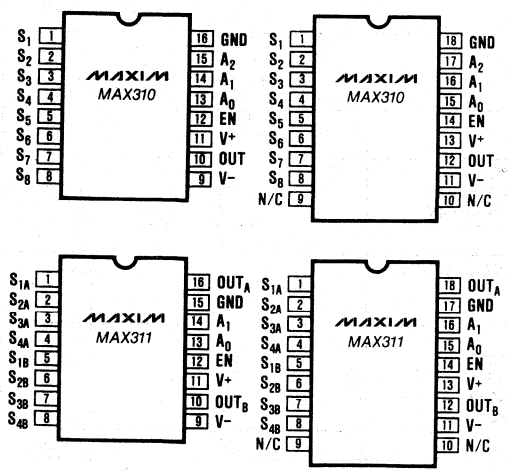
All control inputs are fully compatible with TTL and CMOS logic. Decoding is in standard BCD format and an Enable input is also provided to simplify cascading of devices. The MAX310 and MAX311 will operate with nearly any power supply combination which totals less than 36V ($V^+ - V^-$) including single supply operation at +12V, +15V, and +28V with V^- connected to GND.

Applications

Video Switching and Crosspoint Systems
Automatic Test Equipment
Medical Ultrasound Phased Array Systems
Data Logging of High Frequency Signals
Digital Signal Processing

Pin Configuration

Top View



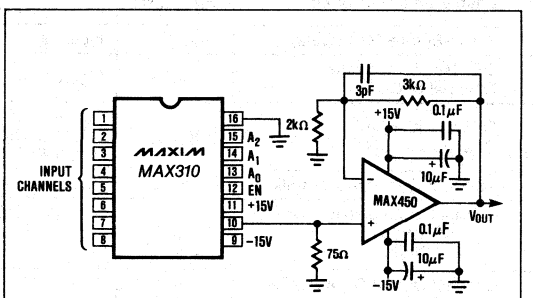
Features

- ♦ **-76dB Typical Off Isolation at 5MHz**
- ♦ **-63dB Typical "All Channel Off" Isolation at 5MHz**
- ♦ **Phase Shift Match Between Channels, <1° at 5MHz**
- ♦ **Break-Before-Make Switching**
- ♦ **Wide Supply Range, ±4.5V to ±16.5V and Single Supply**
- ♦ **Symmetrical, Bi-directional Operation**
- ♦ **Latch-Up Proof Construction**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX310C/D	0°C to +70°C	Dice
MAX310CPE	0°C to +70°C	16 Lead Plastic DIP
MAX310CWN	0°C to +70°C	18 Lead Wide SO
MAX310EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX310EWN	-40°C to +85°C	18 Lead Wide SO
MAX310EJE	-40°C to +85°C	16 Lead CERDIP
MAX310MJE	-55°C to +125°C	16 Lead CERDIP
MAX311C/D	0°C to +70°C	Dice
MAX311CPE	0°C to +70°C	16 Lead Plastic DIP
MAX311CWN	0°C to +70°C	18 Lead Wide SO
MAX311EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX311EWN	-40°C to +85°C	18 Lead Wide SO
MAX311EJE	-40°C to +85°C	16 Lead CERDIP
MAX311MJE	-55°C to +125°C	16 Lead CERDIP

Typical Operating Circuit



No Insertion Loss, 8 Channel Mux

CMOS RF/Video Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage referenced to V⁻
- V⁺ ..... +36V
- GND ..... +24V
- Digital Inputs ..... V⁻ to V⁺

Input Current
- S and COMMON OUT ..... ±50mA
- All pins except S and COM. OUT ..... ±30mA

Lead Temperature ..... +300°C
Storage Temperature ..... -65°C to +150°C

Operating Temperature Range
- MAX310C, MAX311C ..... 0°C to +70°C
- MAX310E, MAX311E ..... -40°C to +85°C
- MAX310M, MAX311M ..... -55°C to +125°C

Power Dissipation (16-Pin packages)
- CERDIP (derate 10mW/°C above +75°C) 750mW
- Plastic DIP (derate 7.35mW/°C above +75°C) 550mW
- Small Outline (derate 9mW/°C above +75°C) 550mW

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Over Temperature, V^+ = +15V, V^- = -15V, GND = 0V unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range		V^+, V^- = ±15V V^+, V^- = ±5V	-15 -5		+12 +2	V
Channel ON Resistance	R_{ON}	V_{IN} = ±5V, I_{OUT} = 10mA T_A = +25°C Over Temp.		150	250 300	Ω
ON Resistance Match	ΔR_{ON}	V_{IN} = ±5V, I_{OUT} = 10mA		6		%
OFF Input Leakage Current	$I_{S(OFF)}$	Figure 10, T_A = +25°C Over Temp		0.4 3	10 100	nA
OFF Output Leakage Current	$I_{D(OFF)}$	Figure 11, T_A = +25°C MAX310 Over Temp. MAX311 Over Temp.		0.8 20 10	10 100 50	nA
ON Channel Leakage Current	$I_{D(ON)}$	Figure 12, T_A = +25°C MAX310 Over Temp. MAX311 Over Temp.		1 30 15	10 200 100	nA
Input Low Threshold	V_{AL}	V^+/V^- = ±15V, ±5V			0.8	V
Input High Threshold	V_{AH}	V^+/V^- = ±15V, ±5V	2.4			V
Input Current (Logic)	I_A	V_A = 0V or 5V			±10	µA
Access Time	t_{ACC}	Figure 7; T_A = +25°C Over Temp.		0.6	1.5 2.0	µs
Enable Delay ON or OFF	$t_{EN(ON/OFF)}$	Figure 8; T_A = +25°C Over Temp.		0.3	1.0 2.0	µs
Break-Before-Make Delay	t_{ON}-t_{OFF}	Figure 9	30	100		ns
OFF Isolation, Single Channel to OUT	ISO_{SC}	Figure 3; T_A = +25°C	-66	-76		dB
OFF Isolation, All Channels to OUT	ISO_{AC}	Figure 4, 5, T_A = +25°C MUX Disabled, EN = +0.8V MUX Enabled, EN = +2.4V		-63 -58		dB
Adjacent Channel Crosstalk	ISO_X	Figure 6, T_A = +25°C		-72		dB
Channel Input Capacitance OFF State ON State	 $C_{S(OFF)}$ $C_{S(ON)}$	T_A = +25°C, V_{IN} = 10mV_{RMS} 10 MHz		 5 45		pF
Channel Output Capacitance OFF State ON State	 $C_{D(OFF)}$ $C_{D(OFF)}$	T_A = +25°C; EN = +0.8V, MAX310 MAX311 EN = +2.4V, MAX310 MAX311		 38 20 57 40		pF
Charge Injection	Q	Figure 13, T_A = +25°C		110		pC
Supply Current; V^+ V^-	I^+ I^-	EN, A0, A1, A2 = 0V or +5V		75 0.1	200 100	µA
Supply Voltage Range		T_A = +25°C	±4.5		±16.5	V

Detailed Description

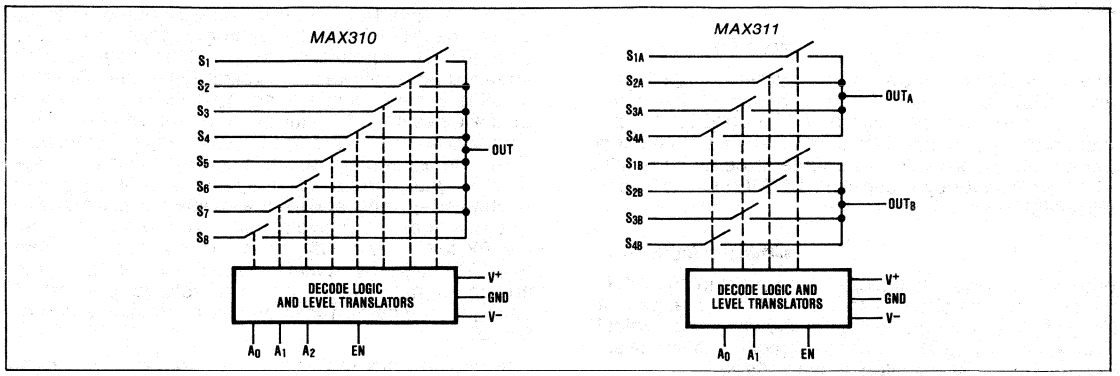


Figure 1. Functional Block Diagrams

The Maxim MAX310 and MAX311 contain 8 video switches combined with an address decoder and level translators (Figure 1). Each of the 8 video switches consists of 3 N-channel FETs configured as shown in Figure 2. This "T" configuration provides the high frequency OFF isolation required when switching wide-band video, audio, or digital signals.

N-channel FETs are used in the MAX310/311's "T" switches because of their low capacitance and consequently superior isolation characteristics. A side effect is that the N-channel ON resistance varies somewhat with the voltage difference between the analog input signal and V^+. This effect is shown in the Typical Operating Characteristics section.

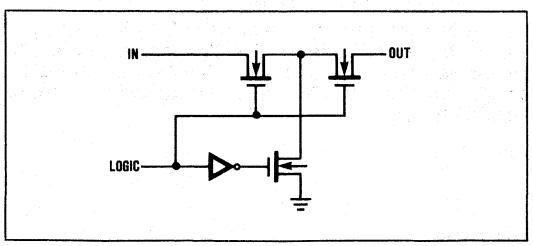


Figure 2. N-channel T Switch

Channel selection is performed by applying a binary input to the address inputs A_0, A_1 and A_2 (A_0 and A_1 only for MAX311). The address decoder selects channels as shown in the truth tables (Table 1). All digital inputs are compatible with TTL and CMOS logic levels.

Break-before-make switch timing is guaranteed for both multiplexers. This prevents momentary shorting of inputs when changing multiplexer channels.

The MAX310 and MAX311 are also fully bilateral and so can be used "backwards", as demultiplexers, with no loss in performance. Specifically, one input signal can be routed to one of several outputs.

TABLE 1. CHANNEL SELECTION INPUT CODES

MAX310					MAX311			
A_2	A_1	A_0	EN	ON Channel	A_1	A_0	EN	ON Channel
0	0	0	1	1	0	0	1	1A + 1B
0	0	1	1	2	0	1	1	2A + 2B
0	1	0	1	3	1	0	1	3A + 3B
0	1	1	1	4	1	1	1	4A + 4B
1	0	0	1	5	X	X	0	ALL OFF
1	0	1	1	6				
1	1	0	1	7				
1	1	1	1	8				
X	X	X	0	ALL OFF				

Application Hints

Maximizing Isolation

With all high frequency circuits, careful printed circuit board layout is essential for optimum performance. To maintain the high frequency isolation of the MAX310/311, signal paths should be of minimum length and ground plane should be used where possible, including between adjacent input pins. A ground or power supply trace between adjacent inputs will markedly improve isolation between channels.

Both V^+ and V^- should be bypassed to ground with 0.1μF ceramic capacitors. The leads of the capacitors should be kept as short as possible to minimize

series inductance. The bypass capacitors should also be located as physically close to the multiplexer as possible.

Input Capacitance

The capacitance of an input channel changes from about 5pF in the OFF state to around 45pF when ON. To minimize bandwidth reduction due to input capacitance, the inputs should be driven from a low impedance source. A 75Ω source impedance results in a 3dB frequency response of 47MHz when loaded with 45pF.

Charge Injection

With ±15V supplies, injected charge from the internal switch drive circuitry to the analog signal path is typically 110 picocoulombs. As shown in the Typical Characteristics graph, charge injection is relatively independent of the analog signal voltage.

Insertion Loss

With ±15V supplies and ±2V video signals, the 120Ω typical ON resistance of the MAX310/311 results in -8.3dB insertion loss when used with a 75Ω output load. This insertion loss is virtually constant from DC to over 20MHz.

TABLE 2. PHASE SHIFT AT 10MHz

INPUT CHANNEL MAX311	OUTPUT - INPUT PHASE SHIFT	
	R_L = 10kΩ	R_L = 75Ω
S_1	-22°	-12°
S_2	-21°	-11.5°
S_3	-20°	-11.5°
S_4	-20°	-11.2°
S_5	-20°	-11.2°
S_6	-20.5°	-11.4°
S_7	-20.7°	-11.5°
S_8	-20.4°	-11.5°

Test Conditions: V^+ = +15V, V^- = -15V, V_{IN} = 1.25V_{RMS} at 10MHz, OFF inputs terminated with 75Ω.

Operation with Power Supplies Other Than ±15V

Table 3 shows how different power supply voltages affect the MAX310/311's analog signal range and channel ON resistance (R_{ON}). This data is also shown graphically in the Typical Operating Characteristics section. Since N-channel FETs are used in the switches, R_{ON} is determined by the voltage difference between V^+ and the input voltage. For lowest R_{ON}, use a negative power supply (V^-) equal to the most negative input voltage, and a positive power supply (V^+) 30V above the negative supply. For example, if only positive signals need to be switched, use 0V for V^- and +30V for V^+ to achieve minimum R_{ON}. This also reduces ON resistance variation with analog signal level and input voltage dependent changes in insertion loss, which minimizes differential gain errors.

The digital input thresholds are nearly independent of V^+, remaining near +1.4V over the entire operating supply voltage range of ±4.5V to ±18V (9V to 36V single supply).

The MAX310/311 switching delay times vary somewhat with power supply voltage. Access time (see Figure 2) increases from typically 600ns with ±15V supplies to 3μs with ±5V supplies. Other switching times are also proportionately longer with ±5V power supplies.

Propagation Delay and Phase Shift

In Table 2, the typical phase shift for each channel is shown. Note that both the phase shift and the phase shift difference between channels are reduced with a 75Ω output load. At 10MHz, the channel-to-channel match is better than 1° with a 75Ω load and improves as the frequency is reduced.

Phase shift measurements for the MAX311 are similar to those in Table 2. The data for the MAX310 channels 1 to 4 corresponds to MAX311 channels 1A to 4A, Channels 5 to 8 correspond to MAX311 channels 1B to 4B.

TABLE 3. SIGNAL RANGE AND R_{ON} vs SUPPLY VOLTAGE

SUPPLY VOLTAGE		SIGNAL RANGE	TYPICAL R_{ON} AT V_{IN}	
V^-	V^+		NEGATIVE	POSITIVE
-15	+15V	-15V to +12V	104Ω at -10V	265Ω at +10V
		-5V to +5V	115Ω at -5V	150Ω at +5V
GND	+15V	0V to +12V	120Ω at 0V	150Ω at +5V
GND	+30V	0V to +27V	90Ω at 0V	100Ω at +5V
-5V	+5V	-5V to +2V	240Ω at -2V	480Ω at +2V
-10V	+10V	-10V to +7V	140Ω at -5V	220Ω at +5V
-5V	+15V	-5V to +12V	115Ω at -5V	150Ω at +5V

OFF Isolation Measurements

Figure 3 is used to test and specify the MAX310/311's single channel OFF isolation. In the case illustrated, channel S_1 has signal applied while all other inputs are grounded through 75Ω except for the ON channel (S_2 in Figure 3). This is shorted directly to ground to prevent pickup from external wiring. Each channel meets this test to an isolation limit of -66dB at 5MHz.

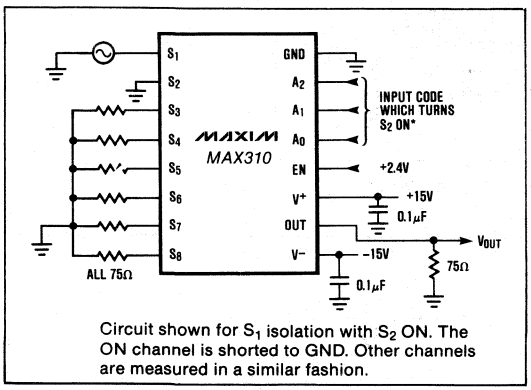


Figure 3. Single Channel OFF Isolation (ISO_{SC}) Test Circuit

Figure 4 shows the test circuit for OFF isolation with all channels driven. The impedance of the source connected to the selected channel (in this case, S_4) significantly affects feedthrough. With a 75Ω source impedance the typical measured OFF isolation is -58dB at 5MHz. This increases to -63dB if the source impedance is reduced to 10Ω or less. OFF isolation also increases with decreasing frequency. For example, when the frequency is reduced from 10MHz to 1MHz the isolation improvement is typically -20dB. Figure 5 shows a similar circuit for testing all-channel isolation with the multiplexer disabled (EN low).

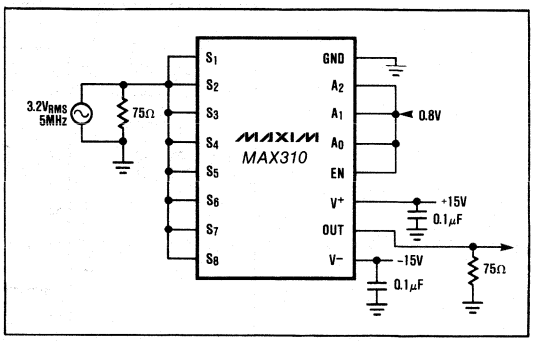


Figure 4. All Channel OFF Isolation (ISO_{AC}) Test Circuit (MUX Disabled)

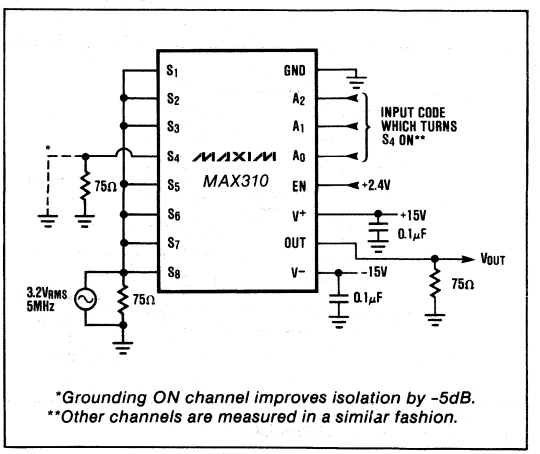
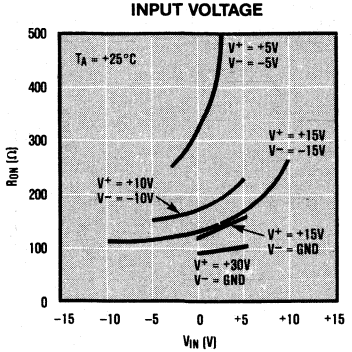


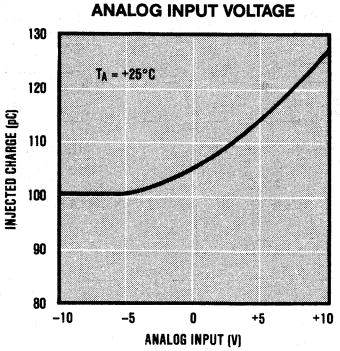
Figure 5. All Channel OFF Isolation (ISO_{AC}) Test Circuit (MUX Enabled)

Typical Operating Characteristics

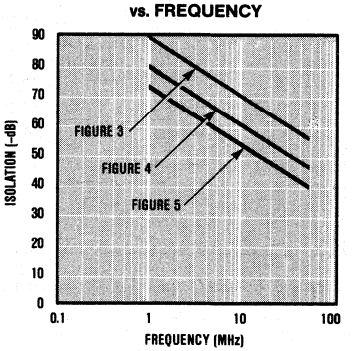
RON vs. SUPPLY VOLTAGE AND INPUT VOLTAGE



CHARGE INJECTION vs. ANALOG INPUT VOLTAGE



OFF ISOLATION vs. FREQUENCY



CMOS RF/Video Multiplexers

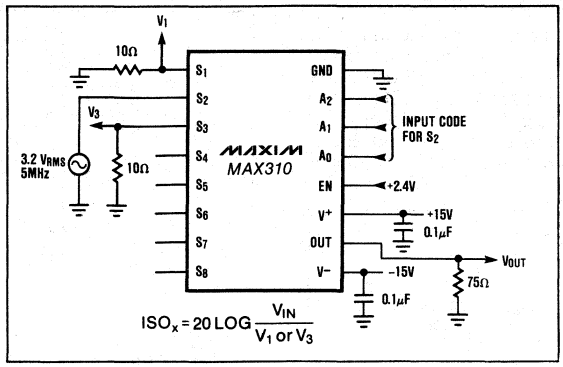
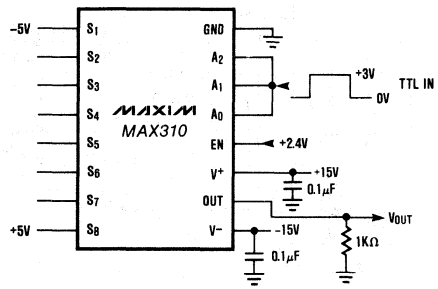
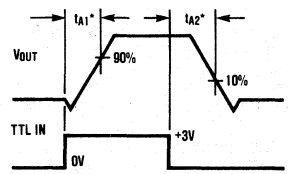


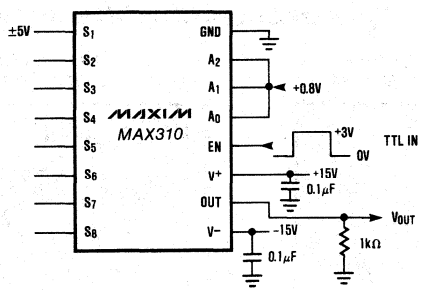
Figure 6. Adjacent Channel Crosstalk (ISO_X) Test Circuit

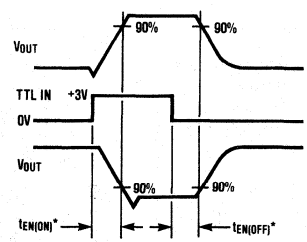




*t_A is defined as the longest of t_{A1} and t_{A2}.

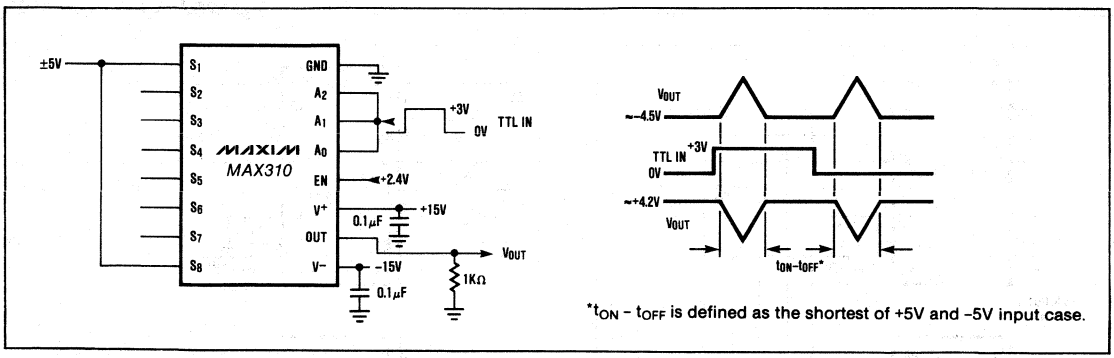
Figure 7. Access Time (t_A) Test Circuit.





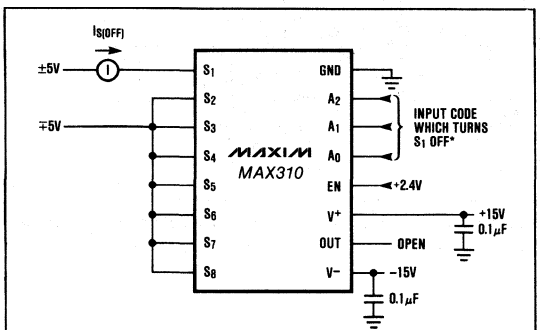
*$t_{EN(ON/OFF)}$ is defined as the longest of +5V and -5V input case.

Figure 8. Enable Delay ($t_{EN(ON/OFF)}$) Test Circuit.



*t_{ON} - t_{OFF} is defined as the shortest of +5V and -5V input case.

Figure 9. Break-Before-Make Delay (t_{ON}-t_{OFF}) Test Circuit.



*Shown for S_1. Other channels are measured in a similar fashion.

Figure 10. OFF Input Leakage Current Test Circuit.

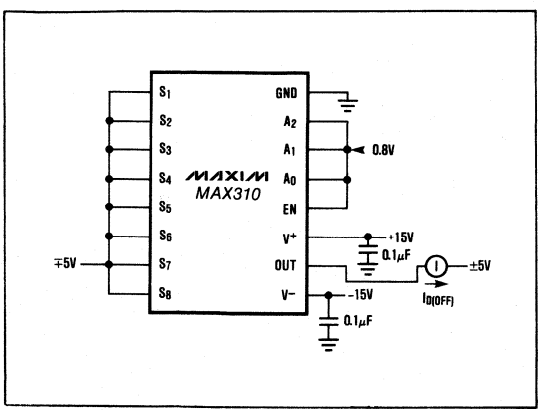
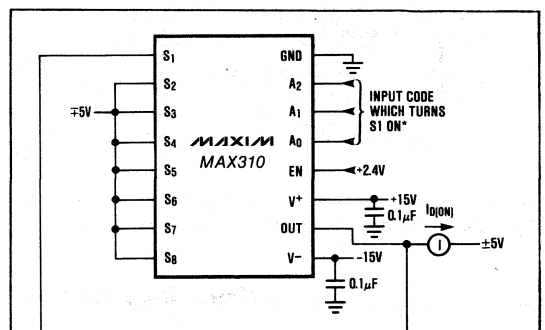


Figure 11. OFF Output Leakage Current Test Circuit.



* shown for S_1. Other channels are measured in a similar fashion.

Figure 12. ON Output Leakage Current Test Circuit.

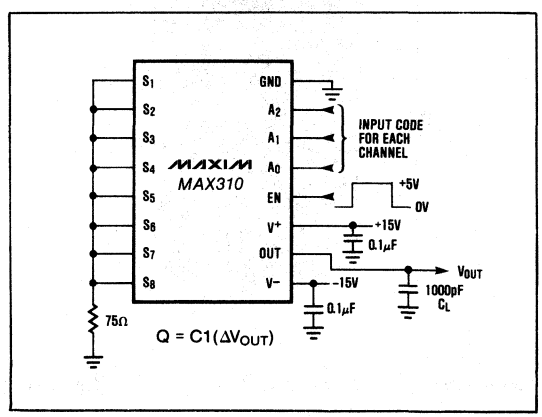


Figure 13. Charge Injection (Q) Test Circuit

CMOS RF/Video Multiplexers

Typical Applications

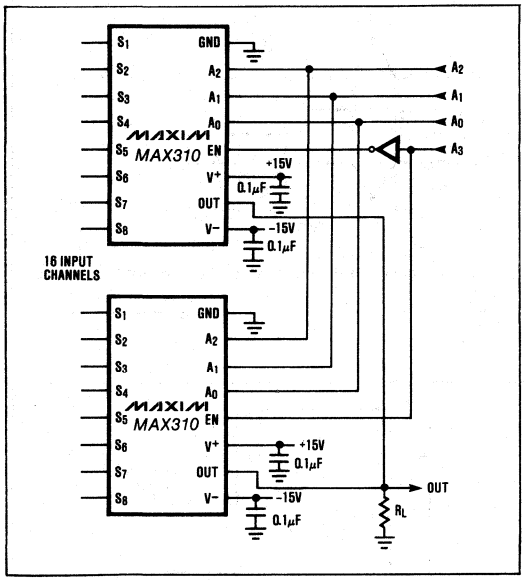


Figure 14. Cascading 2 MAX310s For 1 of 16 Multiplexer

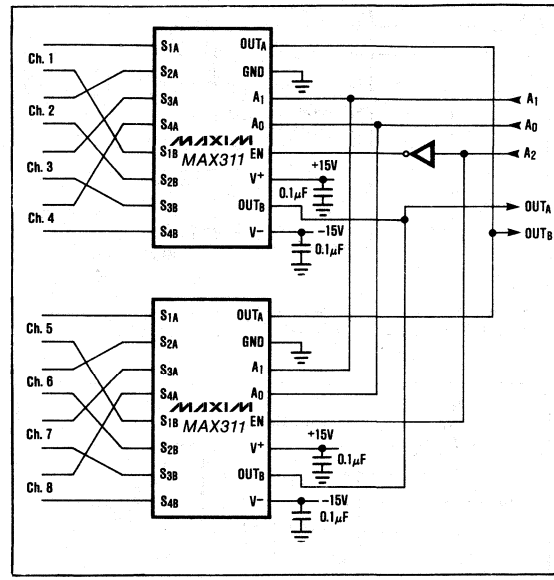
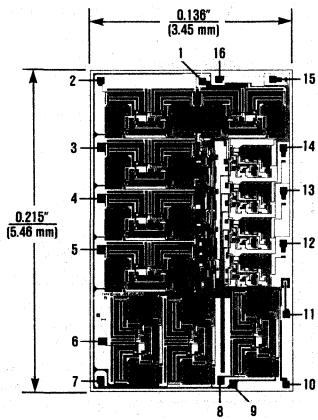


Figure 15. Cascading 2 MAX311s For 1 of 8 Differential Multiplexer.

Chip Topography



(See Pin Configurations for MAX310 and MAX311 pin functions)

MAXIM

Fault-Protected Analog Multiplexer

General Description

Maxim's HI-508A and MAX358 are 8 channel single-ended (1 of 8) multiplexers with fault protection. Maxim's HI-509A and MAX359 are 4 channel differential (2 of 8) multiplexers with fault protection. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significantly improved fault protection. If the power supplies to the Maxim fault-protected multiplexer are inadvertently turned off while input voltages are still applied, *all* channels in the multiplexer are turned off, and only a few nanoamperes of leakage current will flow into the inputs. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The Maxim series N-channel, P-channel, N-channel protection structure has two significant advantages over the simple current limiting protection scheme of the first generation fault protected multiplexers. First, the Maxim protection scheme limits fault currents to nanoamp leakage values rather than many milliamperes. This prevents damage to sensors or other sensitive signal sources. Second, the Maxim fault-protected multiplexers can withstand a *continuous* ±35V overvoltage, unlike the first generation which has a continuous overvoltage limitation of about ±10V imposed by power dissipation considerations.

All digital inputs have logic thresholds of 0.8V and 2.4V, ensuring both TTL and CMOS compatibility without requiring pullup resistors. Break-before-make operation is guaranteed. Power supply currents have been reduced and typical power dissipation is less than 2 milliwatts.

Applications

Data Acquisition Systems

Industrial and Process Control Systems

Avionics Test Equipment

Signal Routing between Systems

Features

- **Improved 2nd Source (See "Maxim Advantage" on 3rd and 5th page)**
- **All Switches Off with Power Supplies Off**
- **On Channel Turns OFF if Overvoltage Occurs**
- **Only Nanoamperes of Input Current under All Fault Conditions**
- **Latchup-proof Construction**
- **Operates from ±4.5 to ±18V Supplies**
- **All Digital Inputs are TTL and CMOS Compatible**

Ordering Information

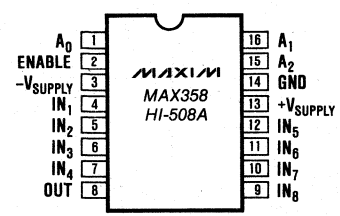
PART	TEMP. RANGE	PACKAGE
MAX358CPE	0°C to +75°C	16 Lead Plastic DIP
MAX358CWE	0°C to +75°C	16 Lead Wide SO
MAX358CJE	0°C to +75°C	16 Lead CERDIP
MAX358EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX358EWE	-40°C to +85°C	16 Lead Wide SO
MAX358EJE	-40°C to +85°C	16 Lead CERDIP
MAX358MJE	-55°C to +125°C	16 Lead CERDIP
MAX358C/D**	0°C to +75°C	Dice
MAX359CPE	0°C to +75°C	16 Lead Plastic DIP
MAX359CWE	0°C to +75°C	16 Lead Wide SO
MAX359CJE	0°C to +75°C	16 Lead CERDIP
MAX359EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX359EWE	-40°C to +85°C	16 Lead Wide SO
MAX359EJE	-40°C to +85°C	16 Lead CERDIP
MAX359MJE	-55°C to +125°C	16 Lead CERDIP
MAX359C/D**	0°C to +75°C	Dice

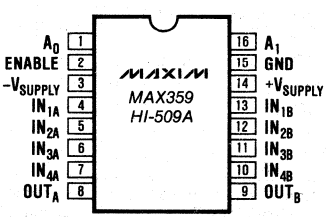
(Ordering Information is continued on last page.)

** The substrate may be allowed to float or be tied to V^+ (JI CMOS).

Pin Configuration

TOP VIEW





The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Fault-Protected Analog Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins ..... +44V
V^+ ..... +22V
V^- ..... -22V
Digital Input Overvoltage:
V_{EN}, V_A { $V_{Supply}(+)$ ..... +4V
{ $V_{Supply}(-)$ ..... -4V
Analog Input Overvoltage with Multiplexer Power On:
V_S { $V_{Supply}(+)$ ..... +20V
{ $V_{Supply}(-)$ ..... -20V
Analog Input Overvoltage with Multiplexer Power Off:
V_S { $V_{Supply}(+)$ ..... +35V
{ $V_{Supply}(-)$ ..... -35V

Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max) 40mA
Power Dissipation (Note 1) (CERDIP) 1.28W
Operating Temperature Range:
MAX358/359M; HI-508A/509A-2, -8 ..... -55°C to +125°C
MAX358/359C; HI-508A/509A-5 ..... 0°C to +75°C
MAX358/359E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Note 1: Derate 12.8mW/°C above T_A = +75°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: HI-508A/509A (See facing page for MAX358/359.)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
STATIC										
ON Resistance	$r_{DS(ON)}$	V_D = ±10V, I_S = 100μA V_{AL} = 0.8V, V_{AH} = 4V	+25°C Full		1.2 1.5	1.5 1.8		1.5 1.8	1.8 2.0	kΩ
OFF Input Leakage Current	$I_{S(OFF)}$	V_S = ±10V, V_D = ∓10V V_{EN} = 0.8V (Note 2)	+25°C Full		0.03	 50		0.03	 50	nA
OFF Output Leakage Current	$I_{D(OFF)}$	V_D = ±10V, V_S = ∓10V V_{EN} = 0.8V HI-508A (Note 2) HI-509A	+25°C Full Full		0.1	 200 100		0.1	 200 100	nA
ON Channel Leakage Current	$I_{D(ON)}$	$V_{S(ALL)}$ = V_D = ±10V (Note 2) V_{AH} = V_{EN} = 4V HI-508A V_{AL} = 0.8V HI-509A	+25°C Full Full		0.1	 200 100		0.1	 200 100	nA
Analog Signal Range	V_{AN}		Full	-15		+15	-15		+15	V
Differential, OFF Output Leakage Current	I_{DIFF}	(HI-509A only)	Full			50			50	nA
FAULT										
Output Leakage Current (with Overvoltage)	$I_{D(OFF)}$	V_D = 0V Analog Overvoltage = ±33V	+25°C Full		4.0	 2.0		4.0		nA μA
INPUT										
Input Low Threshold	V_{AL}	(Note 3)	Full			0.8			0.8	V
Input High Threshold	V_{AH}		Full	4.0			4.0			V
Input Leakage Current (High or Low)	I_A	V_A = 4V or 0V (Note 4)	Full			1.0			1.0	μA
DYNAMIC										
Access Time	t_A		+25°C		0.5	1.0		0.5	1.0	μs
Break-Before-Make Delay	t_{ON}-t_{OFF}	V_{EN} = +5V, V_{IN} = ±10V A_0, A_1, A_2 Strobed	+25°C	25	80		25	80		ns
Enable Delay (ON)	$t_{ON(EN)}$		+25°C Full		300	500 1000		300	 1000	ns
Enable Delay (OFF)	$t_{OFF(EN)}$		+25°C Full		300	500 1000		300	 1000	ns
Settling Time (0.1%) (0.01%)	t_{SETT}		+25°C		1.2 3.5			1.2 3.5		μs

Note 2: Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
Note 3: To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
Note 4: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

Fault-Protected Analog Multiplexer

- ♦ Only Nanoamps of Leakage Under Fault Conditions
- ♦ All Switches OFF With Power Supplies Off
- ♦ Channel Turns OFF When Overvoltage Occurs
- ♦ TTL Compatible, No Pullups Required
- ♦ Significantly Reduced Power Consumption
- ♦ ±4.5V to ±18V Operation

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: MAX358/359 (See facing page for HI-508A/509A.)

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
STATIC										
ON Resistance	$r_{DS(ON)}$	V_D = ±10V, I_S = 100µA V_{AL} = 0.8V, V_{AH} = 2.4V	+25°C Full		1.2 1.5	1.5 1.8		1.5 1.8	1.8 2.0	kΩ
OFF Input Leakage Current	$I_{S(OFF)}$	V_S = ±10V, V_D = ∓10V V_{EN} = 0.8V	+25°C Full		0.03	0.5 50		0.03	1.0 50	nA
OFF Output Leakage Current	$I_{D(OFF)}$	V_D = ±10V, V_S = ∓10V V_{EN} = 0.8V MAX358 MAX359	+25°C Full Full		0.1	1.0 200 100		0.1	2.0 200 100	nA
ON Channel Leakage Current	$I_{D(ON)}$	$V_{S(ALL)}$ = V_D = ±10V (Note 2) V_{AH} = V_{EN} = 2.4V MAX358 V_{AL} = 0.8V MAX359	+25°C Full Full		0.1	2.0 200 100		0.1	5.0 200 100	nA
Analog Signal Range	V_{AN}	(Note 1)	Full	-15		+15	-15		+15	V
Differential, OFF Output Leakage Current	I_{DIFF}	MAX359 only	Full			50			50	nA
FAULT										
Output Leakage Current (with Overvoltage)	$I_{D(OFF)}$	V_D = 0V (Note 2) Analog Overvoltage = ±33V	+25°C Full		4.0	 2.0		4.0		nA µA
Input Leakage Current (with Overvoltage)	$I_{S(OFF)}$	**V_{IN} = ±25V, V_O = ±10V (Note 2)**	**+25°C**			**5.0**			**10**	**µA**
Input Leakage Current (w. Power Supplies Off)	$I_{S(OFF)}$	**V_{IN} = ±25V, V_{EN} = V_O = 0V A_0 = A_1 = A_2 = 0V or 5V**	**+25°C**			**2.0**			**5.0**	**µA**
INPUT										
Input Low Threshold	V_{AL}		Full			0.8			0.8	V
Input High Threshold	V_{AH}		**Full**	**2.4**			**2.4**			**V**
Input Leakage Current (High or Low)	I_A	V_A = 4V or 0V (Note 4)	Full			1.0			1.0	µA
DYNAMIC										
Access Time	t_A	(Figure 1)	+25°C		0.5	1.0		0.5	1.0	µs
Break-Before-Make Delay (Figure 2)	t_{ON}-t_{OFF}	V_{EN} = +5V, V_{IN} = ±10V A_0, A_1, A_2 Strobed	+25°C	25	80		25	80		ns
Enable Delay (ON)	$t_{ON(EN)}$	(Figure 3)	+25°C Full		300	500 1000		300	 1000	ns
Enable Delay (OFF)	$t_{OFF(EN)}$	(Figure 3)	+25°C Full		300	500 1000		300	 1000	ns
Settling Time (0.1%) (0.01%)	t_{SETT}		+25°C		1.2 3.5			1.2 3.5		µs

Note 1: When the analog signal exceeds +13.5V or -12V the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.
Note 2: The value shown is the steady state value. The transient leakage is typically 10µA. See detailed description.
Note 3: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V are used.
Note 4: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

ELECTRICAL CHARACTERISTICS: HI-508A/509A (continued)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC (continued)										
"OFF Isolation" (Note 5)	$OFF_{(ISO)}$	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V = $7V_{RMS}$, f = 100kHz	+25°C	50	68		50	68		dB
Channel Input Capacitance	$C_{S(OFF)}$		+25°C		5			5		pF
Channel Output Capacitance	$C_{D(OFF)}$	HI-508A HI-509A	+25°C		25 12			25 12		pF
Digital Input Capacitance	C_A		+25°C		5			5		pF
Input to Output Capacitance	$C_{DS(OFF)}$		+25°C		0.1			0.1		pF
SUPPLY										
Positive Supply Current	I^+	V_{EN}, V_A = 0V or 4V	Full		0.5	2.0		0.5	2.0	mA
Negative Supply Current	I^-	V_{EN}, V_A = 0V or 4V	Full		0.02	1.0		0.02	1.0	mA

Note 5: Worst case isolation occurs on channel 4 due to proximity to the output pins.

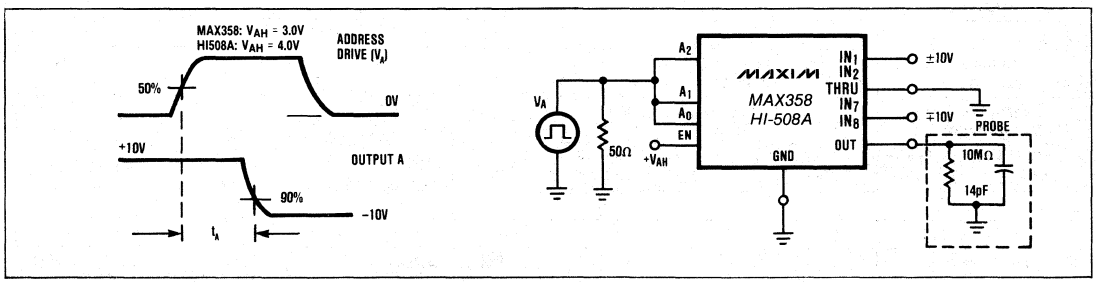


Figure 1. Access Time vs. Logic Level (High)

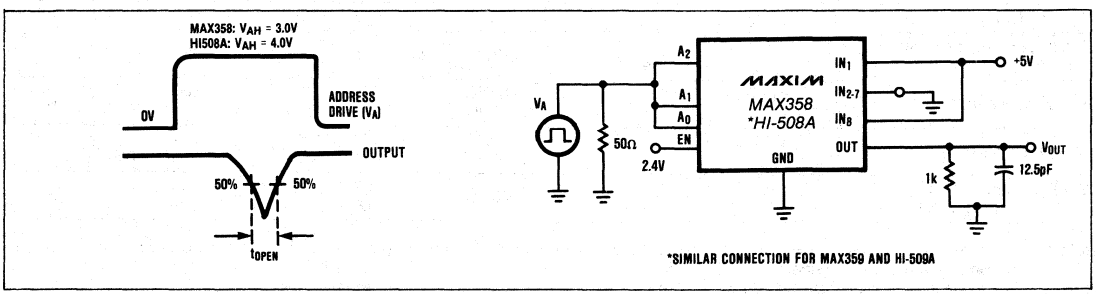


Figure 2. Break Before Make Delay (t_{OPEN})

ELECTRICAL CHARACTERISTICS: MAX358/359 (continued)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +75°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC (continued)										
"OFF Isolation"	$OFF_{(ISO)}$	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V = $7V_{RMS}$, f = 100kHz	+25°C	50	68		50	68		dB
Channel Input Capacitance	$C_{S(OFF)}$		+25°C		5			5		pF
Channel Output Capacitance	$C_{D(OFF)}$	MAX358 MAX359	+25°C		25 12			25 12		pF
Digital Input Capacitance	C_A		+25°C		5			5		pF
Input to Output Capacitance	$C_{DS(OFF)}$		+25°C		0.1			0.1		pF
SUPPLY										
Positive Supply Current	I^+	V_{EN} = 0.8V, or 2.4V All V_A = 0V or 5V	+25°C Full		0.1 0.3	0.6 0.7		0.2 0.5	1.0 1.0	mA
Negative Supply Current	I^-	V_{EN} = 0.8V or 2.4V All V_A = 0V or 5V	+25°C Full		0.01 0.02	0.1 0.2		0.01 0.02	0.1 0.1	mA
Power Supply Range for Continuous Operation	V_{OP}	(Note 5)	+25°C	±4.5		±18	±4.5		±18	V

Note 5: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V are used.

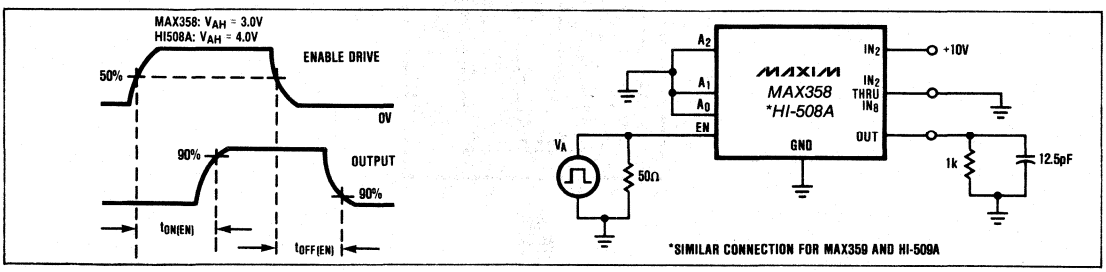


Figure 3. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)

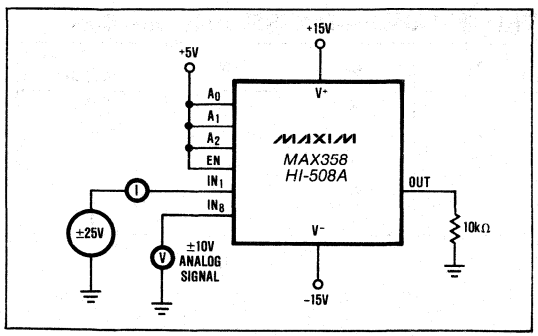


Figure 5. Input Leakage Current (Overvoltage)

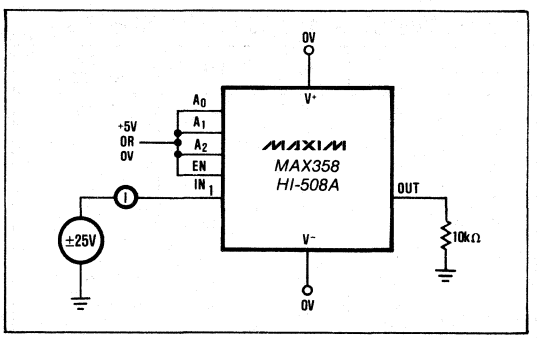


Figure 6. Input Leakage Current (with Power Supplies OFF)

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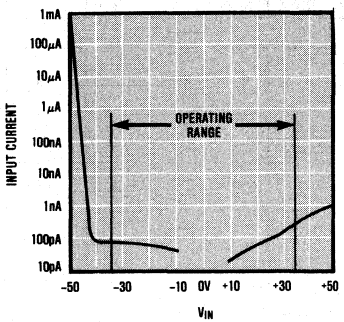
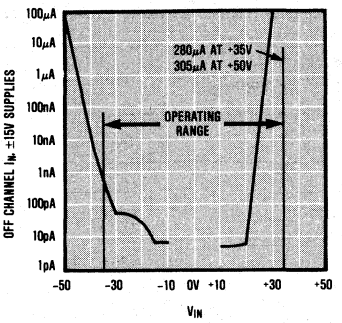
Fault-Protected Analog Multiplexer

Typical Operating Characteristics

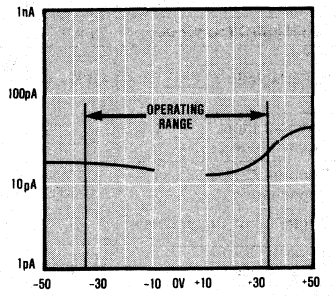
INPUT LEAKAGE VS. INPUT VOLTAGE WITH $V^+ = V^- = 0V$



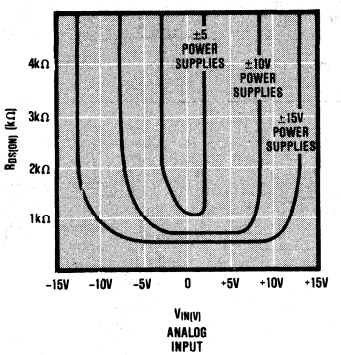
OFF CHANNEL LEAKAGE CURRENT VS. INPUT VOLTAGE WITH ±15V SUPPLIES



OUTPUT LEAKAGE VS. OFF CHANNEL OVERVOLTAGE WITH ±15V SUPPLIES



$R_{DS(ON)}$ VS. INPUT VOLTAGE



TRUTH TABLE—MAX358 AND HI-508A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE—MAX359 AND HI-509A

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTE: Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

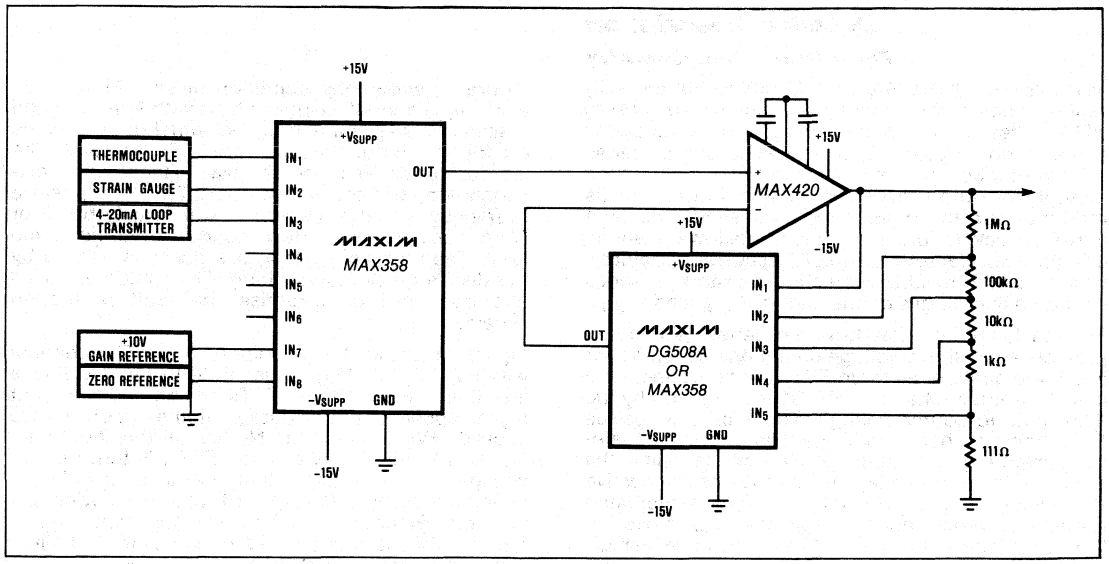


Figure 7. Typical Data Acquistion Front End

Typical Applications

Figure 7 shows a typical data acquisition system using the MAX358 multiplexer. Since the multiplexer is driving a high impedance input, its error is a function of its own resistance ($R_{DS(ON)}$) times the multiplexer leakage current ($I_{D(ON)}$) and the amplifier bias current (I_{BIAS}):

$$V_{ERR} = R_{DS(ON)} \times (I_{D(ON)} + I_{BIAS}\ (MAX420))$$
$$= 1.5k \times (2nA + 30pA)$$
$$= 3.05\mu V \text{ maximum error}$$

In most cases, this error is low enough that preamplification of input signals is not needed, even with very low level signals, such as 40μV/°C from type J thermocouples.

In systems with fewer than 8 inputs, an unused channel can be connected to the system ground reference point for software zero correction. A second channel connected to the system voltage reference allows gain correction of the entire data acquisition system as well.

A MAX 420 precision op-amp is connected as a programmable gain amplifier, with gains ranging from 1 to 10,000. The guaranteed 5μV unadjusted offset of the MAX420 maintains high signal accuracy, while programmable gain allows the output signal level to be scaled to the optimum range for the remainder of the data acquisition system, normally a Sample/Hold and A/D. Since the gain-changing multiplexer is not connected to the external sensors, it can be either a DG508A multiplexer or the fault protected MAX358.

Input switching, however, must be done with a fault protected MAX358 multiplexer if it is to provide the level of protection and isolation required with most data acquisition inputs. Since external signal sources may continue to supply voltage when the multiplexer and system power are turned off, non-fault protected multiplexers, or even first-generation fault protected devices, will allow many milliamps of fault current to flow from outside sources into the multiplexer. The result could be damage to either the sensors or the multiplexer. A non-fault protected multiplexer will also allow input overvoltages to appear at its output, perhaps damaging Sample/Holds or A/Ds. Such input overdrives may also cause input-to-input shorts, allowing the high current output of one sensor to possibly damage another.

The MAX358 eliminates all of the above problems since it not only limits its output voltage to safe levels, with or without power applied ($+V_{SUP}$ and $-V_{SUP}$), but also turns all channels off when power is removed, drawing only sub-microamp fault currents from the inputs, and maintaining isolation between inputs for continuous overvoltages up to ±35V.

Fault-Protected Analog Multiplexer

Detailed Description

Fault Protection Circuitry

Maxim's HI-508A/509A and MAX358/359 are fully fault-protected for continuous input voltages up to ±35V, whether or not the $+V_{SUP}$ and $-V_{SUP}$ power supplies are present. These devices use a "series FET" protection scheme which not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels. This fault current is several orders of magnitude lower than the original manufacturer's HI-508A (several milliamps), which uses 1 to 2kΩ protection resistors in series with parasitic diodes connected to $+V_{SUP}$ and $-V_{SUP}$.

Figures 8 and 9 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -25V input, N-channel FET Q1 is turned on by the +25V gate-to-source voltage. The P-channel device (Q2), however, has +25V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +25V, Q1 has a negative V_{GS}, which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any voltage will turn off either Q1 or Q2.

Figure 10 shows the condition of an OFF channel with $+V_{SUP}$ and $-V_{SUP}$ present. As with Figures 8 and 9, either an N-channel or a P-channel device will be off for any input voltage from -35V to +35V. The leakage current with negative overvoltages will immediately drop to a few nanoamps at 25°C. For positive overvoltages that fault current will initially be 10 or 20μA, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault protection scheme.

Figure 11 shows the condition of the ON channel with $+V_{SUP}$ and $-V_{SUP}$ present. With input voltages less than ±10V, all three FETs are on and the input signal appears at the output. If the input voltage exceeds $+V_{SUP}$ minus the N-channel threshold voltage (V_{TN}), then the N-channel FET will turn off. For voltages more negative than $-V_{SUP}$ minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically 1.5V and V_{TP} is typically 3V, the multiplexer's output swing is limited to about -12V to +13.5V with ±15V supplies.

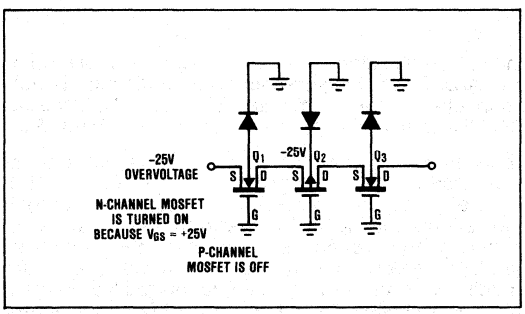


Figure 8. -25V Overvoltage with Multiplexer Power OFF

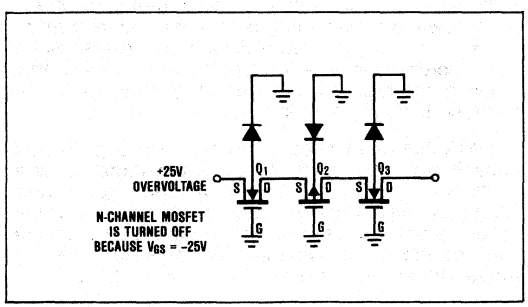


Figure 9. +25V Overvoltage with Multiplexer Power OFF

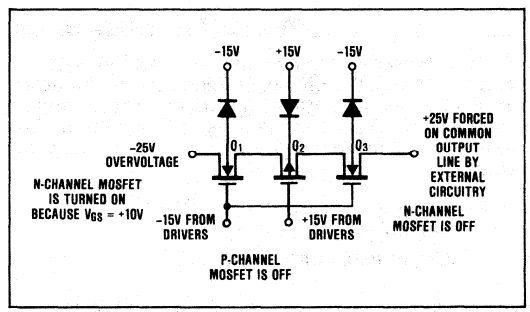


Figure 10. -25V Overvoltage on an OFF Channel with Multiplexer Power Supply ON

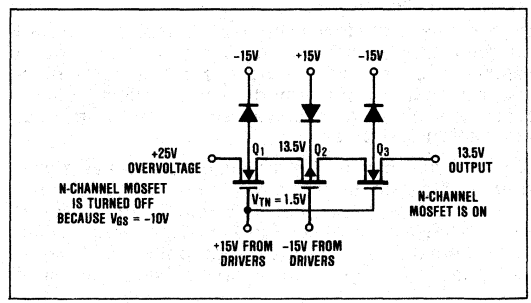


Figure 11. +25V Overvoltage Input to the ON Channel

The Typical Characteristics graphs show typical leakage vs. input voltage curves. Although the maximum rated overvoltage of these devices is ±35V, the MAX358/359 typically has excellent performance up to ±40V, providing additional margin for the unknown transients that exist in the real world. In summary, the MAX358/359 provides superior protection from all fault conditions, while using a standard, readily produced junction isolated CMOS process.

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels vs. power supply voltages and analog input voltage. Note that since the channels are well matched, the differential charge injection for the MAX359/HI-509A is typically less than 5 picocoulombs. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

The channel-to-channel switching time is typically 600ns, with about 200ns of break before make delay. This 200ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system such as Figure 7, the dominant delay is not the switching time of the MAX358 multiplexer, but is the settling time of the following amplifiers and S/H. Another limiting factor is the RC time constant of the multiplexer $R_{DS(ON)}$ plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output will approximately double the settling time to 0.01% accuracy.

Operation with Supply Voltages Other than ±15V

The main effect of supply voltages other than ±15V is the reduction in output signal range. The MAX358 limits the output voltage to about 1.5V below $+V_{SUP}$ and about 3V above $-V_{SUP}$. In other words, the output swing is limited to +3.5V to -2V when operating from ±5V. The typical characteristics graphs show typical $R_{DS(ON)}$ for ±15V, ±10V, and ±5V power supplies. Maxim tests and guarantees the MAX358/359 for operation from ±4.5V to ±18V supplies. The switching delays are increased by about a factor of 2 at ±5V, but break-before-make action is preserved.

The MAX358/9 can be operated with a single +9V to +22V supply, as well as asymmetrical power supplies such at +15V and -5V. The digital threshold will remain approximately 1.6V above the Ground pin, and the analog characteristics such as $R_{DS(ON)}$ are determined by the total voltage difference between $+V_{SUP}$ and $-V_{SUP}$. Connect $-V_{SUP}$ to 0V when operating with a +9V to +22V single supply.

The MAX358 digital threshold is relatively independent of the power supply voltages, going from a typical 1.6V when $+V_{SUP}$ is 15V to 1.5V typical with a 5V $+V_{SUP}$. This means that Maxim HI-508/509A and MAX358/359 will operate with standard TTL logic levels, even with ±5V power supplies. In all cases, the threshold of the ENable pin is the same as the other logic inputs.

Digital Interface Levels

The typical digital threshold of both the address lines and the enable pin is 1.6V, with a temperature coefficient of about -3mV/°C. This ensures compatibility with 0.8V to 2.4V TTL logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from ±15V to ±5V. In all cases, the digital threshold is referenced to the Ground pin.

The digital inputs can also be driven with CMOS logic

Table 1A. MAX358 AND HI-508A CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge
±5V	+1.7V 0V -1.7V	+100pC +70pC +45pC
±10V	+5V 0V -5V	+200pC +130pC +60pC
±15V	+10V 0V -10V	+300pC +180pC +50pC

Test Conditions: C_L = 1000pF on multiplexer output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, $A_1 = A_2$ = 0V, A_0 is toggled at 2kHz rate between 0V and 3V. +100 picocoulombs of charge creates a +100mV step when injected into a 1000pF load capacitance.

Table 1B. MAX359 AND HI-509A CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge		
		Out A	Out B	Differential A - B
±5V	+1.7V 0V -1.7V	+105pC +73pC +48pC	+107pC +74pC +50pC	-2pC -1pC -2pC
±10V	+5V 0V -5V	+215pC +135pC +62pC	+220pC +139pC +63pC	-5pC -4pC -1pC
±15V	+10V 0V -10V	+325pC +180pC +55pC	+330pC +185pC +55pC	-5pC -5pC 0pC

Test Conditions: C_L = 1000pF on Out A and Out B; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, A_1 = 0V, A_0 is toggled from 0V to 3V at a 2kHz rate.

levels swinging from either $+V_{SUP}$ to $-V_{SUP}$ or from $+V_{SUP}$ to Ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1μA. The digital inputs are protected from ESD by a 30V zener diode between the input and $+V_{SUP}$, and can be driven ±6V beyond the supplies without drawing excessive current.

Operation as a Demultiplexer

The MAX358/9 will function as a demultiplexer, where the input is applied to the Output pin, and the Input pins are used as outputs. The MAX358/9 provides both break-before-make action and full fault protection when operated as a demultiplexer, unlike earlier generations of fault protected multiplexers.

Channel-to-Channel Crosstalk, Off Isolation and Digital Feedthrough

At DC and low frequencies the channel-to-channel crosstalk is caused by variations in output leakage currents as the off channel input voltages are varied. The MAX358 output leakage varies only a few picoamps as all 7 off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX358 output, which is $R_{DS(ON)}$ plus the input signal source resistance in most cases since the load driven by the MAX358 is usually a high impedance. For a signal source impedance of 10kΩ or lower, the DC crosstalk exceeds 120dB.

Table 2 shows typical AC crosstalk and off isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled. When the output is disabled, the digital feedthrough is virtually unmeasureable, since the digital pins are physically isolated from the analog section by the Ground and $-V_{SUP}$ pins. The groundplane formed by these lines is continued onto the MAX358/9 die to provide over 100dB isolation between the digital and analog sections.

Table 2A. TYPICAL OFF ISOLATION REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
One Channel Driven	74dB	72dB	66dB
All Channels Driven	64dB	48dB	44dB

Test Conditions: $V_{IN} = 20V_{PK-PK}$ at the tabulated frequency, $R_L = 1.5k$ between OUT and ground, EN = 0V.

$$OIRR = 20 \text{ Log } \frac{20V_{PK-PK}}{V_{OUT\ (PK-PK)}}$$

Table 2B. TYPICAL CROSSTALK REJECTION RATIO

Frequency	100kHz	500kHz	1MHz
R_L = 1.5k	70dB	68dB	64dB
R_L = 10k	62dB	46dB	42dB

Test Conditions: Specified R_L connected from OUT to ground, EN = +5V, $A_0 = A_1 = A_2$ = +5V (Channel 1 selected). $20V_{PK-PK}$ at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

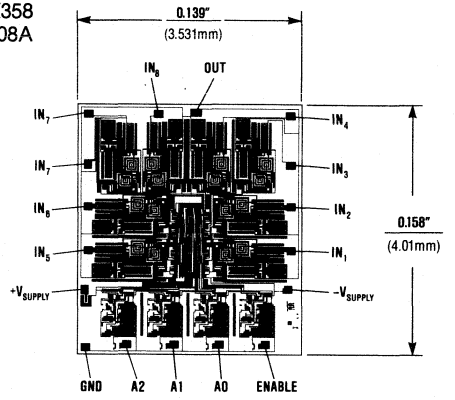
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
HI1-0508A-2	-55°C to +125°C	16 Lead CERDIP
HI1-0508A-5*	0°C to +75°C	16 Lead CERDIP
HI3-0508A-5*	0°C to +75°C	16 Lead Plastic DIP
HI1-0509A-2	-55°C to +125°C	16 Lead CERDIP
HI1-0509A-5*	0°C to +75°C	16 Lead CERDIP
HI3-0509A-5*	0°C to +75°C	16 Lead Plastic DIP

* Maxim burns in all devices at 150°C. Maxim's -5 device is therefore equivalent to the original manufacturer's -7 product.

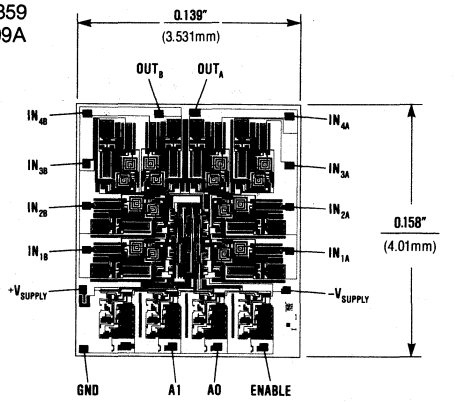
Chip Topographies

MAX358
HI-508A



Note: Connect substrate to $+V_{SUPPLY}$ or Leave It Floating

MAX359
HI-509A



Note: Connect substrate to $+V_{SUPPLY}$ or Leave It Floating

11

MAXIM

Monolithic CMOS Analog Multiplexers

General Description

Maxim's DG506A and DG507A are monolithic CMOS analog multiplexers. The DG506A is a single 16 channel (1 of 16) multiplexer, and the DG507A is a differential 8 channel (2 of 16) multiplexer.

Both devices feature break-before-make switching. Maxim guarantees that these multiplexers will not latch-up if the power supplies are turned off with the input signals still present as long as absolute maximum ratings are not violated. The multiplexers operate over a wide range of power supplies from ±4.5V to ±18V.

Compared to the original manufacturer's devices, Maxim's DG506A and DG507A consume significantly less power, making them ideal for portable equipment.

Maxim's DG506A and DG507A meet or exceed the specifications of, and are drop-in replacements for, Intersil's IH6116 and IH6216, Siliconix's DG506A and DG507A, and Harris' HI506 and HI507.

Applications

Control Systems

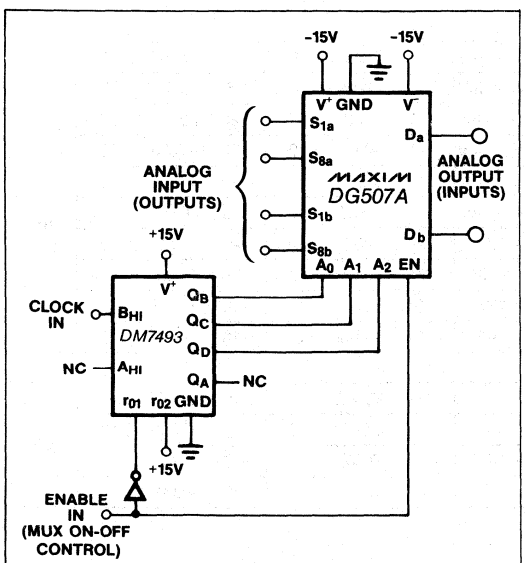
Data Logging Systems

Aircraft Heads Up Displays

Data Acquisition Systems

Signal Routing

Typical Operating Circuit



8 Channel Sequential Differential MUX/DEMUX

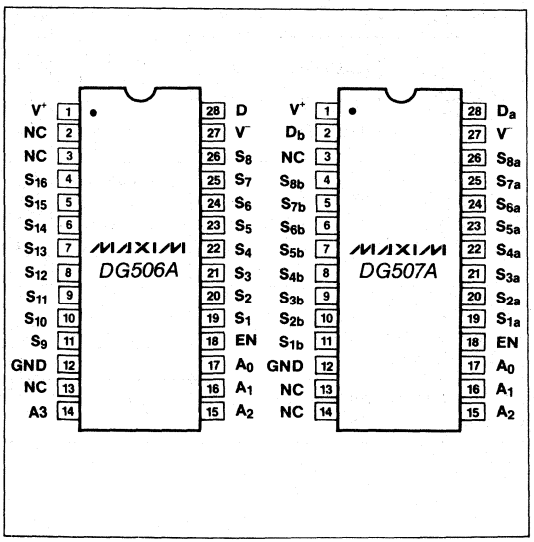
Features

- **Improved 2nd Source!**
- **Pin compatible with Harris, Siliconix, Intersil**
- **Operable with ±4.5V to ±18V Supplies**
- **Symmetrical, Bi-Directional Operation**
- **Logic and Enable inputs, TTL and CMOS Compatible**
- **Latch-Up Proof Construction**
- **Monolithic, Low-Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
DG506AAK	-55°C to +125°C	28 Lead CERDIP
DG506ABK	-20°C to +85°C	28 Lead CERDIP
DG506AC/D	0°C to +70°C	Dice
DG506ACJ	0°C to +70°C	28 Lead Plastic DIP
DG506ACK	0°C to +70°C	28 Lead CERDIP
DG506ACWI	0°C to +70°C	28 Lead Wide SO
DG507AAK	-55°C to +125°C	28 Lead CERDIP
DG507ABK	-20°C to +85°C	28 Lead CERDIP
DG507AC/D	0°C to +70°C	Dice
DG507ACJ	0°C to +70°C	28 Lead Plastic DIP
DG507ACK	0°C to +70°C	28 Lead CERDIP
DG507ACWI	0°C to +70°C	28 Lead Wide SO

Pin Configurations



Monolithic CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V^-
V^+ 44V
GND 25V
Digital Inputs V_S, V_D (Note 1) ..... -2V to (V^+ + 2V) or 20mA, whichever occurs first.
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1msec, 10% duty cycle max) 40mA
Storage Temperature (A & B Suffix) ..... -65°C to 150°C
(C Suffix) ..... -65°C to 125°C
Operating Temperature (A Suffix) ..... -55°C to 125°C
(B Suffix) ..... -25°C to 85°C
(C Suffix) ..... 0°C to 70°C
Power Dissipation (Package)*
28 Pin Ceramic DIP** 1200mW
28 Pin Plastic DIP*** 625mW

*All leads soldered or welded to PC board.
**Derate 16mW/°C above 75°C
***Derate 8.3mW/°C above 75°C

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated.)

PARAMETER		SYMBOL	TEST CONDITIONS		DG506AA DG507AA MIN (Note 2)	DG506AA DG507AA TYP (Note 3)	DG506AA DG507AA MAX	DG506AB/C DG507AB/C MIN (Note 2)	DG506AB/C DG507AB/C TYP (Note 3)	DG506AB/C DG507AB/C MAX	UNITS
SWITCH											
Analog Signal Range		V_{ANALOG}			-15		15	-15		15	V
Drain-Source ON Resistance		$r_{DS(on)}$	Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V, V_{EN} = 2.4V	V_D = 10V, I_S = -200μA		270	400		270	450	Ω
				V_D = -10V, I_S = -200μA		230	400		230	450	
Greatest Change in Drain-Source ON Resistance Between Channels		$\Delta r_{DS(on)}$	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}^{MAX} - r_{DS(on)}^{MIN}}{r_{DS(on)}^{AVE}}\right)$ $-10V \leq V_S \leq 10V$			6			6		%
Source OFF Leakage Current		$I_{S(off)}$	V_{EN} = 0.8V V_{AL} = 0.8V	V_S = 10V, V_D = -10V	-1	0.002	1	-5	0.002	5	nA
				V_S = -10V, V_D = 10V	-1	-0.005	1	-5	-0.005	5	
Drain OFF Leakage Current	DG506A	$I_{D(off)}$		V_D = 10V, V_S = -10V	-10	0.02	10	-20	0.02	20	
				V_D = -10V, V_S = 10V	-10	-0.03	10	-20	-0.03	20	
	DG507A			V_D = 10V, V_S = -10V	-5	0.007	5	-10	0.007	10	
				V_D = -10V, V_S = 10V	-5	-0.015	5	-10	-0.015	10	
Channel ON Leakage Current	DG506A	$I_{D(on)}$[4]	Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V, V_{EN} = 2.4V	$V_{S(all)}$ = V_D = 10V	-10	0.03	10	-20	0.03	20	
				$V_{S(all)}$ = V_D = -10V	-10	-0.06	10	-20	-0.06	20	
	DG507A			$V_{S(all)}$ = V_D = 10V	-5	0.015	5	-10	0.015	10	
				$V_{S(all)}$ = V_D = -10V	-5	-0.03	5	-10	-0.03	10	
INPUT											
Address Input Current, Input Voltage High		I_{AH}	V_A = 2.4V		-10	-0.002		-10	-0.002		μA
			V_A = 15V			0.006	10		0.006	10	
Address Input Current, Input Voltage Low		I_{AL}	All V_A = 0	V_{EN} = 2.4V	-10	-0.002		-10	-0.002		
				V_{EN} = 0	-10	-0.002		-10	-0.002		

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated.)

PARAMETER		SYMBOL	TEST CONDITIONS		DG506AA DG507AA MIN (Note 2)	DG506AA DG507AA TYP (Note 3)	DG506AA DG507AA MAX	DG506AB/C DG507AB/C MIN (Note 2)	DG506AB/C DG507AB/C TYP (Note 3)	DG506AB/C DG507AB/C MAX	UNITS
DYNAMIC											
Switching Time Of Multiplexer		$t_{transition}$	See Figure 1			0.6	1		0.6		μs
Break-Before-Make Interval		t_{open}	See Figure 3			0.2			0.2		μs
Enable Turn-ON Time		$t_{on(EN)}$	See Figure 2			1			1		μs
Enable Turn-OFF Time		$t_{off(EN)}$	See Figure 2			0.4			0.4		μs
OFF Isolation[2]		OIRR	V_{EN} = 0, R_L = 1kΩ, C_L = 15pF, V_S = 7Vrms, f = 500kHz			68			68		dB
Source OFF Capacitance		$C_{S(off)}$	V_{EN} = 0, f = 140kHz	V_S = 0		6			6		pF
Drain OFF Capacitance	DG506A	$C_{D(off)}$	V_{EN} = 0, f = 140kHz	V_D = 0		45			45		pF
	DG507A					23			23		pF
SUPPLY											
Positive Supply Current		I^+	V_{EN} = 0V or 5V, All V_A = 0			.13	.25		.13	.3	mA
Negative Supply Current		I^-	V_{EN} = 0V or 5V, All V_A = 0		-.15	-.07		-.25	-.07		mA

Note 1: Signals on S_X, D_X, or IN_X exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 4: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 5: OFF isolation = $20 \log \frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S.

Monolithic CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS (Over Temperature)

(V^+ = 15V, V^- = -15V, GND = 0V, T_A = Over Temperature Range, unless otherwise indicated.)

PARAMETER		SYMBOL	TEST CONDITIONS		DG506AA DG507AA MIN (Note 2)	DG506AA DG507AA TYP (Note 3)	DG506AA DG507AA MAX	DG506AB/C DG507AB/C MIN (Note 2)	DG506AB/C DG507AB/C TYP (Note 3)	DG506AB/C DG507AB/C MAX	UNITS
SWITCH											
Analog Signal Range		V_{ANALOG}			-15		15	-15		15	V
Drain-Source ON Resistance		$r_{DS(on)}$	Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V, V_{EN} = 2.4V	V_D = 10V, I_S = -200μA			500			550	Ω
				V_D = -10V, I_S = -200μA			500			550	
Source OFF Leakage Current		$I_{S(off)}$	V_{EN} = 0.8V V_{AL} = 0.8V	V_S = 10V, V_D = -10V	-50		50	-50		50	nA
				V_S = -10V, V_D = 10V	-50		50	-50		50	
Drain OFF Leakage Current	DG506A	$I_{D(off)}$		V_D = 10V, V_S = -10V	-300		300	-300		300	
				V_D = -10V, V_S = 10V	-300		300	-300		300	
	DG507A			V_D = 10V, V_S = -10V	-200		200	-200		200	
				V_D = -10V, V_S = 10V	-200		200	-200		200	
Channel ON Leakage Current	DG506A	$I_{D(on)}$[4]	Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V, V_{EN} = 2.4V	$V_{S(all)}$ = V_D = 10V	-300		300	-300		300	
				$V_{S(all)}$ = V_D = -10V	-300		300	-300		300	
	DG507A			$V_{S(all)}$ = V_D = 10V	-200		200	-200		200	
				$V_{S(ALL)}$ = V_D = -10V	-200		200	-200		200	
INPUT											
Address Input Current, Input Voltage High		I_{AH}	V_A = 2.4V		-30			-30			μA
			V_A = 15V				30			30	
Address Input Current, Input Voltage Low		I_{AL}	All V_A = 0	V_{EN} = 2.4V	-30			-30			
				V_{EN} = 0			30			30	

Note 1: Signals on S_X, D_X, or IN_X exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 4: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 5: OFF isolation = $20 \log \frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S.

Truth Tables

DG506A

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG507A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$
"0" = DON'T CARE

Switching Time Test Circuit

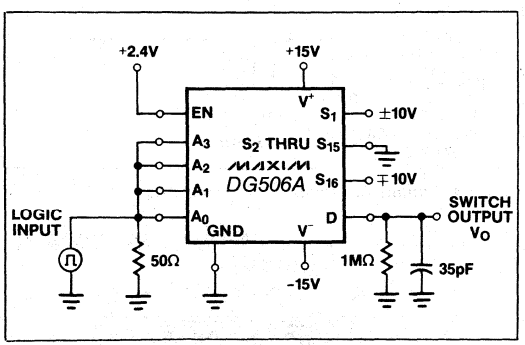


Figure 1A. Transition Switching Time

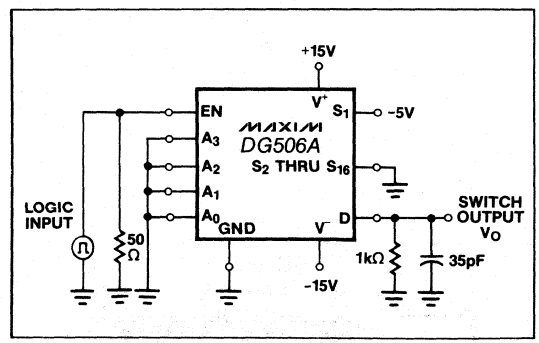


Figure 2A. Enable Switching Time

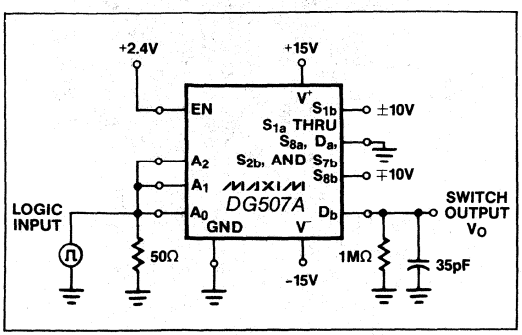


Figure 1B. Transition Switching Time

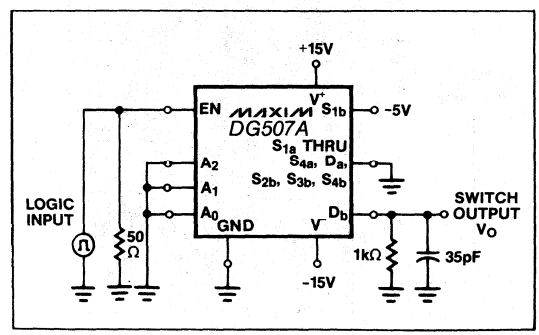


Figure 2B. Enable Switching Time

Monolithic CMOS Analog Multiplexers

Switching Time Test Circuit (continued)

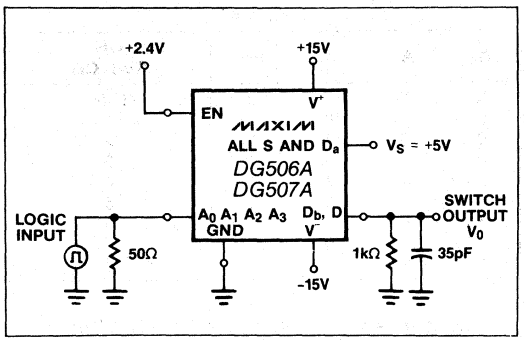


Figure 3. Break-Before-Make

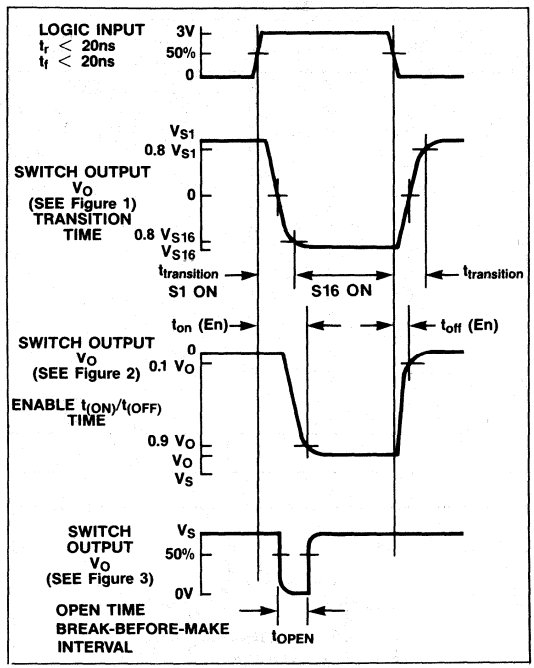
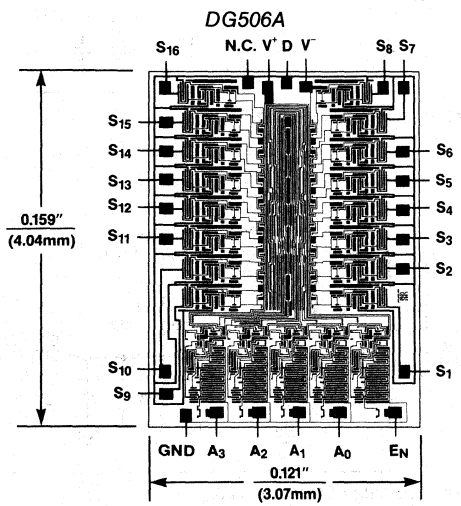
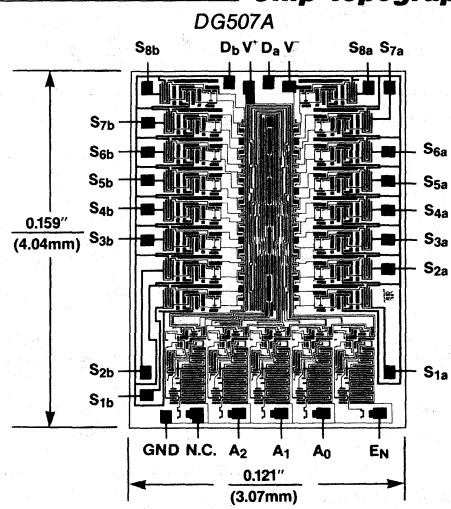


Figure 4. Timing Diagrams for Figures 1, 2, and 3

Chip Topography





MAXIM
Monolithic CMOS Analog Multiplexers

General Description

Maxim's DG508A and DG509A are monolithic CMOS analog multiplexers. The DG508A is a single 8 channel (1 of 8) multiplexer and the DG509A is a differential 4 channel (2 of 8) multiplexer.

Both devices guarantee break-before-make switching. Maxim guarantees that these multiplexers will not latch-up if the power supplies are turned-off with the input signals still present. Maxim also guarantees continuous operation when these devices are powered by supplies ranging from ±4.5V to ±18V.

Compared to the original manufacturer's devices, Maxim's DG508A and DG509A have lower on-resistance, faster enable switching times and significantly lower leakage currents. Maxim's devices also consume significantly lower power, making them ideal for portable equipment.

Maxim's DG508A and DG509A meet or exceed the specifications of, and are drop-in replacements for, Intersil IH6108 and IH6208 respectively.

Applications

Control Systems
Data Logging Systems
Aircraft Heads Up Displays
Data Acquisition Systems
Signal Routing

Features

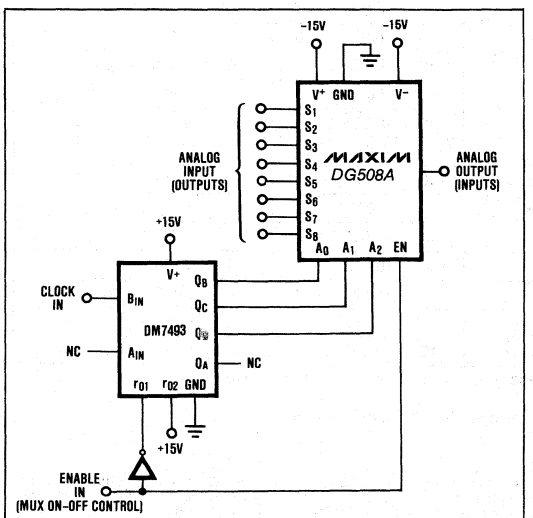
- **Improved 2nd Source! (See pages 3 and 5 for "Maxim Advantage™")**
- **Operable with ±4.5V to ±18V Supplies**
- **Symmetrical, Bi-Directional Operation**
- **Logic and Enable Inputs, TTL and CMOS Compatible**
- **Latch-Up Proof Construction**
- **Monolithic, Low-Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
DG508AAK	-55°C to +125°C	16 Lead CERDIP
DG508ABK	-20°C to +85°C	16 Lead CERDIP
DG508AC/D	0°C to +70°C	Dice
DG508ACJ	0°C to +70°C	16 Lead Plastic DIP
DG508ACWE	0°C to +70°C	16 Lead Wide SO
DG509AAK	-55°C to +125°C	16 Lead CERDIP
DG509ABK	-20°C to +85°C	16 Lead CERDIP
DG509AC/D	0°C to +70°C	Dice
DG509ACJ	0°C to +70°C	16 Lead Plastic DIP
DG509ACWE	0°C to +70°C	16 Lead Wide SO

(Contact factory for devices in ceramic flat packs.)

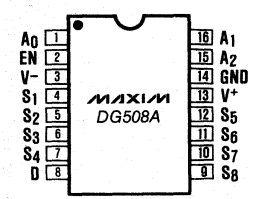
Typical Operating Circuit

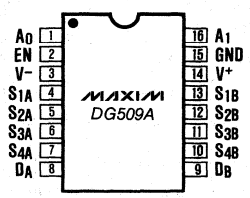


8 Channel Sequential Mux/Demux

Pin Configuration

Top View





The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Monolithic CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V⁻
V⁺ ..... +44V
GND ..... +25V
Digital Inputs (Note 1), V_S, V_D ..... -2V to (V⁺ +2V) or 20mA, whichever occurs first
Current (Any Terminal, Except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1msec, 10% Duty Cycle Max) 40mA
Storage Temperature ..... -65°C to +150°C

Power Dissipation (Package) (Note 2)
16 Pin Ceramic DIP (Note 3) 900mW
16 Pin Plastic DIP (Note 4) 470mW
16 Pin Wide SO (Note 5) 750mW

Note 1: Signals on S_X, D_X, or IN_X exceeding V⁺ or V⁻ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
Note 2: All leads soldered or welded to PC board.
Note 3: Derate 12mW/°C above +75°C.
Note 4: Derate 6.3mW/°C above +75°C.
Note 5: Derate 10mW/°C above +75°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and funcional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C unless otherwise indicated)

	PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS DG508AA DG509AA MIN (Note 6)	TYP (Note 7)	MAX	LIMITS DG508A B/C DG509A B/C MIN (Note 6)	TYP (Note 7)	MAX	UNIT
SWITCH	Analog Signal Range		V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance		$r_{DS(on)}$	V_D = 10V, I_S = -200μA	Seq. Ea. Switch On V_{AL} = 0.8V, V_{AH} = 2.4V		270	400		270	450	Ω
				V_D = -10V, I_S = -200μA			230	400		230	450	
	Greatest Change In Drain Source ON Resistance Between Channels		$\Delta r_{DS(on)}$	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ Max - r_{DS(on)}\ Min}{r_{DS(on)}\ Ave}\right)$ $-10V \le V_S \le +10V$			6			6		%
	Source OFF Leakage Current		$I_{S(off)}$	V_S = 10V, V_D = -10V	V_{EN} = 0V		0.002	1		0.002	5	nA
				V_S = -10V, V_D = 10V		-1	-0.005		-5	-0.005		
	Drain OFF Leakage Current	DG508A	$I_{D(off)}$	V_D = 10V, V_S = -10V			0.01	10		0.01	20	
				V_D = -10V, V_S = 10V		-10	-0.015		-20	-0.015		
		DG509A		V_D = 10V, V_S = -10V			0.005	10		0.005	20	
				V_D = -10V, V_S = 10V		-10	-0.008		-20	-0.008		
	Drain ON Leakage Current	DG508A	$I_{D(on)}$ (Note 8)	$V_{S(all)}$ = V_D = 10V	Seq. Ea. Switch On V_{AL} = 0.8V V_{AH} = 2.4V		0.015	10		0.015	20	
				$V_{S(all)}$ = V_D = -10V		-10	-0.03		-20	-0.03		
		DG509A		$V_{S(all)}$ = V_D = 10V			0.007	10		0.007	20	
				$V_{S(all)}$ = V_D = -10V		-10	-0.015		-20	-0.015		
INPUT	Address Input Current, Input Voltage High		I_{AH}	V_A = 2.4V		-10	-0.002		-10	-0.002		μA
				V_A = 15V			0.006	10		0.006	10	
	Address Input Current Input Voltage Low		I_{AL}	V_{EN} = 2.4V	All V_A = 0V	-10	-0.002		-10	-0.002		
				V_{EN} = 0V		-10	-0.002		-10	-0.002		

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 8: $I_{D(ON)}$ is leakage from driver into "ON" switch.

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Monolithic CMOS Analog Multiplexers

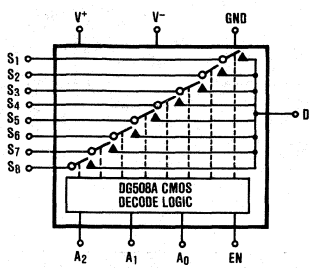
- ♦ Significantly Reduced Leakage Currents
- ♦ Significantly Reduced Supply Currents
- ♦ Lower ON Resistance
- ♦ Faster Enable Switching Times

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

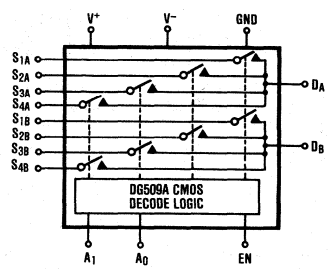
ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C unless otherwise indicated)

	PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS DG508AA DG509AA MIN (Note 6)	TYP (Note 7)	MAX	LIMITS DG508AB/C DG509AB/C MIN (Note 6)	TYP (Note 7)	MAX	UNIT
SWITCH	Analog Signal Range		V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance		$r_{DS(on)}$	V_D = 10V, I_S = -200μA	Seq. Ea. Switch On V_{AL} = 0.8V, V_{AH} = 2.4V		170	300		170	350	Ω
				V_D = -10V, I_S = -200μA			130	300		130	350	
	Greatest Change In Drain Source ON Resistance Between Channels		$\Delta r_{DS(on)}$	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ Max - r_{DS(on)}\ Min}{r_{DS(on)}\ Ave}\right)$ $-10V \le V_S \le +10V$			6			6		%
	Source OFF Leakage Current		$I_{S(off)}$	V_S = 10V, V_D = -10V	V_{EN} = 0V		0.002	0.5		0.002	1	nA
				V_S = -10V, V_D = 10V		-0.5	-0.005		-1	-0.005		
	Drain OFF Leakage Current	DG508A	$I_{D(off)}$	V_D = 10V, V_S = -10V			0.01	2		0.01	5	
				V_D = -10V, V_S = 10V		-2	-0.015		-5	-0.015		
		DG509A		V_D = 10V, V_S = -10V			0.005	2		0.005	5	
				V_D = -10V, V_S = 10V		-2	-0.008		-5	-0.008		
	Drain ON Leakage Current	DG508A	$I_{D(on)}$ (Note 8)	$V_{S(all)}$ = V_D = 10V	Seq. Ea. Switch On V_{AL} = 0.8V, V_{AH} = 2.4V		0.015	2		0.015	5	
				$V_{S(all)}$ = V_D = -10V		2	-0.03		-5	-0.03		
		DG509A		$V_{S(all)}$ = V_D = 10V			0.007	2		0.007	5	
				$V_{S(all)}$ = V_D = -10V		-2	-0.015		-5	-0.015		
INPUT	Address Input Current, Input Voltage High		I_{AH}	V_A = 2.4V		-10	-0.002		-10	-0.002		μA
				V_A + 15V			0.006	10		0.006	10	
	Address Input Current Input Voltage Low		I_{AL}	V_{EN} = 2.4V	All V_A = 0V	-10	-0.002		-10	-0.002		
				V_{EN} = 0V		-10	-0.002		-10	-0.002		

Functional Diagrams



DG508A
8 Channel Single Ended Multiplexer



DG509A
Differential 4 Channel Multiplexer

Note: See page 6 for Truth Tables.

Monolithic CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C unless otherwise indicated)

	PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS DG508AA DG509AA MIN (Note 6)	TYP (Note 7)	MAX	LIMITS DG508AB/C DG509AB/C MIN (Note 6)	TYP (Note 7)	MAX	UNIT
DYNAMIC	Switching Time Of Multiplexer		$t_{transition}$	See Figure 1			0.6	1		0.6		µs
	Break-Before-Make Interval		t_{open}	See Figure 3			0.2			0.2		µs
	Enable Turn-ON Time		$t_{on(EN)}$	See Figure 2			1	1.5		1		µs
	Enable Time-OFF Time		$t_{off(EN)}$	See Figure 2			0.4	1		0.4		µs
	OFF Isolation (Note 8)		OIRR	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF V_S = 7VRMS, f = 500kHz			68			68		dB
	Source OFF Capacitance		$C_{S(off)}$	V_S = 0V	V_{EN} = 0V, f = 140kHz		5			5		pF
	Drain OFF Capacitance	DG508A	$C_{D(off)}$	V_D = 0V	V_{EN} = 0V, f = 140kHz		25			25		pF
		DG509A	$C_{D(off)}$	V_D = 0V	V_{EN} = 0V, f = 140kHz		12			12		pF
SUPPLY	Pos. Supply Current		I^+	V_{EN} = 2.4V	All V_A = 0V, or 2.4V		1.3	2.4		1.3	2.4	mA
	Neg. Supply Current		I^-	V_{EN} = 2.4V	All V_A = 0V, or 2.4V	-1.5	-0.7		-1.5	-0.7		mA
	Pos. Supply Current		I^+Stdby	V_{EN} = 0V	All V_A = 0V, or 2.4V		1.3	2.4		1.3	2.4	mA
	Neg. Supply Current		I^-Stdby	V_{EN} = 0V	All V_A = 0V, or 2.4V	-1.5	-0.7		-1.5	-0.7		mA

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 8: OFF isolation = 20 log $\frac{|V_S|}{|V_D|}$, V_S = input to "OFF" switch, V_D = output due to V_S.

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Switching Time Test Circuits

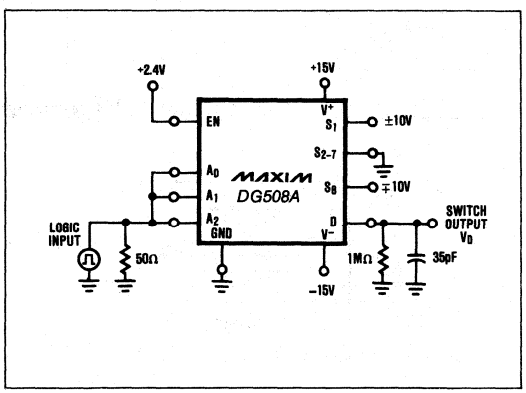

Figure 1(a). Switching Time Test Circuit (DG508A)

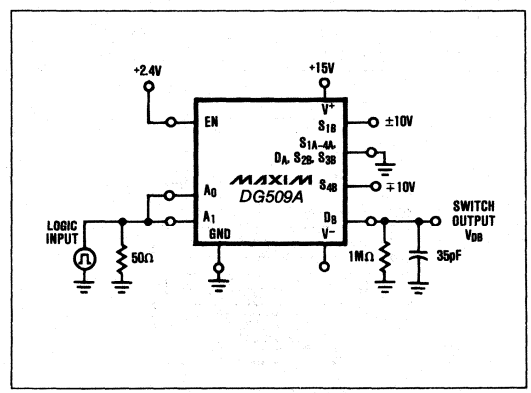

Figure 1(b). Switching Time Test Circuit (DG509A)

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C unless otherwise indicated)

	PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS DG508AA DG509AA MIN (Note 6)	TYP (Note 7)	MAX	LIMITS DG508AB/C DG509AB/C MIN (Note 6)	TYP (Note 7)	MAX	UNIT
DYNAMIC	**Switching Time Of Multiplexer**		$t_{transition}$	**See Figure 1**			**0.6**	**1**		**0.6**	**1**	
	Break-Before-Make Interval		t_{open}	See Figure 3			0.2			0.2		μs
	Enable Turn-ON Time		$t_{on(EN)}$	**See Figure 2**			**0.4**	**1**		**0.4**	**1.5**	
	Enable Time-OFF Time		$t_{off(EN)}$				**0.2**	**0.7**		**0.2**	**1**	
	OFF Isolation (Note 9)		OIRR	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF V_S = 7VRMS, f = 500kHz			68			68		dB
	Source OFF Capacitance		$C_{S(off)}$	V_S = 0V	V_{EN} = 0V, f = 140kHz		5			5		pF
	Drain OFF Capacitance	DG508A	$C_{D(off)}$	V_D = 0V			25			25		
		DG509A					12			12		
SUPPLY	**Pos. Supply Current**		I^+	V_{EN} = 2.4V	All V_A = 0V, or 2.4V		**0.02**	**0.2**		**0.02**	**0.2**	mA
	Neg. Supply Current		I^-			**-0.1**	**-0.01**		**-0.1**	**-0.01**		
	Pos. Supply Current		I^+Stdby	V_{EN} = 0V			**0.02**	**0.2**		**0.02**	**0.2**	
	Neg. Supply Current		I^-Stdby			**-0.1**	**-0.01**		**-0.1**	**-0.01**		
	Power Supply Range For Continuous Operation (Note 10)		V_{OP}			**±4.5**		**±18**	**±4.5**		**±18**	V

Note 10: Electrical characteristics, such as ON Resistance, will change when power supplies, other than ±15V, are used.

Switching Time Test Circuits

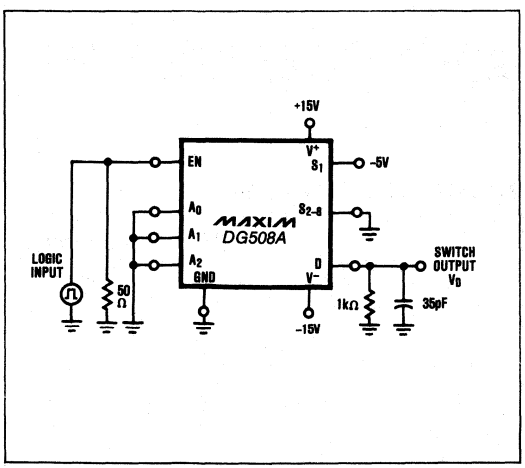

Figure 2(a). Enable Time Test Circuit (DG508A)

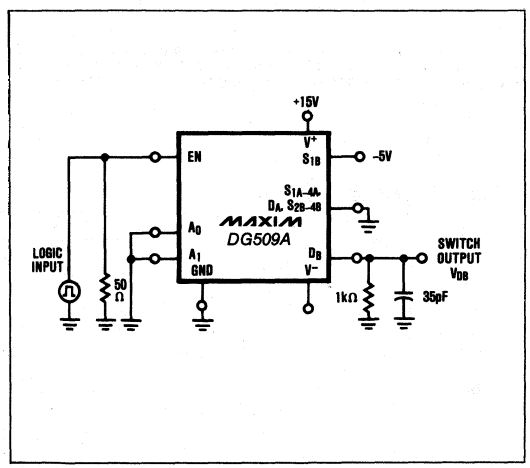

Figure 2 (b). Enable Time Test Circuit (DG509A)

Monolithic CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = +15V, V^- = -15V, Ground = 0V, T_A = Over Temperature Range unless otherwise noted)

	PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS DG508AA DG509AA MIN (Note 6)	TYP (Note 7)	MAX	LIMITS DG508AB/C DG509AB/C MIN (Note 6)	TYP (Note 7)	MAX	UNIT
SWITCH	Analog Signal Range		V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance		$r_{DS(on)}$	V_D = 10V, I_S = -200μA	Seq. Ea. Switch On V_{AL} = 0.8V, V_{AH} = 2.4V			500			550	Ω
				V_D = -10V, I_S = -200μA				500			500	
	Source OFF Leakage Current		$I_{S(off)}$	V_S = 10V, V_D = -10V	V_{EN} = 0V			50			50	nA
				V_S = -10V, V_D = 10V		-50			-50			
	Drain OFF Leakage Current	DG508A	$I_{D(off)}$	V_D = 10V, V_S = -10V				200			200	
				V_D = -10V, V_S = 10V		-200			-200			
		DG509A		V_D = 10V, V_S = -10V				100			100	
				V_D = -10V, V_S = 10V		-100			-100			
	Drain ON Leakage Current	DG508A	$I_{D(on)}$ (Note 8)	$V_{S(all)}$ = V_D = 10V	Seq. Ea. Switch On V_{AL} = 0.8V V_{AH} = 2.4V			200			200	
				$V_{S(all)}$ = V_D = -10V		-200			-200			
		DG509A		$V_{S(all)}$ = V_D = 10V				100			100	
				$V_{S(all)}$ = V_D = -10V		-100			-100			
INPUT	Address Input Current, Input Voltage High		I_{AH}	V_A = 2.4V		-30			-30			μA
				V_A = 15V				30			30	
	Address Input Current Input Voltage Low		I_{AL}	V_{EN} = 2.4V	All V_A = 0V	-30			-30			
				V_{EN} = 0V		-30			-30			

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 8: $I_{D(on)}$ is leakage from driver into "ON" switch.

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TRUTH TABLE—DG508A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE—DG509A

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTE: Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = +15V, V^- = -15V, Ground = 0V, T_A = Over Temperature Range unless otherwise noted)

	PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS DG508AA DG509AA MIN (Note 6)	TYP (Note 7)	MAX	LIMITS DG508AB/C DG509AB/C MIN (Note 6)	TYP (Note 7)	MAX	UNIT
SWITCH	Analog Signal Range		V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance		$r_{DS(on)}$	V_D = 10V, I_S = -200μA	Seq. Ea. Switch On V_{AL} = 0.8V, V_{AH} = 2.4V			400			450	Ω
				V_D = -10V, I_S = -200μA				400			450	
	Source OFF Leakage Current		$I_{S(off)}$	V_S = 10V, V_D = -10V	V_{EN} = 0V			50			50	nA
				V_S = -10V, V_D = 10V		-50			-50			
	Drain OFF Leakage Current	DG508A	$I_{D(off)}$	V_D = 10V, V_S = -10V				200			100	
				V_D = -10V, V_S = 10V		-200			-100			
		DG509A		V_D = 10V, V_S = -10V				100			100	
				V_D = -10V, V_S = 10V		-100			-100			
	Drain ON Leakage Current	DG508A	$I_{D(on)}$ (Note 8)	$V_{S(all)}$ = V_D = 10V	Seq. Ea. Switch On V_{AL} = 0.8V V_{AH} = 2.4V			200			100	
				$V_{S(all)}$ = V_D = -10V		-200			-100			
		DG509A		$V_{S(all)}$ = V_D = 10V				100			100	
				$V_{S(all)}$ = V_D = -10V		-100			-100			
INPUT	Address Input Current, Input Voltage High		I_{AH}	V_A = 2.4V		-30			-30			μA
				V_A = 15V				30			30	
	Address Input Current Input Voltage Low		I_{AL}	V_{EN} = 2.4V	All V_A = 0V	-30			-30			
				V_{EN} = 0V		-30			-30			

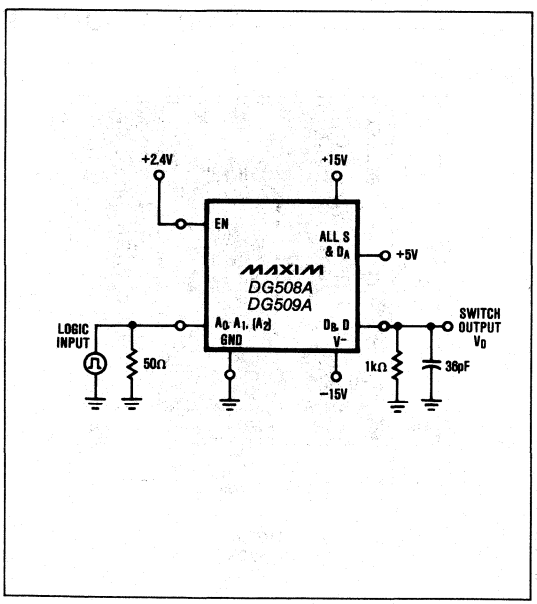


Figure 3. Break-Before-Make Test Circuit

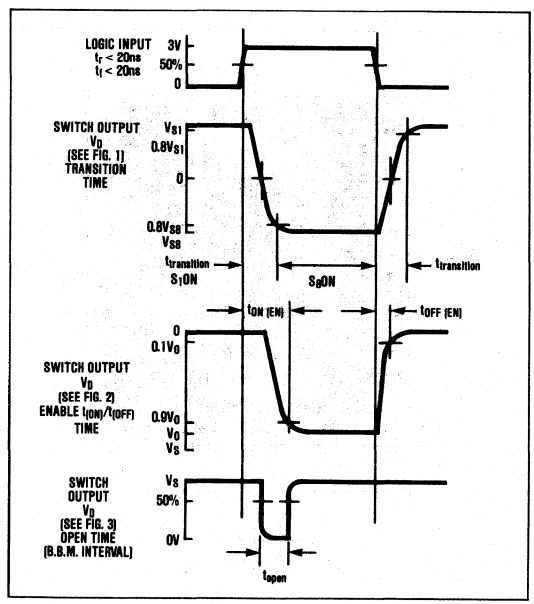
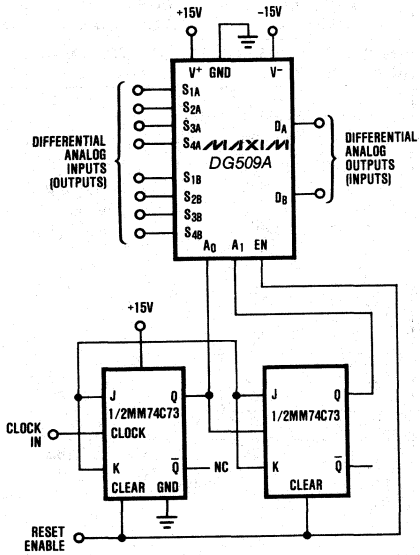


Figure 4. Timing Diagram For Figure 1, 2 & 3

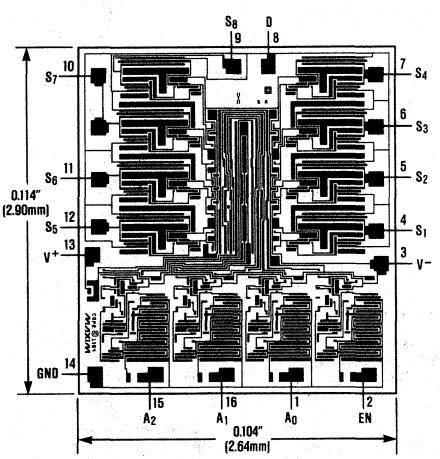
Monolithic CMOS Analog Multiplexers

Typical Operating Circuit

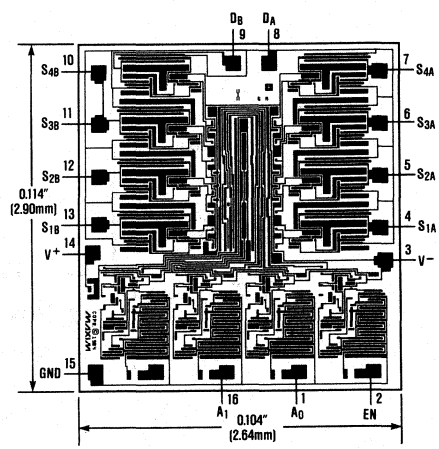


Differential 4 Channel Sequential Mux/Demux

Chip Topography



DG508A
(IH6108)



DG509A
(IH6208)

MAXIM

Analog Switches

Part Number	Function*	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current (I^+/I^- mA max)	Features	Page No.
MAX331	4 SPST NC	175	5	600	450	0.8/2.4	0.01/0.01	Improved DG201	12-1
MAX332	4 SPST NO	175	5	600	450	0.8/2.4	0.01/0.01	Imrpoved DG202	12-9
MAX333	4 SPDT	175	5	1000	500	0.8/2.4	0.25/0.25	Most switches/	12-17
MAX334	4 SPST NC	50	1	120	75	0.8/3.0		pkg. High Speed, with break before make	12-21
DG200A	2 SPST NC	70	2	1000	500	0.8/2.4	0.3/0.01	Low Power	12-31
DG201A	4 SPST NC	175	5	600	450	0.8/2.4	0.1/0.1	Low Power	12-1
DG202	4 SPST NO	175	5	600	450	0.8/2.4	0.1/0.1	Normally Open	12-9
DG211	4 SPST NC	175	5	1000	500	0.8/2.4	0.1/0.1	No V_{LOGIC} Supply	12-1
DG212	4 SPST NO	175	5	1000	500	0.8/2.4	0.1/0.1	Normally Open	12-9
DG300/A	2 SPST NO	50	5	300	250	0.8/2.4	0.5/0.1	$2.4V_{IH}$, Low R_{ON}	12-37
DG301/A	SPDT	50	5	300	250	0.8/2.4	0.5/0.1	$2.4V_{IH}$, Low R_{ON}	12-37
DG302/A	2 SPST NO	50	5	300	250	0.8/2.4	0.5/0.1	$2.4V_{IH}$, Low R_{ON}	12-37
DG303/A	DPDT	50	5	300	250	0.8/2.4	0.5/0.1	$2.4V_{IH}$, Low R_{ON}	12-37
DG304/A	2 SPST NO	50	5	250	150	3.5/11	0.5/0.1	CMOS Logic	12-43
DG305/A	SPDT	50	5	250	150	3.5/11	0.5/0.1	levels, high	12-43
DG306/A	2 DPST NO	50	5	250	150	3.5/11	0.5/0.1	speed, Low R_{ON}	12-43
DG307/A	2 DPDT	50	5	250	150	3.5/11	0.5/0.1		12-43
DG381/A	2 SPST NC	50	5	300	250	0.8/4.0	0.5/0.1	Low R_{ON}	12-49
DG384/A	2 DPDT NO	50	5	300	250	0.8/4.0	0.5/0.1	Low R_{ON}	12-49
DG387/A	SPDT	50	5	300	250	0.8/4.0	0.5/0.1	Low R_{ON}	12-49
DG390/A	2 SPDT	50	5	300	250	0.8/4.0	0.5/0.1	Low R_{ON}	12-49
IH5040	SPST NO	80	5	400	200	0.8/2.4	0.01/0.01	Very Low Power	12-55
IH5041	2 SPST NO	80	5	400	200	0.8/2.4	0.01/0.01	Very Low Power	12-55
IH5042	SPDT	80	5	400	200	0.8/2.4	0.01/0.01	Very Low Power	12-55
IH5043	2 SPDT	80	5	400	200	0.8/2.4	0.01/0.01	Very Low Power	12-55
IH5044	DPST NO	80	5	400	200	0.8/2.4	0.01/0.01	Very Low Power	12-55
IH5045	2 DPST NO	80	5	400	200	0.8/2.4	0.01/0.01	Very Low Power	12-55
IH5048	SPDT NO	45	5	1000	500	0.8/2.4	0.01/0.01	Low Charge Injection	12-59
IH5049	2 SPST NO	45	5	1000	500	0.8/2.4	0.01/0.01	Low Charge Injection	12-59
IH5050	SPDT NO	45	5	1000	500	0.8/2.4	0.01/0.01	Low Charge Injection	12-59
IH5051	2 SPDT	45	5	1000	500	0.8/2.4	0.01/0.01	Low Charge Injection	12-59
IH5140	SPST NO	50	0.1	150	125	0.8/2.4	0.01/0.01	Fast; Low Power	12-63
IH5141	2 SPST NO	50	0.1	150	125	0.8/2.4	0.01/0.01	Fast; Low Power	12-63
IH5142	SPDT	50	0.1	200	125	0.8/2.4	0.01/0.01	Fast; Low Power	12-63
IH5143	2 SPDT	50	0.1	200	125	0.8/2.4	0.01/0.01	Fast; Low Power	12-63
IH5144	DPST NO	50	0.1	200	125	0.8/2.4	0.01/0.01	Fast; Low Power	12-63
IH5145	2 DPST NO	50	0.1	200	125	0.8/2.4	0.01/0.01	Fast; Low Power	12-63

High Voltage Analog Switches

Part Number	Function*	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current (I^+/I^- mA max)	Features	Page No.
MAX341	2 SPST NO	75	60	1000	750	3.5/12	0.3/0.02	High Voltage,	12-25
MAX343	2 SPDT	75	60	1000	750	3.5/12	0.3/0.02	±50V Operation	12-25
MAX345	2 DPST NO	75	60	1000	750	3.5/12	0.3/0.02	with ±50V	12-25
MAX348	2 SPST NO	45	60	1000	750	3.5/12	0.3/0.02	Analog Signal Range	12-25

NC – Normally Closed, NO – Normally Open

MAXIM

Quad SPST CMOS Analog Switches

General Description

The MAX331, DG201A and DG211 are normally closed, quad single-pole-single-throw (SPST) analog switches. These CMOS switches can be continuously operated with power supplies ranging from ±4.5V to ±18V. Maxim guarantees that these switches will not latch-up if the power supplies are disconnected with input signals still connected.

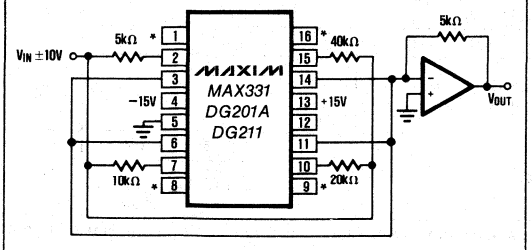
All three devices have guaranteed break-before-make switching. The MAX331 and DG201A differ with the DG211 primarily in switching speeds. The MAX331 and DG201A have a maximum turn-off time of 450ns and a maximum turn-on time of 600ns. The DG211 has a maximum turn-off time of 500ns and a maximum turn-on time of 1000ns.

Compared to the original manufacturer's products, Maxim's DG201A and DG211 consume significantly lower power, making them better suited for portable applications. By specifying the MAX331, the customer is guaranteed low power consumption units. Maxim has also eliminated the need for the third (V_L) power supply that is required for the operation of the original manufacturer's DG211.

Applications

Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Head up Displays
Military Radios

Typical Operating Circuit



Programmable Gain Amplifier

Note: * Pins 1, 8, 9 and 16 are logic control inputs.

Features

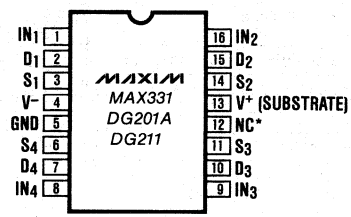
- **Improved 2nd Source! (See pages 3 and 5 for "MAXIM Advantage™")**
- **Guaranteed ±4.5V to ±18V Operation**
- **No V_L Supply Required**
- **Non-Latching with Supplies Turned-off and Input Signals Present**
- **CMOS and TTL Logic Compatible**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX331MJE	-55°C to +125°C	16 Lead CERDIP
DG201AAK	-55°C to +125°C	16 Lead CERDIP
DG201ABK	-25°C to +85°C	16 Lead CERDIP
DG201ACK	0°C to +70°C	16 Lead CERDIP
DG201ACJ	0°C to +70°C	16 Lead Plastic DIP
DG201ACSE	0°C to +70°C	16 Lead Small Outline
DG201C/D	0°C to +70°C	Dice
DG211CJ	0°C to +70°C	16 Lead Plastic DIP
DG211CSE	0°C to +70°C	16 Lead Small Outline
DG211C/D	0°C to +70°C	Dice

Pin Configuration

Top View



LOGIC	SWITCH
0	ON
1	OFF

Note: * Pin 12 can be left open or connected to a logic supply voltage.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Quad SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS (DG211)

V^+ to V^- 40V
V_{IN} to Ground ..... V^-, V^+
V_L to Ground ..... -0.3V, 25V
V_S or V_D to V^+ ..... 0, -40V
V_S or V_D to V^- 0, 40V
V^+ to Ground 25V
V^- to Ground ..... -25V
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1msec, 10% duty cycle max) 70mA

Storage Temperature ..... -65°C to +125°C
Operating Temperature ..... 0°C to +70°C
Power Dissipation (Note 1)
16 Pin Plastic DIP (Note 2) 470mW
16 Pin Small Outline (SE) (Note 3) 400mW

Note 1: Device mounted with all leads soldered to PC board.
Note 2: Derate 6.5mW/°C above +25°C.
Note 3: Derate 7mW/°C above +25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG211)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN (Note 4)	LIMITS TYP (Note 5)	LIMITS MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	V
	Drain-Source ON Resistance	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA			115	175	Ω
	Source OFF Leakage Current	$I_{S\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain OFF Leakage Current	$I_{D\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	5.0	
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain ON Leakage Current (Note 6)	$I_{D\ (on)}$	V_S = V_D = 14V, V_{IN} = 0.8V			0.1	5.0	
			V_S = V_D = -14V, V_{IN} = 0.8V		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit V_S = 2V, R_L = 1kΩ, C_L = 35pF			460	1000	ns
	Turn-OFF Time	t_{off1}				360	500	
		t_{off2}				450		
	Source OFF Capacitance	$C_{S\ (off)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz			5		pF
	Drain OFF Capacitance	$C_{D\ (off)}$	V_D = 0V, V_{IN} = 5V, f = 1MHz			5		
	Channel ON Capacitance	$C_{D+S(on)}$	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz			16		
	OFF Isolation (Note 7)	OIRR	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz			70		dB
	Crosstalk (Channel to Channel)	CCRR				90		
SUPPLY	Positive Supply Current	I^+	V_{IN} = 0V and 2.4V			0.35	0.48	mA
	Negative Supply Current	I^-				0.30	0.48	
	Logic Supply Current	I_L				0.5	1.2	

Note 4: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
Note 5: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 6: $I_{D(on)}$ is leakage from driver into "ON" switch.
Note 7: OFF Isolation = $20 \log \frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.

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Quad SPST CMOS Analog Switches

- ♦ Significantly Reduced Power Consumption
- ♦ Third (Logic) Supply Not Required
- ♦ Fault Protected

ABSOLUTE MAXIMUM RATINGS (DG211) This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS (DG211): Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN (Note 4)	LIMITS TYP (Note 5)	LIMITS MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	V
	Drain-Source ON Resistance	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA			115	175	Ω
	Source OFF Leakage Current	$I_{S\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain OFF Leakage Current	$I_{D\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	5.0	
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain ON Leakage Current (Note 6)	$I_{D\ (on)}$	V_S = V_D = 14V, V_{IN} = 0.8V			0.1	5.0	
			V_S = V_D = -14V, V_{IN} = 0.8V		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit V_S = 2V, R_L = 1kΩ, C_L = 35pF			460	1000	ns
	Turn-OFF Time	t_{off1}				360	500	
		t_{off2}				450		
	Source OFF Capacitance	$C_{S\ (off)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz			5		pF
	Drain OFF Capacitance	$C_{D\ (off)}$	V_D = 0V, V_{IN} = 5V, f = 1MHz			5		
	Channel ON Capacitance	$C_{D+S\ (on)}$	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz			16		
	OFF Isolation (Note 8)	OIRR	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz			70		dB
	Crosstalk (Channel to Channel)	CCRR				90		
SUPPLY	**Positive Supply Current**	**I^+**	**V_{IN} = 0V and 2.4V**			**0.02**	**0.1**	**mA**
	Negative Supply Current	**I^-**				**0.01**	**0.1**	
	Logic Supply Current	**I_L**				**0.0**	**0.0**	
	Power Supply Range for Continuous Operation	**V_{OP}**			**±4.5**		**±18**	**V**

Note 8: Electrical characteristics, such as ON Resistance, will change when power supplies, other than ±15V, are used.

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Quad SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS (MAX331, DG201A)

Voltages Referenced to V⁻
- V⁺ 44V
- GND 25V

Digital Inputs (Note 1), V_S, V_D ..... -2V to (V^+ +2V) or 20mA, whichever occurs first

Current, Any Terminal Except S or D 30mA

Continuous Current, S or D 20mA

Peak Current, S or D (Pulsed at 1msec, 10% duty cycle max.) 70mA

Operating Temperature
- DG201A (A Suffix) ..... -55°C to +125°C
- (B Suffix) ..... -25°C to +85°C
- (C Suffix) ..... 0°C to +70°C
- MAX331MJE ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

Power Dissipation (Note 2)
- 16 Pin CERDIP (Note 3) 900mW
- 16 Pin Plastic DIP (Note 4) 470mW
- 16 Pin Small Outline (SE) (Note 5) 400mW

Note 1: Signals on S_X, D_X, or IN_X exceeding V^+ or V^- on Maxim's MAX331 and DG201A will be clamped by internal diodes, and are also internally current limited to 25mA.
Note 2: Device mounted with all leads soldered to PC board.
Note 3: Derate 12mW/°C above +75°C.
Note 4: Derate 6.5mW/°C above +25°C.
Note 5: Derate 7mW/°C above +25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG201A)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS DG201AA MIN (Note 6)	DG201AA TYP (Note 7)	DG201AA MAX	LIMITS DG201AB,C MIN (Note 6)	DG201AB,C TYP (Note 7)	DG201AB,C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA			115	175		115	200	Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-5.0	-0.02					
	Drain OFF Leakage Current	$I_{D(off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	
				V_S = -14V, V_D = 14V	-5.0	-0.02					
	Drain ON Leakage Current (Note 8)	$I_{D(on)}$	V_S = -14V, V_{IN} = 0.8V			0.1	1.0		0.1	5.0	
			V_D = 14V, V_{IN} = 0.8V		-1.0	-0.15		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0		0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit			480	600		480	600	ns
	Turn-OFF Time	t_{off_1}				370	450		370	450	
	Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω			20			20		pC
	Source OFF Capacitance	$C_{S(off)}$	V_S = 0V, V_{IN} = 5V	f = 140kHz		5			5		pF
	Drain OFF Capacitance	$C_{D(off)}$				5			5		
	Channel ON Capacitance	$C_{D(on)}$ + $C_{S(on)}$	V_D = V_S = 0V, V_{IN} = 0V			16			16		
	OFF Isolation		V_{IN} = 5V, Z_L = 75Ω			70			70		dB
	Crosstalk (Channel to Channel)		V_S = 2.0V, f = 100kHz			90			90		
SUPPLY	Positive Supply Current	I^+	All Channels ON or OFF			0.9	2		0.9	2	mA
	Negative Supply Current	I^-			-1	-0.3		-1	-0.3		

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 8: $I_{D(on)}$ is leakage from driver into "ON" switch.

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Quad SPST CMOS Analog Switches

◆ **Significantly Reduced Power Consumption** ◆ **Lower Input Current Over Temperature**

◆ **No Input Current Spike**

ABSOLUTE MAXIMUM RATINGS (MAX331, DG201A)

This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS (MAX331, DG201A):

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MAX331/DG201AA MIN (Note 6)	MAX331/DG201AA TYP (Note 7)	MAX331/DG201AA MAX	DG201AB,C MIN (Note 6)	DG201AB,C TYP (Note 7)	DG201AB,C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance (Note 9)	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA			115	175		115	200	Ω
	Source OFF Leakage Current	$I_{S\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-1.0	-0.02		-5.0	-0.02		
	Drain OFF Leakage Current	$I_{D\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	
				V_S = -14V, V_D = 14V	-1.0	-0.02		-5.0	-0.02		
	Drain ON Leakage Current (Note 8)	$I_{D\ (on)}$	V_S = -14V, V_{IN} = 0.8V			0.1	1.0		0.1	5.0	
			V_D = 14V, V_{IN} = 0.8V		-1.0	-0.15		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0		0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit			480	600		480	600	ns
	Turn-OFF Time	t_{off_1}				370	450		370	450	
	Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω			20			20		pC
	Source OFF Capacitance	$C_{S\ (off)}$	V_S = 0V, V_{IN} = 5V	f = 140kHz		5			5		pF
	Drain OFF Capacitance	$C_{D\ (off)}$				5			5		
	Channel ON Capacitance	$C_{D\ (on)}$ + $C_{S\ (on)}$	V_D = V_S = 0V, V_{IN} = 0V			16			16		
	OFF Isolation		V_{IN} = 5V, Z_L = 75Ω			70			70		dB
	Crosstalk (Channel to Channel)		V_S = 2.0V, f = 100kHz			90			90		
SUPPLY	**Positive Supply Current**	**I^+**	**All Channels ON or OFF**			**0.02**	**0.1**		**0.02**	**0.1**	mA
	Negative Supply Current	**I^-**	**All Channels ON or OFF**		**-0.1**	**-0.01**		**-0.1**	**-0.01**		
	Power Supply Range for Continuous Operation	**V_{OP}**			**±4.5**		**±18**	**±4.5**		**±18**	V

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 8: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 9: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V, are used.

Quad SPST CMOS Analog Switches

ELECTRICAL CHARACTERISTICS (DG201A)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = Full Operating Temperature Range)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS DG201AA MIN (Note 6)	DG201AA TYP (Note 7)	DG201AA MAX	LIMITS DG201AB,C MIN (Note 6)	DG201AB,C TYP (Note 7)	DG201AB,C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA				250			250	Ω
	Source OFF Leakage Current	$I_{S\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V			100			100	nA
				V_S = -14V, V_D = 14V	-100			-100			
	Drain OFF Leakage Current	$I_{D\ (off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V			100			100	
				V_S = -14V, V_D = 14V	-100			-100			
	Drain ON Leakage Current (Note 10)	$I_{D\ (on)}$	V_S = -14V, V_{IN} = 0.8V				200			200	
			V_D = 14V, V_{IN} = 0.8V		-200			-200			
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0			-10			μA
			V_{IN} = 15V				-10			-10	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-10			-10			

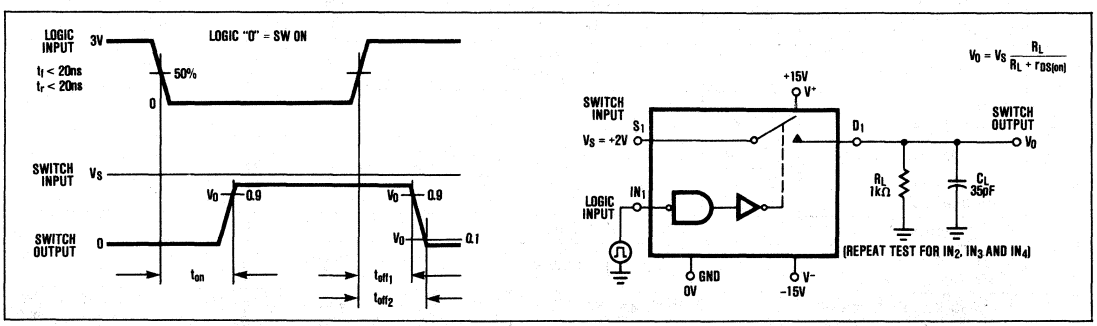
Note 10: $I_{D(on)}$ is leakage from driver into "ON" switch.

The electrical characteristics above are a reproduction of a portion of Siliconix's copyrighted 1985 data book. This information does not constitute any representation by Maxim that Siliconix's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Switching Time Test Circuit

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be +ve or -ve as per switching times test circuit.

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



Typical $R_{DS(ON)}$ vs. Power Supplies for Maxim's MAX331, DG201A and DG211

POWER SUPPLIES	$R_{DS(ON)}$ AT ANALOG SIGNAL LEVEL					
	-5V	+5V	-10V	+10V	-15V	+15V
±5V	350Ω	380Ω				
±10V			165Ω	250Ω		
±15V			125Ω	160Ω	135Ω	155Ω

ELECTRICAL CHARACTERISTICS (MAX331, DG201A):

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = full operating temperature range)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MAX331/DG201AA MIN (Note 6)	MAX331/DG201AA TYP (Note 7)	MAX331/DG201AA MAX	DG201AB,C MIN (Note 6)	DG201AB,C TYP (Note 7)	DG201AB,C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance (Note 11)	$r_{DS(on)}$	V_D = ±10V, V_{IN} = 0.8V, I_S = 1mA				250			250	Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V			100			100	nA
				V_S = -14V, V_D = 14V	-100			-100			
	Drain OFF Leakage Current	$I_{D(off)}$	V_{IN} = 2.4V	V_S = 14V, V_D = -14V			100			100	
				V_S = -14V, V_D = 14V	-100			-100			
	Drain ON Leakage Current (Note 10)	$I_{D(on)}$	V_S = -14V, V_{IN} = 0.8V				200			200	
			V_D = 14V, V_{IN} = 0.8V		-200			-200			
INPUT	**Input Current With Input Voltage High**	I_{INH}	**V_{IN} = 2.4V**		**-1.0**			**-1.0**			µA
			V_{IN} = 15V				**1.0**			**1.0**	
	Input Current With Input Voltage Low	I_{INL}	**V_{IN} = 0V**		**-1.0**			**-1.0**			

Note 10: $I_{D(on)}$ is leakage from driver into "ON" switch.
Note 11: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V, are used.

Protecting Against Fault Conditions

Fault conditions occur when power supplies are turned off when input signals are still present or when over voltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased and conduct current from the signal source. If this current is required to be kept to low (µA) levels then the addition of external protection diodes is recommended.

To provide protection for over-voltages up to 20V above the supplies, a 1N4001 or 1N914 type diode should be placed in series with the positive and negative supplies as shown in Fig. 1. The addition of these diodes will reduce the analog signal range to 1 volt below the positive supply and 1 volt above the negative supply.

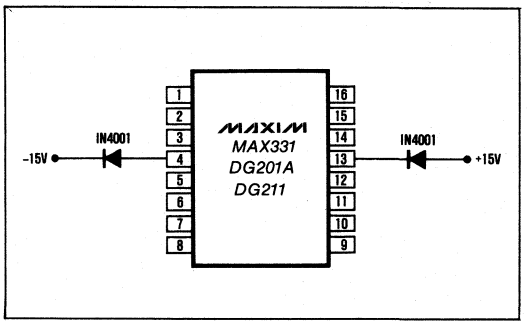


Figure 1. Protection Against Fault Conditions

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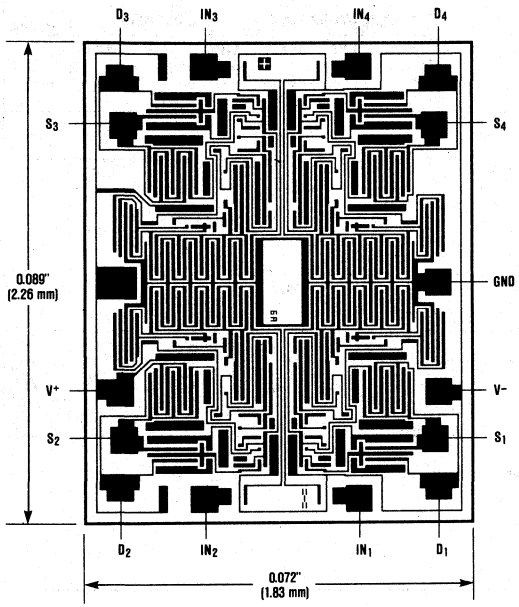
Quad SPST CMOS Analog Switches

Chip Topography



Quad SPST CMOS Analog Switches

General Description

Maxim's MAX332, DG202 and DG212 are normally open, quad single-pole-single-throw (SPST) analog switches. These CMOS switches can be continuously operated with power supplies ranging from ±4.5V to ±18V. Maxim guarantees that the MAX332 and DG202/212 will not latch up if their power supplies are disconnected with input signals still connected.

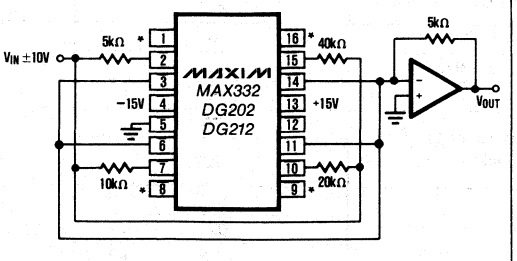
The MAX332 and DG202/DG212 are similar to the DG201 and DG211 except for inverted control inputs. All devices have guaranteed break-before-make switching as well as essentially constant on resistance over the analog signal range. All switches conduct current in either direction and add no offset to the output signal.

Compared to the original manufacturers products, Maxim's MAX332 and DG202/DG212 consume very little power, making them ideally suited for portable applications. Maxim has also eliminated the need for the third logic power supply (V_L), required when operating the original manufacturer's DG212, without sacrificing compatibility.

Applications

Analog Multiplexers
Programmable Gain Amplifiers
Communications Systems
Sample/Holds
Automatic Test Equipment
PBX, PABX

Typical Operating Circuit



Programmable Gain Amplifier

Note: *Pins 1, 8, 9 and 16 are logic control inputs.

Features

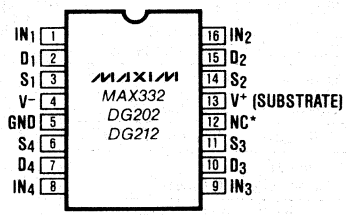
- **Improved 2nd Source! (See pages 3 and 5 for "MAXIM Advantage™")**
- **Guaranteed ±4.5V to ±18V Operation**
- **No V_L Supply Required**
- **Non-Latching with Supplies Turned-off and Input Signals Present**
- **CMOS and TTL Logic Compatible**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX332MJE	-55°C to +125°C	16 Lead CERDIP
DG202C/D	0°C to +70°C	Dice
DG202CJ	0°C to +70°C	16 Lead Plastic DIP
DG202CSE	0°C to +70°C	16 Lead Small Outline
DG202CK	0°C to +70°C	16 Lead CERDIP
DG202BSE	-25°C to +85°C	16 Lead Small Outline
DG202BK	-25°C to +85°C	16 Lead CERDIP
DG202AK	-55°C to +125°C	16 Lead CERDIP
DG212C/D	0°C to +70°C	Dice
DG212CJ	0°C to +70°C	16 Lead Plastic DIP
DG212CSE	0°C to +70°C	16 Lead Small Outline

Pin Configuration

Top View



LOGIC	SWITCH
0	OFF
1	ON

Note: *Pin 12 can be left open or connected to a logic supply voltage.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Quad SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS (DG212)

V^+ to V^- 40V
V_{IN} to Ground ..... V^-, V^+
V_L to Ground ..... -0.3V, 25V
V_S or V_D to V^+ ..... 0, -40V
V_S or V_D to V^- 0, 40V
V^+ to Ground 25V
V^- to Ground ..... -25V
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1msec, 10% duty cycle max) 70mA

Storage Temperature ..... -65°C to +125°C
Operating Temperature ..... 0°C to +70°C
Power Dissipation (Note 1)
16 Pin Plastic DIP (Note 2) 470mW
16 Pin Small Outline (SE) (Note 3) 400mW

Note 1: Device mounted with all leads soldered to PC board.

Note 2: Derate 6.5mW/°C above +25°C.

Note 3: Derate 7mW/°C above +25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG212)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN (Note 4)	LIMITS TYP (Note 5)	LIMITS MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA			115	175	Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain OFF Leakage Current	$I_{D(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	5.0	
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain ON Leakage Current (Note 6)	$I_{D(on)}$	V_S = V_D = 14V, V_{IN} = 2.4V			0.1	5.0	
			V_S = V_D = -14V, V_{IN} = 2.4V		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit V_S = 2V, R_L = 1kΩ, C_L = 35pF			460	1000	ns
	Turn-OFF Time	t_{off1}				360	500	
		t_{off2}				450		
	Source OFF Capacitance	$C_{S(off)}$	V_S = 0V, V_{IN} = 0V, f = 1MHz			5		pF
	Drain OFF Capacitance	$C_{D(off)}$	V_D = 0V, V_{IN} = 0V, f = 1MHz			5		
	Channel ON Capacitance	$C_{D+S(on)}$	V_D = V_S = 5V, V_{IN} = 0V, f = 1MHz			16		
	OFF Isolation (Note 7)	OIRR	V_{IN} = 0V, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz			70		dB
	Crosstalk (Channel to Channel)	CCRR				90		
SUPPLY	Positive Supply Current	I^+	V_{IN} = 0V and 2.4V			0.35	0.48	mA
	Negative Supply Current	I^-				0.30	0.48	
	Logic Supply Current	I_L				0.5	1.2	

Note 4: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

Note 5: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 6: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 7: OFF Isolation = $20 \log \frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.

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Quad SPST CMOS Analog Switches

- ♦ Significantly Reduced Power Consumption
- ♦ Third (Logic) Supply Not Required
- ♦ Fault Protected

ABSOLUTE MAXIMUM RATINGS (DG212): This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS (DG212): Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN (Note 4)	LIMITS TYP (Note 5)	LIMITS MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	V
	Drain-Source ON Resistance	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA			115	175	Ω
	Source OFF Leakage Current	$I_{S\ (off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain OFF Leakage Current	$I_{D\ (off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	5.0	
				V_S = -14V, V_D = 14V	-5.0	-0.02		
	Drain ON Leakage Current (Note 6)	$I_{D\ (on)}$	V_S = V_D = 14V, V_{IN} = 2.4V			0.1	5.0	
			V_S = V_D = -14V, V_{IN} = 2.4V		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit V_S = 2V, R_L = 1kΩ, C_L = 35pF			460	1000	ns
	Turn-OFF Time	t_{off1}				360	500	
		t_{off2}				450		
	Source OFF Capacitance	$C_{S\ (off)}$	V_S = 0V, V_{IN} = 0V, f = 1MHz			5		pF
	Drain OFF Capacitance	$C_{D\ (off)}$	V_D = 0V, V_{IN} = 0V, f = 1MHz			5		
	Channel ON Capacitance	$C_{D+S(on)}$	V_D = V_S = 0V, V_{IN} = 5V, f = 1MHz			16		
	OFF Isolation (Note 8)	OIRR	V_{IN} = 0V, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz			70		dB
	Crosstalk (Channel to Channel)	CCRR				90		
SUPPLY	**Positive Supply Current**	**I^+**	**V_{IN} = 0V and 2.4V**			**0.02**	**0.1**	mA
	Negative Supply Current	**I^-**				**0.00001**	**0.1**	
	Logic Supply Current	**I_L**				**0.0**	**0.0**	
	Power Supply Range for Continuous Operation	**V_{OP}**			**±4.5**		**±18**	V

Note 8: Electrical characteristics, such as ON Resistance, will change when power supplies, other than ±15V, are used.

Quad SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS (DG202)

Voltages Referenced to V⁻
- V^+ 44V
- GND 25V

Digital Inputs (Note 1), V_S, V_D ..... -2V, to (V^+ +2V) or 20mA, whichever occurs first

Current, Any Terminal Except S or D 30mA

Continuous Current, S or D 20mA

Peak Current, S or D (Pulsed at 1msec, 10% duty cycle max.) 70mA

Operating Temperature
- DG202 (A Suffix) ..... -55°C to +125°C
- (B Suffix) ..... -25°C to +85°C
- (C Suffix) ..... 0°C to +70°C
- MAX332MJE ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

Power Dissipation (Note 2)
- 16 Pin CERDIP (Note 3) 900mW
- 16 Pin Plastic DIP (Note 4) 470mW
- 16 Pin Small Outline (SE) (Note 5) 400mW

Note 1: Signals on S_X, D_X, or IN_X exceeding V^+ or V^- on Maxim's MAX332 and DG202 will be clamped by internal diodes, and are also internally current limited to 25mA.
Note 2: Device mounted with all leads soldered to PC board.
Note 3: Derate 12mW/°C above +75°C.
Note 4: Derate 6.5mW/°C above +25°C.
Note 5: Derate 7mW/°C above +25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG202)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS DG202A MIN (Note 6)	DG202A TYP (Note 7)	DG202A MAX	LIMITS DG202B,C MIN (Note 6)	DG202B,C TYP (Note 7)	DG202B,C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA			115	175		115	200	Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-5.0	-0.02					
	Drain OFF Leakage Current	$I_{D(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	
				V_S = -14V, V_D = 14V	-5.0	-0.02					
	Drain ON Leakage Current (Note 8)	$I_{D(on)}$	V_S = -14V, V_{IN} = 2.4V			0.1	1.0		0.1	5.0	
			V_D = 14V, V_{IN} = 2.4V		-1.0	-0.15		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0		0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit			480	600		480	600	ns
	Turn-OFF Time	t_{off}				370	450		370	450	
	Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω			20			20		pC
	Source OFF Capacitance	$C_{S(off)}$	V_S = 0V, V_{IN} = 0V	f = 140kHz		5			5		pF
	Drain OFF Capacitance	$C_{D(off)}$				5			5		
	Channel ON Capacitance	$C_{D(on)}$ + $C_{S(on)}$	V_D = V_S = 0V, V_{IN} = 5V			16			16		
	OFF Isolation		V_{IN} = 0V, Z_L = 75kΩ			70			70		dB
	Crosstalk (Channel to Channel)		V_S = 2.0V, f = 100kHz			90			90		
SUPPLY	Positive Supply Current	I^+	All Channels ON or OFF			0.9	2		0.9	2	mA
	Negative Supply Current	I^-	All Channels ON or OFF		-1	-0.3		-1	-0.3		

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 8: $I_{D(on)}$ is leakage from driver into "ON" switch.

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Quad SPST CMOS Analog Switches

- ♦ Significantly Reduced Power Consumption
- ♦ Lower Input Current Over Temperature
- ♦ No Input Current Spike

ABSOLUTE MAXIMUM RATINGS (MAX332, DG202): This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS (MAX332, DG202): Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MAX332/DG202A MIN (Note 6)	MAX332/DG202A TYP (Note 7)	MAX332/DG202A MAX	DG202B,C MIN (Note 6)	DG202B,C TYP (Note 7)	DG202B,C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance (Note 9)	$r_{DS\ (on)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA			115	175		115	200	Ω
	Source OFF Leakage Current	$I_{S\ (off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	nA
				V_S = -14V, V_D = 14V	-1.0	-0.02		-5.0	-0.02		
	Drain OFF Leakage Current	$I_{D\ (off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V		0.01	1.0		0.01	5.0	
				V_S = -14V, V_D = 14V	-1.0	-0.02		-5.0	-0.02		
	Drain ON Leakage Current (Note 8)	$I_{D\ (on)}$	V_S = -14V, V_{IN} = 2.4V			0.1	1.0		0.1	5.0	
			V_D = 14V, V_{IN} = 2.4V		-1.0	-0.15		-5.0	-0.15		
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004		-1.0	-0.0004		μA
			V_{IN} = 15V			0.003	1.0		0.003	1.0	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-1.0	-0.0004		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit			480	600		480	600	ns
	Turn-OFF Time	t_{off_1}				370	450		370	450	
	Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω			20			20		pC
	Source OFF Capacitance	$C_{S\ (off)}$	V_S = 0V, V_{IN} = 0V	f = 140kHz		5			5		pF
	Drain OFF Capacitance	$C_{D\ (off)}$				5			5		
	Channel ON Capacitance	$C_{D\ (on)}$ + $C_{S\ (on)}$	V_D = V_S = 0V, V_{IN} = 5V			16			16		
	OFF Isolation		V_{IN} = 0V, Z_L = 75kΩ			70			70		dB
	Crosstalk (Channel to Channel)		V_S = 2.0V, f = 100kHz			90			90		
SUPPLY	**Positive Supply Current**	**I^+**	**All Channels ON or OFF**			**0.02**	**0.1**		**0.02**	**0.1**	**mA**
	Negative Supply Current	**I^-**	**All Channels ON or OFF**		**-0.1**	**-0.01**		**-0.1**	**-0.01**		
	Power Supply Range for Continuous Operation	**V_{OP}**			**±4.5**		**±18**	**±4.5**		**±18**	**V**

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
Note 8: $I_{D(on)}$ is leakage from driver into "ON" switch.
Note 9: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V, are used.

Quad SPST CMOS Analog Switches

ELECTRICAL CHARACTERISTICS (DG202)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = Full Operating Temperature Range)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS DG202A MIN (Note 6)	DG202A TYP (Note 7)	DG202A MAX	LIMITS DG202B,C MIN (Note 6)	DG202B,C TYP (Note 7)	DG202B,C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA			250			250		Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V			100			100	nA
				V_S = -14V, V_D = 14V	-100			-100			
	Drain OFF Leakage Current	$I_{D(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V			100			100	
				V_S = -14V, V_D = 14V	-100			-100			
	Drain ON Leakage Current (Note 10)	$I_{D(on)}$	V_S = -14V, V_{IN} = 2.4V				200			200	
			V_D = 14V, V_{IN} = 2.4V		-200			-200			
INPUT	Input Current With Input Voltage High	I_{INH}	V_{IN} = 2.4V		-1.0			-10			μA
			V_{IN} = 15V				-10			-10	
	Input Current With Input Voltage Low	I_{INL}	V_{IN} = 0V		-10			-10			

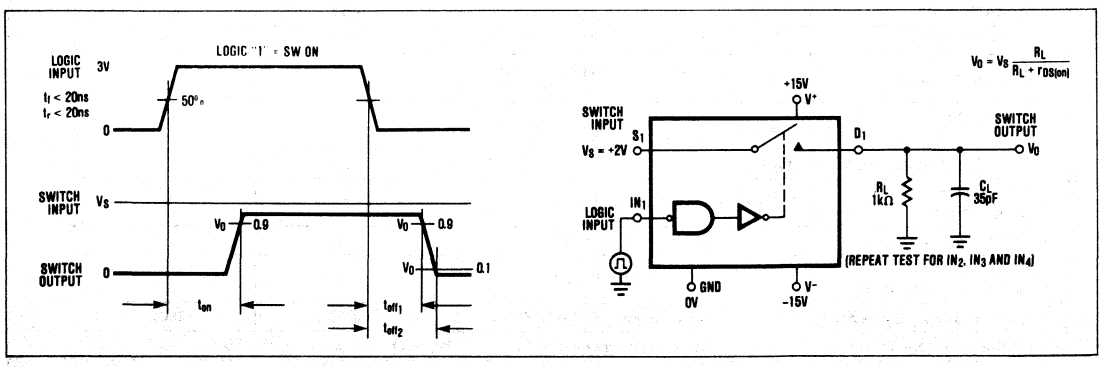
Note 10: $I_{D(on)}$ is leakage from driver into "ON" switch.

The electrical characteristics above are a reproduction of a portion of Siliconix's copyrighted 1985 data book. This information does not constitute any representation by Maxim that Siliconix's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Switching Time Test Circuit

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be +ve or -ve as per switching times test circuit.

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



Typical $R_{DS(ON)}$ vs. Power Supplies for Maxim's MAX332, DG202/DG212

POWER SUPPLIES	$R_{DS(ON)}$ AT ANALOG SIGNAL LEVEL -5V	+5V	-10V	+10V	-15V	+15V
±5V	350Ω	380Ω				
±10V			165Ω	250Ω		
±15V			125Ω	160Ω	135Ω	155Ω

ELECTRICAL CHARACTERISTICS (MAX332, DG202):

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = full operating temperature range)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MAX332/DG202A MIN (Note 6)	TYP (Note 7)	MAX	LIMITS DG202B,C MIN (Note 6)	TYP (Note 7)	MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance (Note 11)	$r_{DS(on)}$	V_D = ±10V, V_{IN} = 2.4V, I_S = 1mA				250			250	Ω
	Source OFF Leakage Current	$I_{S(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V			100			100	nA
				V_S = -14V, V_D = 14V	-100			-100			
	Drain OFF Leakage Current	$I_{D(off)}$	V_{IN} = 0.8V	V_S = 14V, V_D = -14V			100			100	
				V_S = -14V, V_D = 14V	-100			-100			
	Drain ON Leakage Current (Note 10)	$I_{D(on)}$	V_S = -14V, V_{IN} = 2.4V				200			200	
			V_D = 14V, V_{IN} = 2.4V		-200			-200			
INPUT	**Input Current With Input Voltage High**	I_{INH}	**V_{IN} = 2.4V**		**-1.0**			**-1.0**			µA
			V_{IN} = 15V				**1.0**			**1.0**	
	Input Current With Input Voltage Low	I_{INL}	**V_{IN} = 0V**		**-1.0**			**-1.0**			

Note 10: $I_{D(on)}$ is leakage from driver into "ON" switch.
Note 11: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V, are used.

Protecting Against Fault Conditions

Fault conditions occur when power supplies are turned off when input signals are still present or when over voltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased and conduct current from the signal source. If this current is required to be kept to low (µA) levels then the addition of external protection diodes is recommended.

To provide protection for over-voltages up to 20V above the supplies, a 1N4001 or 1N914 type diode should be placed in series with the positive and negative supplies as shown in Fig. 1. The addition of these diodes will reduce the analog signal range to 1 volt below the positive supply and 1 volt above the negative supply.

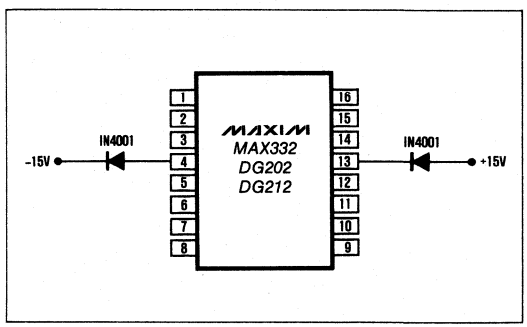


Figure 1. Protection Against Fault Conditions

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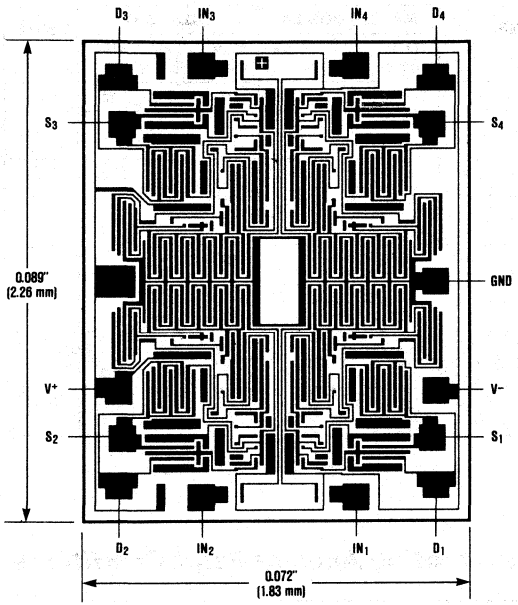
Quad SPST CMOS Analog Switches

Chip Topography



MAXIM

Quad SPDT CMOS Analog Switch

General Description

The MAX333 is a quad single-pole-double-throw (SPDT) analog switch. These four independent switches can be operated with bipolar power supplies ranging from ±5V to ±18V, or single-ended power supplies of +10V to +30V.

The MAX333 has break-before-make switching, (200ns typical), a maximum turn-off time of 500ns, and a maximum turn-on time of 1000ns.

The MAX333 is ideal for portable operation since quiescent current is only 250μA maximum with all inputs high, and less with all inputs low.

Logic inputs are fully TTL and CMOS compatible and guaranteed over a +0.8V to +2.4V range, regardless of supply voltage. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage. The MAX333 is a low-cost replacement for a DG211/DG212 pair when used as a quad SPDT switch.

Applications

Winchester Disk Drives

Test Equipment

Communications Systems

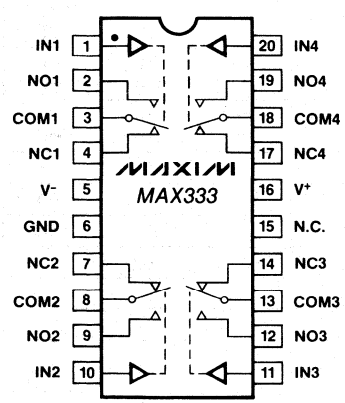
PBX, PABX

Head up Displays

Portable Instruments

Pin Configuration

TOP VIEW



SWITCHES ARE SHOWN WITH LOGICAL 0 INPUT

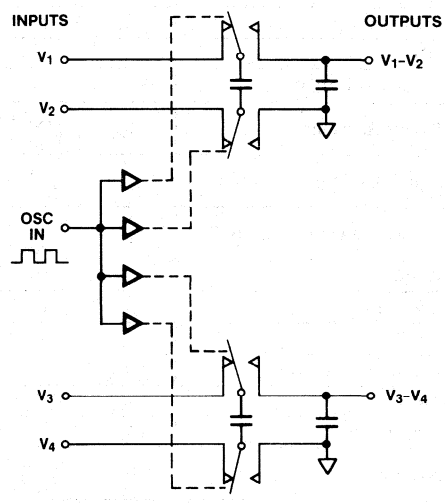
Features

- ◆ **Low Cost Per Channel**
- ◆ **Four Independent SPDT Switches**
- ◆ **Break-Before-Make Switching**
- ◆ **Guaranteed ±5V to ±18V Operation**
- ◆ **Guaranteed +10V to +30V Operation (Single Supply)**
- ◆ **No Separate Logic Supply Required**
- ◆ **CMOS and TTL Logic Compatible**
- ◆ **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX333CPP	0°C to +70°C	20 Lead Plastic DIP
MAX333C/D	0°C to +70°C	Dice
MAX333EPP	-40°C to +85°C	20 Lead Plastic DIP
MAX333MJP	-55°C to +125°C	20 Lead CERDIP
MAX333CWP	0°C to +70°C	20 Lead Wide SO
MAX333EWP	-40°C to +85°C	20 Lead Wide SO

Typical Operating Circuit



FLYING CAPACITOR LEVEL TRANSLATOR (2-CHANNEL)

Quad SPDT CMOS Analog Switch

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 36V
V_{IN}, V_{COM}, V_{NO} or V_{NC} ..... V^- to V^+
$|V_{NO} - V_{NC}|$ 32V
V^+ to Ground 30V
V^- to Ground ..... -30V
Current, Any Terminal Except V_{COM}, V_{NO}, or V_{NC} .. 30mA
Continuous Current, V_{COM}, V_{NO} or V_{NC} 20mA
Peak Current, V_{COM}, V_{NO} or V_{NC}
(Pulsed at 1msec, 10% duty cycle max) 70mA

Storage Temperature ..... -65°C to +150°C
Power Dissipation (Note 1)
20 Pin CERDIP (Note 2) 900mW
20 Pin Plastic DIP (Note 3) 600mW
20 Pin Small Outline (WE) (Note 4) 800mW

Note 1: Device mounted with all leads soldered to PC board.
Note 2: Derate 11.1mW/°C above 70°C.
Note 3: Derate 8mW/°C above 70°C.
Note 4: Derate 10mW/°C above 70°C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(GND = 0V, V^+ = +15V, V^- = -15V, T_A = +25°C, unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN (Note 5)	LIMITS TYP (Note 6)	LIMITS MAX	UNITS
SUPPLY						
Positive Supply Current	I^+			0.13	0.25	mA
Supply Voltage Range	V^+/V^-	Dual Supply; $\|V^+\| = \|V^-\|$	±5		±18	V
Supply Voltage Range	V^+	Single Supply; V^- = GND	+10		+30	V
Negative Supply Current	I^-			0.01	0.25	mA
LOGIC INPUT						
Input Voltage Low	V_{IL}		V^-		+0.8	V
Input Voltage High	V_{IH}		2.4		V^+	V
Input Current	I_{IN}	V_{IN} = V^-, V^+	-10	0.0001	+10	µA
SWITCH						
Analog Signal Range	V_{ANA}		V^-		V^+	V
ON Circuit Resistance	R_{ON}	V_{ANA} = +10V; I_{COM} = 1mA V_{ANA} = -10V; I_{COM} = 1mA		140 125	175 175	Ω Ω
ON Circuit Leakage Current	I_{ONL}	V_{ANA} = +14V; V_{OFF} = -14V V_{ANA} = -14V; V_{OFF} = +14V	-5 -5	0.1 0.2	+5 +5	nA nA
OFF Circuit Leakage Current	I_{OFF}	V_{ANA} = +14V; V_{OFF} = -14V V_{ANA} = -14V; V_{OFF} = +14V	-5 -5	0.01 0.02	+5 +5	nA nA
DYNAMIC						
Turn-off Time	t_{OFF}	(See Switching Time Test Circuit)		50	500	ns
Turn-on Time	t_{ON}			460	1000	ns
Break-before-make Time	t_{OPEN}		50	200		ns
Off Capacitance	C_{OFF}	V_{ANA} = 0V		5		pF
On Capacitance	C_{ON}	V_{ANA} = 0V		5		pF
Off Isolation	OIRR	f = 1MHz, Rl = 75Ω V_{ANA} = 2.3V_{RMS}		72		dB
Crosstalk	CCRR			78		dB

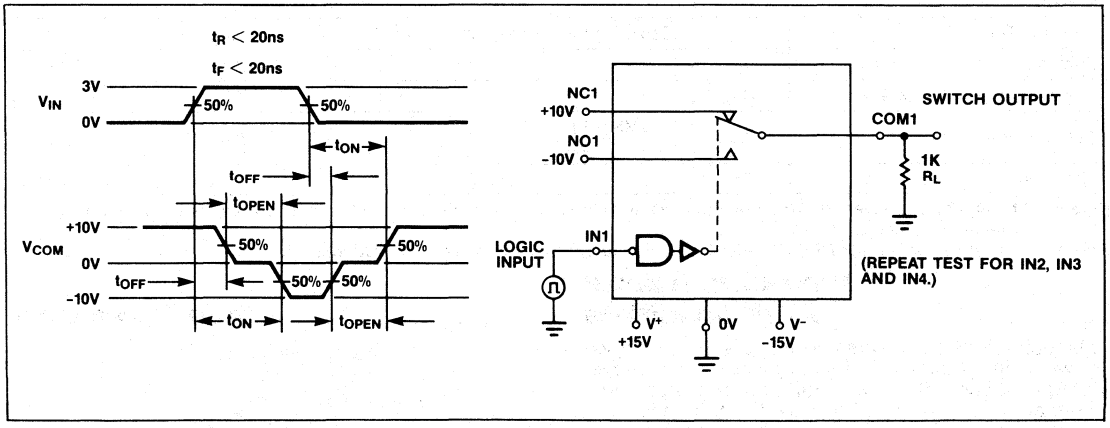
Note 5: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
Note 6: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

ELECTRICAL CHARACTERISTICS

(GND = 0V, V^+ = +15V, V^- = -15V, T_A = Full Operating Temperature Range, unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN (Note 5)	LIMITS TYP (Note 6)	LIMITS MAX	UNITS
LOGIC INPUT						
Input Voltage Low	V_{IL}		V^-		+0.8	V
Input Voltage High	V_{IH}		2.4		V^+	V
Input Current	I_{IN}	V_{IN} = V^-, V^+	-10	0.0001	+10	μA
SWITCH						
Analog Signal Range	V_{ANA}		V^-		V^+	V
ON Circuit Resistance	R_{ON}	V_{ANA} = +10V; I_{COM} = 1mA V_{ANA} = -10V; I_{COM} = 1mA		200 180	250 250	Ω Ω
ON Circuit Leakage Current	I_{ONL}	V_{ANA} = +15V; V_{OFF} = -15V V_{ANA} = -15V; V_{OFF} = +15V		200 200		nA nA
OFF Circuit Leakage Current	I_{OFF}	V_{ANA} = +15V; V_{OFF} = -15V V_{ANA} = -15V; V_{OFF} = +15V		100 100		nA nA

Switching Time Test Circuit



TYPICAL RDS(ON) & SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE

Power Supply Voltage	R_{ON} at Analog Signal Levels (Ω) -15V	-10V	-5V	0V	+5V	+10V	+15V	Quiescent Supply Current (μA)	Charge Injection (pC)
V^- = -15V, V^+ = +15V	117			109			153	130	12
V^- = -10V, V^+ = +10V		158		156		171		80	10
V^- = -5V, V^+ = +5V			297	303	288			30	8
V^- = GND, V^+ = +15V				200			212	115	
V^- = GND, V^+ = +10V				300	312	303		30	

Quad SPDT CMOS Analog Switch

ELECTRICAL CHARACTERISTICS (Single Supply)

(GND = 0V, V^+ = +12V, V^- = 0V, T_A = 25°C, unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN (Note 5)	LIMITS TYP (Note 6)	LIMITS MAX	UNITS
SUPPLY						
Supply Voltage Range	V^+	Single Supply; V^- = GND	+10		+30	V
Positive Supply Current	I^+			0.11	0.25	mA
INPUT						
Input Voltage Low	V_{INLO}		0		+0.8	V
Input Voltage High	V_{INHI}		2.4		V^+	V
Input Current	I_{IN}	V_{IN} = V^+, 0V			1	μA
SWITCH						
Analog Signal Range	V_{ANA}		V^-		V^+	V
ON Circuit Resistance	R_{ON}	V_{ANA} = +10V; I_{COM} = 1mA V_{ANA} = 0V; I_{COM} = 1mA		250 240	350 350	Ω Ω
ON Circuit Leakage Current	I_{ONL}	V_{ANA} = V^+; V_{OFF} = 0V V_{ANA} = 0V; V_{OFF} = V^+		0.05 0.05		nA nA
OFF Circuit Leakage Current	I_{OFF}	V_{ANA} = V^+ V_{ANA} = 0V		0.01 0.01		nA nA
DYNAMIC						
Turn-off Time	t_{OFF}	(See Switching Time Test Circuit)		65		ns
Turn-on Time	t_{ON}			700		ns
Break-before-make Time	t_{OPEN}			200		ns
Off Isolation	OIRR	f = 1MHz, Rl = 75Ω V_{ANA} = 2.3V_{RMS}		70		dB
Crosstalk	CCRR			72		dB

Note 5: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

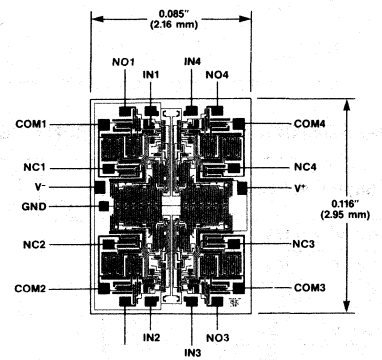
Note 6: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Protecting Against Fault Conditions

Fault conditions occur when power supplies are turned off when input signals are still present or when over voltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased and conduct current from the signal source. If this current is required to be kept to low (μA) levels then the addition of external protection diodes is recommended.

To provide protection for over-voltages up to 20V above the supplies, 1N4001 or 1N914 type diodes should be placed in series with the positive and negative supplies. The addition of these diodes will reduce the analog signal range to 1 volt below the positive supply and 1 volt above the negative supply.

Chip Topography



NOTE: NCx IS CONNECTED TO COMx WHEN INx IS LOW.

High Speed Quad SPST Analog Switch

General Description

The MAX334 is a quad single-pole-single-throw, normally closed (SPST, NC) analog switch, pin compatible with the Harris HI-201HS and Siliconix DG271. The MAX334 has guaranteed break-before-make switching ($t_{OFF} < t_{ON}$), while featuring fast switching speeds. Turn-on time is less than 100ns and turn-off time is less than 50ns; channel on resistance is 50 ohms maximum. CMOS inputs provide reduced input loading and very low leakage currents.

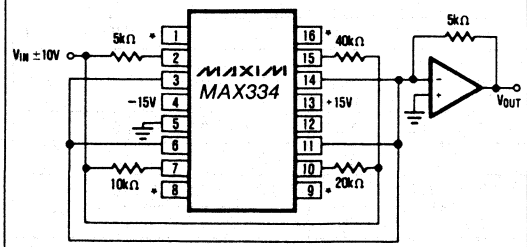
The MAX334 is also a direct replacement for the DG201 and DG211, featuring ¼ the on resistance and five times the speed.

The MAX334 may be used with split supplies (±5V to ±15V) or single positive supplies (+5V to +30V) while retaining CMOS and TTL logic compatible inputs, and maintaining high switching speed.

Applications

Sample and Hold Circuits
Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Heads-up Displays
Military Radios

Typical Operating Circuit



Programmable Gain Amplifier

Note: * Pins 1, 8, 9 and 16 are logic control inputs.

Features

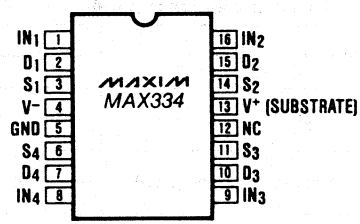
- **$R_{ds(ON)}$ 50Ω (max.)**
- **Guaranteed Break-Before-Make Switching**
- **Single or Bipolar Supply Operation**
- **CMOS and TTL Logic Compatible**
- **Faster, Lower R_{ON} Replacement for DG201 and DG211**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX334CPE	0°C to +70°C	16 Lead Plastic DIP
MAX334CWE	0°C to +70°C	16 Lead Wide SO
MAX334C/D	0°C to +70°C	Dice
MAX334CJE	0°C to +70°C	16 Lead CERDIP
MAX334EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX334EJE	-40°C to +85°C	16 Lead CERDIP
MAX334EWE	-40°C to +85°C	16 Lead Wide SO
MAX334MJE	-55°C to +125°C	16 Lead CERDIP

Pin Configuration

Top View



LOGIC	SWITCH
0	ON
1	OFF

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High Speed Quad SPST Analog Switch

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Between Pins 4 and 13) 36V
Digital Input Voltage (Pins 1, 8, 9, 16) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ −4V
Analog Input Voltage (S to D) ..... $+V_{SUPPLY}$ +2.0V
Pins 2, 3, 6, 7, 10, 11, 14, 15 ..... $-V_{SUPPLY}$ −2.0V
Peak Current, S or D 80mA
Total Power Dissipation (Note 1) 750mW

Maximum Junction Temperature ..... 175°C
Operating Temperature
MAX334M ..... −55°C to +125°C
MAX334E ..... −40°C to +85°C
MAX334C ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V^- = −15V, V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, unless otherwise specified.)

PARAMETER		TEMPERATURE	MAX334M/E			MAX334C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS									
V_S, Analog Signal Range		Full	−15		+15	−15		+15	V
R_{ON}, On Resistance (Note 2)		+25°C		30	50		30	50	Ω
		Full			75			75	
R_{ON} Match		+25°C		3			3		%
$I_{S(OFF)}$, Off Input Leakage Current	V_S = 14V, V_D = −14V	+25°C	−1	.3	1	−1	.3	1	nA
	V_S = −14V, V_D = 14V	Full	−100		100	−50		50	
$I_{D(OFF)}$, Off Output Leakage Current	V_D = 14V, V_S = −14V	+25°C	−1	.3	1	−1	.3	1	nA
	V_D = −14V, V_S = 14V	Full	−100		100	−50		50	
$I_{D(ON)}$, On Leakage Current	V_D = V_S = 14V	+25°C	−1	.1	1	−1	.1	1	nA
	V_D = V_S = −14V	Full	−100		100	−50		50	
DIGITAL INPUT CHARACTERISTICS									
V_{AL} Input Low		+25°C							V
		Full			0.8			0.8	
V_{AH} Input High		+25°C							V
		Full	3.0			3.0			
I_{AL}, Input Leakage Current (Low)		+25°C	−1.0	0.1	1.0	−1.0	0.1	1.0	μA
		Full	−10		10	−10		10	
I_{AH}, Input Leakage Current (High)		+25°C	−1.0	0.1	1.0	−1.0	0.1	1.0	μA
		Full	−10		10	−10		10	

Note 1: Derate 8mW/°C above T_A = 75°C, θ_{JA} = 100°C/W, θ_{JC} = 60°C/W
Note 2: V_{OUT} = ±10V, I_{OUT} = 1mA
Note 3: R_L = 1kΩ, C_L = 35pF, V_{IN} = +10V, V_A = +3V (See Switching Waveforms)
Note 4: V_A = 3V, R_L = 1kΩ, C_L = 10pF, V_{IN} = 3Vrms, f = 100kHz
Note 5: V_A = 3V, R_L = 1kΩ, f = 100kHz, V_{IN} = 3Vrms
Note 6: C_L = 1000pF, V_{IN} = 0V, R_{IN} = 0Ω, $\Delta Q = C_L \times \Delta V_0$
Note 7: V_A = 3V or V_A = 0 for all switches
Note 8: t_{BBM} is fastest turn-on time (of the four switches) minus the slowest turn-off time.

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +15V, V^- = -15V, V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, unless otherwise specified.)

PARAMETER	TEMPERATURE	MAX334M/E			MAX334C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
t_{ON}, Switch ON Time (Note 3)	+25°C		70	100		70	120	ns
t_{ON}, Switch ON Time (Note 3)	Full		100			125		ns
t_{OFF1}, Switch OFF Time (Note 3)	+25°C		40	50		40	75	ns
t_{OFF1}, Switch OFF Time (Note 3)	Full		50			75		ns
t_{OFF2}, Switch OFF Time (Note 3)	+25°C		150			150		ns
Output Settling Time 0.1%	+25°C		180			180		ns
t_{BBM}, Break-Before-Make (Note 8)	+25°C	10	30			30		ns
"Off Isolation" (Note 4)	+25°C		72			72		dB
Crosstalk (Note 5)	+25°C		86			86		dB
Charge Injection (Note 6)	+25°C		10			10		pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		10			10		pF
Output Switch Capacitance $C_{D(OFF)}$	+25°C		10			10		pF
Output Switch Capacitance $C_{D(ON)}$	+25°C		30			30		pF
C_A, Digital Input Capacitance	+25°C		18			18		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		.5			.5		pF
POWER REQUIREMENTS (Note 7)								
P_D, Power Dissipation	+25°C		120			120		mW
	Full							
I^+, Current (Pin 13)	+25°C		4.5			4.5		mA
	Full			10.0			10.0	
I^-, Current (Pin 4)	+25°C		3.5			3.5		mA
	Full			6			6	

Typical Single Supply Operation (V^- = GND, V_S = +10V, R_L = 1000 Ohms)

V^+	$R_{DS(ON)}$ (Ohms)	T_{ON} (ns)	T_{OFF} (ns)	TTL Compatible?	I_{V+} with TTL_{IN} = 3V on all switches
+5*	200	360	25	Yes	6.0μA
+10	85	150	30	Yes	1.5mA
+12	75	140	25	Yes	2.0mA
+15	65	100	25	Yes	4.5mA
+20	55	70	25	Yes	7.0mA
+25	50	50	30	V_{AH} = 4V	10.0mA
+30	45	45	40	V_{AH} = 4V	14.0mA

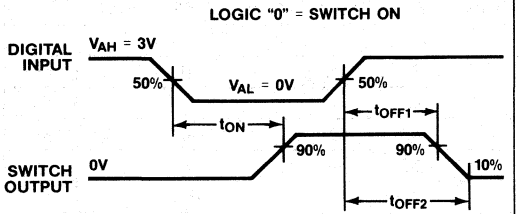
*V_S = +5V, for this case.

Typical Single Supply Charge Injection (C_L = 1000pF)

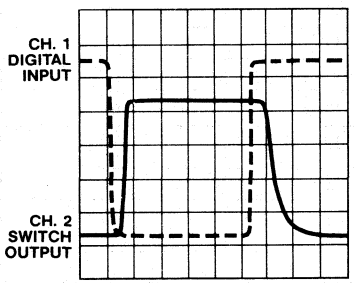
V_{ANALOG}	V^+ SUPPLY VOLTAGE				
	+5V	+10V	+15V	+20V	+30V
0V	7pC	10pC	10pC	6pC	12pC
V^+	4pC	6pC	6pC	6pC	14pC

High Speed Quad SPST Analog Switch

Switching Waveforms



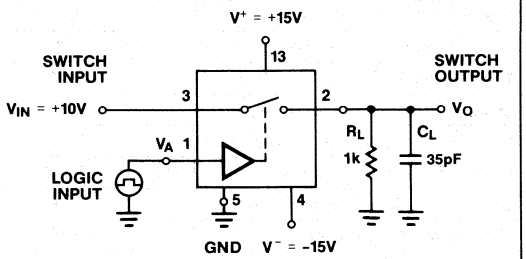
t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +3.0V



CH. 1 = 500.0mVOLTS/DIV
CH. 2 = 2.000 VOLTS/DIV
TIMEBASE = 100ns/DIV

Test Circuit

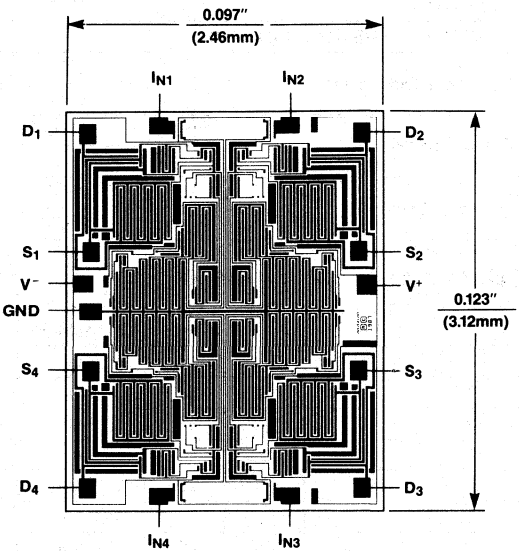
SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1}, t_{OFF2})



$$V_O = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

C_L INCLUDES $C_{FIXTURE}$ + C_{PROBE}

Chip Topography



MAXIM

High Voltage CMOS/DMOS Analog Switches

General Description

The MAX341/43/45/48 are CMOS/DMOS analog switches intended for high voltage use as well as high reliability general purpose applications. The operating supply range is ±20V to ±50V or +20V to +60V when using a single power supply. Signal handling capability extends from the negative to the positive supply voltage, i.e. over a 100V peak-to-peak range with ±50V power supplies.

The switch control inputs can be driven with CMOS or other high level logic signals. All switches are normally closed, i.e. an input "0" level turns the switch ON. The MAX341 and MAX348 are dual SPST switches, the MAX343 is a dual SPDT switch, and the MAX345's configuration is dual DPST. The MAX348 is a reduced R_{ON} version of the MAX341.

Positive supply current for all devices is less than 300μA and negative supply current is less than 100μA with ±50V power supplies. When using a single power supply and logic input levels equal to the supply value, the power supply currents are less than 20μA.

Applications

Medical Ultrasound Equipment
Automatic Test Equipment
Diagnostic Systems
48 Volt Telecom Systems
Stepper and DC Motor Drivers

Features

- ±20V to ±50V and Single Supply Operation
- R_{ON} Less than 55Ω (MAX348)
- -70dB Typical OFF Isolation at 1MHz
- Input Voltage Range Includes Power Supplies
- 100V peak-to-peak Signal Handling Capability
- Guaranteed Break-Before-Make Operation
- Completely Latchup-Proof Construction

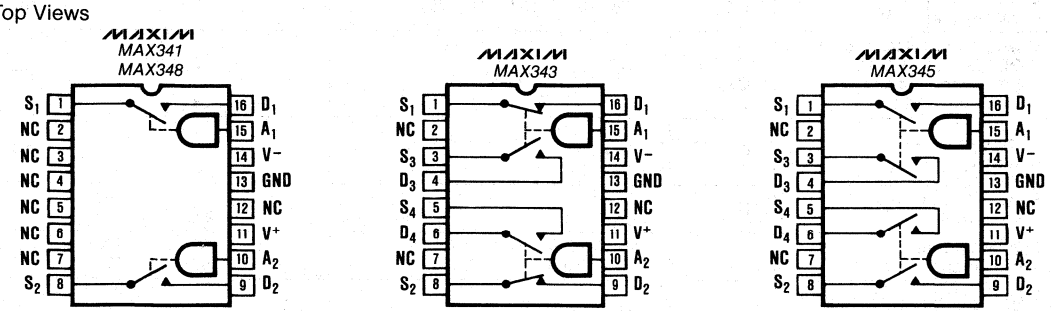
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX341C/D	0°C to +70°C	Dice
MAX341CPE	0°C to +70°C	16 Lead Plastic DIP
MAX341CWE	0°C to +70°C	16 Lead Wide SO
MAX341EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX341EWE	-40°C to +85°C	16 Lead Wide SO
MAX341EJE	-40°C to +85°C	16 Lead CERDIP
MAX341MJE	-55°C to +125°C	16 Lead CERDIP
MAX343C/D	0°C to +70°C	Dice
MAX343CPE	0°C to +70°C	16 Lead Plastic DIP
MAX343CWE	0°C to +70°C	16 Lead Wide SO
MAX343EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX343EWE	-40°C to +85°C	16 Lead Wide SO
MAX343EJE	-40°C to +85°C	16 Lead CERDIP
MAX343MJE	-55°C to +125°C	16 Lead CERDIP

(Ordering Information Continued on Last Page.)

Pin Configurations

Top Views



Dual SPST | Dual SPDT | Dual DPST

Switch States are for Logic "1" Input.

High Voltage CMOS/DMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- Voltage ..... +120V
V^+ to GND Voltage ..... +65V
Digital Input Voltage ..... V^- to V^+
Input Current
S and D ..... +200mA
All pins except S and D ..... ±30mA
Lead Temperature (Soldering 10 sec) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Operating Temperature Range
MAX34XC ..... 0°C to +70°C
MAX34XE ..... -40°C to +85°C
MAX34XM ..... -55°C to +125°C
Power Dissipation (16 pin packages)
CERDIP (derate 10mW/°C above +75°C) 750mW
Plastic DIP (derate 7.35mW/°C above +75°C) 550mW
Small Outline (derate 9mW/°C above +75°C) 680mW

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation at these or any other conditions above those indicated in the operations section of the specifications is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Over Temperature, V^+ = +50V, V^- = -50V, GND = 0V unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range	V_S, V_D		V^+		V^-	V
Channel ON Resistance MAX341/43/45 MAX341/43/45 MAX348 MAX348	R_{ON}	V_S = ±50V, I_S = 10mA T_A = +25°C Over Temp. T_A = +25°C Over Temp		80 35	110 160 55 80	Ω
ON Resistance Match	ΔR_{ON}	V_S = ±50V, I_S = 10mA		7		%
OFF Leakage Current (Figure 7)	$I_{D(OFF)}$, $I_{S(OFF)}$	V_S = ±50V, V_D = ∓50V T_A = +25°C Over Temp.		10 1000	50 5000	nA
ON Output Leakage Current (Figure 8)	$I_{D(ON)}$, $I_{S(ON)}$	V_S = V_D = ±50V T_A = +25°C Over Temp.		10 1000	60 5000	nA
Input Low Threshold	V_{AL}				3.5	V
Input High Threshold	V_{AH}		12			V
Input Current (Logic)	I_A	V_A = 0V to +15V		0.1	10	µA
Turn-On Time (Figure 9)	t_{ON}	T_A = +25°C Over Temp.		0.5	1.0 1.5	µs
Turn-Off Time (Figure 9)	t_{OFF}	T_A = 25°C Over Temp.		0.4	0.75 1.0	µs
OFF Isolation (Figure 4)	ISO_{OFF}	T_A = +25°C, 1MHz, R_L = 75Ω		-70		dB
Channel-Channel Crosstalk (Figure 5)	ISO_X	T_A = +25°C, 1MHz, R_L = 75Ω		-75		dB
Channel Input Capacitance OFF State, C to Gnd OFF State, C to Out ON State, C to Gnd	$C_{S(OFF)}$ $C_{SD(OFF)}$ $C_{S(ON)}$	T_A = +25°C, V_S = 0V		17 1 38		pF
Charge Injection (Figure 6)	Q	V_S = +50V V_S = 0V V_S = -50V		100 240 480		pC
Supply Current V^+ Current	I^+	T_A = +25°C Over Temp.		 200	300 600	µA
Supply Current V^- Current	I^-	T_A = +25°C Over Temp.		40 55	100 200	µA
Supply Voltage Range Split Supplies Single Supply		GND = 0V V^- = GND = 0V	±20 +20		±50 +60	V

Detailed Description

Analog Signal Range

The MAX341 family's analog signal range is equal to the power supply value, up to ±50V with split power supplies and +60V with a single power supply (V^- connected to GND). An ON switch is also capable of passing up to 0.5A on a peak current basis. Maximum continuous current is limited only by the package power dissipation (see Absolute Maximum Ratings)

ON Resistance

The ON resistance of the MAX341 series switches is typically 40Ω. R_{ON} does, however increase as the switch voltage (V_S) approaches V^+. For example, with ±50V supplies and a +50V analog signal, R_{ON} will be typically less than 100Ω (50Ω for the MAX348), and 45Ω (25Ω for the MAX348) for -50V signals. With ±50V power supplies, and ±40V switch voltages, R_{ON} is about 40Ω for the +40V case and 30Ω for the -40V case. ON resistance can be reduced and current handling capacity can be increased by connecting switches in parallel. This is especially useful in power switching applications. Table 1 and the graph in the Typical Characteristics section further describe the relation between R_{ON} and V^+.

Table 1: ON Resistance

V^+/V^-	R_{ON} AT $V_S = V^+$	R_{ON} AT $V_S = V^-$
+20V/-20V	127Ω	39Ω
+30V/-30V	105Ω	36Ω
+40V/-40V	92Ω	32Ω
+50V/-50V	84Ω	30Ω
+40V/GND	127Ω	39Ω
+60V/GND	105Ω	36Ω

Note:
Typical R_{ON} for the MAX348 is approximately one half of the above values.

Power Supply Current

The maximum supply current for V^+ and V^- at 25°C is 300μA and 100μA respectively. However, the positive supply current (I^+) is partly dependent on the input logic level and can be reduced if control signals of a larger amplitude than 0V and +15V are used. If the control inputs swing to within 4V of V^+ and V^- then I^+ drops to a typical value of 20μA.

Control Inputs

15V logic level inputs are required to turn switches on or off, but the control inputs can also accept levels up to V^+ and V^-. A input greater than 12V constitutes a "1" state (switch OFF), and an input less than 3.5V will constitute a "0" state (switch ON).

Standard TTL logic can be used with MAX341 series switches if a level shifter such as the MC14504 is used to drive the control inputs as shown in in figure 1. Open collector drivers, with external pull-up resistors, can be used in a similar fashion as well.

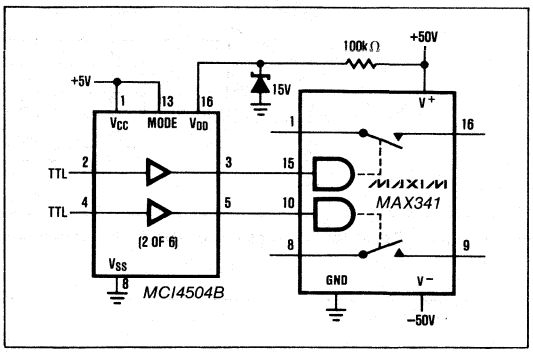


Figure 1. Using TTL Control Levels.

Applications

Flying Capacitor Input

A "flying capacitor" differential to single-ended converter takes advantage of the MAX343's wide input voltage range, which allows large common mode inputs to be rejected. As shown in Figure 2, a capacitor is alternately charged by the differential input signal and then is connected to an op-amp or A-to-D input. An instrumentation amplifier is not required since the output signal can be referenced to ground. Sample-hold operation is also built in to the design and the MAX343's break-before-make operation ensures that the output sees only the differential portion of the input signal. A similar approach can also be used for single-ended to differential signal conversion as well.

Parallel Switches

In designs where power switching ability is needed, any of the MAX341 series switches can be connected in parallel to increase current handling capability and reduce ON resistance. Applications such as ultrasonics, RF power, and DC motor drive are areas where this is often important. A MAX348 is shown in a parallel configuration in figure 3. The resulting SPST switch has a typical R_{ON} of 12Ω (5Ω for signals more than 10V below V^+) and can handle pulsed loads of up to 0.5 Amps. With ±50V power supplies, the peak-to-peak signal range is still 100V and 10MHz signals can be switched while maintaining typically -50dB of isolation.

High Voltage CMOS/DMOS Analog Switches

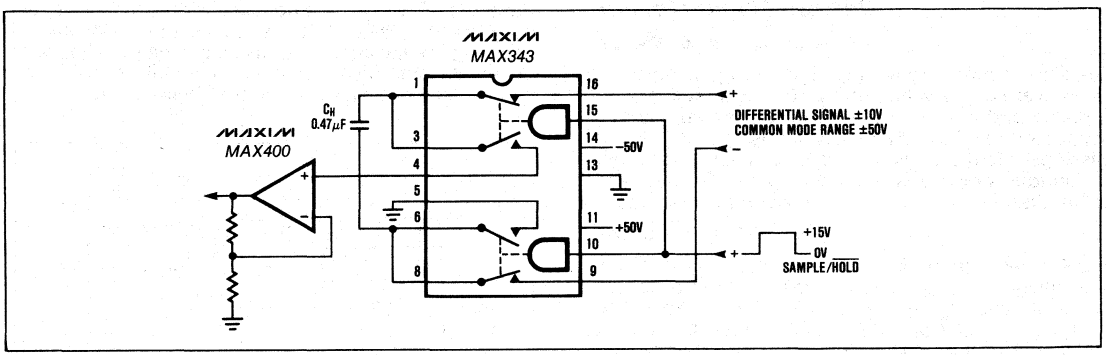


Figure 2. Flying Capacitor Differential to Single-Ended Converter with ±50V Common-Mode Range.

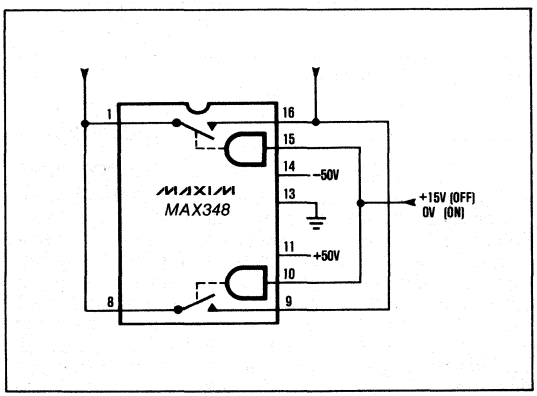


Figure 3. Minimum R_{ON} (5 to 10Ω typ.) High Voltage Switch.

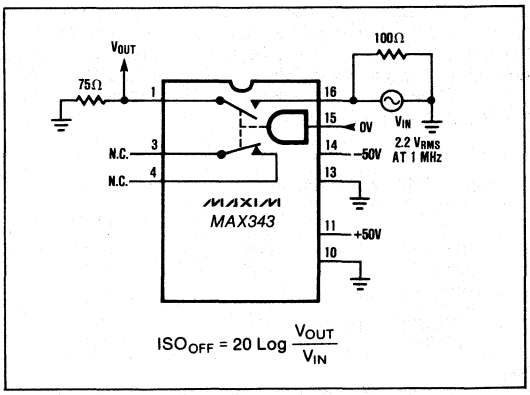


Figure 4. OFF Isolation Test Circuit.

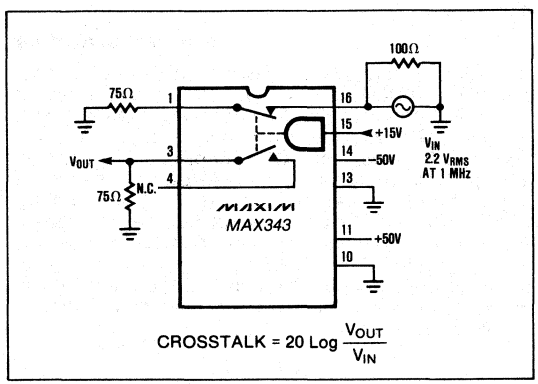


Figure 5. Channel-Channel Crosstalk Test Circuit.

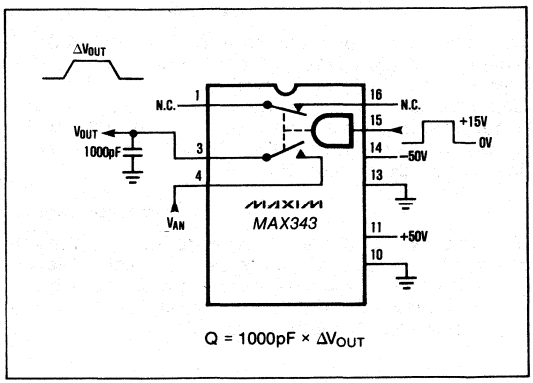
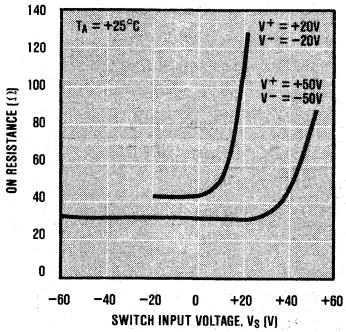


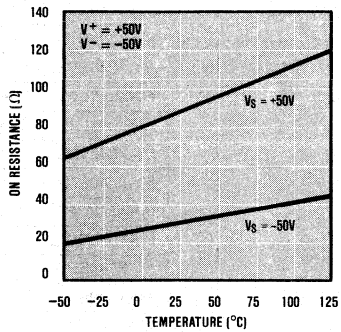
Figure 6. Charge Injection Test Circuit.

Typical Operating Characteristics

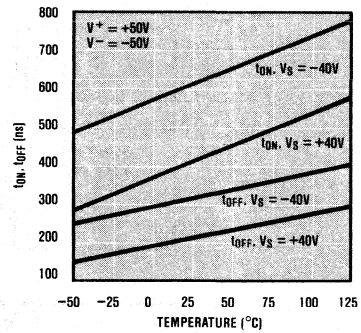
ON RESISTANCE vs. SWITCH INPUT VOLTAGE



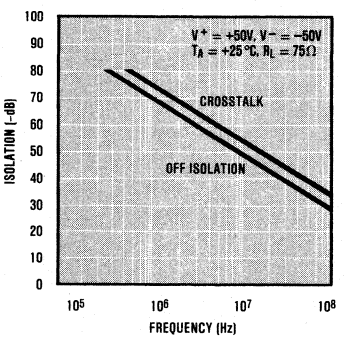
ON RESISTANCE vs. TEMPERATURE



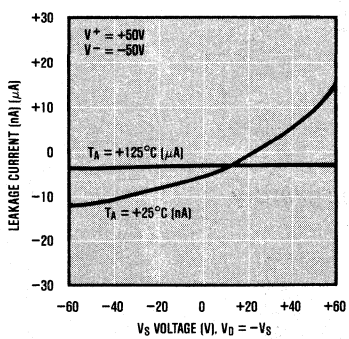
SWITCHING TIME vs. TEMPERATURE



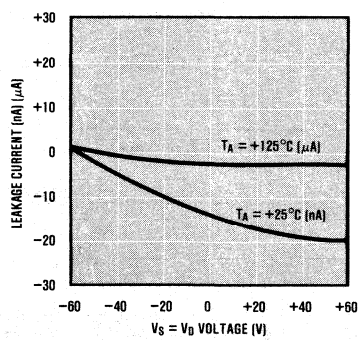
OFF ISOLATION AND CROSSTALK vs. FREQUENCY



OFF LEAKAGE vs. SWITCH VOLTAGE



ON LEAKAGE vs. SWITCH VOLTAGE



Test Circuits

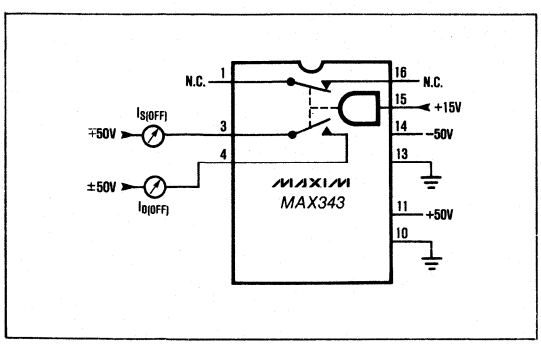


Figure 7. OFF Leakage Test Circuit.

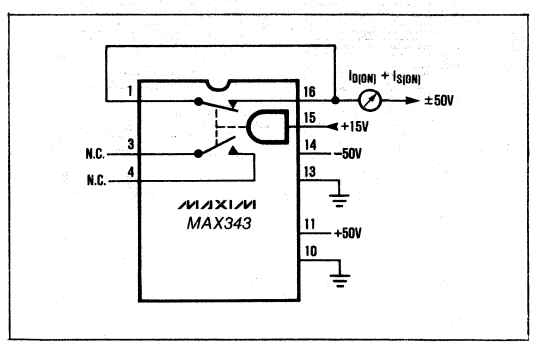


Figure 8. ON Leakage Test Circuit.

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High Voltage CMOS/DMOS Analog Switches

Test Circuit

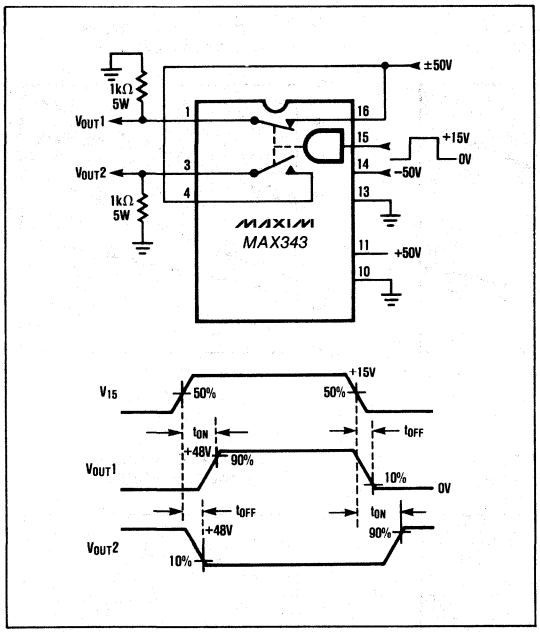
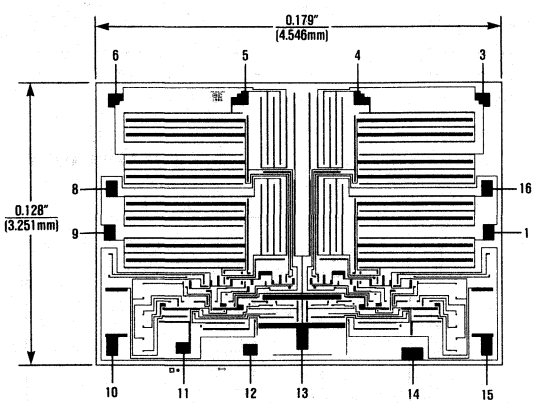


Figure 9. Switching Time Test Circuit.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX345C/D	0°C to +70°C	Dice
MAX345CPE	0°C to +70°C	16 Lead Plastic DIP
MAX345CWE	0°C to +70°C	16 Lead Wide SO
MAX345EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX345EWE	-40°C to +85°C	16 Lead Wide SO
MAX345EJE	-40°C to +85°C	16 Lead CERDIP
MAX345MJE	-55°C to +125°C	16 Lead CERDIP
MAX348C/D	0°C to +70°C	Dice
MAX348CPE	0°C to +70°C	16 Lead Plastic DIP
MAX348CWE	0°C to +70°C	16 Lead Wide SO
MAX348EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX348EWE	-40°C to +85°C	16 Lead Wide SO
MAX348EJE	-40°C to +85°C	16 Lead CERDIP
MAX348MJE	-55°C to +125°C	16 Lead CERDIP

Chip Topography



See Pin Configurations for pin functions.

MAXIM

Dual Monolithic SPST CMOS Analog Switch

General Description

The DG200A is a dual, normally closed, single-pole-single-throw (SPST) analog switch. This CMOS switch can be operated with power supplies ranging from ±4.5V to ±18V. The DG200A has guaranteed break-before-make switching. Its maximum turn-off time is 500ns, and its maximum turn-on time is 100ns.

Maxim guarantees that the DG200A will not latch-up if the power supplies are turned off with input signals still connected as long as absolute maximum ratings are not violated.

Compared to the original manufacturer's product, Maxim's DG200A consumes significantly lower power, making it better suited for portable applications.

Applications

Winchester Disk Drives
Test Equipment
Communications Systems
PBX, PABX
Guidance and Control Systems
Head up Displays
Military Radios

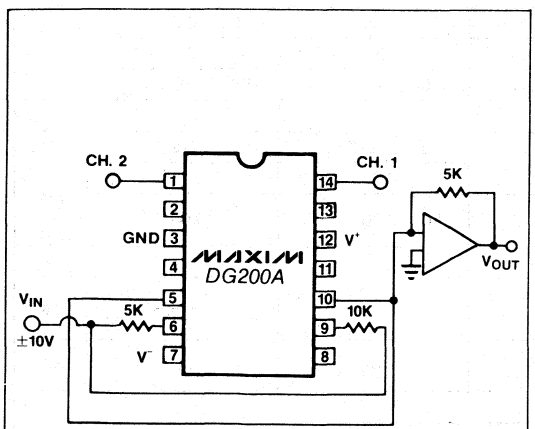
Features

- **Improved 2nd Source! Power Supply Current <300μA**
- **Wide Supply Range ±4.5V to ±18V**
- **Single Supply Operation**
- **Non-Latching with Supplies Turned-off and Input Signals Present**
- **CMOS and TTL Logic Compatible**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
DG200AAK	-55°C to +125°C	14 Lead CERDIP
DG200ABK	-25°C to +85°C	14 Lead CERDIP
DG200ACK	0°C to +70°C	14 Lead CERDIP
DG200ACJ	0°C to +70°C	14 Lead Plastic DIP
DG200ACY	0°C to +70°C	14 Lead Small Outline
DG200AC/D	0°C to +70°C	Dice
DG200AAA	-55°C to +125°C	10 Pin Metal Can
DG200ABA	-25°C to +85°C	10 Pin Metal Can
DG200ACA	0°C to +70°C	10 Pin Metal Can

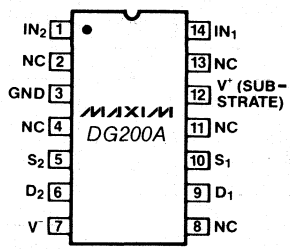
Typical Operating Circuit



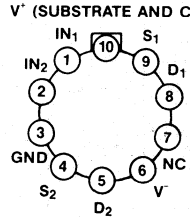
Programmable Gain Amplifier

Pin Configuration

Top View



V+ (SUBSTRATE AND CASE)



Dual Monolithic SPST CMOS Analog Switch

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V^-
V^+ 44V
GND 25V
Digital Inputs V_S, V_D (Note 1) ..... -2V to (V^+ + 2V) or 20mA, whichever occurs first.
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
(Pulsed at 1msec, 10% duty cycle max) 100mA
Storage Temperature (A & B Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... -25 to 85°C
Power Dissipation (Package)*
Metal Can** 450mW
14 Pin Ceramic DIP*** 825mW
14 Pin Plastic DIP**** 470mW
*All leads soldered or welded to PC board.
**Derate 6mW/°C above 75°C.
***Derate 11mW/°C above 75°C.
****Derate 6.5mW/°C above 25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS DG200A MIN (Note 2)	DG200A TYP (Note 3)	DG200A MAX	LIMITS DG200 B/C/D MIN (Note 2)	DG200 B/C/D TYP (Note 3)	DG200 B/C/D MAX	UNITS
SWITCH										
Analog Signal Range (Note 1)	V_{ANALOG}			-15		15	-15		15	V
Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10V, V_{in} = 0.8V, I_S = 1mA			45	70		45	80	Ω
Source OFF Leakage Current	$I_{S(off)}$	V_{in} = 2.4V	V_S = 14V, V_D = -14V		0.01	2.0		0.01	5.0	nA
			V_S = -14V, V_D = 14V	-2.0	-0.02		-5.0	-0.02		
Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V		0.01	2.0		0.01	5.0	
			V_S = 14V, V_D = -14V	-2.0	-0.02		-5.0	-0.02		
Drain ON Leakage Current (Note 4)	$I_{D(on)}$	V_{in} = 0.8V	V_S = V_D = 14V		0.1	2.0		0.1	5.0	
			V_S = V_D = -14V	-2.0	-0.1		-5.0	-0.1		
INPUT										
Input Current with Input Voltage High	I_{INH}	V_{in} = 2.4V, V_{in} = 15V		-1.0	0.0009		-1.0	0.0009		μA
					0.005	1.0		0.005	1.0	
Input Current with Input Voltage Low	I_{INL}	V_{in} = 0V		-1.0	-0.0015		-1.0	-0.0015		
DYNAMIC										
Turn-ON Time	t_{on}	See Switching Time Test Circuit (Figure 1)			440	1000		440	1000	ns
Turn-OFF Time	t_{off}				70	500		70	500	
Charge Injection	Q	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω (Figure 2)			10			10		pC
Source OFF Capacitance	$C_{S(off)}$	f = 140kHz, V_{in} = 5V or V_S = 0V	V_S = 0V		9.0			9.0		pF
Drain OFF Capacitance	$C_{D(off)}$		V_D = 0V		9.0			9.0		
Channel ON Capacitance	$C_{D(on)}$ + $C_{S(on)}$		V_D = V_S = 0V		25			25		
OFF Isolation Figure 3 (Note 5)		V_{in} = 5V, Z_L = 75Ω, V_S = 2.0V, f = 1MHz			75			75		dB
Crosstalk Figure 4 (Channel to Channel)					90			90		

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			DG200A			DG200 B/C/D			
			MIN (Note 2)	TYP (Note 3)	MAX	MIN (Note 2)	TYP (Note 3)	MAX	
SUPPLY									
Positive Supply Current	I+	Both Channels ON or OFF V_{in} = 0 and 2.4V		180	300		200	500	μA
Negative Supply Current	I-		-10	-0.1		-100	-0.1		

ELECTRICAL CHARACTERISTICS (Over Temperature)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = Over Temperature Range, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS					UNITS
				DG200A			DG200 B/C		
				MIN (Note 2)	TYP (Note 3)	MAX	MIN (Note 2)	TYP (Note 3)	MAX	
SWITCH										
Analog Signal Range (Note 1)	V_{ANALOG}			-15		15	-15		15	V
Drain-Source ON Resistance	$r_{DS(on)}$	V_D = ±10V, V_{in} = 0.8V, I_S = 1mA			100			100		Ω
Source OFF Leakage Current	$I_{S(off)}$	V_{in} = 2.4V	V_S = 14V, V_D = -14V		100			100		nA
			V_S = -14V, V_D = 14V	-100			-100			
Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V		100			100		
			V_S = 14V, V_D = -14V	-100			-100			
Drain ON Leakage Current (Note 4)	$I_{D(on)}$	V_{in} = 0.8V	V_S = V_D = 14V		200			200		
			V_S = V_D = -14V	-200			-200			
INPUT										
Input Current/ Voltage High	I_{INH}	V_{in} = 2.4V, V_{in} = 15V		-10			-10			μA
					10			10		
Input Current/ Voltage Low	I_{INL}	V_{in} = 0V		-10			-10			

Note 1: Signals on S_X, D_X, or IN_X, exceeding V^- or V^+ will be clamped by internal diodes. LIMIT FORWARD DIODE CURRENT to maximum current ratings.

Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

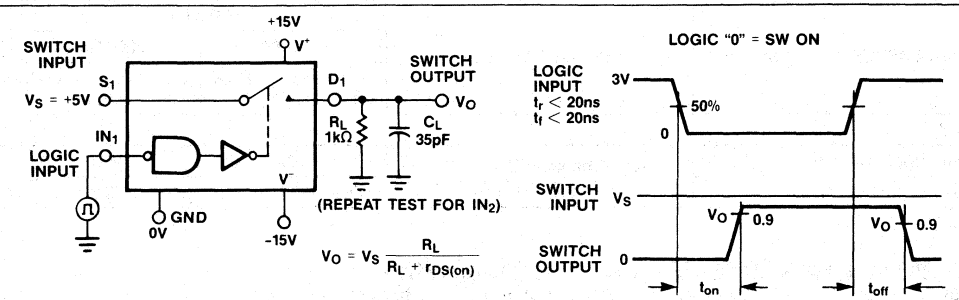
Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 4: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 5: "OFF" isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = output.

Dual Monolithic SPST CMOS Analog Switch

Test Circuits



NOTE: Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

Figure 1. Switching Time Test Circuit

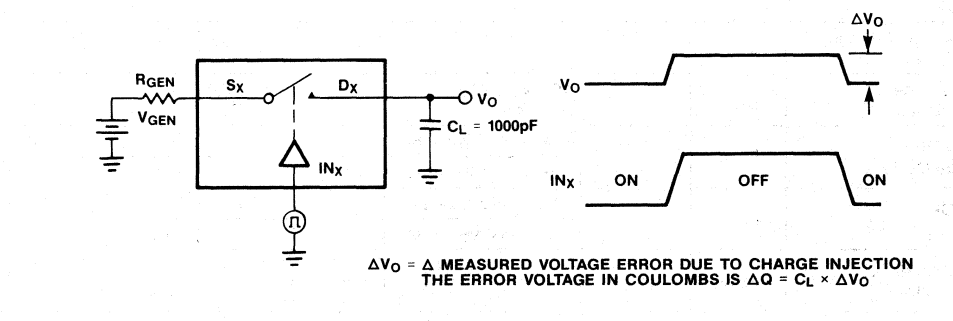


Figure 2. Charge Injection Test Circuit

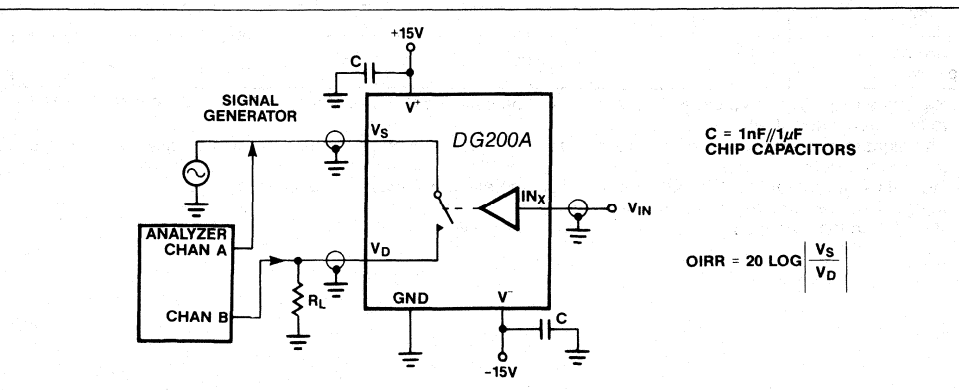


Figure 3. OFF Isolation Test Circuit

Test Circuits (continued)

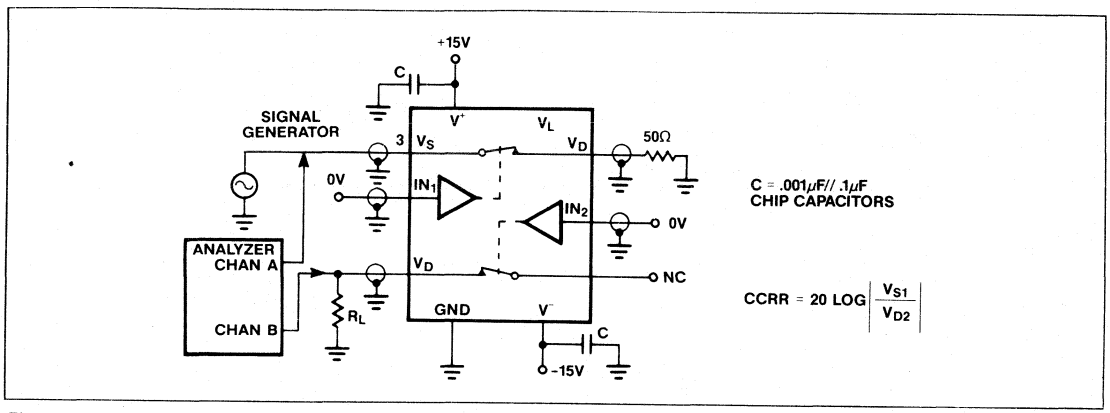
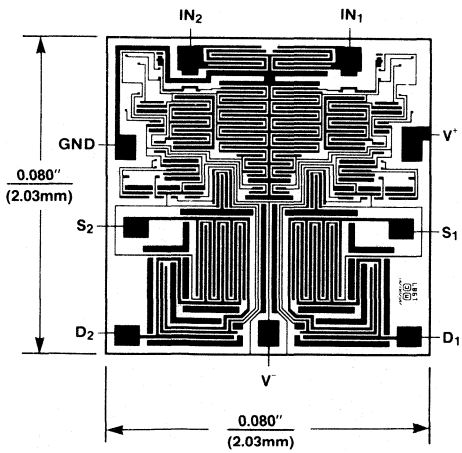


Figure 4. Channel To Channel Crosstalk Test Circuit

Chip Topography



TTL Compatible CMOS Analog Switches

General Description

Maxim's DG300-DG303 and DG300A-DG303A CMOS dual and quad analog switches combine low power operation with fast switching times and superior DC and AC switch characteristics. On resistance is less than 50Ω and is essentially constant over the analog signal range. Device specifications are ideal for battery powered circuitry.

These switches are available in a variety of formats as outlined below in the Pin Configurations section. The switch control logic inputs are fully TTL and CMOS compatible. Also featured are "break-before-make" switching and low charge injection.

Maxim's DG300-DG303 and DG300A-DG303A families are electrically compatible and pin compatible with the original manufacturer's devices. All devices will operate with power supplies ranging from ±5V to ±18V. Single supply operation is implemented by connecting V^- to GND.

Applications

Portable Instruments
Low Power Sample/Holds
Power Supply Switching
Programmable Gain Amplifiers
SPDT and DPDT Functions
Process Control and Telemetry

Features

- **Monolithic Low Power CMOS**
- **Latch-Up Proof Construction**
- **Fully Compatible 2nd Source**
- **Low On Resistance, <50Ω**
- **Fast Switching Time**
- **V^+ to V^- Analog Signal Range**
- **Single Supply Capability**

Ordering Information

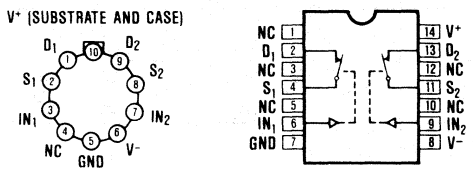
PART	TEMP. RANGE	PACKAGE
DG300C/D	0°C to +70°C	Dice
DG300CJ	0°C to +70°C	14 Lead Plastic DIP
DG300CWE	0°C to +70°C	16 Lead Wide SO
DG300CK	0°C to +70°C	14 Lead CERDIP
DG300BWE	-25°C to +85°C	16 Lead Wide SO
DG300BK	-25°C to +85°C	14 Lead CERDIP
DG300BA	-25°C to +85°C	10 Lead Metal Can
DG300AK	-55°C to +125°C	14 Lead CERDIP
DG300AA	-55°C to +125°C	10 Lead Metal Can

(Ordering Information is continued on last page.)

Pin Configurations

Top View

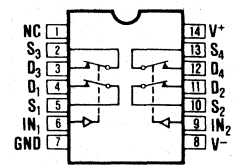
*Dual SPST DG300/DG300A



LOGIC	SWITCH
0	OFF
1	ON

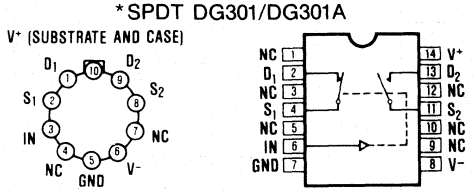
*Note: Pins 8 and 9 of the 16-lead Wide Small Outline Package are not connected.

*Dual DPST DG302/DG302A



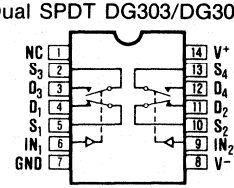
LOGIC	SWITCH
0	OFF
1	ON

*SPDT DG301/DG301A



LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

*Dual SPDT DG303/DG303A



LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Switch states are for Logic "1" Inputs (Positive Logic).

TTL Compatible CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V^-
V^- (DG300-DG303) 36V
V^+ (DG300A-DG303A) 44V
GND 25V
Digital Inputs, V_S, V_D (Note 1) ..... -4V to (V^+ + 4V) or 30mA, whichever occurs first.
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 30mA
(Pulsed at 1msec, 10% duty cycle max) 100mA
Storage Temperature (A & B Suffix) ..... -65°C to 150°C
(C Suffix) ..... -65°C to 125°C
Operating Temperature (A Suffix) ..... -55°C to 125°C
(B Suffix) ..... -25°C to 85°C
(C Suffix) ..... 0°C to 70°C
Lead Temperature (Soldering 10 sec.) ..... +300°C
Power Dissipation*
Cerdip (K) (Derate 11mW/°C above 75°C) 825mW
Plastic DIP (J) (Derate 6.5mW/°C above 25°C) .. 470mW
Metal Can (A) (Derate 6mW/°C above 75°C) 450mW

* Device mounted with all leads soldered or welded to PC board.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS		DG300-DG303A DG300A-DG303AA MIN (Note 2)	DG300-DG303A DG300A-DG303AA TYP (Note 3)	DG300-DG303A DG300A-DG303AA MAX	DG300-DG303B/C DG300A-DG303AB/C MIN (Note 2)	DG300-DG303B/C DG300A-DG303AB/C TYP (Note 3)	DG300-DG303B/C DG300A-DG303AB/C MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}	I_S = 10mA, V_{in} = 0.8V or 4.0V		-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$		I_S = -10mA, V_D = 10V		30	50		30	50	Ω
				I_S = 10mA, V_D = -10V		30	50		30	50	
	Source OFF Leakage Current	$I_{S(off)}$	V_{in} = 0.8V or V_{in} = 4.0V	V_S = 14V, V_D = -14V		0.1	1		0.1	5	nA
				V_S = -14V, V_D = 14V	-1	-0.1		-5	-0.1		
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V		0.1	1		0.1	5	
				V_S = 14V, V_D = -14V	-1	-0.1		-5	-0.1		
	Drain ON Leakage Current	$I_{D(on)}$		V_D = V_S = 14V		0.1	1		0.1	5	
				V_D = V_S = -14V	-2	-0.1		-5	-0.1		
INPUT	Input Current/ Voltage High	I_{INH}	V_{in} = 5.0V		-1	-0.001		-1	-0.001		μA
			V_{in} = 15V			0.001	1		0.001	1	
	Input Current/ Voltage Low	I_{INL}	V_{in} = 0V		-1	-0.001		-1	-0.001		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit			150	300		150	300	ns
	Turn-OFF Time	t_{off}				130	250		130	250	
	Break-Before-Make Interval	t_{on}-t_{off}	See Break-Before-Make Time Test Circuit DG301(A)/DG303(A) Only			50			50		
	Charge Injection	Q	C_L = 10nF, R_{gen} = 0Ω, V_{gen} = 0V			12			12		pC
	Source OFF Capacitance	$C_{S(off)}$	f = 1MHz, V_{in} = 0.8V or V_{in} = 4.0V	V_S = 0V		14			14		pF
	Drain OFF Capacitance	$C_{D(off)}$		V_D = 0V		14			14		
	Channel ON Capacitance	$C_{D(on)}$ + $C_{S(on)}$		V_S = V_D = 0V		40			40		
	Input Capacitance	C_{in}	f = 1MHz	V_{in} = 0V		6			6		
				V_{in} = 15V		7			7		
	Off Isolation (Note 4)		V_{in} = 0V, R_L = 1kΩ V_S = 1 V_{RMS}, f = 500kHz			62			62		dB
	Crosstalk (Channel to Channel)					74			74		

(See Notes next page).

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS	DG300-DG303A DG300A-DG303AA MIN (Note 2)	TYP (Note 3)	MAX	DG300-DG303B/C DG300A-DG303AB/C MIN (Note 2)	TYP (Note 3)	MAX	UNITS
SUPPLY	Positive Supply Current	I^+	V_{in} = 4V (One Input) (All Others = 0)		0.23	0.5		0.23	0.5	mA
	Negative Supply Current	I^-		-10	-0.001		-10	-0.001		μA
	Positive Supply Current	I^+	V_{in} = 0.8V (All Inputs)		0.001	10		0.001	10	
	Negative Supply Current	I^-		-10	-0.001		-10	-0.001		

ELECTRICAL CHARACTERISTICS (Over Temperature)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = Over Temperature Range, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS		DG300-DG303A DG300A-DG303AA MIN (Note 2)	TYP (Note 3)	MAX	DG300-DG303B/C DG300A-DG303AB/C MIN (Note 2)	TYP (Note 3)	MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}	I_S = 10mA, V_{in} = 0.8V or 4.0V		-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_{in} = 0.8V or V_{in} = 4.0V	I_S = -10mA, V_D = 10V			75			75	Ω
				I_S = 10mA, V_D = -10V			75			75	
	Source OFF Leakage Current	$I_{S(off)}$		V_S = 14V, V_D = -14V			100			100	nA
				V_S = -14V, V_D = 14V	-100			-100			
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V			100			100	
				V_S = 14V, V_D = -14V	-100			-100			
	Drain ON Leakage Current	$I_{D(on)}$		V_D = V_S = 14V			100			100	
				V_D = V_S = -14V	-200			-200			
INPUT	Input Current/ Voltage High	I_{INH}	V_{in} = 5.0V		-1			-10			μA
			V_{in} = 15V				1			10	
	Input Current/ Voltage Low	I_{INL}	V_{in} = 0V		-1			-10			
SUPPLY	Positive Supply Current	I^+	V_{in} = 4V (One Input) (All Others = 0)				1			1	mA
	Negative Supply Current	I^-			-100			-200			μA
	Positive Supply Current	I^+	V_{in} = 0.8V (All Inputs)				100			200	
	Negative Supply Current	I^-			-100			-200			

Note 1: Signals on S_X, D_X, or IN_X exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

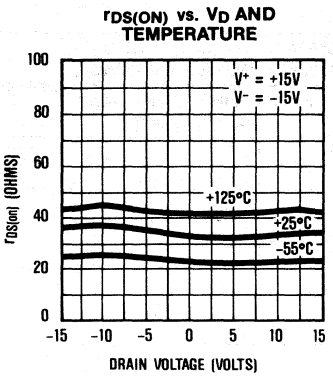
Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.

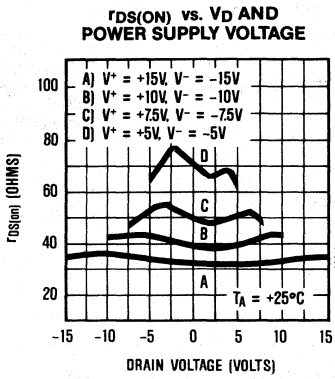
Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

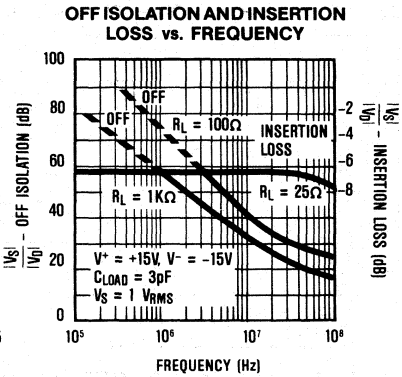
Note 4: OFF isolation = $20 \log \frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = Output.

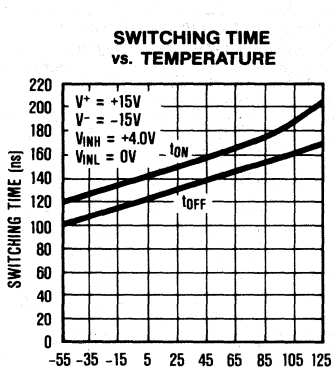
TTL Compatible CMOS Analog Switches

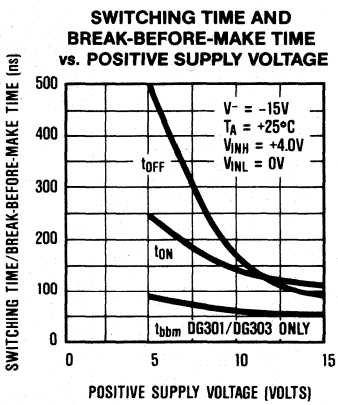
Typical Operating Characteristics

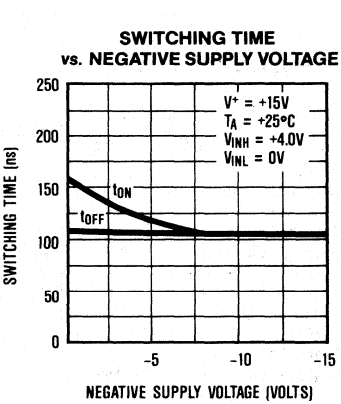












Test Circuits

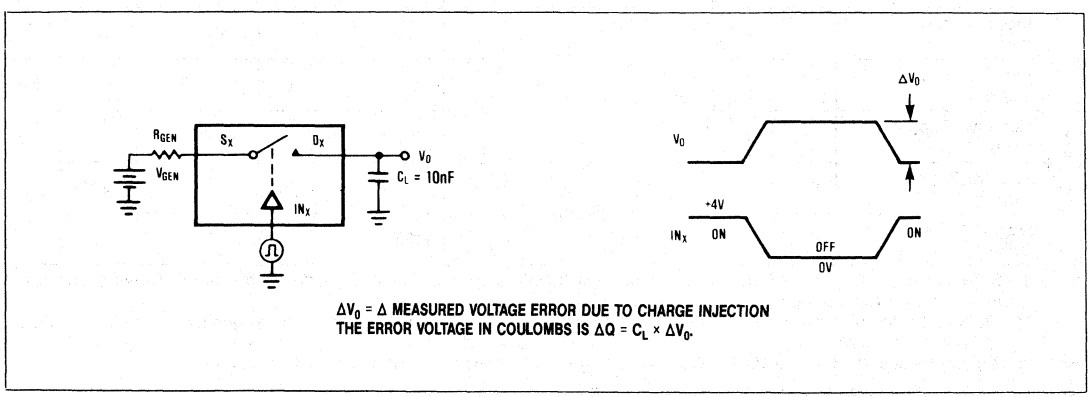


Figure 1. Charge Injection Test Circuit.

Test Circuits (Continued)

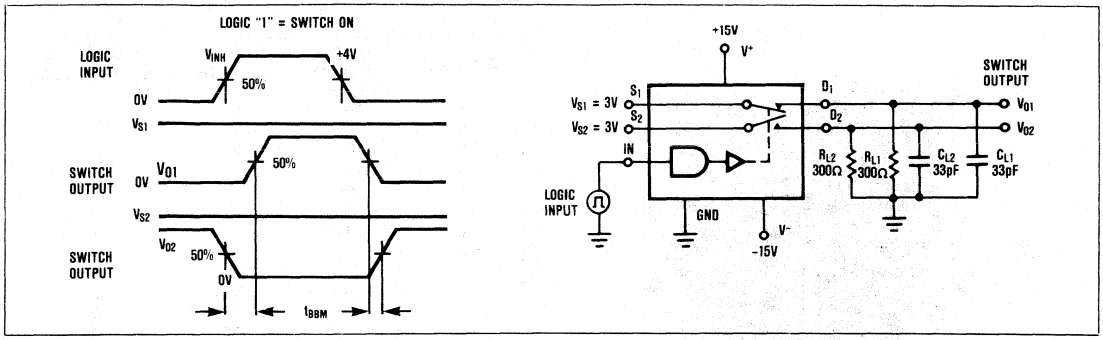


Figure 2. Break-Before-Make Time Test Circuit SPDT (DG301(A), DG303(A)).

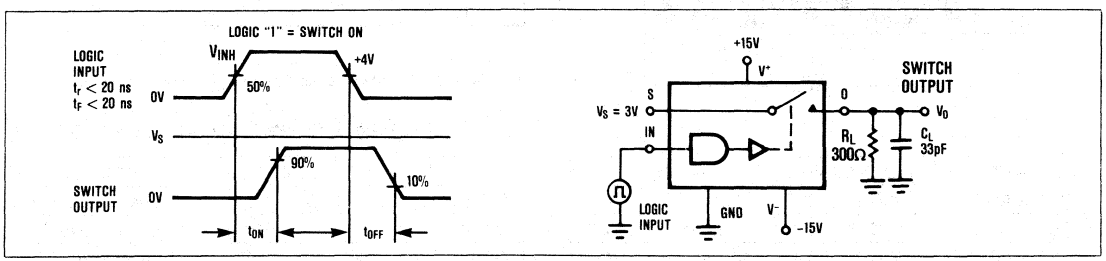


Figure 3. Switching Time Test Circuit.

Application Information

All DG300 family switches will operate with ±5 to ±15V power supplies. They can also be used with single ended power supplies ranging from +10V to +30V where the V^- terminal is connected to ground. In either case analog signals ranging from V^+ to V^- can be switched.

The on resistance variation with analog signal and supply voltage is shown in the Typical Operating Characteristics graphs. The temperature coefficient of R_{ON} is typically 0.5%/°C. Typical on resistance matching from channel to channel is 10%. In addition, Table 1 outlines some typical parameters for single supply operation.

Table 1. Typical Single Supply Parameters

	V^+ SUPPLY VOLTAGE (V^- = 0V)			
	+10V	+15V	+20V	+30V
Switching Time (R_L = 1kΩ)				
t_{ON}	190ns	150ns	110ns	70ns
t_{OFF}	40ns	40ns	40ns	40ns
On Resistance				
V_{SIGNAL} = +1V	71Ω	51Ω	42Ω	31Ω
V_{SIGNAL} = V^+/2	77Ω	54Ω	43Ω	30Ω
V_{SIGNAL} = V^+	84Ω	63Ω	54Ω	43Ω
Input Logic Levels	0.8V, 4.0V	0.8V, 4.0V	0.8V, 4.0V	0.8V, 4.5V

The charge injection test circuit is shown in Figure 1. Table 2 lists the typical injected charge for DG300 series switches with various input voltages.

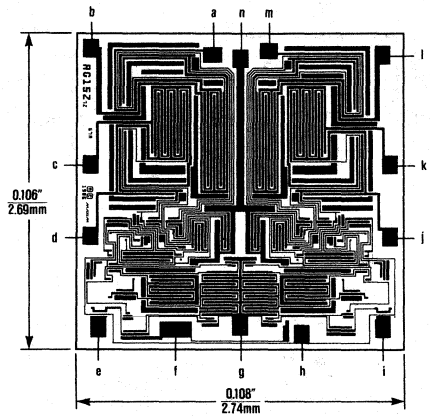
Table 2. Charge Injection (±15V Supplies)

ANALOG INPUT	INJECTED Q
+10V	4pC
+5V	8pC
0V	12pC
-5V	8pC
-10V	5pC

TTL Compatible CMOS Analog Switches

Chip Topography

DG300/1/2/3 ONLY



DIE PAD	DG300 DG300A	DG301 DG301A	DG302/303 DG302A/303A
a	N.C.	N.C.	S3
b	D1	D1	D3
c	D1	S1	D1
d	S1	IN1	S1
e	IN1	IN1	IN1
f	V^+	V^+	V^+
g	GND	GND	GND
h	V^-	V^-	V^-
i	IN2	GND	IN2
j	S2	V^-	S2
k	D2	S2	D2
l	D2	D2	D4
m	N.C.	N.C.	S4
n	V^+	V^+	V^+

For DG300A/1A/2A/3A Chip Topography, contact Factory.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
DG300AC/D	0°C to +70°C	Dice
DG300ACJ	0°C to +70°C	14 Lead Plastic DIP
DG300ACWE	0°C to +70°C	16 Lead Wide SO
DG300ACK	0°C to +70°C	14 Lead CERDIP
DG300ABWE	-25°C to +85°C	16 Lead Wide SO
DG300ABK	-25°C to +85°C	14 Lead CERDIP
DG300ABA	-25°C to +85°C	10 Lead Metal Can
DG301C/D	0°C to +70°C	Dice
DG301CJ	0°C to +70°C	14 Lead Plastic DIP
DG301CWE	0°C to +70°C	16 Lead Wide SO
DG301CK	0°C to +70°C	14 Lead CERDIP
DG301BWE	-25°C to +85°C	16 Lead Wide SO
DG301BK	-25°C to +85°C	14 Lead CERDIP
DG301BA	-25°C to +85°C	10 Lead Metal Can
DG301AK	-55°C to +125°C	14 Lead CERDIP
DG301AA	-55°C to +125°C	10 Lead Metal Can
DG301AC/D	0°C to +70°C	Dice
DG301ACJ	0°C to +70°C	14 Lead Plastic DIP
DG301ACWE	0°C to +70°C	16 Lead Wide SO
DG301ACK	0°C to +70°C	14 Lead CERDIP
DG301ABWE	-25°C to +85°C	16 Lead Wide SO
DG301ABK	-25°C to +85°C	14 Lead CERDIP
DG301ABA	-25°C to +85°C	10 Lead Metal Can
DG302C/D	0°C to +70°C	Dice
DG302CJ	0°C to +70°C	14 Lead Plastic DIP

PART	TEMP. RANGE	PACKAGE
DG302CWE	0°C to +70°C	16 Lead Wide SO
DG302CK	0°C to +70°C	14 Lead CERDIP
DG302BWE	-25°C to +85°C	16 Lead Wide SO
DG302BK	-25°C to +85°C	14 Lead CERDIP
DG302AK	-55°C to +125°C	14 Lead CERDIP
DG302AC/D	0°C to +70°C	Dice
DG302ACJ	0°C to +70°C	14 Lead Plastic DIP
DG302ACWE	0°C to +70°C	16 Lead Wide SO
DG302ACK	0°C to +70°C	14 Lead CERDIP
DG302ABWE	-25°C to +85°C	16 Lead Wide SO
DG302ABK	-25°C to +85°C	14 Lead CERDIP
DG303C/D	0°C to +70°C	Dice
DG303CJ	0°C to +70°C	14 Lead Plastic DIP
DG303CWE	0°C to +70°C	16 Lead Wide SO
DG303CK	0°C to +70°C	14 Lead CERDIP
DG303BWE	-25°C to +85°C	16 Lead Wide SO
DG303BK	-25°C to +85°C	14 Lead CERDIP
DG303AK	-55°C to +125°C	14 Lead CERDIP
DG303AC/D	0°C to +70°C	Dice
DG303ACJ	0°C to +70°C	14 Lead Plastic DIP
DG303ACWE	0°C to +70°C	16 Lead Wide SO
DG303ACK	0°C to +70°C	14 Lead CERDIP
DG303ABWE	-25°C to +85°C	16 Lead Wide SO
DG303ABK	-25°C to +85°C	14 Lead CERDIP

MAXIM

CMOS Analog Switches

General Description

Maxim's DG304-DG307 and DG304A-DG307A CMOS dual and quad analog switches combine low power operation with fast switching times and superior DC and AC switch characteristics. On resistance is less than 50Ω and is essentially constant over the analog signal range. Device specifications are ideal for battery powered circuitry.

These switches are available in a variety of formats as outlined below in the Pin Configurations section. The switch control logic inputs are compatible with CMOS logic. Also featured are "break-before-make" switching and low charge injection.

Maxim's DG304-DG307 and DG304A-DG307A families are electrically compatible and pin compatible with the original manufacturer's devices. All devices will operate with power supplies ranging from ±5V to ±18V. Single supply operation is implemented by connecting V^- to GND.

Applications

Portable Instruments

Low Power Sample/Holds

Power Supply Switching

Programmable Gain Amplifiers

SPDT and DPDT Functions

Process Control and Telemetry

Features

- **Monolithic Low Power CMOS**
- **Latch-Up Proof Construction**
- **Fully Compatible 2nd Source**
- **Low On Resistance, <50Ω**
- **Fast Switching Time**
- **V^+ to V^- Analog Signal Range**
- **Single Supply Capability**

Ordering Information

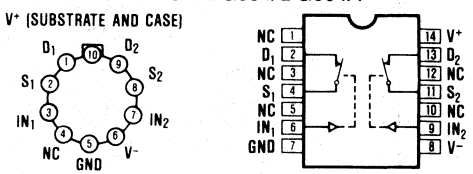
PART	TEMP. RANGE	PACKAGE
DG304C/D	0°C to +70°C	Dice
DG304CJ	0°C to +70°C	14 Lead Plastic DIP
DG304CWE	0°C to +70°C	16 Lead Wide SO
DG304CK	0°C to +70°C	14 Lead CERDIP
DG304BWE	-25°C to +85°C	16 Lead Wide SO
DG304BK	-25°C to +85°C	14 Lead CERDIP
DG304BA	-25°C to +85°C	10 Lead Metal Can
DG304AK	-55°C to +125°C	14 Lead CERDIP
DG304AA	-55°C to +125°C	10 Lead Metal Can

(Ordering Information is continued on last page.)

Pin Configurations

Top View

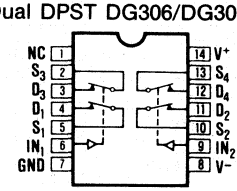
*Dual SPST DG304/DG304A



LOGIC	SWITCH
0	OFF
1	ON

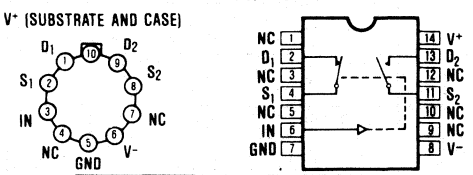
*Note: Pins 8 and 9 of the 16-lead Wide Small Outline Package are not connected.

*Dual DPST DG306/DG306A



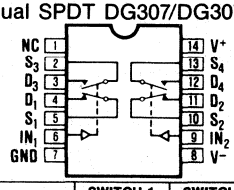
LOGIC	SWITCH
0	OFF
1	ON

*SPDT DG305/DG305A



LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

*Dual SPDT DG307/DG307A



LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Switch states are for Logic "1" Inputs (Positive Logic).

CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V^-
V^+ (DG304-DG307) 36V
V^+ (DG304A-DG307A) 44V
GND 25V
Digital Inputs, V_S, V_D (Note 1) ..... -4V to (V^+ + 4V) or 30mA, whichever occurs first.
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 30mA
(Pulsed at 1msec, 10% duty cycle max) 100mA
Storage Temperature (A & B Suffix) ..... -65°C to 150°C
(C Suffix) ..... -65°C to 125°C
Operating Temperature (A Suffix) ..... -55°C to 125°C
(B Suffix) ..... -25°C to 85°C
(C Suffix) ..... 0°C to 70°C
Lead Temperature (Soldering 10 sec.) ..... +300°C
Power Dissipation*
Cerdip (K) (Derate 11mW/°C above 75°C) 825mW
Plastic DIP (J) (Derate 6.5mW/°C above 25°C) .. 470mW
Metal Can (A) (Derate 6mW/°C above 75°C) 450mW

* Device mounted with all leads soldered or welded to PC board.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS		DG304-DG307A DG304A-DG307AA MIN (Note 2)	TYP (Note 3)	MAX	DG304-DG307B/C DG304A-DG307AB/C MIN (Note 2)	TYP (Note 3)	MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}	I_S = 10mA, V_{in} = 3.5V or 11.0V		-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_{in} = 3.5V or V_{in} = 11.0V	I_S = -10mA, V_D = 10V		30	50		30	50	Ω
				I_S = 10mA, V_D = -10V		30	50		30	50	
	Source OFF Leakage Current	$I_{S(off)}$		V_S = 14V, V_D = -14V		0.1	1		0.1	5	nA
				V_S = -14V, V_D = 14V	-1	-0.1		-5	-0.1		
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V		0.1	1		0.1	5	
				V_S = 14V, V_D = -14V	-1	-0.1		-5	-0.1		
	Drain ON Leakage Current	$I_{D(on)}$		V_D = V_S = 14V		0.1	1		0.1	5	
				V_D = V_S = -14V	-2	-0.1		-5	-0.1		
INPUT	Input Current/ Voltage High	I_{INH}	V_{in} = 5.0V		-1	-0.001		-1	-0.001		μA
			V_{in} = 15V			0.001	1		0.001	1	
	Input Current/ Voltage Low	I_{INL}	V_{in} = 0V		-1	-0.001		-1	-0.001		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit			110	250		110	250	ns
	Turn-OFF Time	t_{off}				70	150		70	150	
	Break-Before-Make Interval	t_{on}-t_{off}	See Break-Before-Make Time Test Circuit DG305(A)/DG307(A) Only			50			50		
	Charge Injection	Q	C_L = 10nF, R_{gen} = 0Ω, V_{gen} = 0V			12			12		pC
	Source OFF Capacitance	$C_{S(off)}$	f = 1MHz, V_{in} = 3.5V or V_{in} = 11.0V	V_S = 0V		14			14		pF
	Drain OFF Capacitance	$C_{D(off)}$		V_D = 0V		14			14		
	Channel ON Capacitance	$C_{D(on)}$ + $C_{S(on)}$		V_S = V_D = 0V		40			40		
	Input Capacitance	C_{in}	f = 1MHz	V_{in} = 0V		6			6		
				V_{in} = 15V		7			7		
	Off Isolation (Note 4)		V_{in} = 0V, R_L = 1kΩ V_S = 1 V_{RMS}, f = 500kHz			62			62		dB
	Crosstalk (Channel to Channel)					74			74		

(See Notes next page).

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS	DG304-DG307A DG304A-DG307AA			DG304-DG307B/C DG304A-DG307AB/C			UNITS
				MIN (Note 2)	TYP (Note 3)	MAX	MIN (Note 2)	TYP (Note 3)	MAX	
SUPPLY	Positive Supply Current	I^+	V_{in} = 15.0V (All Inputs)		0.001	10		0.001	10	μA
	Negative Supply Current	I^-		-10	-0.001		-10	-0.001		
	Positive Supply Current	I^+	V_{in} = 0V (All Inputs)		0.001	10		0.001	10	
	Negative Supply Current	I^-		-10	-0.001		-10	-0.001		

ELECTRICAL CHARACTERISTICS (Over Temperature)

(V^+ = +15V, GND = 0V, T_A = Over Temperature Range, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		DG304-DG307A DG304A-DG307AA			DG304-DG307B/C DG304A-DG307AB/C			UNITS
					MIN (Note 2)	TYP (Note 3)	MAX	MIN (Note 2)	TYP (Note 3)	MAX	
SWITCH	Analog Signal Range	V_{ANALOG}	I_S = 10mA, V_{in} = 3.5V or 11.0V		-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_{in} = 3.5V or V_{in} = 11.0V	I_S = -10mA, V_D = 10V			75			75	Ω
				I_S = 10mA, V_D = -10V			75			75	
	Source OFF Leakage Current	$I_{S(off)}$		V_S = 14V, V_D = -14V			100			100	nA
				V_S = -14V, V_D = 14V	-100			-100			
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V			100			100	
				V_S = 14V, V_D = -14V	-100			-100			
	Drain ON Leakage Current	$I_{D(on)}$		V_D = V_S = 14V			100			100	
				V_D = V_S = -14V	-200			-200			
INPUT	Input Current/ Voltage High	I_{INH}	V_{in} = 5.0V		-1			-10			μA
			V_{in} = 15V				1			10	
	Input Current/ Voltage Low	I_{INL}	V_{in} = 0V		-1			-10			
SUPPLY	Positive Supply Current	I^+	V_{in} = 15.0V (All Inputs)				100			200	μA
	Negative Supply Current	I^-			-100			-200			
	Positive Supply Current	I^+	V_{in} = 0V (All Inputs)				100			200	
	Negative Supply Current	I^-			-100			-200			

Note 1: Signals on S_X, D_X, or IN_X exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

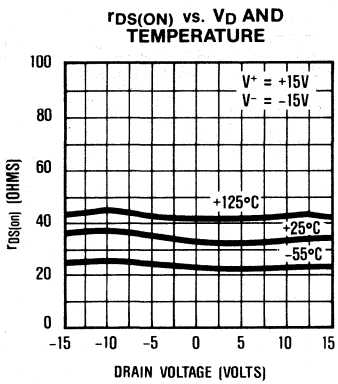
Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.

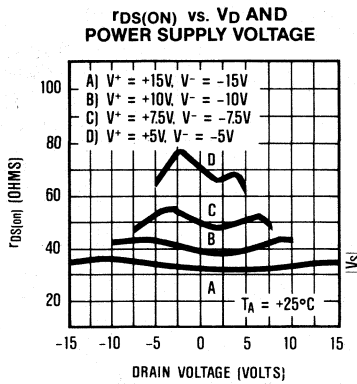
Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

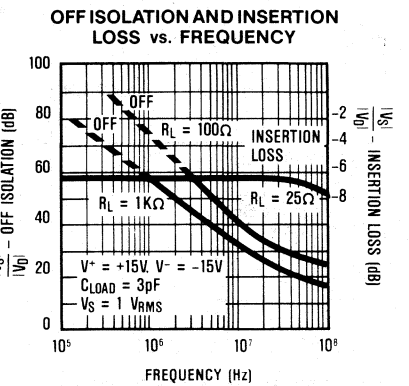
Note 4: OFF isolation = $20 \log \frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = Output.

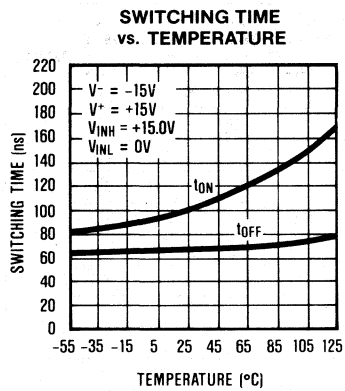
CMOS Analog Switches

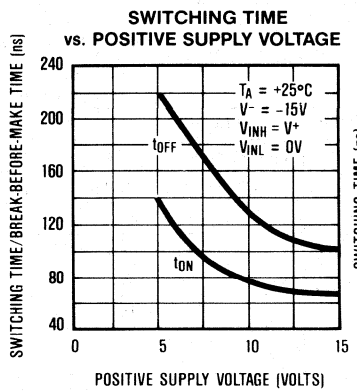
Typical Operating Characteristics

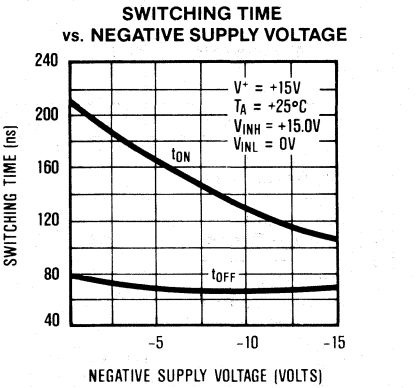












Test Circuits

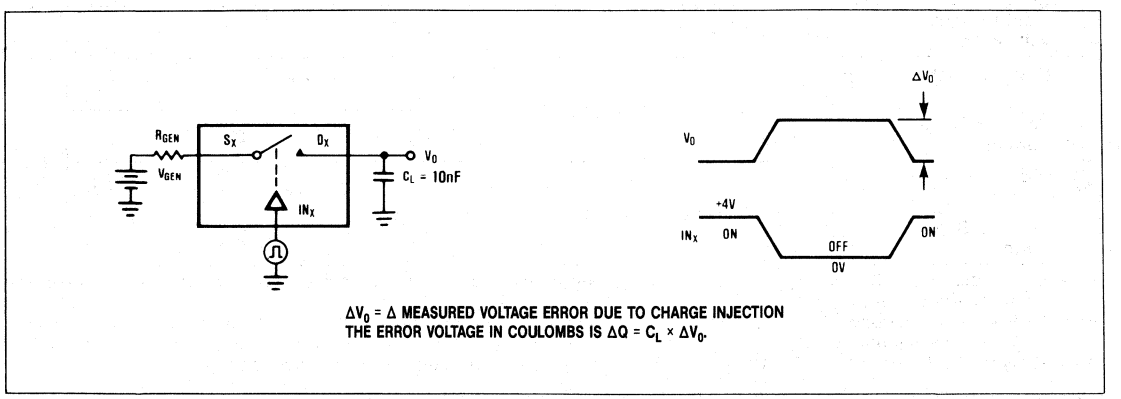


Figure 1. Charge Injection Test Circuit.

Test Circuits (Continued)

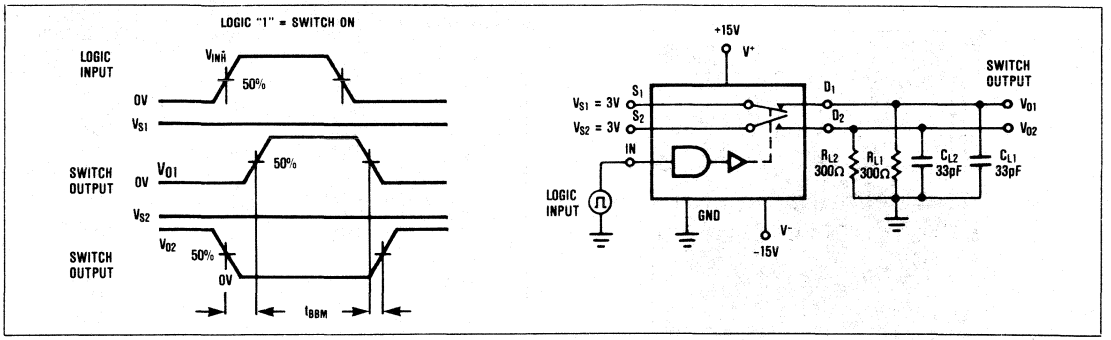


Figure 2. Break-Before-Make Time Test Circuit SPDT DG305(A), DG307(A).

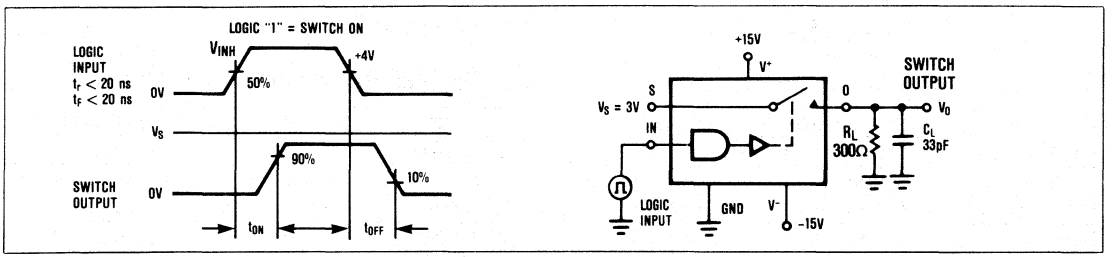


Figure 3. Switching Time Test Circuit.

Application Information

All DG304 family switches will operate with ±5 to ±15V power supplies. They can also be used with single ended power supplies ranging from +10V to +30V where the V^- terminal is connected to ground. In either case analog signals ranging from V^+ to V^- can be switched.

The on resistance variation with analog signal and supply voltage is shown in the Typical Operating Characteristics graphs. The temperature coefficient of R_{ON} is typically 0.5%/°C. Typical on resistance matching from channel to channel is 10%. In addition, Table 1 outlines some typical parameters for single supply operation.

Table 1. Typical Single Supply Parameters

	V^+ SUPPLY VOLTAGE (V^- = 0V)			
	+10V	+15V	+20V	+30V
Switching Time (R_L = 1kΩ)				
t_{ON}	220ns	180ns	165ns	110ns
t_{OFF}	60ns	40ns	30ns	20ns
On Resistance				
V_{SIGNAL} = +1V	71Ω	51Ω	42Ω	31Ω
V_{SIGNAL} = V^+/2	77Ω	54Ω	43Ω	30Ω
V_{SIGNAL} = V^+	84Ω	63Ω	54Ω	43Ω
Input Logic Levels	3.5V, 11.0V	3.5V, 11.0V	3.5V, 12.5V	3.5V, 22.0V

The charge injection test circuit is shown in Figure 1. Table 2 lists the typical injected charge for DG304 series switches with various input voltages.

Table 2. Charge Injection (±15V Supplies)

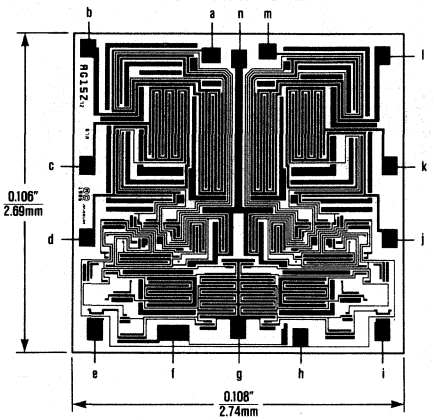
ANALOG INPUT	INJECTED Q
+10V	4pC
+5V	8pC
0V	12pC
-5V	8pC
-10V	5pC

12

CMOS Analog Switches

Chip Topography

DG304/5/6/7 ONLY



DIE PAD	DG304 DG304A	DG305 DG305A	DG306/307 DG306A/307A
a	N.C.	N.C.	S3
b	D1	D1	D3
c	D1	S1	D1
d	S1	IN1	S1
e	IN1	IN1	IN1
f	V^+	V^+	V^+
g	GND	GND	GND
h	V^-	V^-	V^-
i	IN2	GND	IN2
j	S2	V^-	S2
k	D2	S2	D2
l	D2	D2	D4
m	N.C.	N.C.	S4
n	V^+	V^+	V^+

For DG304A/5A/6A/7A Chip Topography, contact Factory.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
DG304AC/D	0°C to +70°C	Dice
DG304ACJ	0°C to +70°C	14 Lead Plastic DIP
DG304ACWE	0°C to +70°C	16 Lead Wide SO
DG304ACK	0°C to +70°C	14 Lead CERDIP
DG304ABWE	-25°C to +85°C	16 Lead Wide SO
DG304ABK	-25°C to +85°C	14 Lead CERDIP
DG304ABA	-25°C to +85°C	10 Lead Metal Can
DG305C/D	0°C to +70°C	Dice
DG305CJ	0°C to +70°C	14 Lead Plastic DIP
DG305CWE	0°C to +70°C	16 Lead Wide SO
DG305CK	0°C to +70°C	14 Lead CERDIP
DG305BWE	-25°C to +85°C	16 Lead Wide SO
DG305BK	-25°C to +85°C	14 Lead CERDIP
DG305BA	-25°C to +85°C	10 Lead Metal Can
DG305AK	-55°C to +125°C	14 Lead CERDIP
DG305AA	-55°C to +125°C	10 Lead Metal Can
DG305AC/D	0°C to +70°C	Dice
DG305ACJ	0°C to +70°C	14 Lead Plastic DIP
DG305ACWE	0°C to +70°C	16 Lead Wide SO
DG305ACK	0°C to +70°C	14 Lead CERDIP
DG305ABWE	-25°C to +85°C	16 Lead Wide SO
DG305ABK	-25°C to +85°C	14 Lead CERDIP
DG305ABA	-25°C to +85°C	10 Lead Metal Can

PART	TEMP. RANGE	PACKAGE
DG306C/D	0°C to +70°C	Dice
DG306CJ	0°C to +70°C	14 Lead Plastic DIP
DG306CWE	0°C to +70°C	16 Lead Wide SO
DG306CK	0°C to +70°C	14 Lead CERDIP
DG306BWE	-25°C to +85°C	16 Lead Wide SO
DG306BK	-25°C to +85°C	14 Lead CERDIP
DG306AK	-55°C to +125°C	14 Lead CERDIP
DG306AC/D	0°C to +70°C	Dice
DG306ACJ	0°C to +70°C	14 Lead Plastic DIP
DG306ACWE	0°C to +70°C	16 Lead Wide SO
DG306ACK	0°C to +70°C	14 Lead CERDIP
DG306ABWE	-25°C to +85°C	16 Lead Wide SO
DG306ABK	-25°C to +85°C	14 Lead CERDIP
DG307C/D	0°C to +70°C	Dice
DG307CJ	0°C to +70°C	14 Lead Plastic DIP
DG307CWE	0°C to +70°C	16 Lead Wide SO
DG307CK	0°C to +70°C	14 Lead CERDIP
DG307BWE	-25°C to +85°C	16 Lead Wide SO
DG307BK	-25°C to +85°C	14 Lead CERDIP
DG307AK	-55°C to +125°C	14 Lead CERDIP
DG307AC/D	0°C to +70°C	Dice
DG307ACJ	0°C to +70°C	14 Lead Plastic DIP
DG307ACWE	0°C to +70°C	16 Lead Wide SO
DG307ACK	0°C to +70°C	14 Lead CERDIP
DG307ABWE	-25°C to +85°C	16 Lead Wide SO
DG307ABK	-25°C to +85°C	14 Lead CERDIP

General Purpose CMOS Analog Switches

General Description

Maxim's DG381-DG390 and DG381A-DG390A CMOS dual and quad analog switches combine low power operation with fast switching times and superior DC and AC switch characteristics. On resistance is less than 50Ω and is essentially constant over the analog signal range. Device specifications are ideal for battery powered circuitry.

These switches are available in a variety of formats as outlined below in the Pin Configurations section. The switch control logic inputs are fully TTL and CMOS compatible. Also featured are "break-before-make" switching and low charge injection.

Maxim's DG381-DG390 and DG381A-DG390A families are electrically compatible and pin compatible with the original manufacturer's devices. All devices will operate with power supplies ranging from ±5V to ±18V. Single supply operation is implemented by connecting V^- to GND.

Applications

Portable Instruments
Low Power Sample/Holds
Power Supply Switching
Programmable Gain Amplifiers
SPDT and DPDT Functions
Process Control and Telemetry

Features

- Monolithic Low Power CMOS
- Latch-Up Proof Construction
- Fully Compatible 2nd Source
- Low On Resistance, <50Ω
- Fast Switching Time
- V^+ to V^- Analog Signal Range
- Single Supply Capability

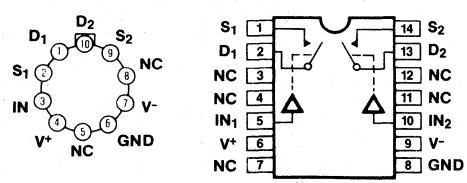
Ordering Information

PART	TEMP. RANGE	PACKAGE
DG381C/D	0°C to +70°C	Dice
DG381CJ	0°C to +70°C	14 Lead Plastic DIP
DG381CWE	0°C to +70°C	16 Lead Wide SO
DG381CK	0°C to +70°C	14 Lead CERDIP
DG381BWE	-25°C to +85°C	16 Lead Wide SO
DG381BK	-25°C to +85°C	14 Lead CERDIP
DG381BA	-25°C to +85°C	10 Lead Metal Can
DG381AK	-55°C to +125°C	14 Lead CERDIP
DG381AA	-55°C to +125°C	10 Lead Metal Can

(Ordering Information is continued on last page.)

Pin Configurations

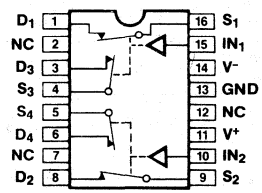
*Dual SPST DG381/DG381A Top View



*Note: Pins 8 and 9 of the 16-lead Wide Small Outline Package are not connected.

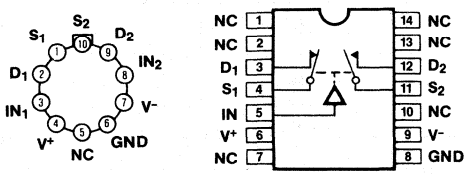
LOGIC	SWITCH
0	ON
1	OFF

Dual DPST DG384/DG384A



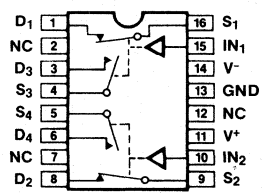
LOGIC	SWITCH
0	OFF
1	ON

*SPDT DG387/DG387A



LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Dual SPDT DG390/DG390A



LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Switch states are for Logic "1" Inputs (Positive Logic).

General Purpose CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V⁻
V⁺ (DG381-DG390) 36V
V⁺ (DG381A-DG390A) 44V
GND 25V
Digital Inputs, V_S, V_D (Note 1) ..... -4V to (V⁺ + 4V) or 30mA, whichever occurs first.
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 30mA
(Pulsed at 1msec, 10% duty cycle max) 100mA
Storage Temperature (A & B Suffix) ..... -65°C to 150°C
(C Suffix) ..... -65°C to 125°C
Operating Temperature (A Suffix) ..... -55°C to 125°C
(B Suffix) ..... -25°C to 85°C
(C Suffix) ..... 0°C to 70°C
Lead Temperature (Soldering 10 sec.) ..... +300°C
Power Dissipation*
Cerdip (K) (Derate 11mW/°C above 75°C) 825mW
Plastic DIP (J) (Derate 6.5mW/°C above 25°C) .. 470mW
Metal Can (A) (Derate 6mW/°C above 75°C) 450mW

* Device mounted with all leads soldered or welded to PC board.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS		DG381-DG390A DG381A-DG390AA MIN (Note 2)	TYP (Note 3)	MAX	DG381-DG390B/C DG381A-DG390AB/C MIN (Note 2)	TYP (Note 3)	MAX	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}	I_S = 10mA, V_{in} = 0.8V or 4.0V		-15		15	-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$		I_S = -10mA, V_D = 10V		30	50		30	50	Ω
				I_S = 10mA, V_D = -10V		30	50		30	50	
	Source OFF Leakage Current	$I_{S(off)}$	V_{in} = 0.8V or V_{in} = 4.0V	V_S = 14V, V_D = -14V		0.1	1		0.1	5	nA
				V_S = -14V, V_D = 14V	-1	-0.1		-5	-0.1		
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V		0.1	1		0.1	5	
				V_S = 14V, V_D = -14V	-1	-0.1		-5	-0.1		
	Drain ON Leakage Current	$I_{D(on)}$		V_D = V_S = 14V		0.1	1		0.1	5	
				V_D = V_S = -14V	-2	-0.1		-5	-0.1		
INPUT	Input Current/ Voltage High	I_{INH}	V_{in} = 5.0V		-1	-0.001		-1	-0.001		μA
			V_{in} = 15V			0.001	1		0.001	1	
	Input Current/ Voltage Low	I_{INL}	V_{in} = 0V		-1	-0.001		-1	-0.001		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit			150	300		150	300	ns
	Turn-OFF Time	t_{off}				130	250		130	250	
	Break-Before-Make Interval	t_{on}-t_{off}	See Break-Before-Make Time Test Circuit DG387(A)/DG390(A) Only			50			50		
	Charge Injection	Q	C_L = 10nF, R_{gen} = 0Ω, V_{gen} = 0V			12			12		pC
	Source OFF Capacitance	$C_{S(off)}$	f = 1MHz, V_{in} = 0.8V or V_{in} = 4.0V	V_S = 0V		14			14		pF
	Drain OFF Capacitance	$C_{D(off)}$		V_D = 0V		14			14		
	Channel ON Capacitance	$C_{D(on)}$ + $C_{S(on)}$		V_S = V_D = 0V		40			40		
	Input Capacitance	C_{in}	f = 1MHz	V_{in} = 0V		6			6		
				V_{in} = 15V		7			7		
	Off Isolation (Note 4)		V_{in} = 0V, R_L = 1kΩ V_S = 1 V_{RMS}, f = 500kHz			62			62		dB
	Crosstalk (Channel to Channel)					74			74		

(See Notes next page).

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS	DG381-DG390A DG381A-DG390AA MIN (Note 2)	TYP (Note 3)	MAX	DG381-DG390B/C DG381A-DG390AB/C MIN (Note 2)	TYP (Note 3)	MAX	UNITS
SUPPLY	Positive Supply Current	I^+	V_{in} = 4V (One Input) (All Others = 0)		0.23	0.5		0.23	0.5	mA
	Negative Supply Current	I^-		-10	-0.001		-100	-0.001		μA
	Positive Supply Current	I^+	V_{in} = 0.8V (All Inputs)		0.001	10		0.001	100	
	Negative Supply Current	I^-		-10	-0.001		-100	-0.001		

ELECTRICAL CHARACTERISTICS (Over Temperature)

(V^+ = +15V, V^- = -15V, GND = 0V, T_A = Over Temperature Range, unless otherwise indicated)

	PARAMETER	SYMBOL	TEST CONDITIONS		DG381-DG390A DG381A-DG390AA MIN (Note 2)	MAX (Note 3)	DG381-DG390B/C DG381A-DG390AB/C MIN (Note 2)	MAX (Note 3)	UNITS
SWITCH	Analog Signal Range	V_{ANALOG}	I_S = 10mA, V_{in} = 0.8V or 4.0V		-15	15	-15	15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	V_{in} = 0.8V or V_{in} = 4.0V	I_S = -10mA, V_D = 10V		75		75	Ω
				I_S = 10mA, V_D = -10V		75		75	
	Source OFF Leakage Current	$I_{S(off)}$		V_S = 14V, V_D = -14V		100		100	nA
				V_S = -14V, V_D = 14V	-100		-100		
	Drain OFF Leakage Current	$I_{D(off)}$		V_S = -14V, V_D = 14V		100		100	
				V_S = 14V, V_D = -14V	-100		-100		
	Drain ON Leakage Current	$I_{D(on)}$		V_D = V_S = 14V		100		100	
				V_D = V_S = -14V	-200		-200		
INPUT	Input Current/ Voltage High	I_{INH}	V_{in} = 5.0V		-1		-10		μA
			V_{in} = 15V			1		10	
	Input Current/ Voltage Low	I_{INL}	V_{in} = 0V		-1		-10		
SUPPLY	Positive Supply Current	I^+	V_{in} = 4V (One Input) (All Others = 0)			1		1.5	mA
	Negative Supply Current	I^-			-100		-200		μA
	Positive Supply Current	I^+	V_{in} = 0.8V (All Inputs)			100		200	
	Negative Supply Current	I^-			-100		-200		

Note 1: Signals on S_X, D_X, or IN_X exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

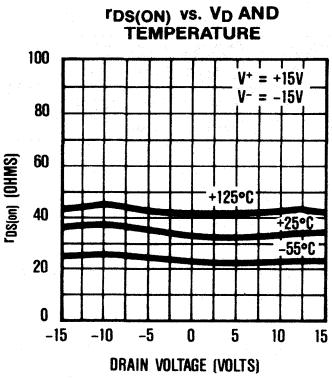
Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum is used in this data sheet.

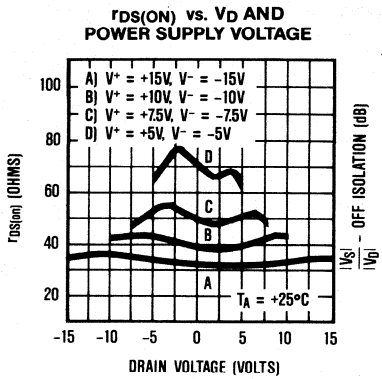
Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

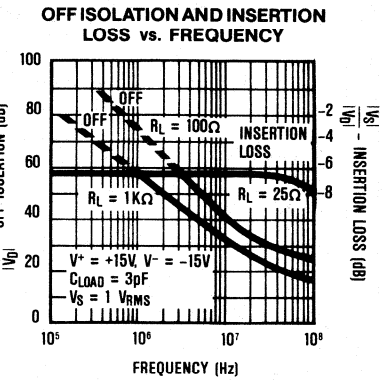
Note 4: OFF isolation = $20 \log \frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = Output.

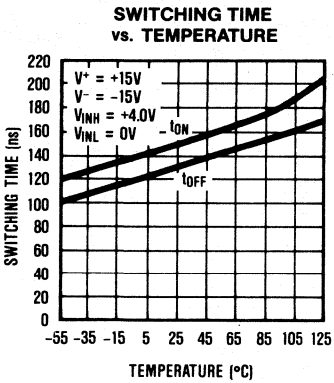
General Purpose CMOS Analog Switches

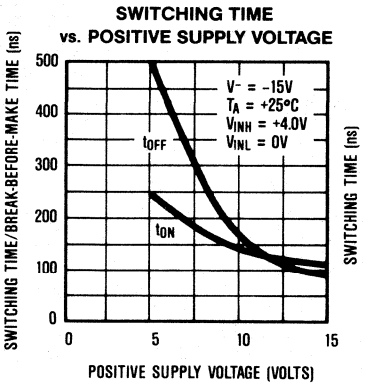
Typical Operating Characteristics

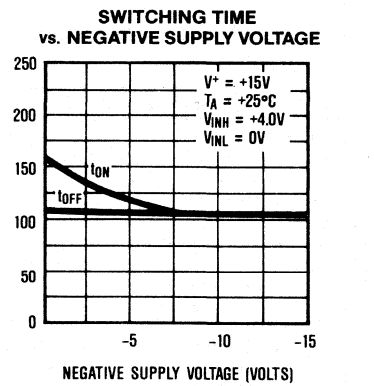












Test Circuits

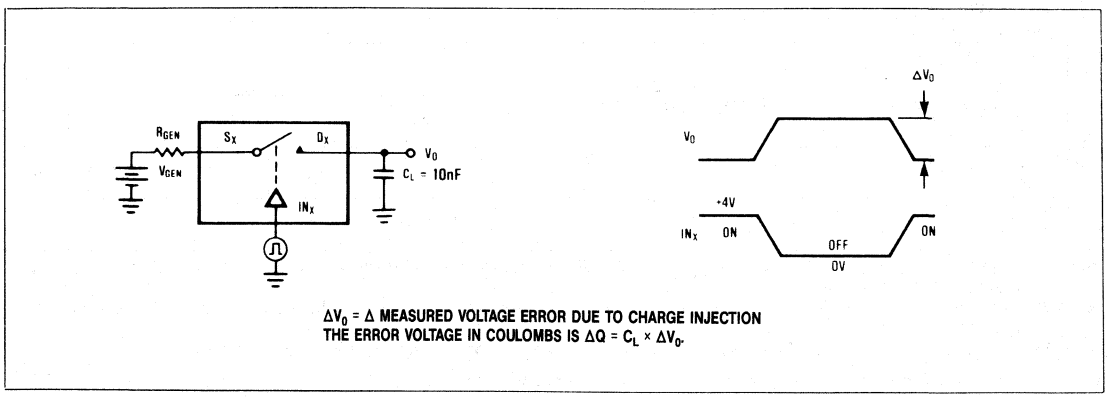


Figure 1. Charge Injection Test Circuit.

Test Circuits (Continued)

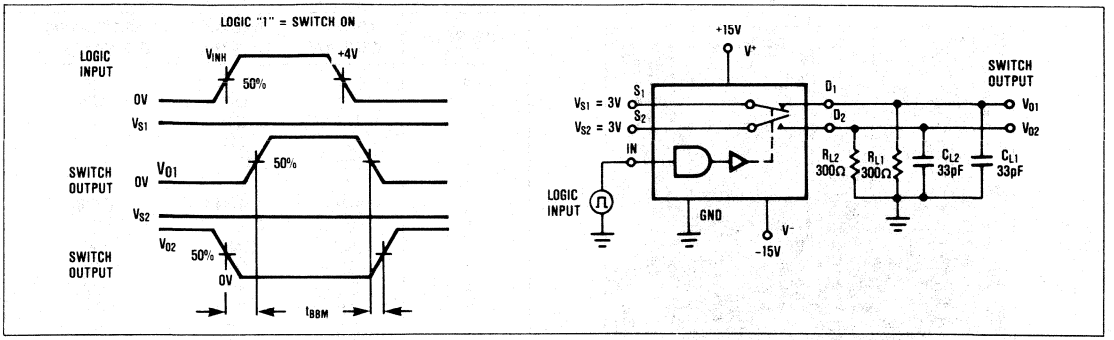


Figure 2. Break-Before-Make Time Test Circuit SPDT (DG387(A)/DG390(A)).

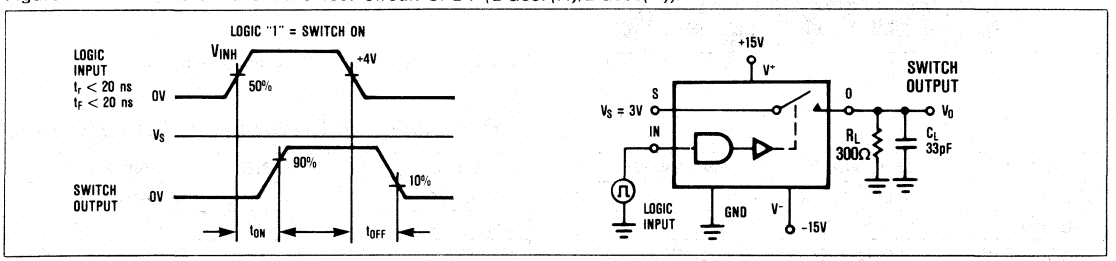


Figure 3. Switching Time Test Circuit.

Application Information

All DG381 family switches will operate with ±5 to ±15V power supplies. They can also be used with single ended power supplies ranging from +10V to +30V where the V^- terminal is connected to ground. In either case analog signals ranging from V^+ to V^- can be switched.

The on resistance variation with analog signal and supply voltage is shown in the Typical Operating Characteristics graphs. The temperature coefficient of R_{ON} is typically 0.5%/°C. Typical on resistance matching from channel to channel is 10%. In addition, Table 1 outlines some typical parameters for single supply operation.

Table 1. Typical Single Supply Parameters

	V^+ SUPPLY VOLTAGE (V^- = 0V)			
	+10V	+15V	+20V	+30V
Switching Time (R_L = 1kΩ)				
t_{ON}	190ns	150ns	110ns	70ns
t_{OFF}	40ns	40ns	40ns	40ns
On Resistance				
V_{SIGNAL} = +1V	71Ω	51Ω	42Ω	31Ω
V_{SIGNAL} = $V^+/2$	77Ω	54Ω	43Ω	30Ω
V_{SIGNAL} = V^+	84Ω	63Ω	54Ω	43Ω
Input Logic Levels	0.8V, 4.0V	0.8V, 4.0V	0.8V, 4.0V	0.8V, 4.5V

The charge injection test circuit is shown in Figure 1. Table 2 lists the typical injected charge for DG381 series switches with various input voltages.

Table 2. Charge Injection (±15V Supplies)

ANALOG INPUT	INJECTED Q
+10V	4pC
+5V	8pC
0V	12pC
-5V	8pC
-10V	5pC

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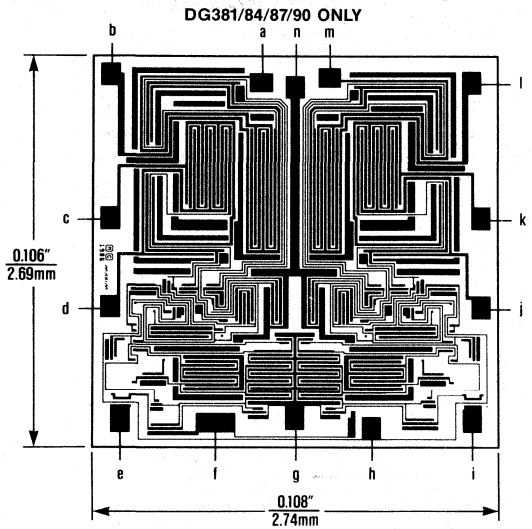
General Purpose CMOS Analog Switches

Chip Topography



Ordering Information (continued)

DIE PAD	DG381 DG381A	DG387 DG387A	DG384/390 DG384A/390A
a	N.C.	N.C.	S3
b	D1	D1	D3
c	D1	S1	D1
d	S1	IN1	S1
e	IN1	IN1	IN1
f	V^+	V^+	V^+
g	GND	GND	GND
h	V^-	V^-	V^-
i	IN2	GND	IN2
j	S2	V^-	S2
k	D2	S2	D2
l	D2	D2	D4
m	N.C.	N.C.	S4
n	V^+	V^+	V^+

For DG381A/84A/87A/90A Chip Topography, contact Factory.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
DG381AC/D	0°C to +70°C	Dice
DG381ACJ	0°C to +70°C	14 Lead Plastic DIP
DG381ACWE	0°C to +70°C	16 Lead Wide SO
DG381ACK	0°C to +70°C	14 Lead CERDIP
DG381ABWE	-25°C to +85°C	16 Lead Wide SO
DG381ABK	-25°C to +85°C	14 Lead CERDIP
DG381ABA	-25°C to +85°C	10 Lead Metal Can
DG384C/D	0°C to +70°C	Dice
DG384CJ	0°C to +70°C	16 Lead Plastic DIP
DG384CWE	0°C to +70°C	16 Lead Wide SO
DG384CK	0°C to +70°C	16 Lead CERDIP
DG384BWE	-25°C to +85°C	16 Lead Wide SO
DG384BK	-25°C to +85°C	16 Lead CERDIP
DG384AK	-55°C to +125°C	16 Lead CERDIP
DG384AC/D	0°C to +70°C	Dice
DG384ACJ	0°C to +70°C	16 Lead Plastic DIP
DG384ACWE	0°C to +70°C	16 Lead Wide SO
DG384ACK	0°C to +70°C	16 Lead CERDIP
DG384ABWE	-25°C to +85°C	16 Lead Wide SO
DG384ABK	-25°C to +85°C	16 Lead CERDIP
DG387C/D	0°C to +70°C	Dice
DG387CJ	0°C to +70°C	14 Lead Plastic DIP
DG387CWE	0°C to +70°C	16 Lead Wide SO
DG387CK	0°C to +70°C	14 Lead CERDIP
DG387BWE	-25°C to +85°C	16 Lead Wide SO

PART	TEMP. RANGE	PACKAGE
DG387BK	-25°C to +85°C	14 Lead CERDIP
DG387BA	-25°C to +85°C	10 Lead Metal Can
DG387AK	-55°C to +125°C	14 Lead CERDIP
DG387AA	-55°C to +125°C	10 Lead Metal Can
DG387AC/D	0°C to +70°C	Dice
DG387ACJ	0°C to +70°C	14 Lead Plastic DIP
DG387ACWE	0°C to +70°C	16 Lead Wide SO
DG387ACK	0°C to +70°C	14 Lead CERDIP
DG387ABWE	-25°C to +85°C	16 Lead Wide SO
DG387ABK	-25°C to +85°C	14 Lead CERDIP
DG387ABA	-25°C to +85°C	10 Lead Metal Can
DG390C/D	0°C to +70°C	Dice
DG390CJ	0°C to +70°C	16 Lead Plastic DIP
DG390CWE	0°C to +70°C	16 Lead Wide SO
DG390CK	0°C to +70°C	16 Lead CERDIP
DG390BWE	-25°C to +85°C	16 Lead Wide SO
DG390BK	-25°C to +85°C	16 Lead CERDIP
DG390AK	-55°C to +125°C	16 Lead CERDIP
DG390AC/D	0°C to +70°C	Dice
DG390ACJ	0°C to +70°C	16 Lead Plastic DIP
DG390ACWE	0°C to +70°C	16 Lead Wide SO
DG390ACK	0°C to +70°C	16 Lead CERDIP
DG390ABWE	-25°C to +85°C	16 Lead Wide SO
DG390ABK	-25°C to +85°C	16 Lead CERDIP

General Purpose CMOS Analog Switches

General Description

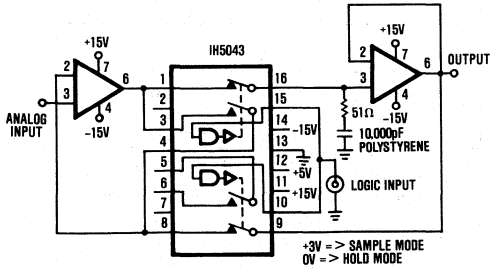
The IH5040 family consists of six CMOS analog switches that are intended for general purpose applications. These switches are latch-up proof, break-before-make single and dual versions of all the popular switch formats — SPST, SPDT, and DPST. Key features of the family include low leakage current of 1nA and quiescent current of less than 1μA.

Maxim IH5040 family has faster switching times than the original manufacturer's devices. All devices are bi-directional and maintain almost constant ON resistance throughout their operating range. These devices are guaranteed to operate from ±4.5V to ±18V, and will switch input signals that include the supplies.

Applications

PBX, PABX
Disc Drives
Guidance and Control Systems
Test Equipment
Sample and Holds
Military Radios

Typical Operating Circuit



Improved Sample & Hold
Using IH5043

Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Guaranteed ±4.5V to ±18V Operation**
- **Input Voltage Range Includes Supplies**
- **Latch-Up Proof Construction**
- **TTL, CMOS Logic Compatible**
- **Quiescent Current Less Than 1μA**
- **Monolithic Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
SINGLE POLE SINGLE THROW (SPST)		
IH5040C/D	0°C to +70°C	DICE
IH5040CJE	0°C to +70°C	16 Lead CERDIP
IH5040CPE	0°C to +70°C	16 Lead Plastic DIP
IH5040CWE	0°C to +70°C	16 Lead Wide SO
IH5040M/D	-55°C to +125°C	DICE
IH5040MJE	-55°C to +125°C	16 Lead CERDIP
DUAL SINGLE POLE SINGLE THROW (DUAL SPST)		
IH5041C/D	0°C to +70°C	DICE
IH5041CJE	0°C to +70°C	16 Lead CERDIP
IH5041CPE	0°C to +70°C	16 Lead Plastic DIP
IH5041CTW	0°C to +70°C	10 Lead Metal Can
IH5041CWE	0°C to +70°C	16 Lead Wide SO
IH5041M/D	-55°C to +125°C	DICE
IH5041MJE	-55°C to +125°C	16 Lead CERDIP
IH5041MTW	-55°C to +125°C	10 Lead Metal Can
SINGLE POLE DOUBLE THROW (SPDT)		
IH5042C/D	0°C to +70°C	DICE
IH5042CJE	0°C to +70°C	16 Lead CERDIP
IH5042CPE	0°C to +70°C	16 Lead Plastic DIP
IH5042CWE	0°C to +70°C	16 Lead Wide SO
IH5042M/D	-55°C to +125°C	DICE
IH5042MJE	-55°C to +125°C	16 Lead CERDIP
DUAL SINGLE POLE DOUBLE THROW (DUAL SPDT)		
IH5043C/D	0°C to +70°C	DICE
IH5043CJE	0°C to +70°C	16 Lead CERDIP
IH5043CPE	0°C to +70°C	16 Lead Plastic DIP
IH5043CWE	0°C to +70°C	16 Lead Wide SO
IH5043M/D	-55°C to +125°C	DICE
IH5043MJE	-55°C to +125°C	16 Lead CERDIP

(Ordering information continued on fourth page.)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

General Purpose CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) ..... < 30mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above +70°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltages
$V^+ - V^-$ ..... < 38V
$V^+ - V_D$ ..... < 30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... < 33V
$V_L - V_{IN}$ ..... < 30V
V_L - GND ..... < 20V
V_{IN} - GND ..... < 20V
Digital Inputs ..... $(V^+ + 0.3V)$ to $(V^+ - 38V)$
V_S or V_D ..... -0.3V to $(V^+ + 0.3V)$ (Note 1)

Note 1: Signals on S, D and digital inputs which exceed V^- or V^+ will be clamped by internal diodes. Limit forward diode current to 30mA maximum.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V^- = -15V, V_L = +5V, T_A = +25°C unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN./MAX. LIMITS						UNITS
			MILITARY			COMMERCIAL			
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
Input Logic Current	$I_{IN(ON)}$	V_{IN} = 2.4V (Note 3)	±1	±1	10	±1	±1	10	µA
Input Logic Current	$I_{IN(OFF)}$	V_{IN} = 0.8V (Note 3)	±1	±1	10	±1	±1	10	µA
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = 10mA V_{ANALOG} = -10V to +10V	75	75	150	80	80	130	Ω
Channel to Channel $r_{DS(ON)}$ Match	$\Delta r_{DS(ON)}$			25 (typ)			30 (typ)		Ω
Minimum Analog Signal Handling Capability	V_{ANALOG}			±11 (typ)			±10 (typ)		V
Switch OFF Leakage Current	$I_D/I_{S(OFF)}$	V_{ANALOG} = -10V to +10V		±1	100		±5	100	nA
Switch ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_D = V_S$ = -10V to +10V		±2	200		±10	100	nA
Switch "ON" Time	t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V.		750			1000		ns
Switch "OFF" Time	t_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V.		350			500		ns
Charge Injection	$Q_{(INJ.)}$			15 (typ)			20 (typ)		mV
Minimum Off Isolation Rejection Ratio	OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF		54 (typ)			50 (typ)		dB
V^+ Power Supply Quiescent Current	I^+_Q		1	1	10	10	10	100	µA
V^- Power Supply Quiescent Current	I^-_Q	V^+ = +15V, V^- = -15V, V_L = +5V	1	1	10	10	10	100	µA
+5V Supply Quiescent Current	I^-_{LQ}		1	1	10	10	10	100	µA
Ground Supply Quiescent Current	I_{GND}		1	1	10	10	10	100	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio	CCRR	One Channel Off.		54 (typ)			50 (typ)		dB

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted 1986 Component Data Catalog. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

General Purpose CMOS Analog Switches

- ◆ Guaranteed ±4.5V to ±18V Operation
- ◆ Guaranteed To Switch Signals Up To Either Supply
- ◆ Faster Switching Speeds

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +15V, V^- = -15V, V_L = +5V, T_A = +25°C unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN./MAX. LIMITS						UNITS
			MILITARY			COMMERCIAL			
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
Input Logic Current	$I_{IN(ON)}$	V_{IN} = 2.4V	±1	±1	10	±1	±1	10	µA
Input Logic Current	$I_{IN(OFF)}$	V_{IN} = 0.8V	±1	±1	10	±1	±1	10	µA
Input Logic Low	V_{IL}		0.8	0.8	0.8	0.8	0.8	0.8	V
Input Logic High	V_{IH}		2.4	2.4	2.4	2.4	2.4	2.4	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = -10V to +10V	75	75	150	80	80	130	Ω
Channel to Channel $r_{DS(ON)}$ Match	$\Delta r_{DS(ON)}$			3 (typ)			5 (typ)		Ω
Minimum Analog Signal Handling Capability	V_{ANALOG}			±15			±15		V
Switch OFF Leakage Current	$I_D/I_{S(OFF)}$	V_{ANALOG} = -10V to +10V		±1	100		±5	100	nA
Switch ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_D = V_S$ = -10V to +10V		±2	200		±10	100	nA
Switch "ON" Time	t_{ON}	Fig. A		400			400		ns
Switch "OFF" Time	t_{OFF}	Fig. A		200			200		ns
Charge Injection	$Q_{(INJ.)}$	Fig. B (Note 2)		15			20		mV
Minimum Off Isolation Rejection Ratio	OIRR	Fig. C, C_L < 5pF		54 (typ)			50 (typ)		dB
V^+ Quiescent Current	I^+_Q		1	1	10	10	10	100	µA
V^- Quiescent Current	I^-_Q		-1	-1	-10	-10	-10	-100	µA
+5V Quiescent Current	I_{LQ}		1	1	10	10	10	100	µA
Ground Quiescent Current	I_{GND}		1	1	10	10	10	100	µA
Min. Channel to Channel Cross Coupling Rej. Ratio	CCRR	One Channel Off (Note 2)		54 (typ)			50 (typ)		dB
Power Supply Range For Continuous Operation	V_{OP}	**Min. (Note 3)** **Max. (Note 3)**		±4.5 ±18			±4.5 ±18		V

Note 2: Not tested in production.
Note 3: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V are used.

Test Circuits

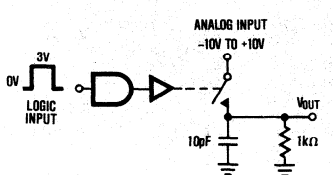


Figure A. Switching Time

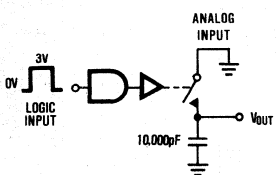


Figure B. Charge Injection

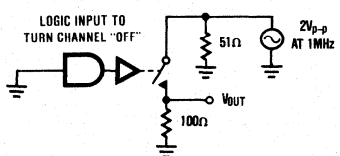
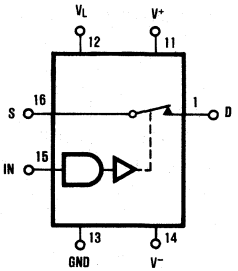


Figure C. Off Isolation Rejection Ratio

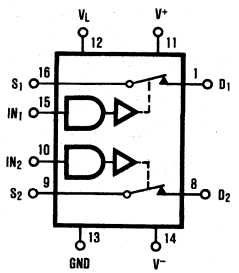
General Purpose CMOS Analog Switches

Pin Configuration & Switching State Diagrams

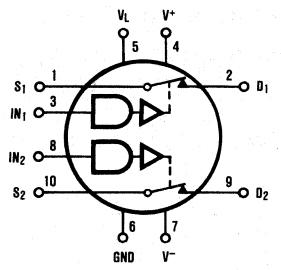
IH5040 SPST
DIP (JE, PE, WE)



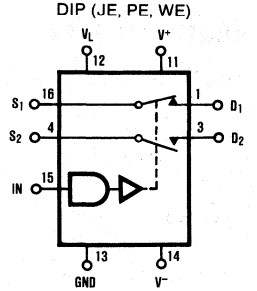
IH5041 Dual SPST
DIP (JE, PE, WE)



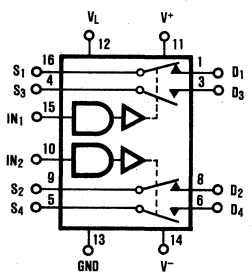
IH5041 Dual SPST
T0-100 Metal Can



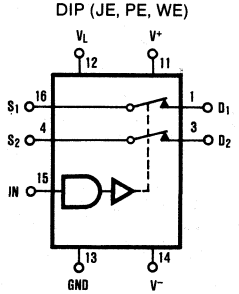
IH5042 SPDT
DIP (JE, PE, WE)



IH5043 Dual SPDT
DIP (JE, PE, WE)



IH5044 DPST
DIP (JE, PE, WE)



IH5045 Dual DPST
DIP (JE, PE, WE)

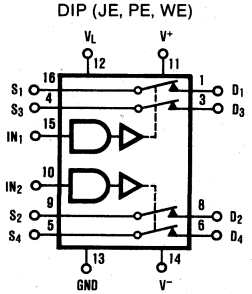


Table 1. USING THE 5040 FAMILY WITH ONLY 2 SUPPLIES

(V_L tied to V^+)

SUPPLY VOLTAGES	MIN. LOGIC I/P FOR "1" STATE
±15V	+12.6V
±12V	+9.6V
±10V	+7.6V
±5V	+2.6V

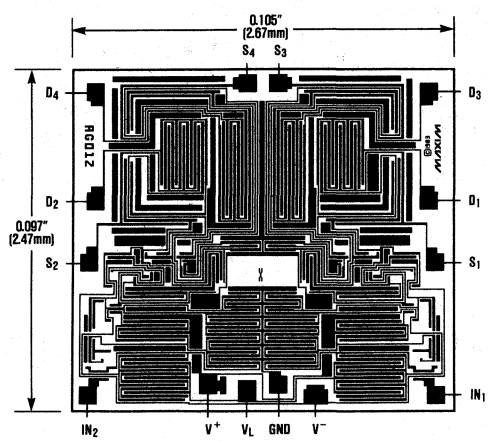
Note: Switch states are for logic "1" input.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
DOUBLE POLE SINGLE THROW (DPST)		
IH5044C/D	0°C to +70°C	DICE
IH5044CJE	0°C to +70°C	16 Lead CERDIP
IH5044CPE	0°C to +70°C	16 Lead Plastic DIP
IH5044CWE	0°C to +70°C	16 Lead Small Outline
IH5044M/D	-55°C to +125°C	DICE
IH5044MJE	-55°C to +125°C	16 Lead CERDIP
DUAL DOUBLE POLE SINGLE THROW (DUAL DPST)		
IH5045C/D	0°C to +70°C	DICE
IH5045CJE	0°C to +70°C	16 Lead CERDIP
IH5045CPE	0°C to +70°C	16 Lead Plastic DIP
IH5045CWE	0°C to +70°C	16 Lead Small Outline
IH5045M/D	-55°C to +125°C	DICE
IH5045MJE	-55°C to +125°C	16 Lead CERDIP

For the IH5042 and IH5044 in 10 Lead Metal Can Package Contact Factory. For all devices in Ceramic Flat Package Contact Factory.

Chip Topography



Low Charge Injection CMOS Analog Switches

General Description

Maxim's IH5048 Series of analog switches are designed for low charge injection and low leakage. They feature extremely low on resistance (35Ω typical) as well as quiescent power supply current below 1μA. The switch control inputs are fully compatible with both CMOS and TTL logic.

These switches are pin-for-pin replacements of the original manufacturer's devices with specification improvements in analog signal range and switch ON and OFF times. They are also compatible with the IH5040 family of analog switches. The IH5048 series is supplied in 16 pin Dual-In-Line and Small Outline packages.

Applications

Precision Sample/Hold Circuits

Transducer and Sensor Switching

Low Level Signal Conditioning

Battery Powered Instrumentation

Programmable Gain Amplifiers

Features

- Low Charge Injection (10pC Typ.)
- Quiescent Current Below 1μA
- TTL and CMOS Compatible
- Low On Resistance (40Ω Max.)
- Latch-Up Proof Construction

Ordering Information

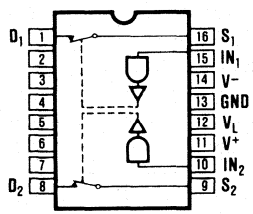
PART	TEMP. RANGE	PACKAGE
IH5048C/D	0°C to +70°C	Dice
IH5048CPE	0°C to +70°C	16 Lead Plastic DIP
IH5048CWE	0°C to +70°C	16 Lead Wide SO
IH5048CJE	0°C to +70°C	16 Lead CERDIP
IH5048M/D	-55°C to +125°C	Dice
IH5048MJE	-55°C to +125°C	16 Lead CERDIP

(Ordering Information is continued on last page.)

Pin Configurations

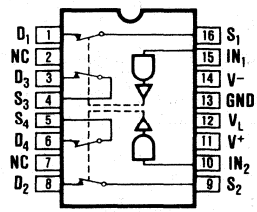
Top View

IH5048 - Dual SPST



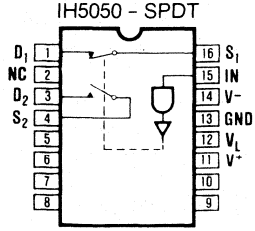
LOGIC	SWITCH
0	OFF
1	ON

IH5049 - Dual DPST



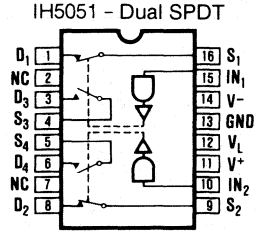
LOGIC	SWITCH
0	OFF
1	ON

IH5050 - SPDT



LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

IH5051 - Dual SPDT



LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Switch states are for Logic "1" Inputs (Positive Logic).

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Charge Injection CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltages
- $V^+ - V^-$ 36V
- $V^+ - V_D$ 30V
- $V_D - V^-$ 30V
- $V_D - V_S$ ..... ±28V
- $V_L - V^-$ 33V
- $V_L - V_{IN}$ 30V
- V_L - GND 20V
- V_{IN} - GND 20V
- Digital Inputs ..... $(V^+ + 0.3V)$ to $(V^+ - 38V)$
- V_S or V_D ..... -0.3V to $(V^+ + 0.3V)$ (Note 1)

Current (Any Terminal) 30mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above +70°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Note 1: Signals on S, D and digital inputs which exceed V^- or V^+ will be clamped by internal diodes. Limit forward diode current to 30mA maximum.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $T_A = 25°C$ unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN./MAX. LIMITS						UNITS
			MILITARY			COMMERCIAL			
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
Input Logic Current	$I_{IN(ON)}$	$V_{IN} = 2.4V$	±1	±1	10	±1	±1	10	µA
Input Logic Current	$I_{IN(OFF)}$	$V_{IN} = 0.8V$	±1	±1	10	±1	±1	10	µA
Drain-Source On Resistance	$r_{DS(ON)}$	$I_S = 10mA$ $V_{ANALOG} = -10V$ to $+10V$		40	60		45	75	Ω
Channel to Channel $r_{DS(ON)}$ Match	$\Delta r_{DS(ON)}$			15 (typ)			15 (typ)		Ω
Minimum Analog Signal Handling Capability	V_{ANALOG}			±10			±10		V
Switch OFF Leakage Current	$I_D/I_{S(OFF)}$	$V_{ANALOG} = -10V$ to $+10V$		±1	100		±5	100	nA
Switch ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_D = V_S = -10V$ to $+10V$		±2	200		±10	200	nA
Switch "ON" Time	t_{ON}	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$		500			1000		ns
Switch "OFF" Time	t_{OFF}	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$		250			500		ns
Charge Injection	$Q_{(INJ)}$			1 (typ)			2 (typ)		mV
Minimum Off Isolation Rejection Ratio	OIRR	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$		54 (typ)			50 (typ)		dB
V^+ Power Supply Quiescent Current	I^+_Q		1	1	10	10	10	100	µA
V^- Power Supply Quiescent Current	I^-_Q	$V^+ = +15V$, $V^- = -15V$, $V_L = +5V$	-1	-1	-10	-10	-10	-100	µA
+5V Supply Quiescent Current	I^-_{LQ}		1	1	10	10	10	100	µA
Ground Supply Quiescent Current	I_{GND}		1	1	10	10	10	100	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio	CCRR	One Channel Off		54 (typ)			50 (typ)		dB

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted 1987 Component Data Catalog. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excepts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Charge Injection CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +15V, V^- = -15V, V_L = +5V, T_A = 25°C unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN./MAX. LIMITS						UNITS
			MILITARY			COMMERCIAL			
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
Input Logic Current	$I_{IN(ON)}$	V_{IN} = 2.4V	±1	±1	10	±1	±1	10	μA
Input Logic Current	$I_{IN(OFF)}$	V_{IN} = 0.8V	±1	±1	10	±1	±1	10	μA
Input Logic Low	**V_{IL}**		**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	**V**
Input Logic High	**V_{IH}**		**2.4**	**2.4**	**2.4**	**2.4**	**2.4**	**2.4**	**V**
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = 10mA V_{ANALOG} = -10V to +10V	40	40	60	45	45	75	Ω
Channel to Channel $r_{DS(ON)}$ Match	$\Delta r_{DS(ON)}$			8 (typ)			8 (typ)		Ω
Minimum Analog Signal Handling Capability	**V_{ANALOG}**		**±14**	**±14**	**±14**	**±14**	**±14**	**±14**	**V**
Switch OFF Leakage Current	$I_D/I_{S(OFF)}$	V_{ANALOG} = -10V to +10V		±1	100		±5	100	nA
Switch ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -10V to +10V		±2	200		±10	200	nA
Switch "ON" Time	**t_{ON}**	**Fig. A**		**400**			**600**		**ns**
Switch "OFF" Time	**t_{OFF}**	**Fig. A**		**200**			**300**		**ns**
Charge Injection	Q_{INJ}	Fig. B (Note 2)		10 (typ)			10 (typ)		pC
Minimum Off Isolation Rejection Ratio	OIRR	Fig. C, C_L < 5pF		54 (typ)			50 (typ)		dB
V^+ Quiescent Current	I^+_Q	V_{IN} = 0.8V or 2.4V V^+ = +15V, V^- = -15V, V_L = +5V	1	1	10	10	10	100	μA
V^- Quiescent Current	I^-_Q		-1	-1	-10	-10	-10	-100	μA
+5V Quiescent Current	I^-_{LQ}		1	1	10	10	10	100	μA
Ground Quiescent Current	I_{GND}		1	1	10	10	10	100	μA
Minimum Channel to Channel Cross Coupling Rejection Ratio	CCRR	One Channel Off (Note 2)		54 (typ)			50 (typ)		dB

Note 2: Not tested in production.

Test Circuits

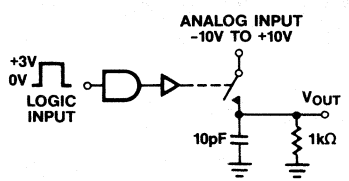


Figure A. Switching Time

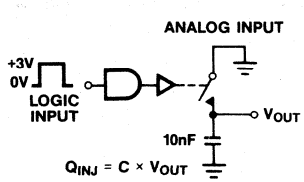


Figure B. Charge Injection

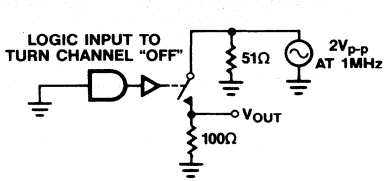
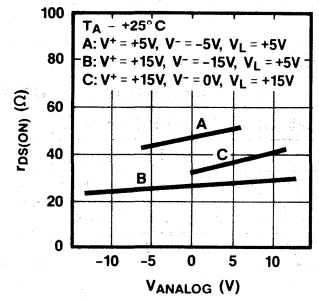


Figure C. Off Isolation Rejection Ratio

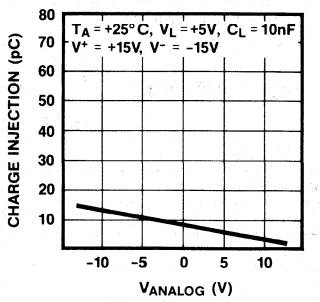
Low Charge Injection CMOS Analog Switches

Typical Operating Characteristics

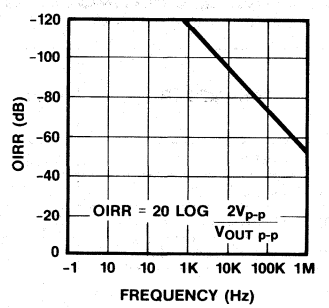
$r_{DS(ON)}$ vs. ANALOG SIGNAL



CHARGE INJECTION vs. V_{ANALOG} (See Fig. B)



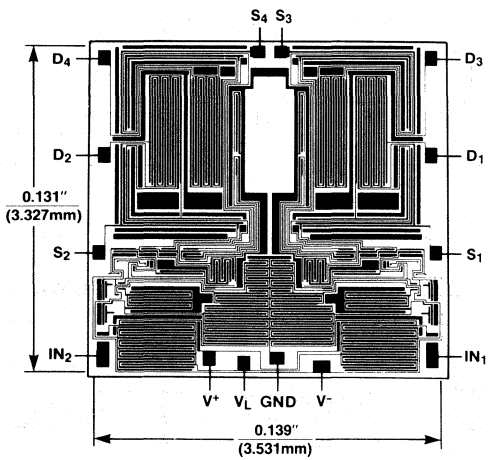
OFF ISOLATION REJECTION RATIO (OIRR) (See Fig. C)



Logic Inputs

The IH5048 family operates with plus/minus as well as single ended power supplies (with V^- = 0V). Full TTL compatibility is maintained for the control inputs over a wide power supply range when V_L = +5V. When V_L is connected to voltages other than +5V, the logic input thresholds are +0.8V for a logic LOW and V_L - 1V for a logic HIGH. This means that when V_L is connected to V^+ at voltages other than 5V, CMOS logic levels should be used.

Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
IH5049C/D	0°C to +70°C	Dice
IH5049CPE	0°C to +70°C	16 Lead Plastic DIP
IH5049CWE	0°C to +70°C	16 Lead Wide SO
IH5049CJE	0°C to +70°C	16 Lead CERDIP
IH5049M/D	-55°C to +125°C	Dice
IH5049MJE	-55°C to +125°C	16 Lead CERDIP
IH5050C/D	0°C to +70°C	Dice
IH5050CPE	0°C to +70°C	16 Lead Plastic DIP
IH5050CWE	0°C to +70°C	16 Lead Wide SO
IH5050CJE	0°C to +70°C	16 Lead CERDIP
IH5050M/D	-55°C to +125°C	Dice
IH5050MJE	-55°C to +125°C	16 Lead CERDIP
IH5051C/D	0°C to +70°C	Dice
IH5051CPE	0°C to +70°C	16 Lead Plastic DIP
IH5051CWE	0°C to +70°C	16 Lead Wide SO
IH5051CJE	0°C to +70°C	16 Lead CERDIP
IH5051M/D	-55°C to +125°C	Dice
IH5051MJE	-55°C to +125°C	16 Lead CERDIP

Contact factory for devices in Flat Pack packages.

Low Power Fast CMOS Analog Switches

General Description

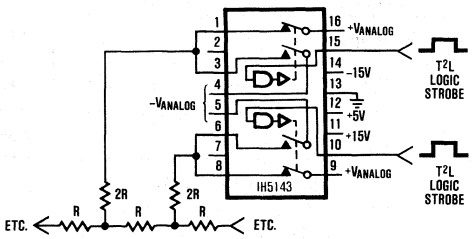
The IH5140 family consists of six CMOS analog switches that are intended for high speed general purpose applications. These switches are latch-up proof, break-before-make single and dual versions of all the popular switch formats — SPST, SPDT, and DPST. Key features of the family include toggle rates in excess of 1MHz, t_{ON} times of 80ns typical and t_{OFF} times of 50ns. OFF leakage current is less than 100pA maximum at +25°C and quiescent currents are 1μA maximum, making the switches ideal for portable equipment.

Maxim has significantly improved the design of these switches versus the original manufacturer. Maxim's switches are guaranteed to operate from ±4.5V to ±18V, and will switch input signals that include the supplies.

Applications

High Speed Test Equipment
Sample and Hold Circuits
Guidance and Control Systems
Radar Systems
Aircraft Head-Up Displays
Military Radios

Typical Operating Circuit



Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

Features

- ♦ Pin for Pin 2nd Source!
- ♦ Break-Before-Make Switching Action
- ♦ Fast t_{ON} (80ns typ.) and t_{OFF} (50ns)
- ♦ Input Signal Range Includes Supply Rails
- ♦ Guaranteed ±4.5V to ±18V Operation
- ♦ Low OFF Leakage Current — 100pA max.
- ♦ Greater than 1MHz Toggle Rate
- ♦ TTL and CMOS Compatible

Ordering Information

PART	TEMP. RANGE	PACKAGE
SINGLE POLE SINGLE THROW (SPST)		
IH5140C/D	0°C to +70°C	DICE
IH5140CJE	0°C to +70°C	16 Lead CERDIP
IH5140CPE	0°C to +70°C	16 Lead Plastic DIP
IH5140CWE	0°C to +70°C	16 Lead Wide SO
IH5140M/D	-55°C to +125°C	DICE
IH5140MJE	-55°C to +125°C	16 Lead CERDIP
DUAL SINGLE POLE SINGLE THROW (DUAL SPST)		
IH5141C/D	0°C to +70°C	DICE
IH5141CJE	0°C to +70°C	16 Lead CERDIP
IH5141CPE	0°C to +70°C	16 Lead Plastic DIP
IH5141CTW	0°C to +70°C	10 Lead Metal Can
IH5141CWE	0°C to +70°C	16 Lead Wide SO
IH5141M/D	-55°C to +125°C	DICE
IH5141MJE	-55°C to +125°C	16 Lead CERDIP
IH5141MTW	-55°C to +125°C	10 Lead Metal Can
SINGLE POLE DOUBLE THROW (SPDT)		
IH5142C/D	0°C to +70°C	DICE
IH5142CJE	0°C to +70°C	16 Lead CERDIP
IH5142CPE	0°C to +70°C	16 Lead Plastic DIP
IH5142CWE	0°C to +70°C	16 Lead Wide SO
IH5142M/D	-55°C to +125°C	DICE
IH5142MJE	-55°C to +125°C	16 Lead CERDIP
DUAL SINGLE POLE DOUBLE THROW (DUAL SPDT)		
IH5143C/D	0°C to +70°C	DICE
IH5143CJE	0°C to +70°C	16 Lead CERDIP
IH5143CPE	0°C to +70°C	16 Lead Plastic DIP
IH5143CWE	0°C to +70°C	16 Lead Wide SO
IH5143M/D	-55°C to +125°C	DICE
IH5143MJE	-55°C to +125°C	16 Lead CERDIP

(Ordering information continued on fourth page.)

Low Power Fast CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) ..... < 30mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above +70°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltages
$V^+ - V^-$ ..... < 38V
$V^+ - V_D$ ..... < 30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... < 33V
$V_L - V_{IN}$ ..... < 30V
V_L - GND ..... < 20V
V_{IN} - GND ..... < 20V
Digital Inputs ..... $(V^+ + 0.3V)$ to $(V^+ - 38V)$
V_S or V_D ..... -0.3V to $(V^+ + 0.3V)$ (Note 1)

Note 1: Signals on S, D and digital inputs which exceed V^- or V^+ will be clamped by internal diodes. Limit forward diode current to 30mA maximum.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(All Parameters with $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN./MAX. LIMITS						UNITS
			MILITARY			COMMERCIAL			
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
Input Logic Current	I_{INH}	V_{IN} = 2.4V (Note 2)	±1	±1	10	±1	±1	10	µA
Input Logic Current	I_{INL}	V_{IN} = 0.8V (Note 2)	±1	±1	10	±1	±1	10	µA
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -10mA V_{ANALOG} = -10V to +10V	50	50	75	75	75	100	Ω
Channel to Channel $r_{DS(ON)}$ Match	$\Delta r_{DS(ON)}$			3 (typ)			5 (typ)		Ω
Minimum Analog Signal Handling Capability	V_{ANALOG}			±15			±15		V
Switch OFF Leakage Current	$I_{D(OFF)}$ + $I_{S(OFF)}$	V_D = +10V, V_S = -10V V_D = -10V, V_S = +10V		±0.5 ±0.5	100 100		±5 ±5	100 100	nA
Switch ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	$V_D = V_S$ = -10V to +10V		±1	200		±2	200	nA
Switch "ON" Time Switch "OFF" Time	t_{ON} t_{OFF}		See switching time specifications and timing diagrams.						
Charge Injection	$Q_{(INJ.)}$	(Note 3)		10 (typ)			15 (typ)		pC
Minimum Off Isolation Rejection Ratio	OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF (Note 3)		54 (typ)			50 (typ)		dB
+ Power Supply Quiescent Current	I^+	V^+ = +15V, V^- = -15V, V_L = +5V	1.0	1.0	10.0	10	10	100	µA
- Power Supply Quiescent Current	I^-		-1.0	-1.0	-10.0	-10	-10	-100	µA
+5V Supply Quiescent Current	I_L		1.0	1.0	10.0	10	10	100	µA
Ground Supply Quiescent Current	I_{GND}		1.0	1.0	10.0	10	10	100	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio	CCRR	One Channel Off (Note 3)		54 (typ)			50 (typ)		dB
Power Supply Range for Continuous Operation	V_{OP}	(Note 4)		±4.5 (min) ±18V (max)			±4.5 (min) ±18V (max)		V

Note:
2. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however, 0.8V to 2.4V describes the minimum range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
3. Typical values are for design aid only, not guaranteed and not subject to production testing.
4. Electrical characteristics, such as ON Resistance, will change when power supplies, other than ±15V, are used.

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

PART NUMBER	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MILITARY -55°C	MILITARY +25°C	MILITARY +125°C	COMMERCIAL 0°C	COMMERCIAL +25°C	COMMERCIAL +70°C	UNITS
IH5140-5141	Switch "ON" time	t_{on}	Figure 1		100*			150		ns
	Switch "OFF" time	t_{off}			75*			125		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		
	Switch "ON" time	t_{on}	Figure 2		150			175		ns
	Switch "OFF" time	t_{off}			125			150		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		
IH5142-5143	Switch "ON" time	t_{on}	Figure 1		175*			250		ns
	Switch "OFF" time	t_{off}			125*			150		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		
	Switch "ON" time	t_{on}	Figure 2		200			300		ns
	Switch "OFF" time	t_{off}			125			150		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		
	Switch "ON" time	t_{on}	Figure 3		175*			250		ns
	Switch "OFF" time	t_{off}			125*			150		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		
	Switch "ON" time	t_{on}	Figure 4		200			300		ns
	Switch "OFF" time	t_{off}			125			150		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		
IH5144-5145	Switch "ON" time	t_{on}	Figure 1		175*			250		ns
	Switch "OFF" time	t_{off}			125*			150		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		
	Switch "ON" time	t_{on}	Figure 2		200			300		ns
	Switch "OFF" time	t_{off}			125			150		
	Break-before-make	t_{on}-t_{off}			10* TYP			5		

Note: Switching times are measured at 90% points.

* Guaranteed but not subjected to production testing.

Switching Time Test Circuits

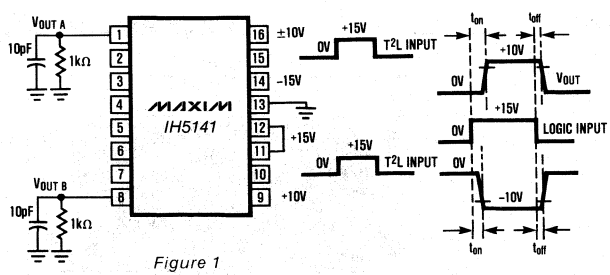


Figure 1

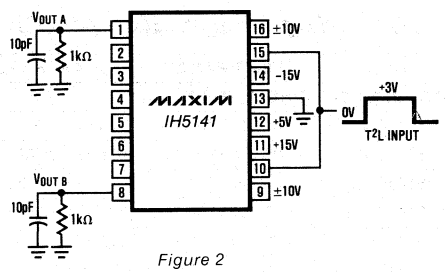


Figure 2

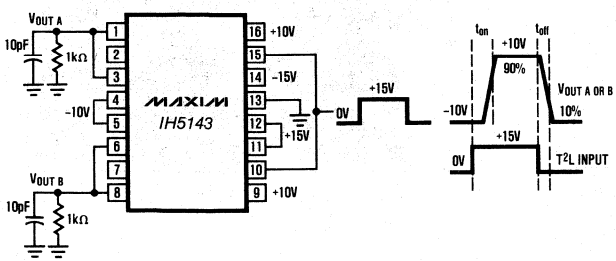


Figure 3

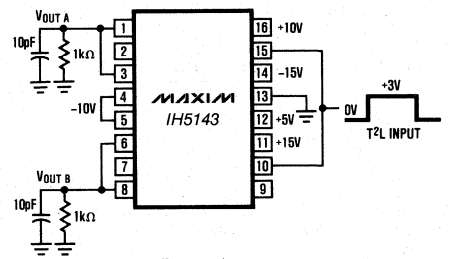
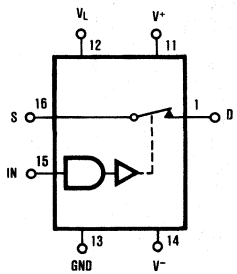


Figure 4

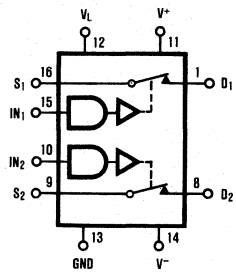
Low Power Fast CMOS Analog Switches

Pin Configuration and Switching State Diagrams

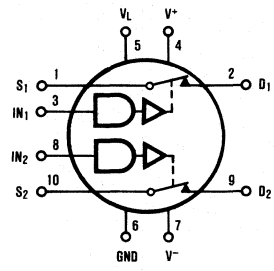
IH5140 SPST
DIP (JE, PE, WE)



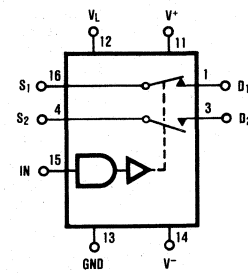
IH5141 Dual SPST
DIP (JE, PE, WE)



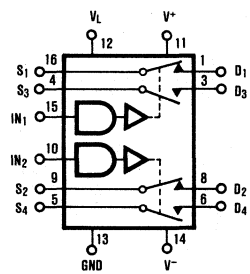
IH5141 Dual SPST
TO-100 Metal Can



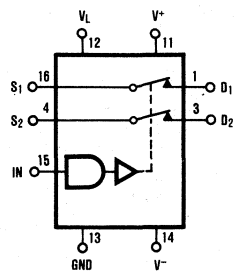
IH5142 SPDT
DIP (JE, PE, WE)



IH5143 Dual SPDT
DIP (JE, PE, WE)



IH5144 DPST
DIP (JE, PE, WE)



IH5145 Dual DPST
DIP (JE, PE, WE)

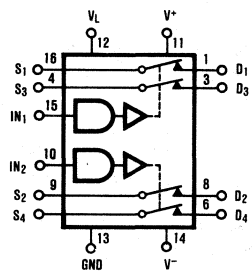


Table 1. USING THE 5140 FAMILY WITH ONLY 2 SUPPLIES

(V_L tied to V^+)

SUPPLY VOLTAGES	MIN. LOGIC I/P FOR "1" STATE
±15V	+12.6V
±12V	+9.6V
±10V	+7.6V
±5V	+2.6V

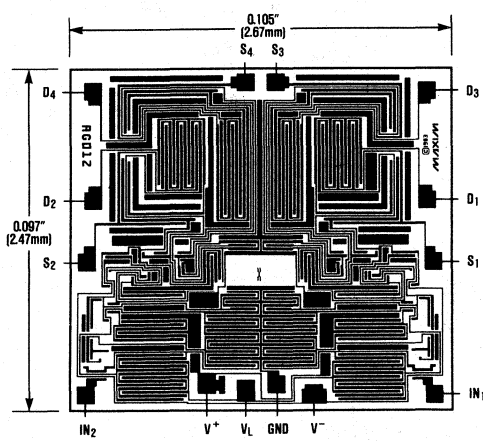
Note: Switch states are for logic "1" input.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
DOUBLE POLE SINGLE THROW (DPST)		
IH5144C/D	0°C to +70°C	DICE
IH5144CJE	0°C to +70°C	16 Lead CERDIP
IH5144CPE	0°C to +70°C	16 Lead Plastic DIP
IH5144CWE	0°C to +70°C	16 Lead Wide SO
IH5144M/D	-55°C to +125°C	DICE
IH5144MJE	-55°C to +125°C	16 Lead CERDIP
DUAL DOUBLE POLE SINGLE THROW (DUAL DPST)		
IH5145C/D	0°C to +70°C	DICE
IH5145CJE	0°C to +70°C	16 Lead CERDIP
IH5145CPE	0°C to +70°C	16 Lead Plastic DIP
IH5145CWE	0°C to +70°C	16 Lead Wide SO
IH5145M/D	-55°C to +125°C	DICE
IH5145MJE	-55°C to +125°C	16 Lead CERDIP

For the IH5142 and IH5144 in 10 Lead Metal Can package contact factory. For all devices in Ceramic Flat Package contact factory.

Chip Topography



General Description

The IH5341 and the IH5352 are dual and quad, single pole single throw (SPST) switches designed specifically for switching RF and video signals. Maxim's IH5341 and IH5352 incorporate an enhanced series-shunt-series structure, providing 70dB of OFF isolation and cross coupling rejection (an additional 10dB compared with other manufacturers' products).

Both devices can be operated with supplies ranging from ±5V to ±15V. The switches typically have a t_{ON} = 160ns and a t_{OFF} = 70ns, assuring break-before-make switching. The channel thruput resistance of 50Ω provides excellent matching to video impedances. In the D.C. state, with switches being either on or off, power supply quiescent currents are typically 100nA. This limits the quiescent current drain to 3μ watts—ideal for portable equipment.

Applications

These devices are used in applications requiring the routing, blocking or switching of video or RF signals such as:

Winchester Disk Drives
Commercial TV Cameras
Video Special Effects
Low Power RF Switching
Radar Switching
Mil and Space Communications

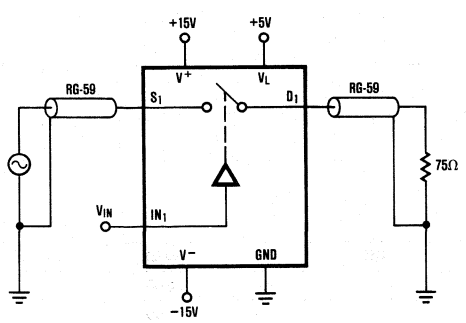
Features

- **"OFF" Isolation ≥ 70dB @ 10MHz**
- **Cross Coupling Isolation ≥ 70dB @ 10MHz**
- **$r_{ds(on)}$ < 75Ω, < 3dB Loss from DC to 100 MHz**
- **±5V to ±15V Operating Supply Range**
- **Supply Currents < 1μA**
- **Fast, Break-Before-Make Switching (70ns/160ns typ.)**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
IH5341CPD	0°C to +70°C	14 Lead Plastic DIP
IH5341IJD	-20°C to +85°C	14 Lead CERDIP
IH5341ITW	-20°C to +85°C	10 Lead TO-100
IH5341MJD	-55°C to +125°C	14 Lead CERDIP
IH534IMTW	-55°C to +125°C	10 Lead TO-100
IH5341C/D	0°C to 70°C	Dice
IH5352CPE	0°C to +70°C	16 Lead Plastic DIP
IH5352IJE	-20°C to +85°C	16 Lead
IH5352MJE	-55°C to +125°C	16 Lead CERDIP
IH5352C/D	0°C to 70°C	Dice

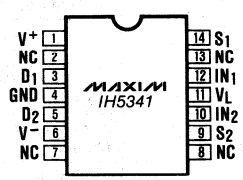
Typical Operating Circuit



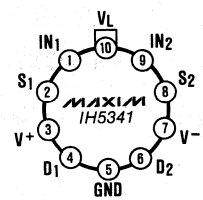
75Ω Video Switch
(Only one channel shown)

Pin Configuration

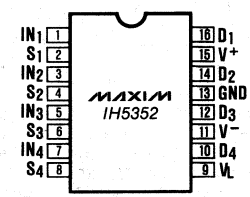
Top View



14 Lead DIP



10 Lead TO-100



16 Lead DIP

Dual/Quad RF/Video Switches

ABSOLUTE MAXIMUM RATINGS

Supply Voltages V^+ and V^- ..... ±17V
Current in any Terminal 50mA
Analog Input Voltage ..... V^+ to V^-
Operating Temperature Range
(M Version) -55°C to +125°C
(I Version) -20°C to +85°C
(C Version) 0°C to +70°C

Power Dissipation 250mW
(Derate 7.5mW/°C above 25°C)
Storage Temperature Range ..... -65°C to +150°C
Logic Control Voltage ..... V^+ to V^-
Voltage on V_L Pin ..... V^+ to V^-
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V_L = +5V, V^- = -15V, T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	TYP (Note 1)	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
				-55°C	+25°C	+125°C	-20/ 0°C	+25°C	+85/ +70°C	
Supply Voltage Ranges Positive Supply Logic Supply Negative Supply	 V^+ V_L V^-	(Note 3)	 4.5 > 16 4.5 > V^+ -4 > -16		 5 to 15 5 to V^+ -5 to -15			 5 to 15 5 to V^+ -5 to -15		V
Switch "ON" Resistance (Note 4)	$r_{ds(ON)}$	V_D - 5V to +5V		75	75	100	75	75	100	Ω
		I_S = 10 mA, V_{IN} = 2.4V V_D = -10V to +10V		125	125	175	150	150	175	
Switch "ON" Resistance	$r_{ds(ON)}$	V = V_L = 5V, V_{IN} = 3V V^- = -5V, V_D = ±3V		250	250	350	300	300	350	
On Resistance Match		I_S = 10mA, V_D = ±5V	5							
Switch "OFF" Leakage (Notes 2 and 4)	$I_{D(OFF)}$ or $I_{S(OFF)}$	$V_{S/D}$ = +5V to -5V V_{IN} = 0.8V			±1	50		±2	100	nA
		$V_{S/D}$ = +14V to -14V			±1	50		±2	100	
Switch "ON" Leakage	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = +5V or -5V V_{IN} = 2.4V			±1	100		±2	100	
		V_D = +14V to -14V			±1	100		±2	100	
Input Logic Current	I_{IN}	V_{IN} > 2.4V or < 0	0.001	1	1	10	1	1	10	µA
Positive Supply Quiescent Current	I^+	V_{IN} = 0V or +5V (Note 5)	0.01	1	1	10	1	1	10	
Negative Supply Quiescent Current	I^-	V_{IN} = 0V or +5V (Note 5)	0.01	1	1	10	1	1	10	
Logic Supply Quiescent Current	I_L	V_{IN} = 0V or +5V (Note 5)	0.01	1	1	10	1	1	10	

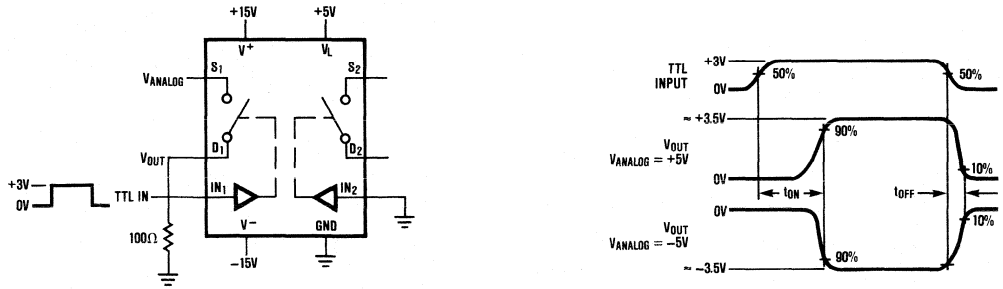
AC ELECTRICAL CHARACTERISTICS

V^+ = +15V, V_L = +5V, V^- = 0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch "ON" Time	t_{ON}	See Figure 1		160	300	ns
Switch "OFF" Time	t_{OFF}	See Figure 1		70	150	
"OFF" Isolation Rejection Ratio	OIRR	See Figure 2 (Note 6)	70	80		dB
Cross Coupling Rejection Ratio	CCRR	Figure 3 IH5341 (Note 6) IH5352	70 66	80 72		
Frequency where $r_{ds(ON)}$ = 0.7 x DC		(Note 6)	100			MHz

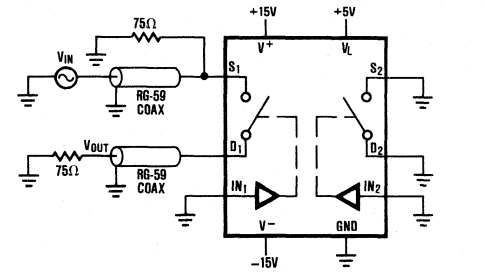
Note 1: Typical values are not tested in production. They are given as a design aid only.
Note 2: Positive and negative voltages applied to opposite sides of switch, in both directions successively.
Note 3: These are the operating voltages at which the other parameters are tested, and are not directly tested.
Note 4: The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.
Note 5: Maximum values shown are for the dual (IH5341). They are doubled for the quad (IH5352).
Note 6: All AC parameters are sample tested only. Test circuits should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

Test Circuits



Note: Only one channel shown. Others act identically.

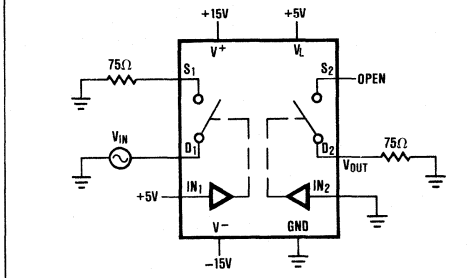
Figure 1. Switching Time Test Circuit and Waveforms



V_{IN} = ±5V ($10V_{p-p}$) @ f = 10MHz OIRR = $20 \log \frac{V_{IN}}{V_{OUT}}$

Note: Only one channel shown. Others act identically.

Figure 2. OFF Isolation Test Circuit

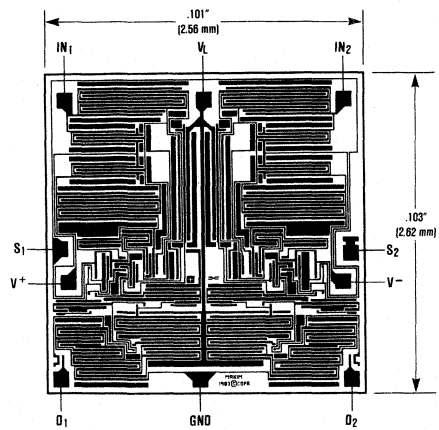


V_{IN} 225mVrms @ f = 10MHz

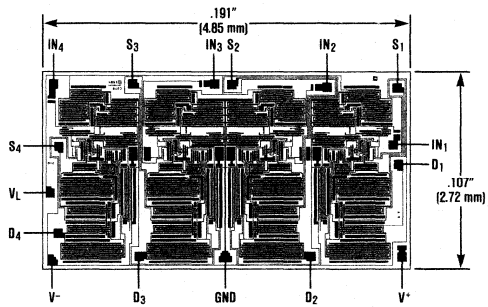
CCRR = $20 \log \frac{V_{IN}}{V_{OUT}}$

Figure 3. Cross-Coupling Rejection Test Circuit

Chip Topography



IH5341 (Dual SPST)



IH5352 (Quad SPST)

Appendix

A

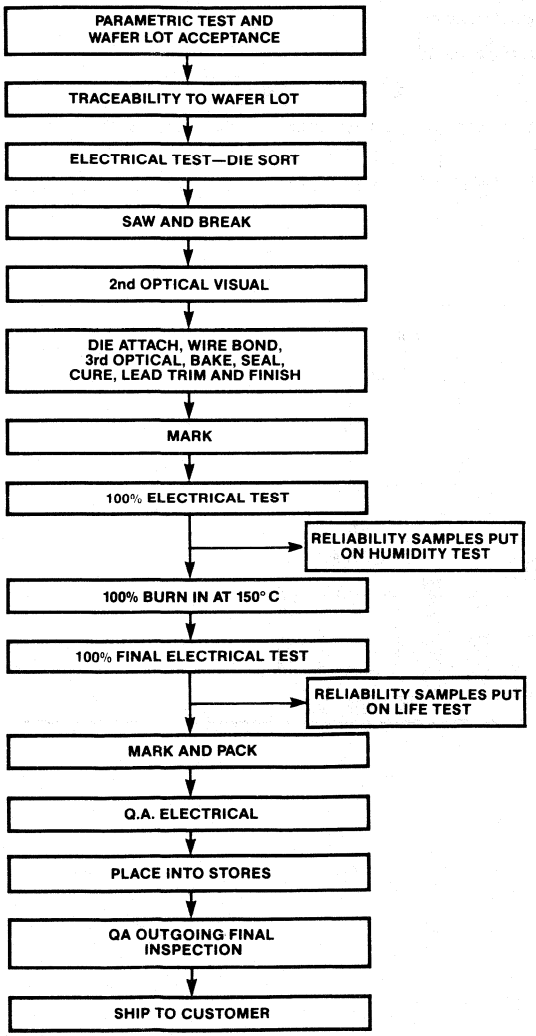
Package Unit Process Flow

Wafer Inspection

All wafers are fabricated using specifically developed processes with extremely tight control. Each must pass numerous in-process check-points for oxide thickness, critical dimensions, pin hole densities, and other requirements, and must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are inspected optically to detect any physical defects. Then they are parametrically tested to insure full conformity to Maxim's specifications. Our parametric measurement capability has been specially designed by Maxim to make the precision measurements which are mandatory to insure reliability and reproducibility in analog circuits. We believe this quality control technology to be the best in the industry, capable of resolving below IpA current levels, and less than IpF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters which are crucial to predicting long term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.



Testing

After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested *over temperature.* This is not a common practice in the industry. By using the latest high speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

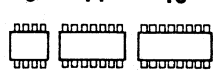
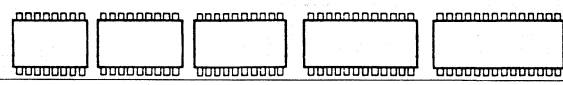
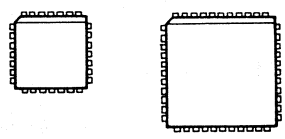
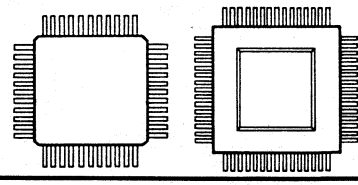
Sophisticated testing is an integral part of delivering the highest quality data acquisition products. Maxim's analog test capability represents an order of magnitude improvement in accuracy, noise performance, and speed when compared to current industry standards. This provides the customer with total assurance that he will receive the part he paid for every time, without fail.

Product Conditioning and Qualification

Reliability of Maxim's products is further assured by subjecting parts to qualification cycles that include accelerated life tests equivalent to 20 million operating hours, as well as pressure and humidity (85°C/85%) cycles. In addition, *every unit shipped has been burned-in* (with the exception of reversed lead and Surface Mount Products—see below) to further reduce the possibility of field failure.

Products processed to this level are normally available from other manufacturers at a price premium, by ordering special process flows. *Maxim provides this testing and conditioning, including a 100% burn-in, at no additional cost.*

Maxim is committed to providing high quality, high reliability 8 to 60 lead plastic surface mount products. With few exceptions, every monolithic product will be offered in a surface mount package. These products are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels, with the exception of 100% burn-in and cold test. They receive the same product conditioning and lot qualification as the DIPs. Maxim still assures the reliability of every lot by subjecting a sample from each lot to a long term life test prior to shipment.

PACKAGE	PKG ALPHA	LEAD COUNTS AVAILABLE
0.150" JEDEC SOIC	S	8 14 16 
0.300" JEDEC SOIC	W	16 18 20 24 28 
CERAMIC LEADLESS CHIP CARRIER (LCC)	L	20 
QUAD PACK JEDEC PLCC	Q	28 44 
FLAT PACK (PFP) 0.8 mm LEAD CENTERS	M	44 60 

Pin Convention

0.150" JEDEC SOIC (S) parts have the same pinout as in the 0.300" DIP package equivalents.

0.300" JEDEC SOIC (W) parts also have the same pinout as in the 0.300" DIP package except for selected products in the 16 lead. 14 lead products that are too large for the 0.150" 14 lead (S) package are made available in the 0.300" 16 lead (W) package.

Flatpack Pin Convention

No fixed convention exists for 40-lead products assembled in either 44-lead or 60-lead flatpack. Consult product marketing for specific pin-outs.

Quad Pack Pin Convention

1.) Devices in the 28 Lead Quad Pack are pin for pin number compatible with the DIP package. That is to say, pin 1 on the 28L Quad will be the same function as pin 1 on the DIP package.

2.) All 40 Lead devices planned for the 44 Lead Quad pack will have the following pin convention:

DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#
	1 N/C		12 N/C		23 N/C		34 N/C
1	2	11	13	21	24	31	35
2	3	12	14	22	25	32	36
3	4	13	15	23	26	33	37
4	5	14	16	24	27	34	38
5	6	15	17	25	28	35	39
6	7	16	18	26	29	36	40
7	8	17	19	27	30	37	41
8	9	18	20	28	31	38	42
9	10	19	21	29	32	39	43
10	11	20	22	30	33	40	44

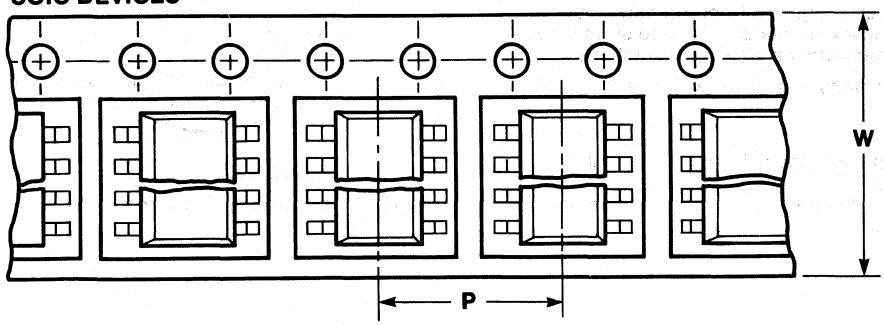
Surface Mount Packages In Reeled Tape

Maxim surface mount packages are normally shipped in antistatic plastic rails. They are also available mounted in pockets on embossed tape for customers using automatic placement systems. The tape is wound and shipped on reels.

The following table and diagrams indicate the tape sizes used for the various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
SOIC	8L	12	8
	14L	16	8
	16L	16	8
SOIC	16L	16	12
	18L	24	12
	20L	24	12
	24L	24	12
	28L	24	12
PLCC	28L	24	16
	44L	32	24
PFP	44L	24	16
	60L	44	32

SOIC DEVICES



USER DIRECTION OF FEED

All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow" the standard to ensure lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet 25°C worst case parameters.

Generally, the parameters or parameter limits listed in the packaged unit data sheets are tested during electrical probe. However some parameters are impossible to test or test with absolute accuracy on unassembled product. Information regarding any of these parameters/parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	3"	4"	UNITS
Chip Thickness Backlapped wafers	13 ± 1	15 ± 1	mils
Die length/width tolerance	± 1		mils
Bonding pads dimensions (minimum)	4.0 x 4.0		mils
Bonding pad and interconnect material thickness	10K–15K		A
Storage temperature	-40 to +150		°C
Operating temperature	-20 to +70		°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010.2, Condition B with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by HF etching or by plasma etching. The bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.

Maxim guarantees die and wafer AQL levels as follows:

Visual	1.0%
Functional Electrical Testing	0.65%
Parametric DC Testing	2.5%
Untested Parameters	6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry ambient—preferably inert gas. Extreme care should be taken when handling die. Both electrical and visual damage can occur as a result of an unclean environment or harsh handling techniques.

Die Attach

To prevent oxidization the die attach operation should be done under a gaseous nitrogen ambient atmosphere. If an eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C.

Bonding

Thermosonic or thermocompression gold ball bonding may be used with 1.0 or 1.3 mil diameter 99.99% pure gold wire. Ultrasonic bonding may be used with 1.0 or 1.25 mil diameter 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Die and wafers are packaged as shown in Figures 1 and 2, respectively.

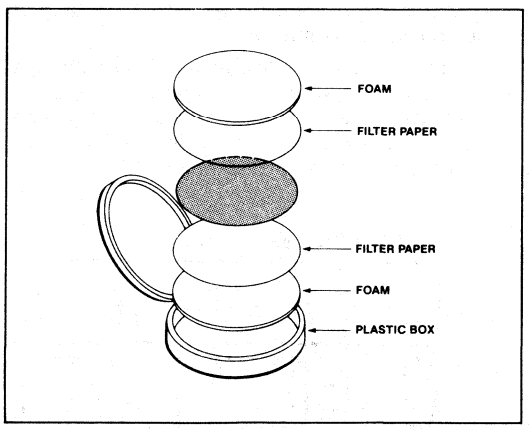


Figure 1. Wafer Carrier Package

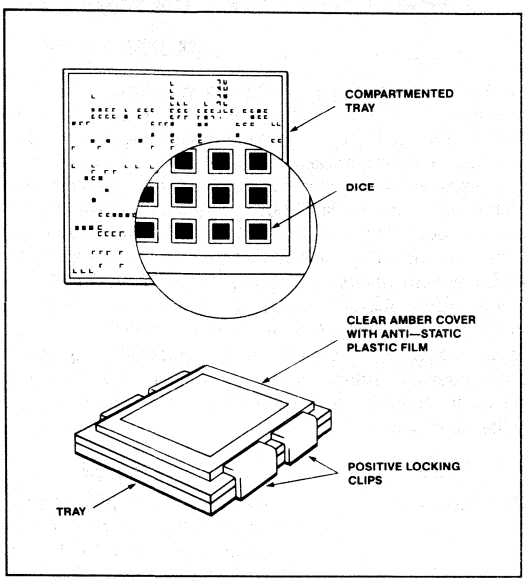


Figure 2. Die Carrier Package

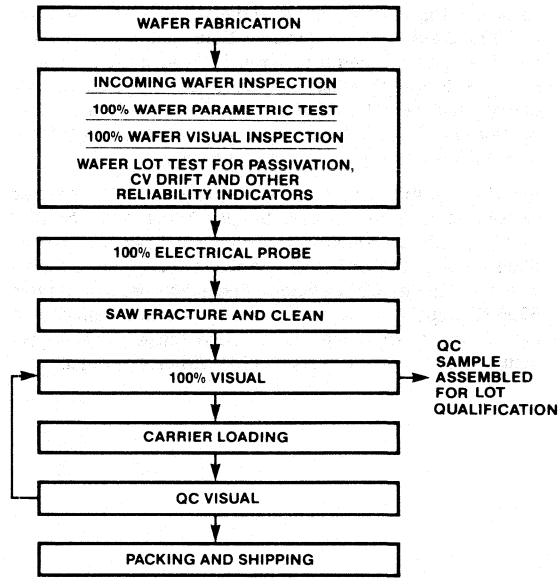
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the shipment date of the die to the user. Maxim assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

Dice Process Flow



Ordering Information

Die orders are identified by a /D suffix.
Example: ICL7109C/D

When ordering die in wafer form replace "D" in the part numbers with a "W"
Example: MAX7231C/D Die = MAX7231C/W Wafer.

A

Maxim's /883 and /HR Program

883 PROGRAM

As of July 1st, 1988, Maxim is a certified manufacturer of Mil-Std-883, Class B, Rev. C product. Becoming a manufacturer capable of processing product to 883 requirements entails operator training, equipment calibration, documentation, design baselines etc., that are intangible and transparent for the product. In addition to factory certification, every device must be individually certified and qualified.

In summary, this program produces devices that are tested to operate over the military temperature range (-55°C to +125°C) and are meticulously processed per Mil. Method 5004. Finally, the 883 device manufacturing lots are subjected to Quality Conformance inspection per Mil. Method 5005 (Groups A, B, C, and D testing). Once a manufacturing lot has been processed through these two stringent methods, it is ready for sale as /883 compliant product.

HR PROGRAM

Prior to the inception of the 883 program, Maxim offered its products in an /HR (High Reliability) Flow. Maxim will continue to offer this highly successful processing program for customers requiring military grade product, but who do not want to pay the substantial cost added for certified product in full compliance to Mil-Std-883. The /HR program offers device processing which emulates Mil. Method 5004 processing, including full material traceability and process genealogy from Incoming Raw Materials through Final Shipment. However, full QCI testing will not be performed unless requested. Only Group A of Mil. Method 5005 will be done per lot. Groups B, C, and D must be specifically requested during order placement. This is done simply by placing a single letter suffix (B, C, or D) at the end of the ordered part number (see chart).

Ordered Part #	Processing
MAX358MJE/HR	Device will be processed through the full /HR Flow emulating Mil Method 5004 and QCI tested to Group A of Mil Method 5005.
MAX358MJE/HRB	Same as above with the addition of Mil Method 5005 Group B testing. QCI contains both Group A and B.
MAX358MJE/HRC	Same as above except now QCI includes Group C. QCI now contains Groups A, B, and C.
MAX358MJE/HRD	Same as above except now QCI includes Group D. QCI now contains Groups A, B, C, and D.

To order /883 or /HR devices, contact the Maxim sales representative or distributor in your area.

Maxim /HR Flow
Hybrid Components

- FULL MATERIAL TRACEABILITY AND PROCESS GENEALOGY
- DEVICE ASSEMBLY
- PRESEAL INTERNAL VISUAL
  MIL-STD-883, METHOD 2017, CLASS B 100%
- SEAL 100%
- STABILIZATION BAKE
  MIL-STD-883, METHOD 1008, CONDITION C 100%
- TEMPERATURE CYCLING
  MIL-STD-883, METHOD 1010, CONDITION C 100%
- CONSTANT ACCELERATION
  MIL-STD-883, METHOD 2001, CONDITION E (Y1 only 100%)*
- FINE LEAK TEST
  MIL-STD-883, METHOD 1014, CONDITION B 100%
- GROSS LEAK TEST
  MIL-STD-883, METHOD 1014, CONDITION C 100%
- 25°C ELECTRICAL TEST 100%
- BURN IN
  160 HOURS AT 125°C (OR EQUIVALENT) 100%
- ELECTRICAL TEST
  25°C, 125°C, -55°C 100%
- QA ACCEPTANCE PER APPLICABLE DEVICE SPECIFICATION
  MIL-STD-883, METHOD 5005, GROUP A
- LOT QUALIFICATION
  MIL-STD-883, METHOD 5008, GROUP B, C & D
  (OPTIONAL FOR /HR PROGRAM)
- EXTERNAL VISUAL
  MIL-STD-883, METHOD 2009 100%
- BOX STOCK

* If seal perimeter is greater than 2.0 inches, Condition A applies.

Maxim /883 /HR Flow
Monolithic ICs

- FULL MATERIAL TRACEABILITY AND PROCESS GENEALOGY
- WAFER FABRICATION AND DEVICE ASSEMBLY
- PRESEAL INTERNAL VISUAL
  MIL-STD-883, METHOD 2010, CLASS B 100%
- SEAL 100%
- STABILIZATION BAKE
  MIL-STD-883, METHOD 1008, CONDITION C 100%
- TEMPERATURE CYCLING
  MIL-STD-883, METHOD 1010, CONDITION C 100%
- CONSTANT ACCELERATION
  MIL-STD-883, METHOD 2001, CONDITION E (Y1 only 100%)
- FINE LEAK TEST
  MIL-STD-883, METHOD 1014, CONDITION B 100%
- GROSS LEAK TEST
  MIL-STD-883, METHOD 1014, CONDITION C 100%
- 25°C ELECTRICAL TEST 100%
- BURN IN
  160 HOURS AT 125°C (OR EQUIVALENT) 100%
- ELECTRICAL TEST
  25°C, 125°C, -55°C 100%
- QA ACCEPTANCE PER APPLICABLE DEVICE SPECIFICATION
  MIL-STD-883, METHOD 5005, GROUP A
- LOT QUALIFICATION
  MIL-STD-883, METHOD 5005, GROUP B, C & D
  (OPTIONAL FOR /HR PROGRAM)
- EXTERNAL VISUAL
  MIL-STD-883, METHOD 2009 100%
- BOX STOCK

Proprietary and Second Source Numbering System

Maxim's Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped by their functions into certain categories. Maxim presently uses a "MAX" as the prefix to the device's unique number. The categories are as follows:

MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op-Amps, Buffers and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power Supply Circuits and Voltage References
MAX700-799	μP Peripherals and Display Drivers
MAX800-899	Open
MAX900-999	Open

Within each category, blocks of numbers are reserved for sub-groups.

3 Letter Suffixes

EXAMPLE: MAX358CPD

- C — Operating Temperature
- P — Package Designator
- D — Lead Count

Temperature Range

"C"	0°C to +70°C
"I"	-20°C to +85°C
"E"	-40°C to +85°C
"M"	-55°C to +125°C

Package

"A"	TO-237
"C"	TO-220
"D"	Ceramic Sidebraze
"F"	Ceramic Flat-Pack
"H"	TO-66
"J"	CERDIP Dual-In-Line
"K"	TO-3
"L"	Leadless, Ceramic
"M"	Plastic Flat Pack
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	Plastic Chip Carrier (Quad Pak)
"R"	Narrow CERDIP
"S"	Small Outline, Slim (8 or more leads), 150 mil
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-78, TO-99, TO-100)
"U"	TO-72 Type (also TO-18, TO-71)
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"Z"	TO-92
"/D"	Dice
"/W"	Wafer
"-1"	On Package Information Indicates Hybrid Circuit

Number of Pins

"A"	8	"P"	20
"B"	10	"Q"	2
"C"	12	"R"	3
"D"	14	"S"	4
"E"	16	"T"	6
"F"	22	"U"	60
"G"	24	"V"	8 (0.200" pin circle, isolated case)
"H"	44		
"I"	28	"W"	10 (0.230" pin circle, isolated case)
"J"	32		
"K"	35	"Y"	8 (0.200" pin circle, case to pin 4)
"L"	40		
"M"	48	"Z"	10 (0.230" pin circle, case to pin 5)
"N"	18		

4 Letter Suffixes

The first letter of the suffix is used to denote product grade, for example, MAX631ACPA means 5% output accuracy (A), the remaining 3 letters denote temperature range, package type and number of leads. Therefore, the MAX631ACPA operates over the 0°C to +70°C and is in a Plastic Dual-in-Line package and has 8 leads.

Second Source Products

In most cases, Maxim's part number for a multiple source product follows the numbering system that is most widely accepted in the industry for that particular part, rather than our own convention. This includes original designators for package type, temperature range, and performance grades as well as the most commonly recognized prefix.

Multiple source products are frequently supplied by Maxim in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, such a device is given the part number that it would have if the original numbering convention were followed. For example, if a military temperature grade of a product is not supplied by other sources but is available from Maxim, the original manufacturer's designation for military temperature will be used. As a result, a specific part number supplied by Maxim may not be listed by the "original" manufacturer.

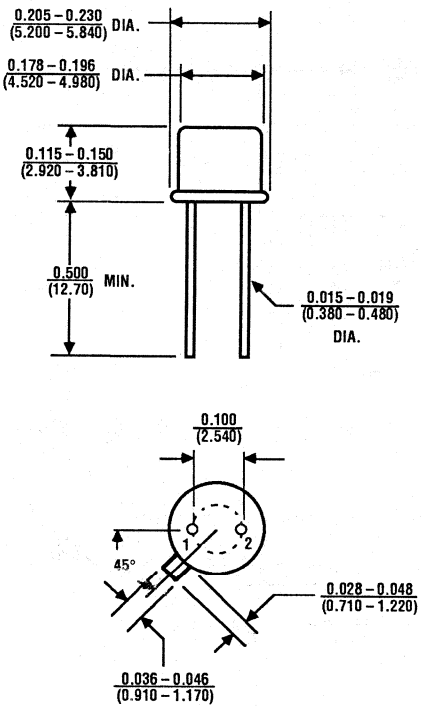
Package Information

This section contains physical dimensions and thermal data for all packages currently supplied by Maxim. Each drawing is followed by a two letter code which indicates package type (Plastic DIP, Small Outline, etc.) and number of leads. This code is also used, along with indicators for temperature range and device grade (where appropriate) in the part number suffix for each of Maxim's proprietary devices.

Alpha-Numeric Index

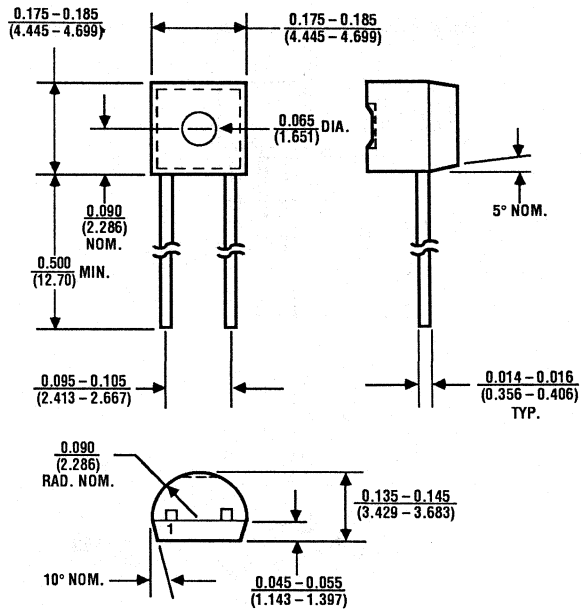
A

Alpha-Numeric Index



TO-52 Metal Can – 2 Lead (SQ)

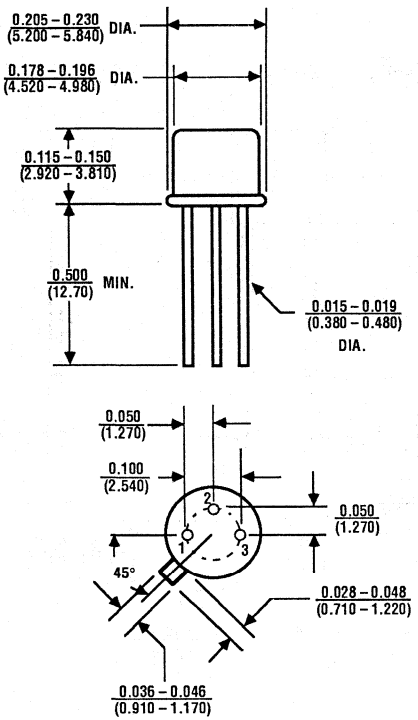
θ_{JA} = 220°C/W
θ_{JC} = 60°C/W



TO-92 Plastic – 2 Lead (ZQ)

θ_{JA} = 200°C/W
θ_{JC} = 70°C/W

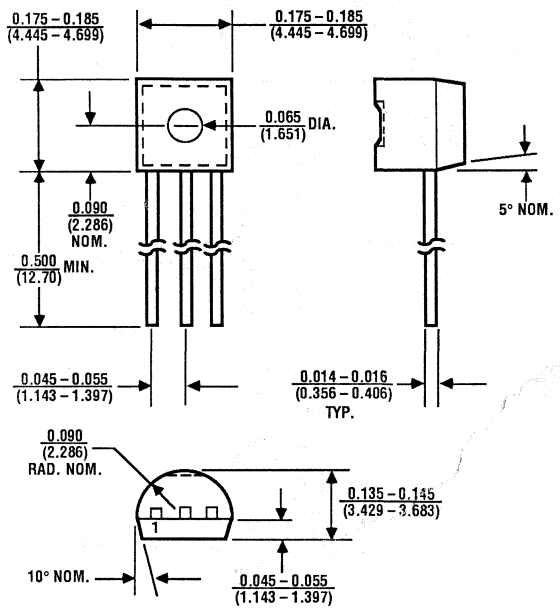
A



TO-52 Metal Can – 3 Lead (SR)

θ_{JA} = 220°C/W

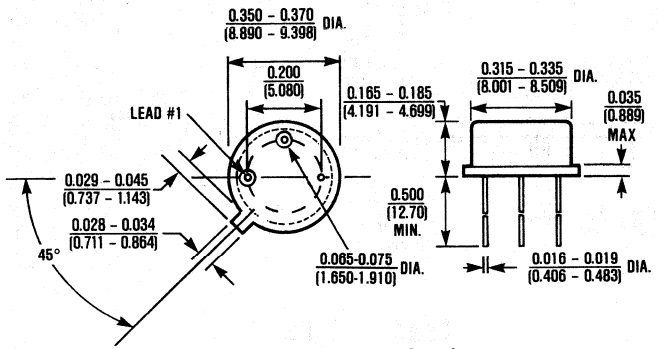
θ_{JC} = 60°C/W



TO-92 Plastic – 3 Lead (ZR)

θ_{JA} = 200°C/W

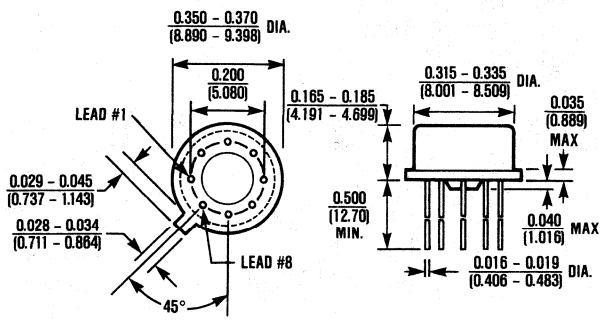
θ_{JC} = 70°C/W



3 Lead TO-39 (VR)

θ_{JA} = 150°C/W

θ_{JC} = 15°C/W

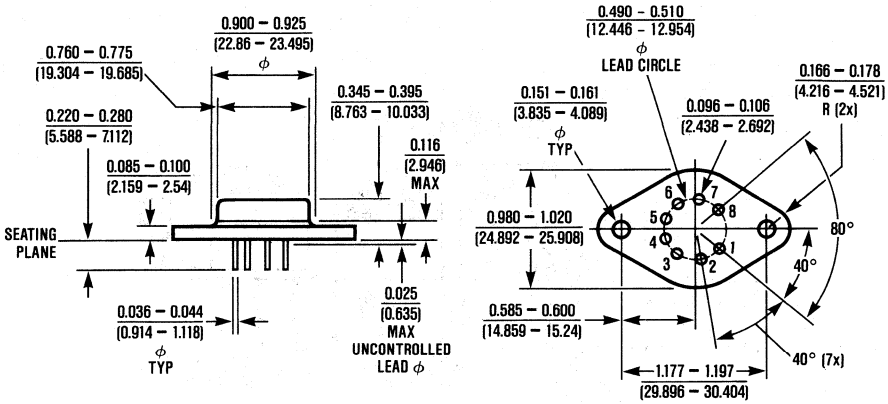


8 Lead TO-99 (TV)

θ_{JA} = 150°C/W

θ_{JC} = 45°C/W

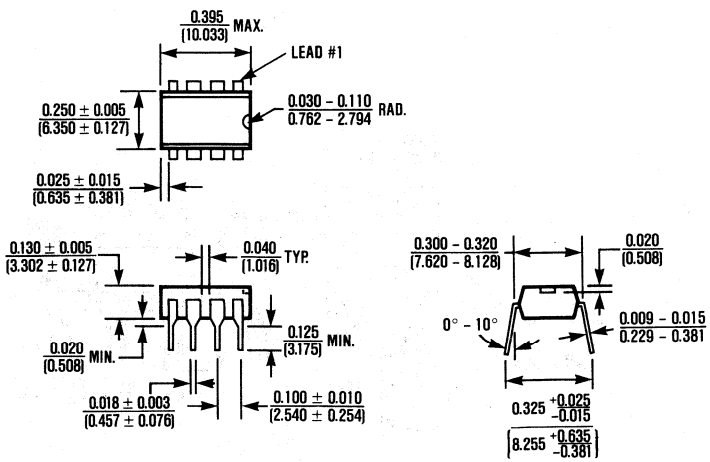
A



8 Lead TO-3 Can (KA)

θ_{JA} = 25°C/W

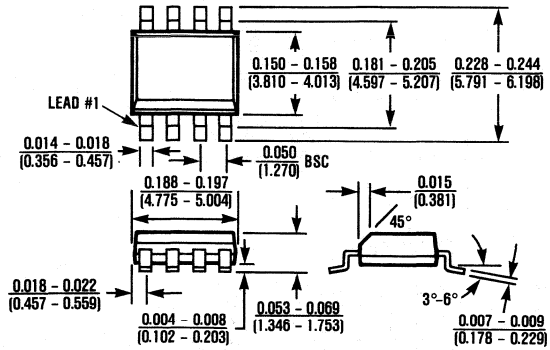
θ_{JC} = 2°C/W



8 Lead Plastic DIP (PA)

θ_{JA} = 120°C/W

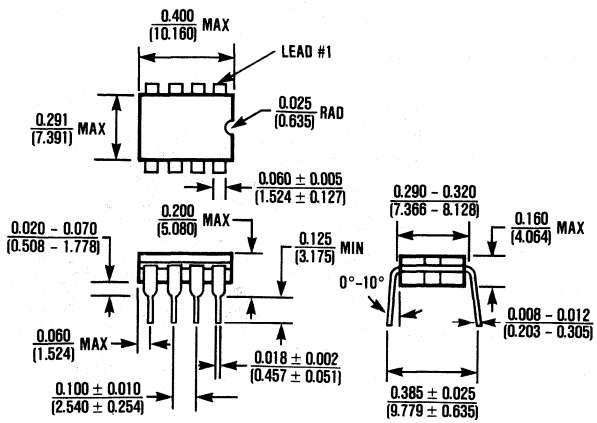
θ_{JC} = 70°C/W



8 Lead Small Outline (SA)

θ_{JA} = 170°C/W

θ_{JC} = 80°C/W

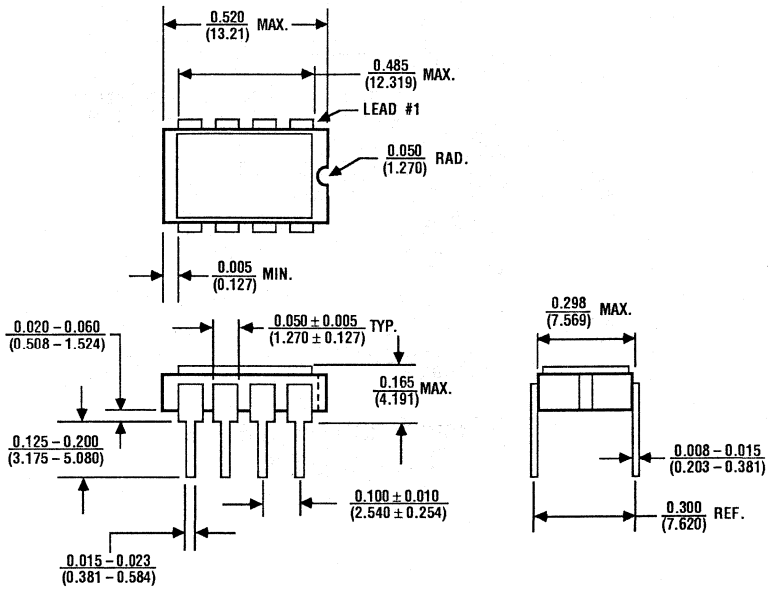


8 Lead CERDIP (JA)

θ_{JA} = 125°C/W

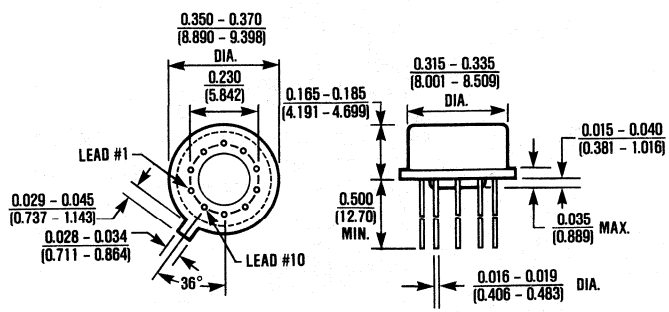
θ_{JC} = 55°C/W

A



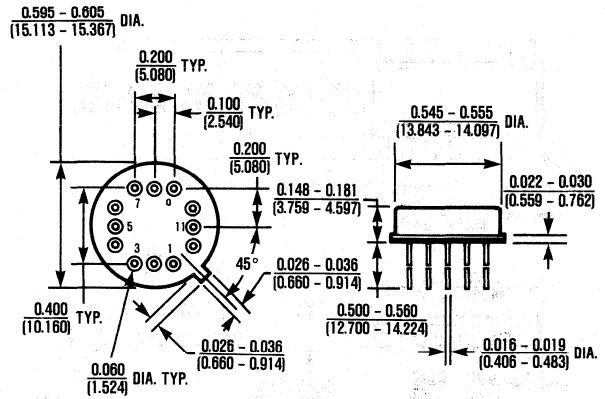
8 Lead Ceramic Sidebraze (DA)

θ_{JA} = 120°C/W
θ_{JC} = 50°C/W



10 Lead TO-100 Can (TW)

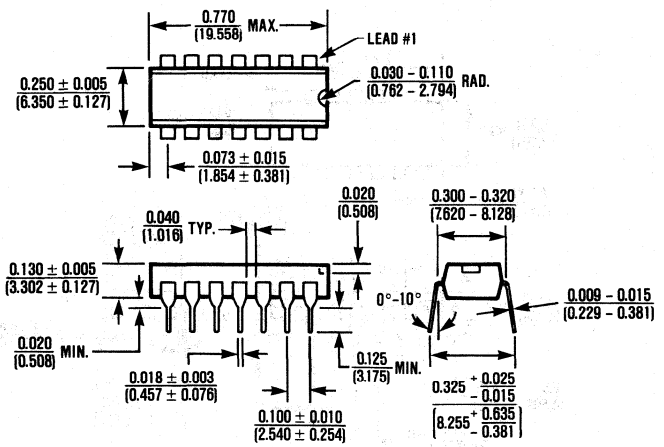
θ_{JA} = 150°C/W
θ_{JC} = 45°C/W



12 Lead TO-8 Can (G)

θ_{JA} = 100°C/W

θ_{JC} = 60°C/W

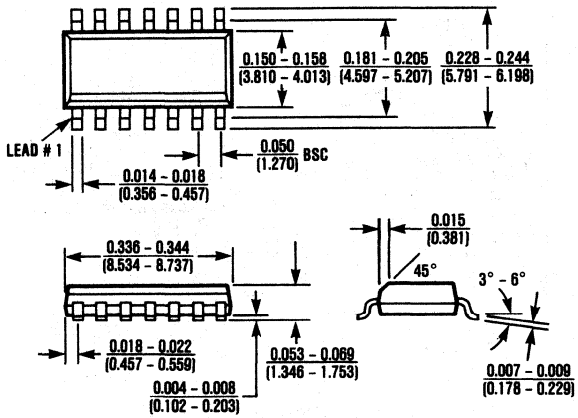


14 Lead Plastic DIP (PD)

θ_{JA} = 140°C/W

θ_{JC} = 70°C/W

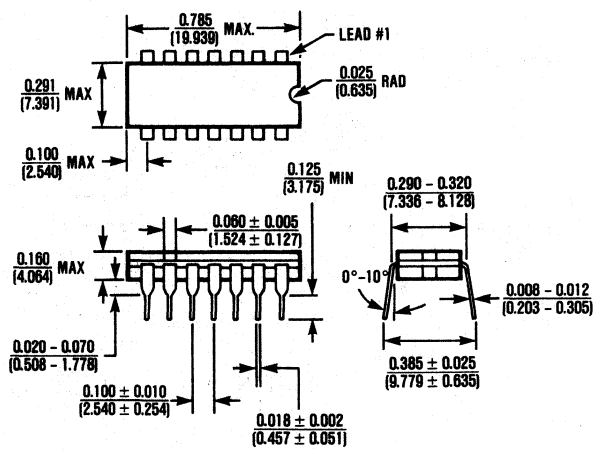
A



14 Lead Small Outline (SD)

θ_{JA} = 115°C/W

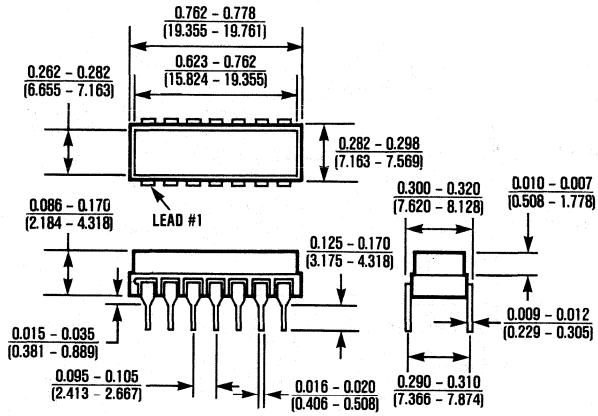
θ_{JC} = 60°C/W



14 Lead CERDIP (JD)

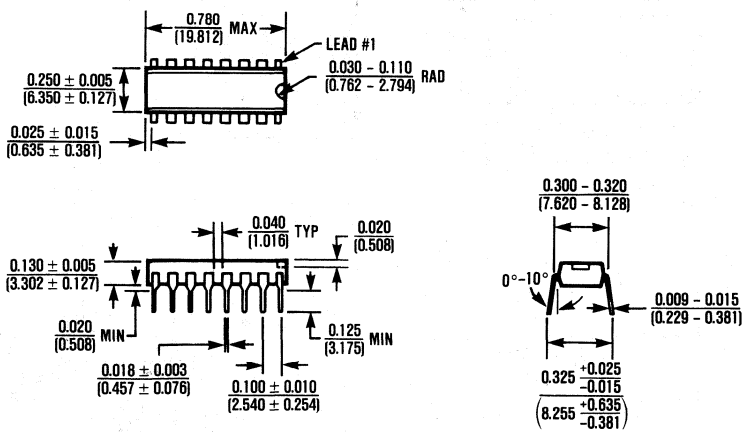
θ_{JA} = 105°C/W

θ_{JC} = 50°C/W



14 Lead Ceramic Sidebraze (DD) -1

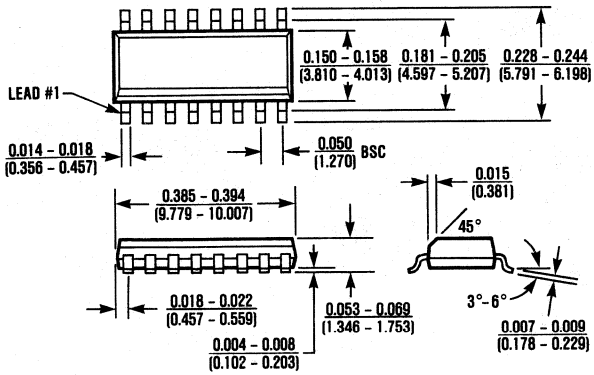
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W



16 Lead Plastic DIP (PE)

θ_{JA} = 135°C/W
θ_{JC} = 65°C/W

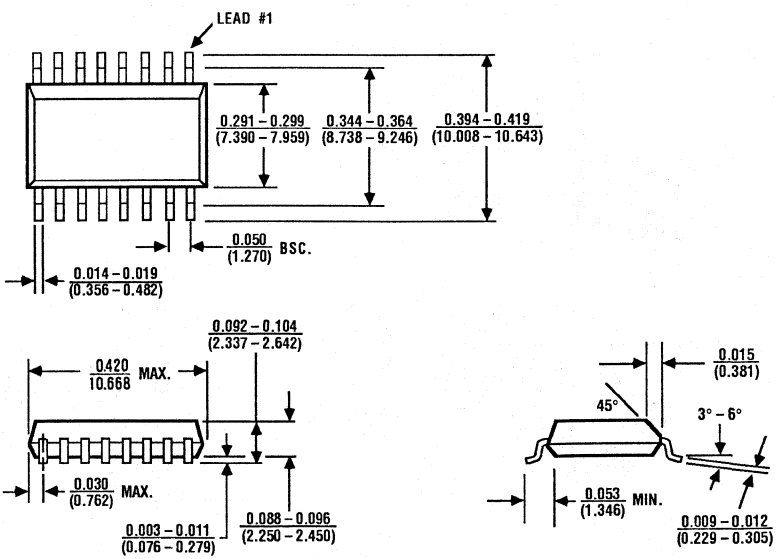
A



16 Lead Small Outline (SE)

θ_{JA} = 110°C/W

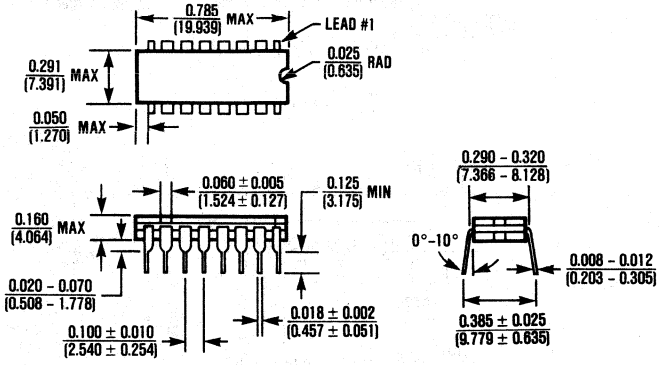
θ_{JC} = 60°C/W



16 Lead Small Outline, Wide (WE)

θ_{JA} = 105°C/W

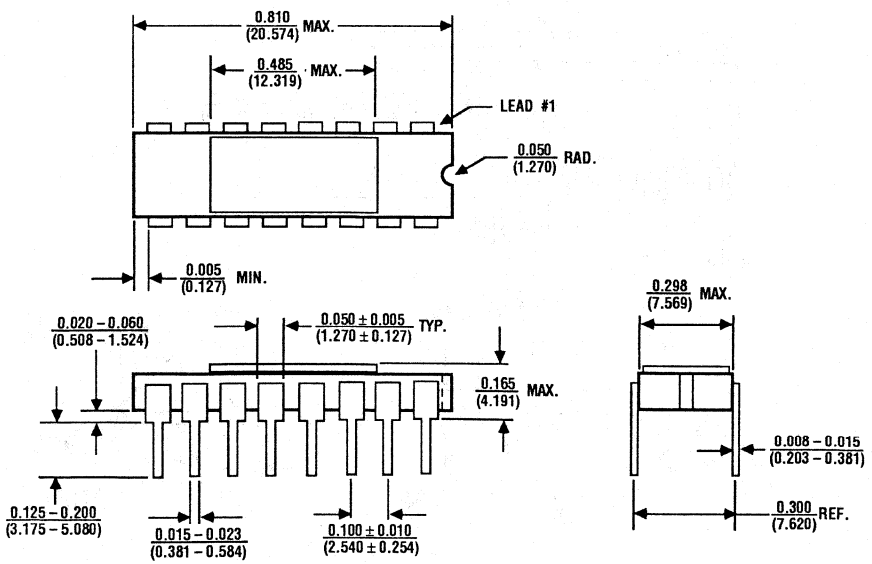
θ_{JC} = 60° C/W



16 Lead CERDIP (JE)

θ_{JA} = 100°C/W

θ_{JC} = 50°C/W

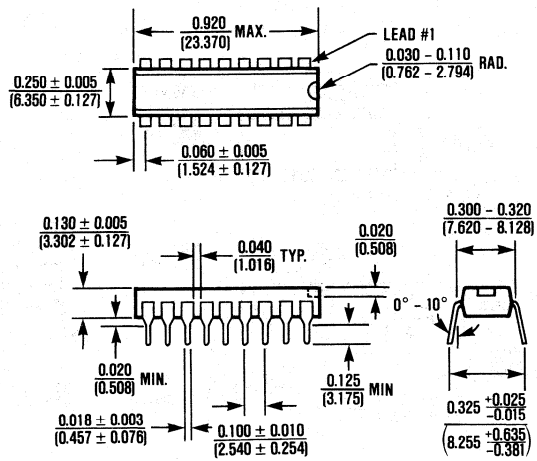


16 Lead Ceramic Sidebraze (DE)

θ_{JA} = 95°C/W

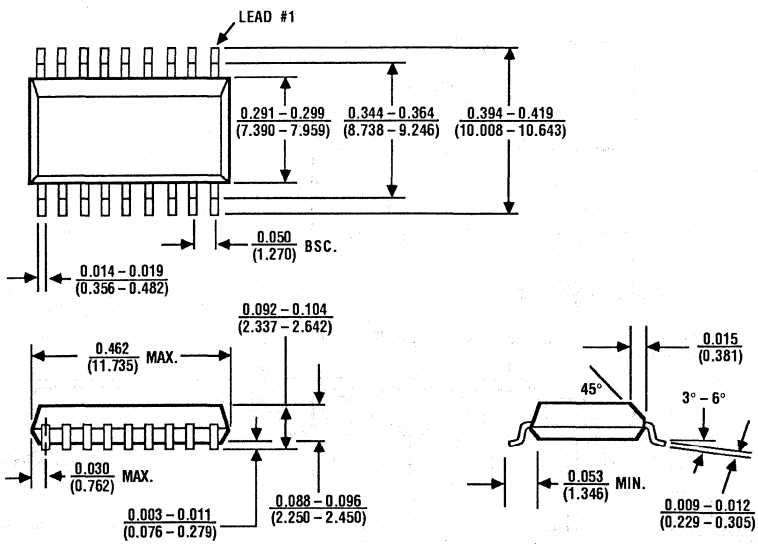
θ_{JC} = 45°C/W

A



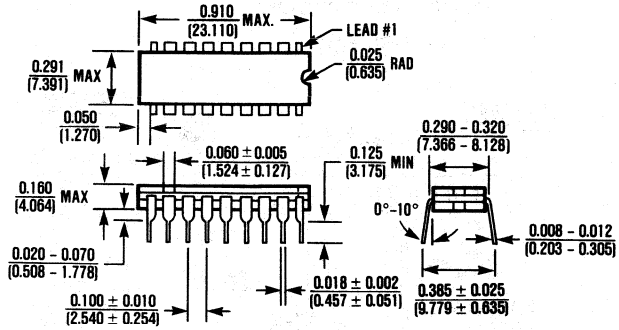
18 Lead Plastic DIP (PN)

θ_{JA} = 130°C/W
θ_{JC} = 60°C/W



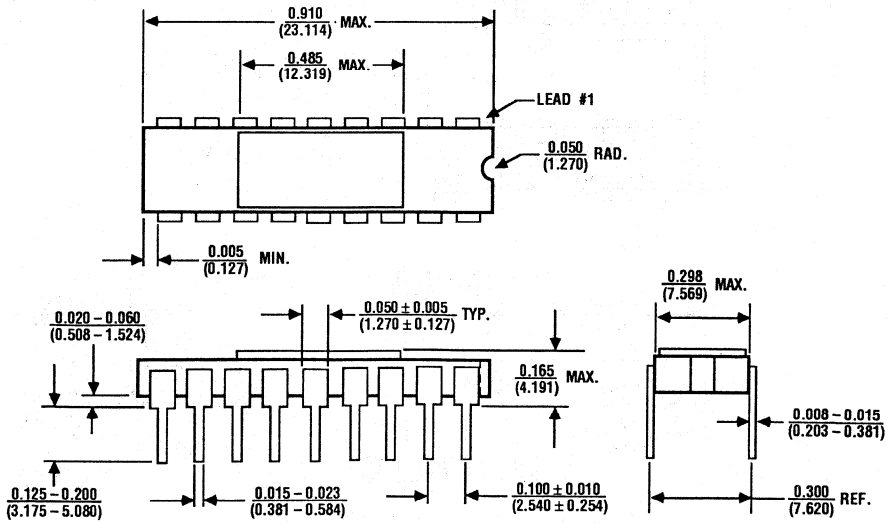
18 Lead Small Outline, Wide (WN)

θ_{JA} = 105°C/W
θ_{JC} = 60° C/W



18 Lead CERDIP (JN)

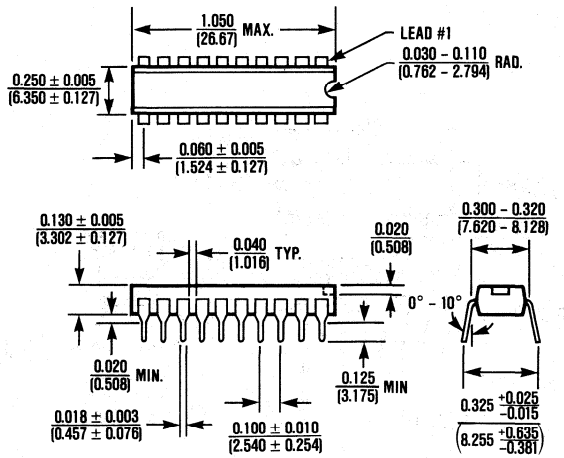
θ_{JA} = 90°C/W
θ_{JC} = 45°C/W



18 Lead Ceramic Sidebraze (DN)

θ_{JA} = 90°C/W
θ_{JC} = 40°C/W

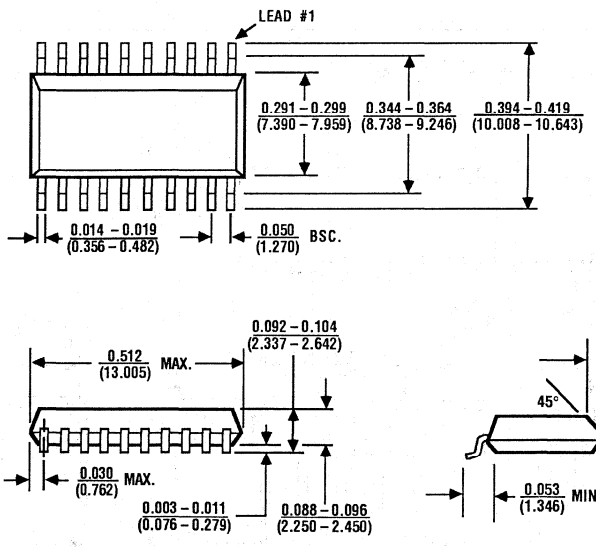
A



20 Lead Plastic DIP (PP)

θ_{JA} = 125°C/W

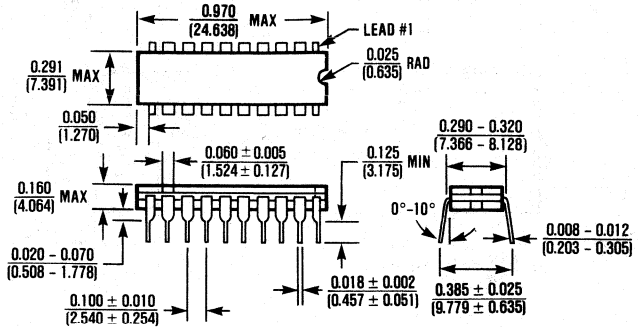
θ_{JC} = 60°C/W



20 Lead Small Outline, Wide (WP)

θ_{JA} = 100°C/W

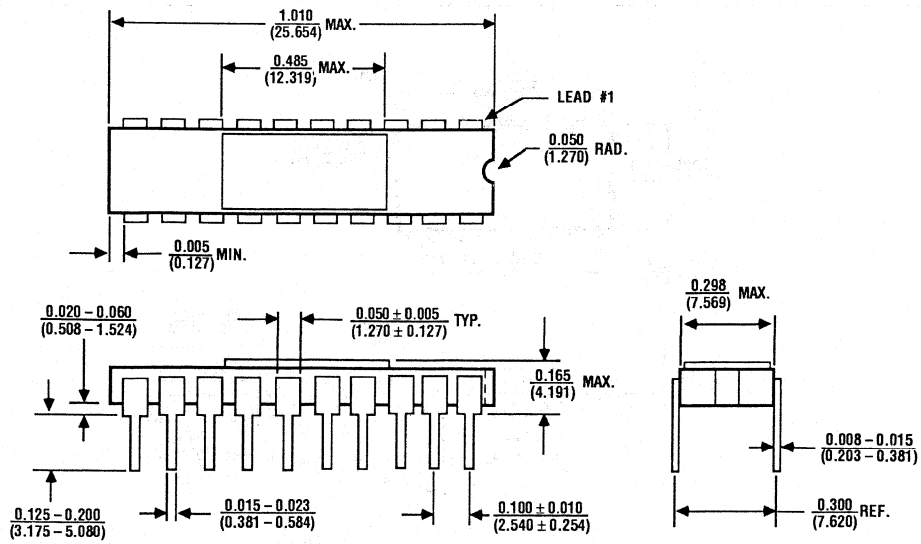
θ_{JC} = 50° C/W



20 Lead CERDIP (JP)

θ_{JA} = 90°C/W

θ_{JC} = 40°C/W

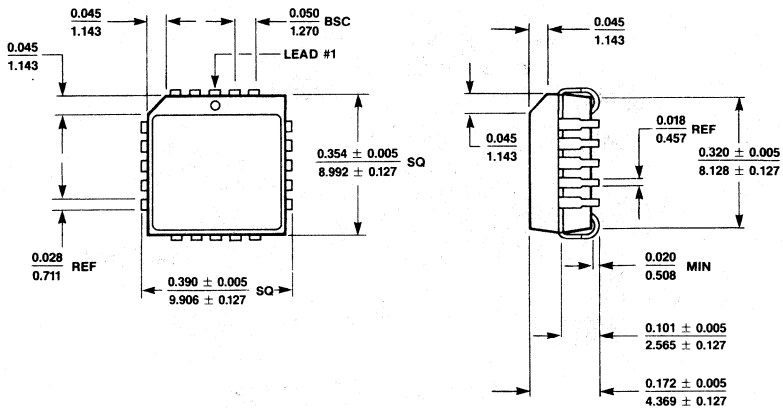


20 Lead Ceramic Sidebraze (DP)

θ_{JA} = 85°C/W

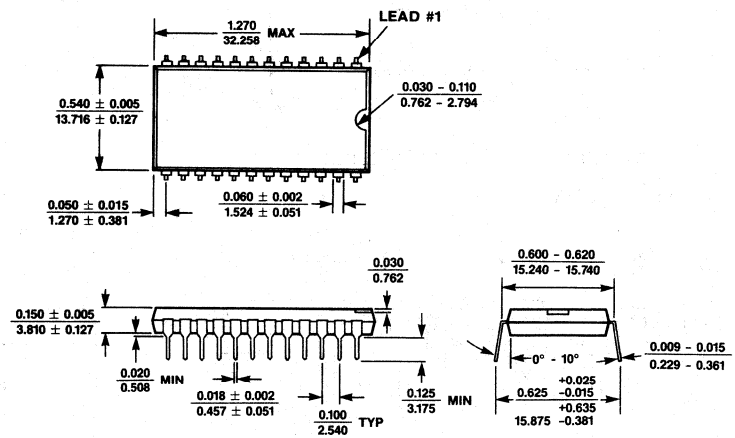
θ_{JC} = 35°C/W

A



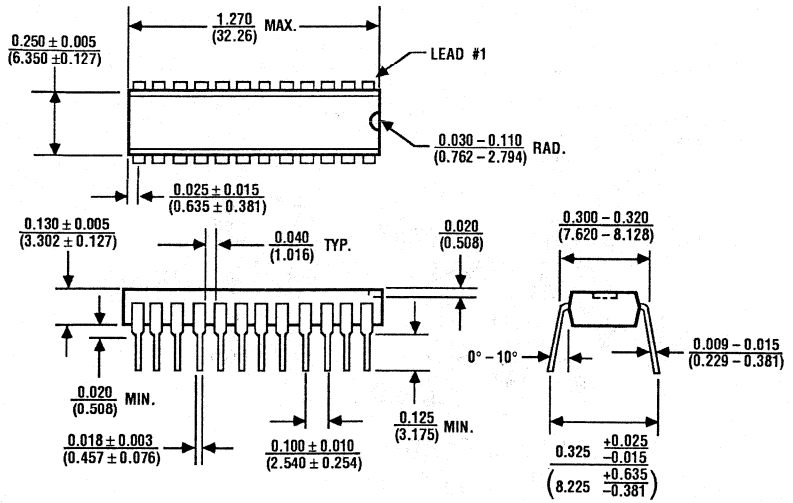
20 Lead Plastic Chip Carrier (Quad Pak) (QP)

θ_{JA} = 110°C/W
θ_{JC} = 50°C/W



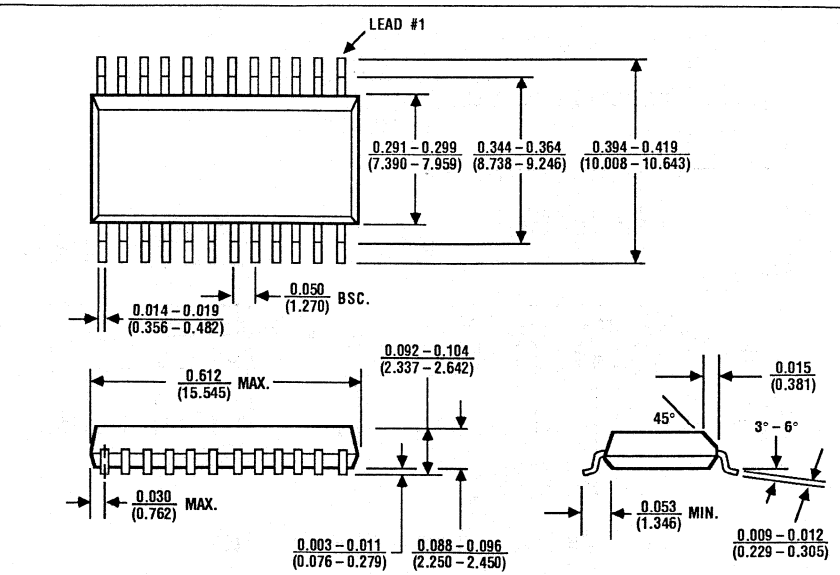
24 Lead Plastic DIP (PG)

θ_{JA} = 110°C/W
θ_{JC} = 50°C/W



24 Lead Plastic Narrow DIP (NG)

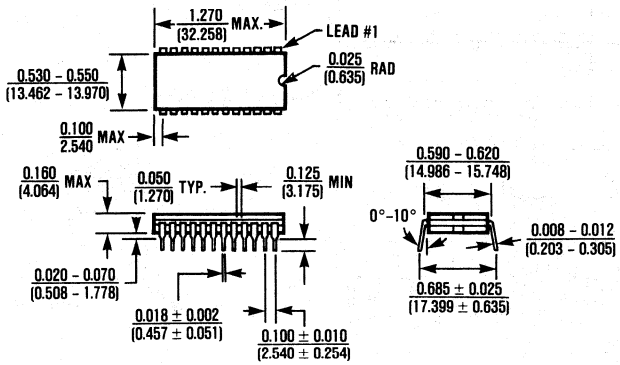
θ_{JA} = 120°C/W
θ_{JC} = 60°C/W



24 Lead Small Outline, Wide (WG)

θ_{JA} = 85°C/W
θ_{JC} = 45° C/W

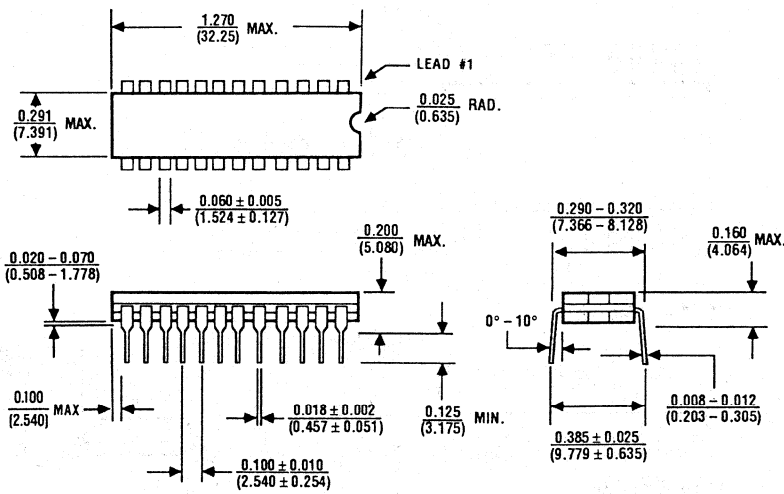
A



24 Lead CERDIP (JG)

θ_{JA} = 55°C/W

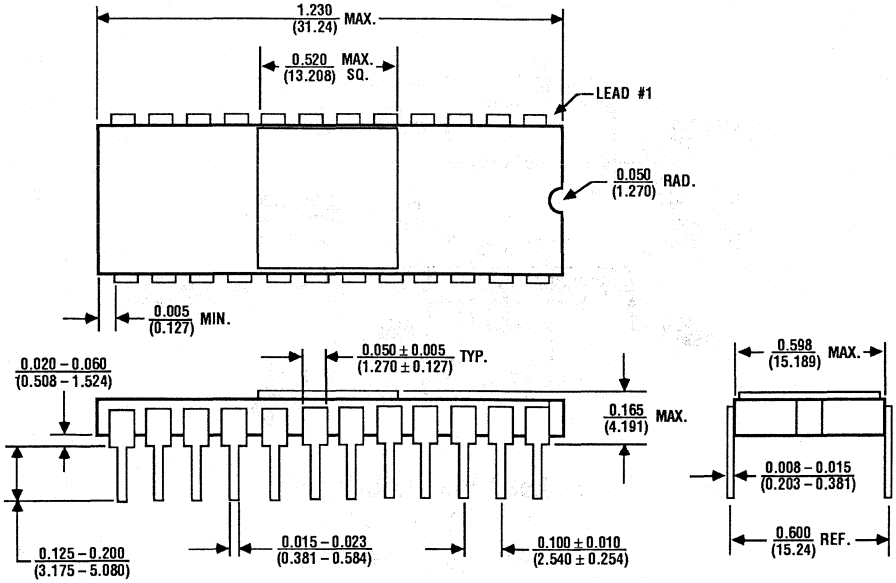
θ_{JC} = 20°C/W



24 Lead Narrow CERDIP (RG)

θ_{JA} = 80°C/W

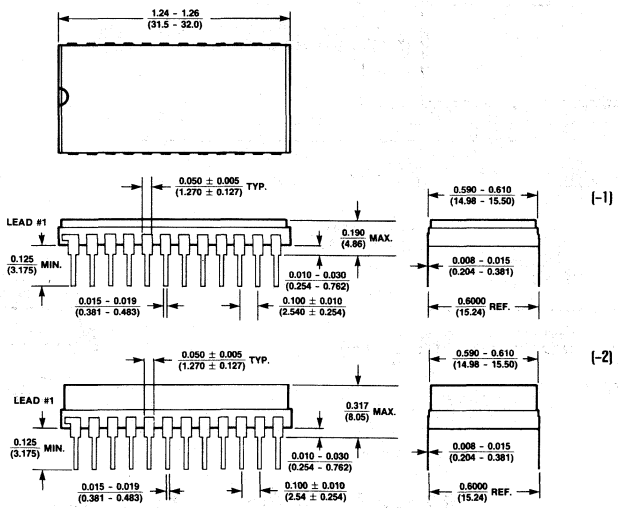
θ_{JC} = 40°C/W



24 Lead Ceramic Sidebraze (DG)

θ_{JA} = 50°C/W

θ_{JC} = 15°C/W

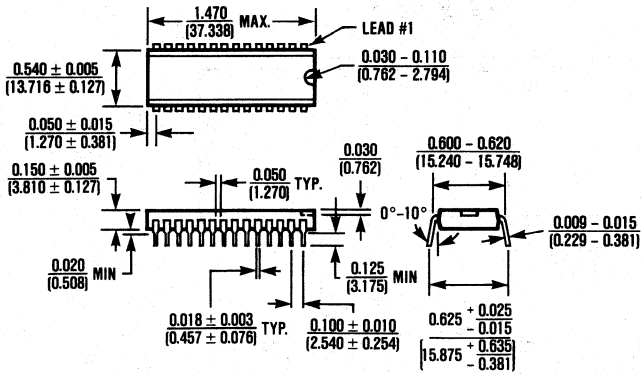


24 Lead Ceramic Sidebraze (DG) -1,-2

θ_{JA} = 50°C/W

θ_{JA} = 15°C/W

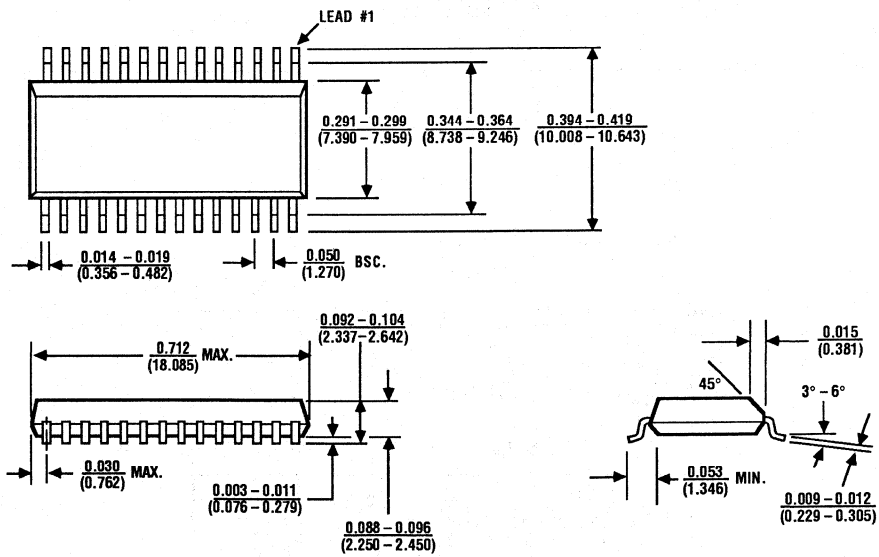
A



28 Lead Plastic DIP (PI)

θ_{JA} = 110°C/W

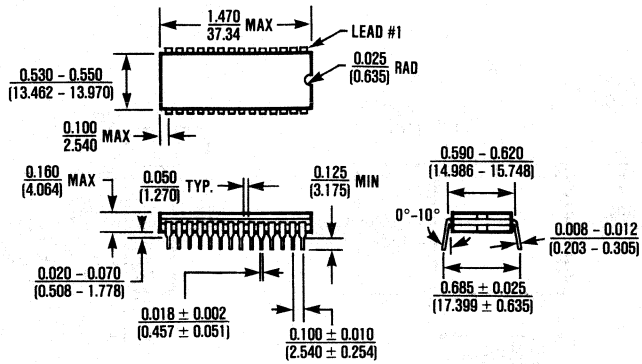
θ_{JC} = 50°C/W



28 Lead Small Outline, Wide (WI)

θ_{JA} = 80°C/W

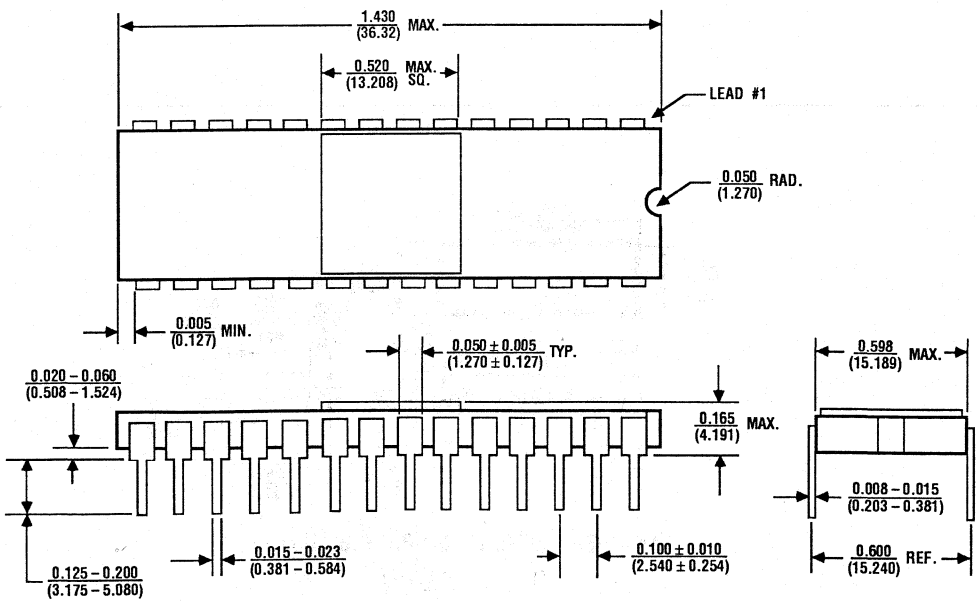
θ_{JC} = 45°C/W



28 Lead CERDIP (JI)

θ_{JA} = 55°C/W

θ_{JC} = 20°C/W

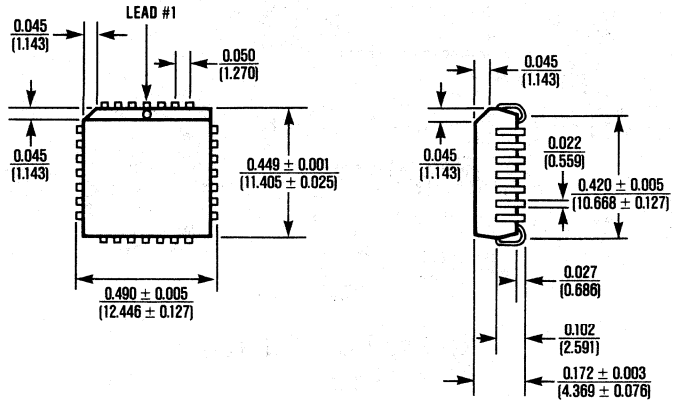


28 Lead Ceramic Sidebraze (DI)

θ_{JA} = 50°C/W

θ_{JC} = 15°C/W

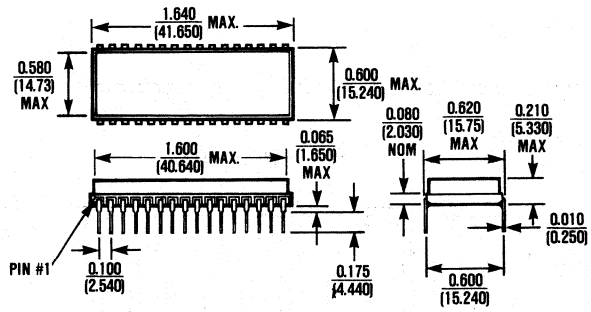
A



28 Lead Plastic Chip Carrier (Quad Pak) (QI)

θ_{JA} = 100°C/W

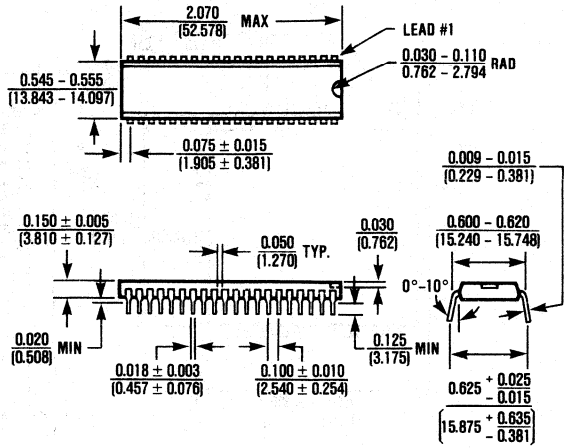
θ_{JC} = 45°C/W



32 Lead Ceramic Sidebraze (DJ) -1

θ_{JA} = 48°C/W

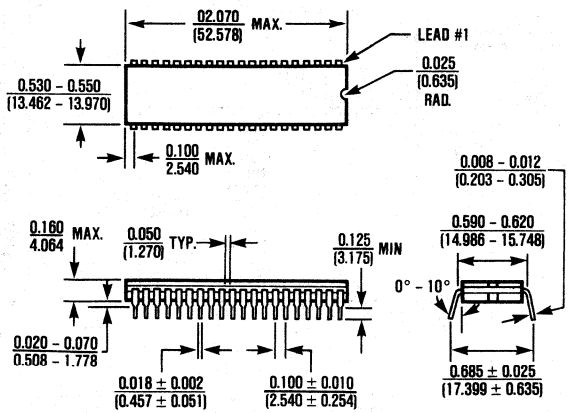
θ_{JC} = 18°C/W



40 Lead Plastic DIP (PL)

θ_{JA} = 100°C/W

θ_{JC} = 45°C/W

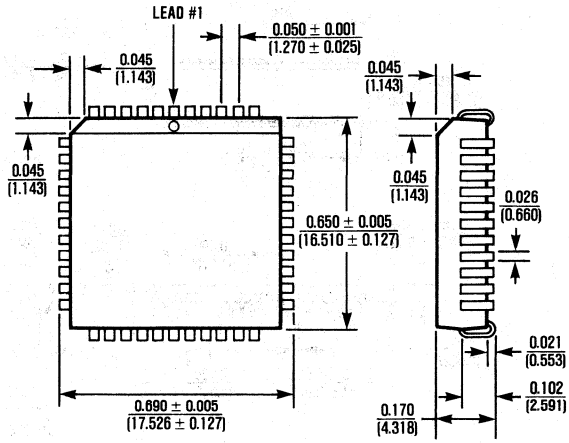


40 Lead CERDIP (JL)

θ_{JA} = 45°C/W

θ_{JC} = 20°C/W

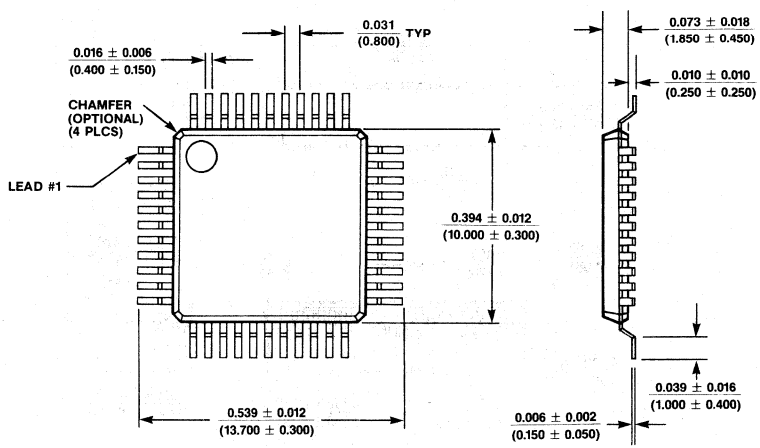
A



44 Lead Plastic Chip Carrier (Quad Pak) (QH)

θ_{JA} = 80°C/W

θ_{JC} = 40°C/W



44 Lead Plastic Flat Pack (MH)

θ_{JA} = 170°C/W

θ_{JC} = 70°C/W

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Portland, OR 97225
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FAX: (503) 292-8827

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FAX: (312) 577-0325

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4470 N. College Avenue
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FAX: (913) 339-9449

Dy-Tronix
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Wichita, KS 67203
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Telex: 629-14-257
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Telex: 510-600-9460
FAX: (301) 644-5707

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FAX: (617) 449-7407

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Telex: 224-120
FAX: (313) 968-3239

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Minneapolis, MN 55435
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Bridgeton, MO 63044
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FAX: (513) 278-3609

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Richfield, OH 44286
Tel: (216) 659-9224
Telex: 810-427-9103
FAX: (216) 659-9227

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Westerville, OH 43081
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1143 Rockingham
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Richardson, TX 75080
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FAX: (214) 231-7662

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400 E. Anderson Lane
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Tel: (205) 837-8700
FAX: (205) 830-2565

Pioneer
4825 University Square
Suite 1
Huntsville, AL 35816
Tel: (205) 837-9300
Telex: 810-726-2197
FAX: (205) 837-9358

Arizona

Anthem
1727 East Weber Drive
Tempe, AZ 85281
Tel: (602) 966-6600
FAX: (602) 966-4826

Bell Industries
140 S. Lindon Lane
Tempe, AZ 85281
Tel: (602) 966-7800
Telex: 910-950-0133
FAX: (602) 967-6584

Hall-Mark Electronics
4637 S. 36th Place
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Tel: (602) 437-1200
Telex: 910-950-0191
FAX: (602) 437-2348

California

Anthem
1040 East Brokaw Road
San Jose, CA 95131
Tel: (408) 295-4200
FAX: (408) 282-1542

Anthem
1 Oldfield
Irvine, CA 92718-2809
Tel: (714) 768-4444
FAX: (714) 380-4747

Anthem
9369 Carroll Park Drive
San Diego, CA 92121
Tel: (619) 453-9005
FAX: (619) 546-7893

Anthem
20640 Bahama Street
Chatsworth, CA 91311
Tel: (818) 700-1000
FAX: (818) 709-7639

Anthem
580 Menlo Drive
Suite 8
Rocklin, CA 95677
Tel: (916) 624-9744
FAX: (916) 624-9750

Bell Industries
11095 Knott Avenue
Suite E
Cyprus, CA 90630
Tel: (714) 895-7801
Telex: 910-596-2362
FAX: (714) 891-4570

California (continued)

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306 East Alondra Blvd.
Gardena, CA 90247
Tel: (213) 515-1800
Telex: 910-346-6336
FAX: (213) 777-3111
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11812 San Vicente Blvd.
Los Angeles, CA 90049
Tel: (213) 826-6778
FAX: (213) 258-6932

Bell Industries
7450 Ronson Road
San Diego, CA 92111
Tel: (619) 268-1277
FAX: (619) 268-3733

Bell Industries
1829A DeHavilland Drive
Thousand Oaks, CA 91320
Tel: (805) 499-6821
Telex: 910-321-3799
FAX: (805) 499-6810

Bell Industries
4311 Anthony Court
Suite 100
Rocklin, CA 95677
Tel: (916) 652-0414
FAX: (916) 652-0403

Bell Industries
1161 North Fairoaks Avenue
Sunnyvale, CA 94089
Tel: (408) 734-8570
Telex: 910-339-9378
FAX: (408) 734-8875

Hall-Mark Electronics
3878 Ruffin Road
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San Diego, CA 92123
Tel: (619) 268-1201
Telex: 910-335-1279
FAX: (619) 268-0209

Hall-Mark Electronics
9420 Topanaga Canyon Blvd.
Chatsworth, CA 91331
Tel: (213) 217-8400
FAX: (213) 773-4555

Hall-Mark Electronics
14831 Franklin Avenue
Tustin, CA 92680
Tel: (714) 669-4100
FAX: (714) 730-0543

Hall-Mark Electronics
580 Menlo Drive
Suite 2
Rocklin, CA 95677
Tel: (916) 624-9781
FAX: (916) 961-0922

Hall-Mark Electronics
1110 Ringwood Court
San Jose, CA 95131
Tel: (408) 432-0900
FAX: (408) 433-0745

Colorado

Anthem
373 Inverness Drive South
Englewood, CO 80112
Tel: (303) 790-4500
FAX: (303) 790-4532

Bell Industries
12421 West 49th Avenue
Wheat Ridge, CO 80033
Tel: (303) 424-1985
Telex: 910-938-0393
FAX: (303) 424-0932

Hall-Mark Electronics
12503 E. Euclid Drive
Suite 20
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Tel: (303) 790-1662
FAX: (303) 790-4991

Connecticut

Lionex/Anthem
170 Research Parkway
Meriden, CT 06450
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FAX: (203) 237-6026

Hall-Mark Electronics
691 Business Park
Bldg. #3
615 West Johnson Avenue
Cheshire, CT 06410
Tel: (203) 271-2844
FAX: (203) 272-1704

Pioneer
112 Main Street
Norwalk, CT 06851
Tel: (203) 853-1515
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Florida

Bell Industries
600 South-North Lake Blvd.
Suite 100
Altamonte Springs, FL 32701
Tel: (407) 339-0078
FAX: (407) 339-0139

Bell Industries
638 S. Military Trail
Deerfield Beach, FL 33442
Tel: (305) 421-1997
FAX: (305) 421-5705

Bell Industries
10810 72nd Street N.
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FAX: (813) 546-6418

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15301 Roosevelt Blvd.
Suite 303
Clearwater, FL 34620
Tel: (813) 530-4543
FAX: (813) 530-3865

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7648 Southland Blvd., #100
Orlando, FL 32809
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FAX: (305) 855-4020
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Hall-Mark Electronics
3161 S.W. 15th Street
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337 South-North Lake Blvd.
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Altamonte Springs, FL 32701
Tel: (305) 834-9090
Telex: 810-853-0284
FAX: (305) 834-0865

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Tel: (813) 536-0445
FAX: (813) 531-5037

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Deerfield Beach, FL 33441
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Telex: 510-955-9653
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3020 A Business Park Drive
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Hall-Mark Electronics
6410 Atlantic Blvd.
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FAX: (404) 448-9654

Pioneer
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180 Crossen Avenue
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Bell Industries
515 Busse Road
Elk Grove Village, IL 60007
Tel: (312) 640-1910
Telex: 910-223-4519
FAX: (312) 640-0474

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730 W. Killarney
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Hall-Mark Electronics
210 Mittel Drive
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Pioneer
2171 Executive Drive
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Fort Wayne, IN 46801
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Bell Industries
5230 West 79th Street
Indianapolis, IN 46268
Tel: (317) 875-8200
FAX: (317) 875-8219

Hall-Mark Electronics
4275 W. 96th Street
Indianapolis, IN 46268
Tel: (317) 872-8875
FAX: (317) 876-7165

Pioneer
6408 Castleplace Drive
Indianapolis, IN 46278
Tel: (317) 849-7300
Telex: 810-260-1794
FAX: (317) 842-5998

Iowa
Bell Industries
1221 Park Place N.E.
Cedar Rapids, IA 52402
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Telex: 751-093
FAX: (319) 395-9761

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FAX: (913) 888-0523

Pioneer
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Lenexa, KS 66215
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Hall-Mark Electronics
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Columbia, MD 21046
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FAX: (301) 381-2036

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9100 Gaither Road
Gaitherburg, MD 20877
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FAX: (301) 921-4255

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FAX: (508) 657-6387

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Pinehurst Park
Billerica, MA 01821
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Lexington, MA 02173
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814 Phoenix Drive
Ann Arbor, MI 48104
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Grand Rapids, MI 49508
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Telex: 510-600-8456
FAX: (616) 698-1831

Pioneer
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Livonia, MI 48150
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Telex: 810-242-3271
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FAX: (612) 941-5778

Pioneer
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Earth City, MO 63045
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311 Route 46 West
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FAX: (201) 227-9246

Hall-Mark Electronics
107 Fairfield Road
Suite 1B
Fairfield, NJ 07006
Tel: (201) 575-4415
FAX: (201) 882-9398

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Hall-Mark Electronics
11000 Midlantic Drive
Mt. Laurel, NJ 08054
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Pine Brook, NJ 07058
Tel: (201) 882-8300
FAX: (201) 882-8398

Pioneer
45 Route #46
Pine Brook, NJ 07058
Tel: (201) 575-3510
Telex: 710-734-4382
FAX: (201) 575-3454

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Bell Industries
11728 Linn N. E.
Albuquerque, NM 87123
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Telex: 910-989-0625
FAX: (505) 275-2819

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Hauppauge, NY 11788
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FAX: (516) 273-1823

Hall-Mark Electronics
101 Comac Street
Ronkonkoma, NY 11779
Tel: (516) 737-0600
FAX: (516) 737-0838

Nu Horizons
6000 New Horizons Blvd.
Amityville, NY 11701
Tel: (516) 226-6000
FAX: (516) 226-6140

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E. Rochester, NY 14445
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Fairport, NY 14450
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Telex: 510-253-7001
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68 Corporate Drive
Binghamton, NY 13904
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Telex: 510-252-0893
FAX: (607) 722-9562

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60 Crossways Park West
Woodbury, NY 11797
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Telex: 510-221-2184
FAX: (516) 921-2143

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Raleigh, NC 27604
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FAX: (919) 878-8729

Pioneer
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Charlotte, NC 28217
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Telex: 810-621-0366
FAX: (704) 522-8564

Pioneer
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Suite 148
Durham, NC 27713
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FAX: (919) 544-5885

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Bell Industries
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Dayton, OH 45459
Tel: (513) 434-8231
FAX: (513) 434-8103

Bell Industries
(Industrial Customers)
444 Windsor Park Drive
Dayton, OH 45459
Tel: (513) 435-8660
Telex: 810-459-1615
FAX: (513) 435-6765

Hall-Mark Electronics
5821 Harper Road
Solon, OH 44139
Tel: (216) 349-4632
FAX: (216) 248-4803

Hall-Mark Electronics
400 E. Wilson Bridge Rd., # S
Worthington, OH 43085
Tel: (614) 888-3313
FAX: (614) 888-0767

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4800 E. 131st Street
Cleveland, OH 44105
Tel: (216) 587-3600
Telex: 810-421-0011
FAX: (216) 587-3906

Pioneer
4433 Interpoint Blvd.
Dayton, OH 45424
Tel: (513) 236-9900
Telex: 810-459-1622
FAX: (513) 236-8133

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Anthem
9705 S.W. Sunshine Court
Suite 900
Beaverton, OR 97005
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FAX: (503) 626-7928

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6024 S.W. Jean Road
Lake Oswego, OR 97035
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Telex: 910-455-8177
FAX: (503) 635-4095

Pennsylvania
Lionex/Anthem
Horsham Business Center
355 Business Center Drive
Horsham, PA 19044
Tel: (215) 443-5150
FAX: (215) 675-9875

CAM-RPC Electronics
620 Alpha Drive
RIDC Park
Pittsburgh, PA 15238
Tel: (412) 782-3770
Telex: 4974222
FAX: (412) 963-6210

Pioneer
261 Gibraltar Road
Horsham, PA 19044
Tel: (215) 674-4000
Telex: 510-665-6778
FAX: (215) 674-3107

Pioneer
259 Kappa Drive
Pittsburgh, PA 15238
Tel: (412) 782-2300
Telex: 710-795-3122
FAX: (412) 963-8255

Tennessee
Bell Industries
1661 Murfreesboro Road
Suite G
Nashville, TN 37217
Tel: (615) 367-4400
FAX: (615) 367-4540

Texas
Anthem
651 N. Plano Road
Suite 429
Richardson, TX 75081
Tel: (214) 238-7100
FAX: (214) 238-0237

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12211 Technology Blvd.
Austin, TX 78727
Tel: (512) 258-8848
FAX: (512) 258-3777

Hall-Mark Electronics
11420 Pagemill Road
Dallas, TX 75243-5506
Tel: (214) 553-4300
FAX: (214) 553-4395

Hall-Mark Electronics
11333 Pagemill Road
P.O. Box 222035
Dallas, TX 75243
Tel: (214) 343-5000
FAX: (214) 343-5988

Hall-Mark Electronics
8000 Westglen
Houston, TX 77063
Tel: (713) 781-6100
FAX: (713) 953-8420

Pioneer
1826 Kramer Lane
Suite D
Austin, TX 78758
Tel: (512) 835-4000
Telex: 910-874-1323
FAX: (512) 838-9829

Pioneer
13710 Omega Road
Dallas, TX 75244
Tel: (214) 386-7300
Telex: 910-860-5563
FAX: (214) 490-6419

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Pioneer
5853 Point West Drive
Houston, TX 77036
Tel: (713) 988-5555
Telex: 910-881-1606
FAX: (713) 988-1732

Utah
Anthem
1279 West 2200 South
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FAX: (801) 973-8909

Bell Industries
6912 South 185 West
Suite B
Midvale, UT 84047-3756
Tel: (801) 255-9611
FAX: (801) 255-2477

Hall-Mark Electronics
2264 South 1300 West
West Valley City, UT 84119-1461
Tel: (801) 972-1008
FAX: (801) 972-3446

Washington
Anthem
19017 120th Avenue N.E.
Suite 102
Bothell, WA 98011
Tel: (206) 483-1700
FAX: (206) 885-4041

Washington (continued)
Bell Industries
8553 154th Avenue N.E.
Redmond, WA 98052
Tel: (206) 885-9963
Telex: 910-443-2482
FAX: (206) 867-5159

Wisconsin
Bell Industries
W227 N913 Westmound Drive
Waukesha, WI 53186
Tel: (414) 547-8879
Telex: 910-265-3665
FAX: (414) 547-6547

Hall-Mark Electronics
16255 W. Lincoln Avenue
New Berlin, WI 53151
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FAX: (414) 797-9259

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MCI
West Peabody Office Park
83 Pine Street
Suite 112
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Master Chips
Boulevard St. Lazare 4
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Tech-Trek
148 Colonnade Road
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Tech-Trek
7033 Trans-Canada Hwy.
Suite 202
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Future Electronics
237 Hymus Blvd.
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Quebec H9R 5C7, Canada
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Telex: 05-823-554/9
610-421-3251
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1050 Baxter Road
Ottawa
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106 King Edwards St., East
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155 Colonnade Road South
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